Datasheet

MB86064

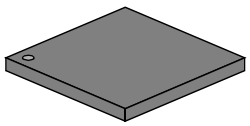
October 2005
Version 1.2

FME/MS/DAC80/DS/4972

Dual 14-bit 1GSa/s DAC

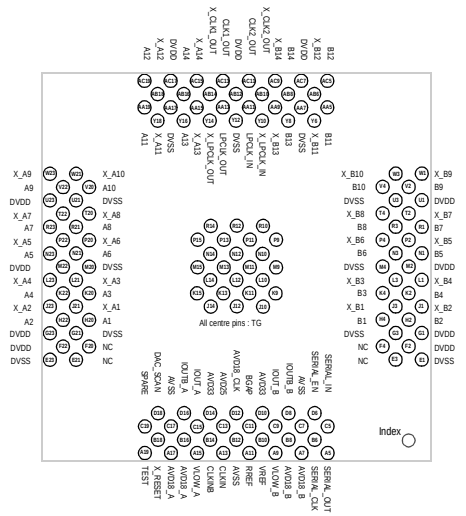
The Fujitsu MB86064 is a Dual 14-bit 1GSa/s digital to analog converter (DAC), delivering exceptional dynamic performance. Each high performance DAC core is capable of generating multi-standard, multi-carrier communication transmit signals, suitable for 2, 2.5 and 3G systems. DAC data is input via two high-speed LVDS ports. These operate in a pseudo double data rate (DDR) mode, with data latched on both rising and falling edges of the clock. Alternatively, the device can be configured as a multiplexed dual-port single DAC. To simplify system integration the DAC operates from a clock running at half the DAC conversion rate.

PLASTIC PACKAGE
EFBGA-120



Package Dimensions
12 mm x 12 mm

PIN ASSIGNMENT



Not to scale. Viewed from above.

Features

- Dual 14-bit, 1GSa/s Digital to Analog conversion
- Exceptional dynamic performance
  - 74dBc ACLR for 4 UMTS carriers @ 276MHz direct-IF
- 100MHz image-free generated bandwidth capability
  - supports UMTS plus digital pre-distortion bandwidth
- Proprietary performance enhancement features
- LVDS data interface
- Register selectable on-chip LVDS termination resistors
- Fujitsu 4-wire serial control interface
- Two 16k point programmable on-chip waveform memories
- Low power 3.3V analog and 1.8V digital operation
- 750mW single DAC operation power dissipation at 1GSa/s
- 0.18µm CMOS technology with Triple Well
- Performance enhanced EFBGA package
- Industrial temperature range operation (-40°C to +85°C)

Applications

- Multi-carrier, Multi-standard cellular infrastructure
  - CDMA, W-CDMA, GSM/EDGE, UMTS
- Wideband communications systems
- High Direct-IF architectures
- Arbitrary waveform generation
- Test equipment
- Radar, video & display systems

Contents

CAUTION

ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1 Functional Description

The MB86064 is a high performance Dual 14-bit 1GSa/s DAC. In addition to two DAC cores the device features a host of features designed to help both system integration and operation. A functional block diagram is shown in Figure 1.

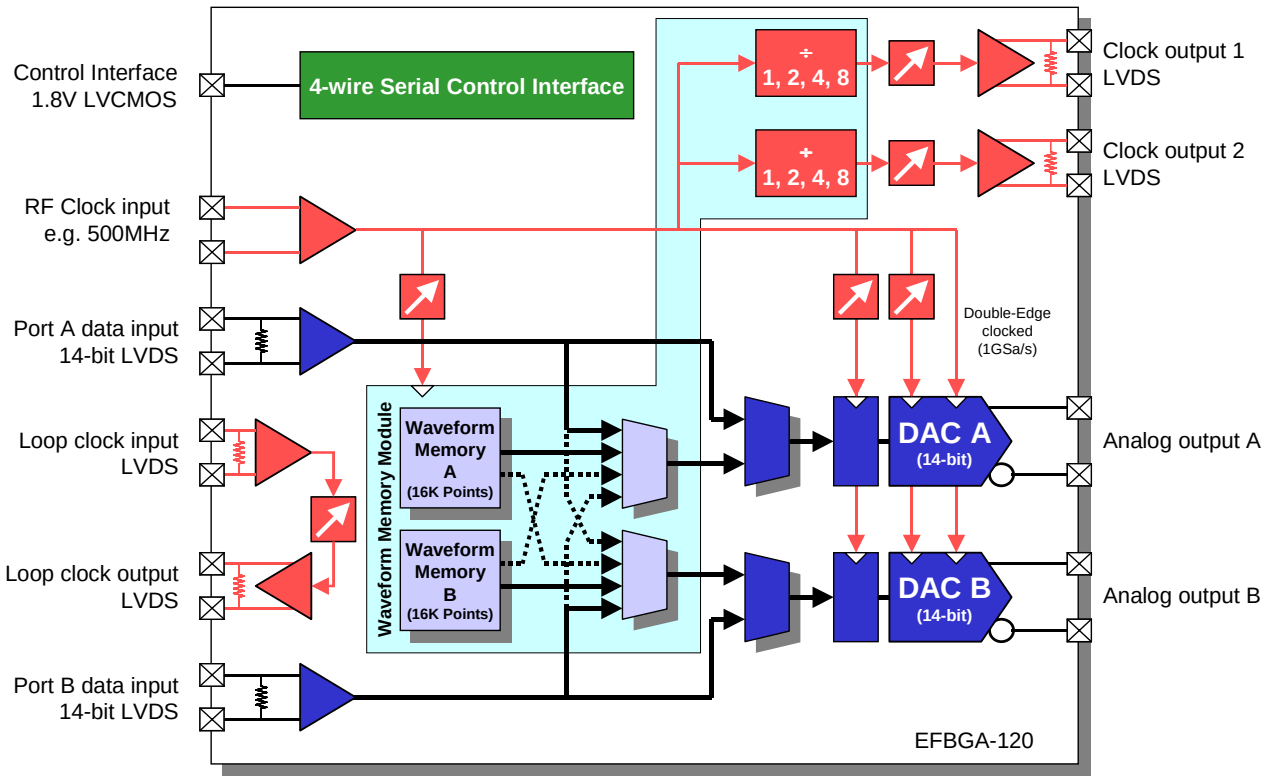


Figure 1 MB86064 Functional Block Diagram

The device features a number of proprietary performance enhancement features. For example, analog performance at high frequencies is enhanced by novel current switch and switch driver designs which provide constant data-independent switching delay, reducing jitter and distortion. Each DAC core can be regarded as two interleaved DACs running at half rate. The main reason for adopting this approach is that the switch driver inherently includes a multiplex function through its two input ports. Compared to a conventional switch driver this allows twice as long to acquire and convert, though because the two paths share current sources they match exactly at low frequencies. In terms of input data, this approach allows easy interfacing to DDR data generating devices.

Also integrated into the device is a comprehensive Waveform Memory Module (WMM). Waveforms can be downloaded, via the serial control interface, to drive the DAC cores in the absence of a suitable external data generator.

1.1 Clock

The device requires an input clock at half the DAC conversion rate, with sufficient spectral purity to not impact the target analog output performance. The DAC cores are clocked on both rising and falling edges of the input clock. This forms an effect of two interleaved converters in each DAC core. A characteristic of this architecture is a suppressed image of the generated signal, appearing reflected about Fs(dac)/4 = (Fclk-Fsig). Any duty cycle error in the input clock will exacerbate this image. This can be minimised by trimming the differential DC offset at the clock input pins.

1.1.1 Input Clock

The input clock should be applied to the MB86064 through input pins CLKIN and CLKINB. The device is designed to accept a differential sinusoidal clock. Once on chip and converted to CMOS the clock is distributed to a number of blocks throughout the device. The DAC cores are supplied directly from the input clock buffer to ensure minimal degradation to the clock's purity.

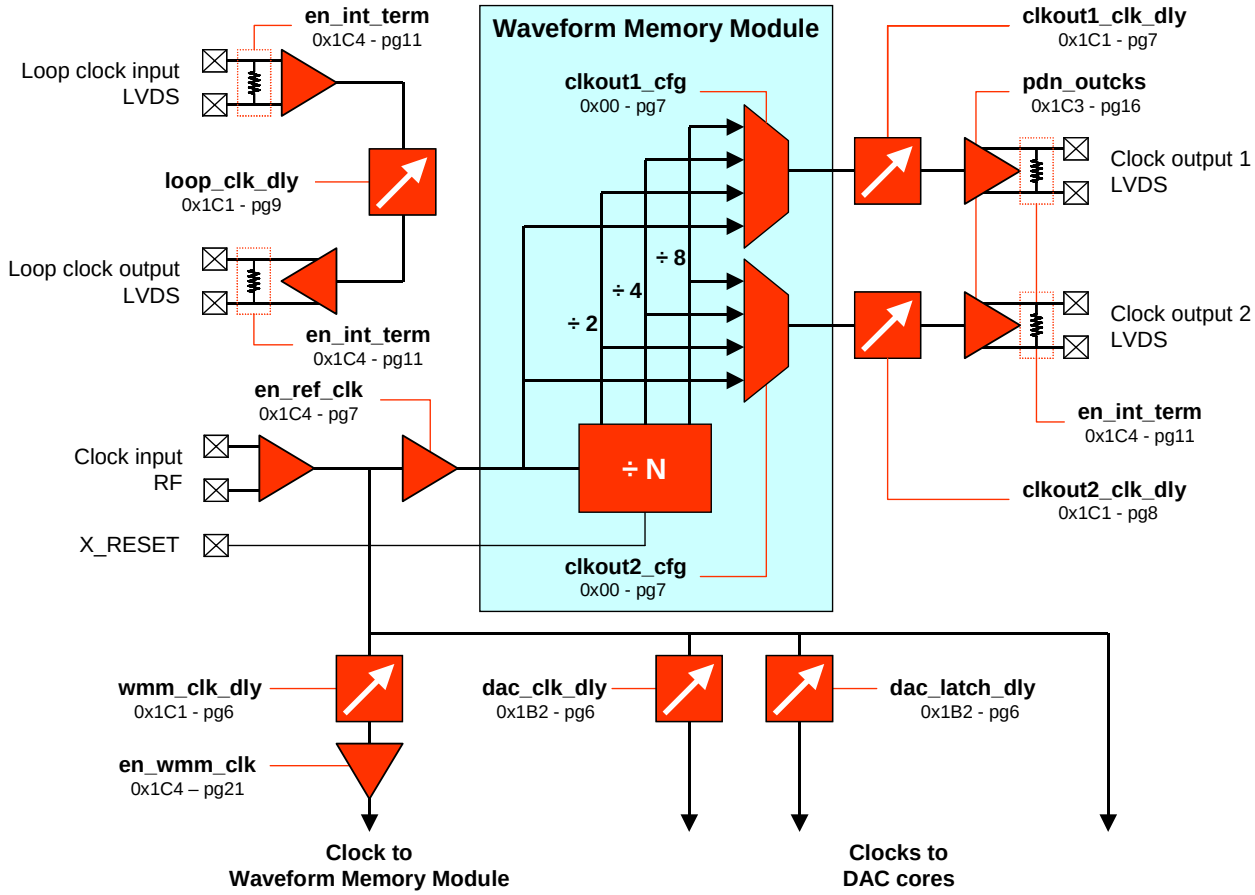


Figure 2 Clock Distribution

1.1.2 DAC Core Clocks Programmable Delays

The DAC core clocks contain programmable delays. These allow adjustment to the point at which data is clocked into the DAC core and when the analog portion of the DAC subsequently latches the

data. The delay settings are programmed through register DAC CORE CLOCK DELAYS, bits *dac_clk_dly* and *dac_latch_dly*. Based on detailed evaluation by Fujitsu these registers should be programmed in accordance with the recommendations given in Table 1.

Table 1: DAC Core Register: DAC CORE CLOCK DELAYS [0x1B2]

Label	Reg Bits 3	2	1	0	DAC Core Digital Clock Delay (0 - 1.5ns, 100ps steps)
dac_clk_dly	0	0	0	0	Minimum (* Recommended *)
	:	:	:	:	
	0	**1**	**0**	**0**	**Medium (default)**
	:	:	:	:	
	1	1	1	1	Maximum

Label	Reg Bits 7	6	5	4	DAC Core Analog Latch Clock Delay (0 - 1.5ns, 100ps steps)
dac_latch_dly	0	0	0	0	Minimum (* Recommended *)
	:	:	:	:	
	0	**1**	**0**	**0**	**Medium (default)**
	:	:	:	:	
	1	1	1	1	Maximum

*Note: **Bold** type indicates default setting. See Appendix A.*

1.1.3 Waveform Memory Module Clock Programmable Delay

A programmable delay stage is provided in the clock path prior to being applied to the Waveform Memory Module. This delay stage is programmed through register SYSTEM CLOCK DELAYS, bits *wmm_clk_dly*. See Table 2.

Table 2: DAC Core Register: SYSTEM CLOCK DELAYS [0x1C1] (Part 1 of 4)

Label	Reg Bits 15	14	13	12	Waveform Memory Module Clock Delay (0 - 1.5ns, 100ps steps)
wmm_clk_dly	**0**	**0**	**0**	**0**	**Minimum (default & recommended)**
	:	:	:	:	
	1	1	1	1	Maximum

1.1.4 Clock Outputs

Two clock outputs, CLK1_OUT and CLK2_OUT, are provided to enable synchronisation of data generating devices to the DAC. The reference clock used by the Clock Output block can be disabled if required. See Table 3.

Table 3: DAC Core Register: SYSTEM MISC [0x1C4] (Part 1 of 3)

SYSTEM MISC (bit)	Label	Function
0	en_ref_clk	Reference clock control 0 = Enabled **(default)**, 1 = Disabled

The output frequency can be individually selected as the input clock divided-by-1, 2, 4 or 8. Configuration is through register WMM CONFIG, bits *clkout1_cfg* and *clkout2_cfg*. See Table 4.

Table 4: Waveform Memory Module Register: WMM CONFIG [0x00] (Part 1 of 2)

Label	Reg Bits				Divided Clock Output Configuration
	3	2	1	0	
clkout1_cfg			**0**	**0**	**Clock output 1 = clock input (default)**
			0	1	Clock output 1 = clock input divided by 2
			1	0	Clock output 1 = clock input divided by 4
			1	1	Clock output 1 = clock input divided by 8
clkout2_cfg	**0**	**0**			**Clock output 2 = clock input (default)**
	0	1			Clock output 2 = clock input divided by 2
	1	0			Clock output 2 = clock input divided by 4
	1	1			Clock output 2 = clock input divided by 8

Also, programmable delay stages are provided in both CLK1_OUT and CLK2_OUT outputs. These clock output delays are programmed through register SYSTEM CLOCK DELAYS *clkout1_clk_dly* and *clkout2_clk_dly*. See Table 5 and Table 6.

Table 5: DAC Core Register: SYSTEM CLOCK DELAYS [0x1C1] (Part 2 of 4)

Label	Reg Bits				Clock Output Delay (0 - 1.5ns, 100ps steps)
	7	6	5	4	
clkout1_clk_dly	**0**	**0**	**0**	**0**	**Minimum (default)**
	:	:	:	:	
	1	1	1	1	Maximum

Table 6: DAC Core Register: SYSTEM CLOCK DELAYS [0x1C1] (Part 3 of 4)

Label	Reg Bits 3	2	1	0	Clock Output Delay (0 - 1.5ns, 100ps steps)
clkout2_clk_dly	**0**	**0**	**0**	**0**	**Minimum (default)**
	:	:	:	:	
	1	1	1	1	Maximum

The clock outputs are designed to drive a doubly-terminated LVDS line (7mA drive into a bridged 50Ω load) for the best possible signal integrity. 100Ω termination resistors should be connected across the Q and $\overline{Q}$ signals at each end of the differential line. Enabling the internal LVDS terminations provides the required source termination on-chip.

1.1.5 Loop Clock

Maintaining valid clock-to-data timing becomes increasingly difficult at higher clock rates, particularly over tolerance with device-to-device variations. The MB86064 minimises potential problems through its DDR data interface and by providing a unique loop-clock facility.

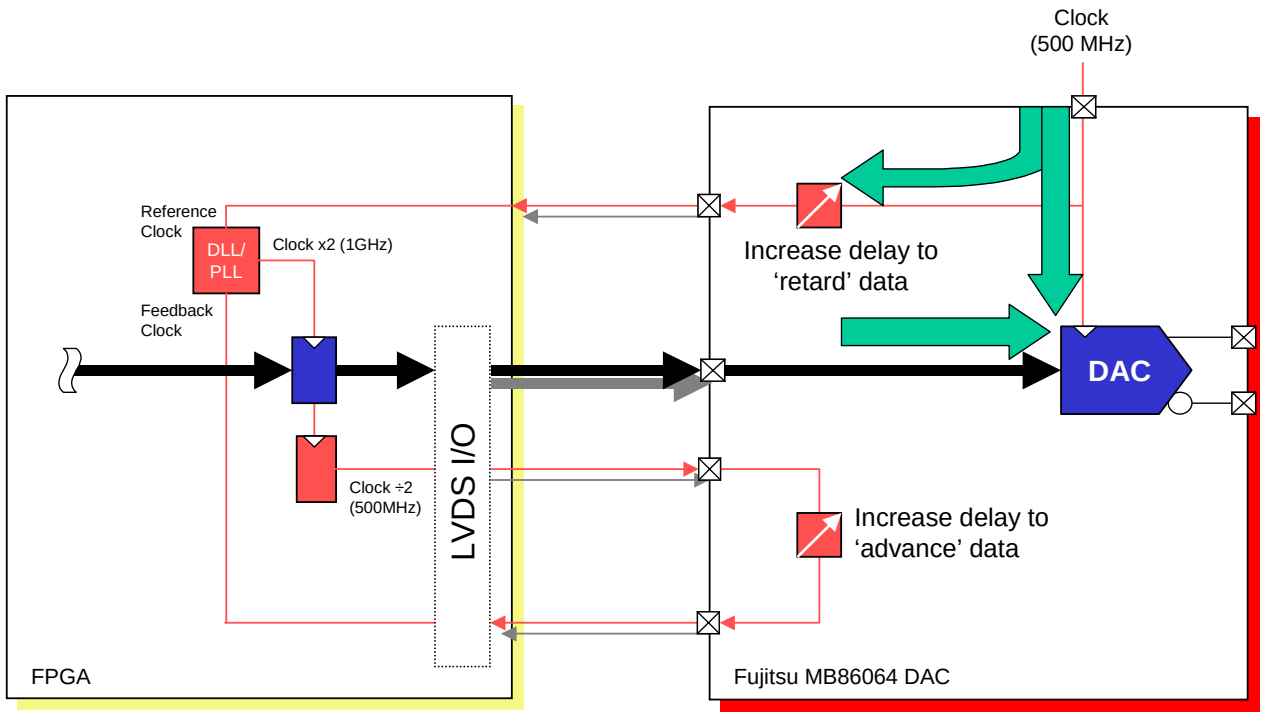


Figure 3 Loop Clock Implementation

The on-chip 'loop' consists of an LVDS input buffer connected to an LVDS output buffer through a programmable delay stage. This loop-through, and the associated tracking from/to the data

generating device, can be incorporated in the feedback loop of a Delay-Locked Loop (DLL) or Phase-Locked Loop (PLL) clock generator, within the generating device. This enables the system to compensate for variations in input/output (I/O) and propagation delays in both the data generating device and the DAC. PCB and/or cable propagation delays within the loop are also compensated for but these are not expected to exhibit significant variation between systems. It is the I/O & on-chip delays that will dominate.

It is important to make sure that the Clock Output frequency is within the specification of the DLL/PLL. If it is too high an appropriate divided clock output should be programmed as detailed in Table 7.

With the loop clock implemented as illustrated in Figure 3, increasing the Clock Output delay delays the data arriving at the DAC relative to the DAC input clock. By contrast increasing the Loop Clock delay, within the feedback loop of the DLL/PLL, advances the relative timing.

It is important not to adjust both delays simultaneously else they will counteract each other. Either the Clock Output delay or the Loop Clock delay, or both, should be zero.

Connections to the loop clock are via pins LPCLK_IN and LPCLK_OUT. The loop clock delay is programmed through register SYSTEM CLOCK DELAYS, *loop_clk_dly*. See Table 7.

Table 7: DAC Core Register: SYSTEM CLOCK DELAYS [0x1C1] (Part 4 of 4)

Label	Reg Bits				Loop Clock Delay (0 - 1.5ns, 100ps steps)
	11	10	9	8	
loop_clk_dly	**0**	**0**	**0**	**0**	**Minimum (default)**
	:	:	:	:	
	1	1	1	1	Maximum

With the DAC Core Clock Delays set to their recommended values (0x00), monitoring the analog output for a valid signal while adjusting the Clock Output and Loop Clock delays enables a diagram of valid & invalid data latching points to be produced. An example is illustrated in Figure 4.

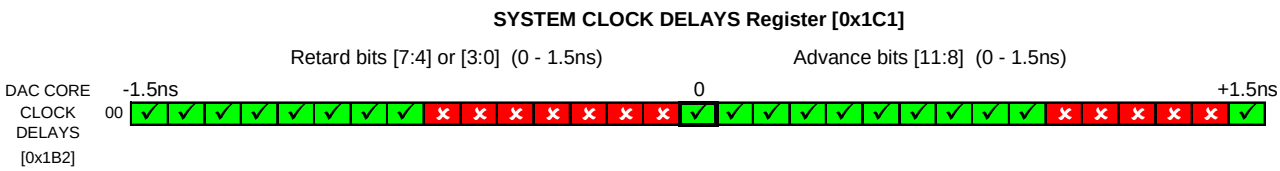


Figure 4 Finding Valid Data Eyes Using Loop Clock

This example used an Altera Stratix FPGA evaluation platform driving a Fujitsu development kit at 800MSa/s. Another circuit implementation would exhibit different absolute timings but similar relative adjustments.

Having evaluated a prototype design and final loop clock delay settings chosen, the real benefit of using the loop clock facility is in maintaining valid clock-to-data timing at these settings. Figure 5 illustrates this in operation by using excessive variation in supply voltages to emulate both fast and slow FPGA and DAC components being used together in production.

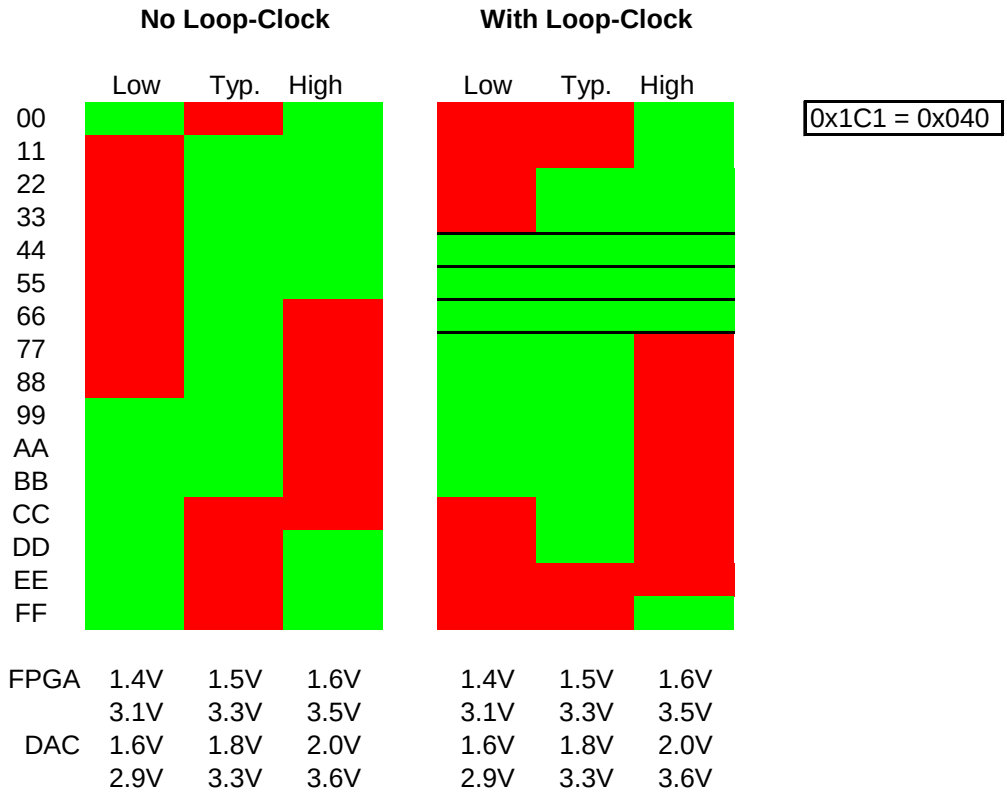


Figure 5 Maintaining Valid Clock-to-Data Timing using Look Clock

1.2 DAC Data

Each DAC core can be considered as two identical halves, referred to as ODD and EVEN. EVEN samples are latched on the falling edge of Clock Output, whilst ODD samples are latched on the rising edge.

Data should be presented to the DAC cores as unsigned binary, 14-bit data. Bit 14 is the MSB, and bit 1 is the LSB.

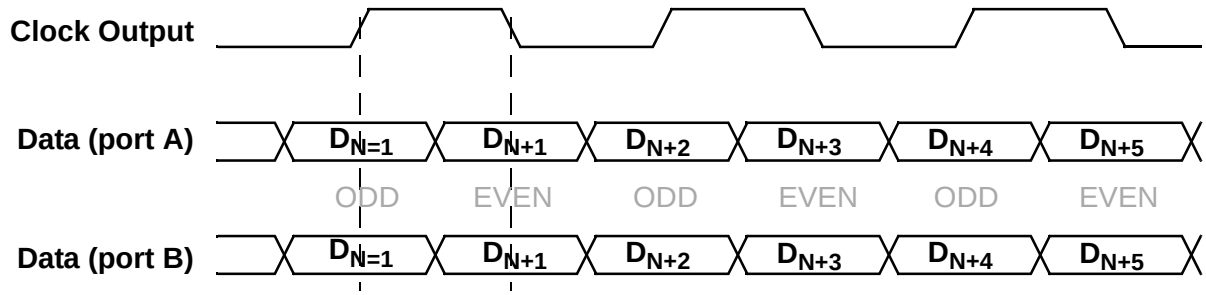


Figure 6 ODD and EVEN Data Sampling

Data can be supplied to the DAC cores either externally via the LVDS data bus or internally from the Waveform Memory Module.

1.2.1 Data from the LVDS Interface

External data is input to the MB86064 through LVDS data ports A (pins A[14:1]) and B (pins B[14:1]). On-chip 100Ω termination resistors are provided to reduce the external component count, selectable through register SYSTEM MISC *en_int_term*. See Table 8 on page 11.

Table 8: DAC Core Register: SYSTEM MISC [0x1C4] (Part 2 of 3)

SYSTEM MISC (bit)	Label	Function
7	en_int_term	Internal 100R LVDS termination enable (All LVDS data inputs, loop clock input, loop clock output and reference clock outputs) 0 = Disabled, **1 = Termination enabled (default)**

The data may be routed to the DAC cores through a number of paths. The most direct path routes data straight from the LVDS input buffers to the DAC core input latches. This is the default configuration, with the DAC input multiplexers set to accept data from the LVDS inputs according to register WMM CONFIG, *data_direct*. See Table 9 below.

The DAC exhibits a pipeline delay through the device of 18 input clock edges.

Table 9: Waveform Memory Module Register: WMM CONFIG [0x00] (Part 2 of 2)

WMM CONFIG (bit)	Label	Function
4	data_direct	DAC A and DAC B data source **0 = LVDS data directly (default)**, 1 = Waveform Memory Module

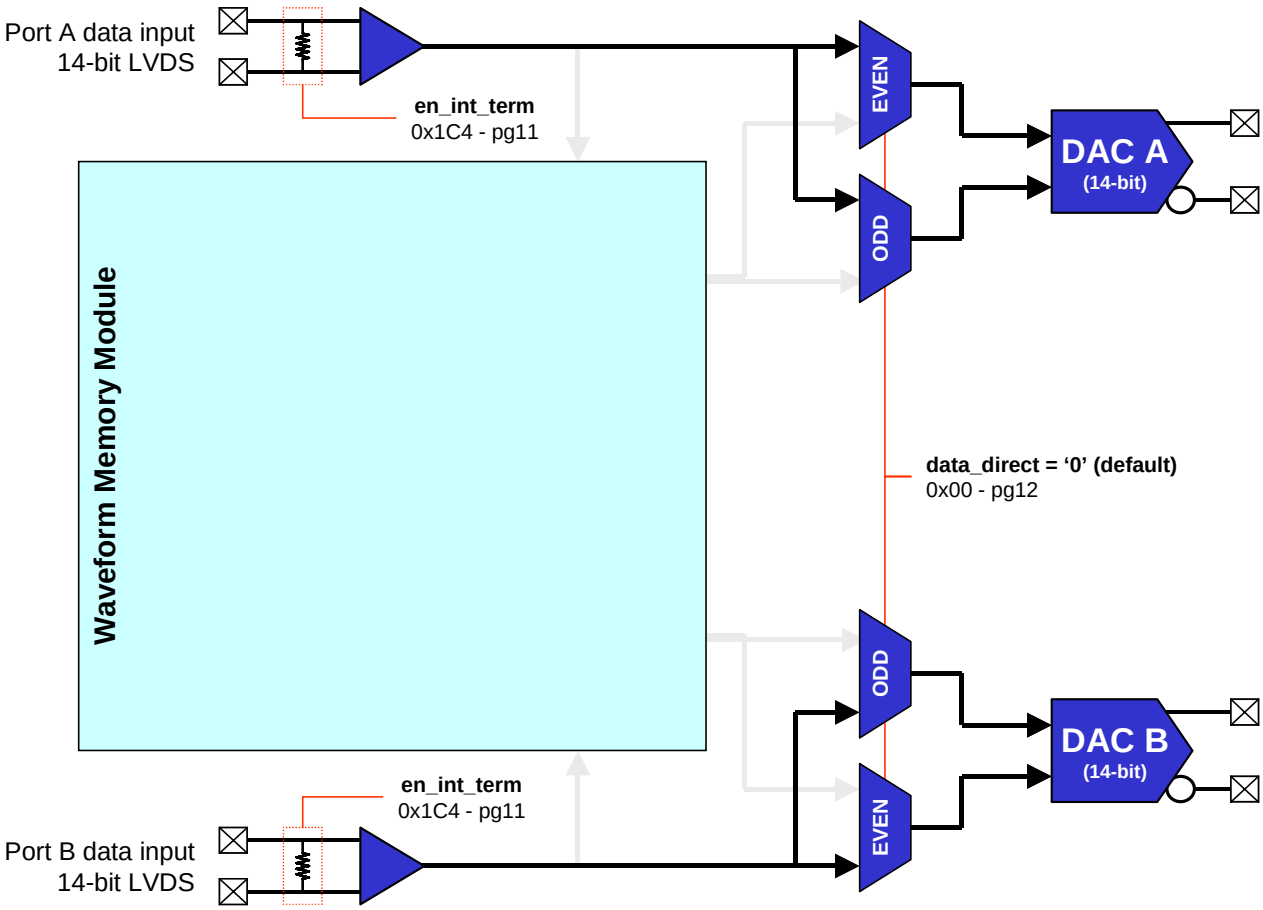


Figure 7 Direct Data Routing from the LVDS Interface

1.2.2 Adjusting the Input Data Timing

When using the Clock Outputs to synchronise the data generator it is possible to adjust the relative input data timing through DAC Core register SYSTEM CLOCK DELAYS [7:4] & [3:0], *clkout1_clk_dly & clkout2_clk_dly*. See Table 5 and Table 6. Increasing this setting delays the arrival of input data.

When using the Loop Clock, the delay set by *loop_clk_dly* (Table 7) opposes this and effectively advances the input data relative to the reference clock edge. Together these adjustments provide approximately 3ns trim range for clock-to-data timing, in 100ps steps.

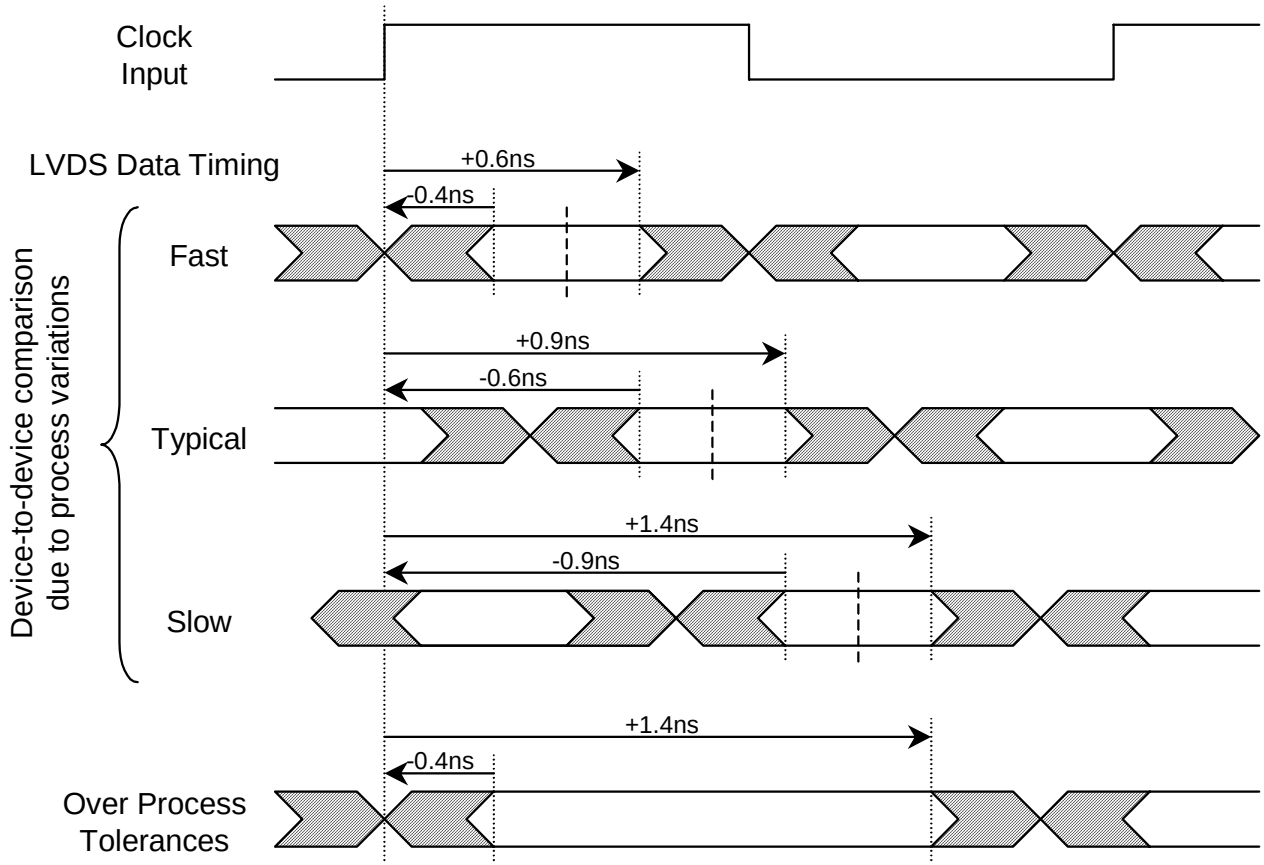


Figure 8 LVDS Input Data Timing

For further details refer to sections 1.1.4 and 1.1.5.

1.2.3 Data from the Waveform Memory Module

Data routing within the Waveform Memory Module is flexible enough to allow A and B data to be interleaved onto a single DAC core. However, primarily the Waveform Memory Module is intended to be loaded with waveforms and subsequently read back to drive the DAC cores. A complete description of how to use the Waveform Memory Module is given in Section 3.

1.3 DAC Core Current References

Internal current references are required to be configured according to which DAC core(s) are enabled. These are controlled by the DAC Core Register DAC CONFIG.

Table 10: DAC Core Register: DAC CONFIG [0x1C0]

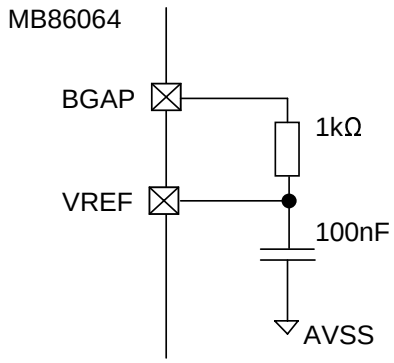
DAC CONFIG (bits)		Configuration
1	0	
X	X	With DAC A and DAC B disabled
1	X	With DAC A enabled, DAC B disabled
X	1	With DAC A disabled, DAC B enabled
0	0	**With DAC A and DAC B enabled (default)**

The appropriate setting of these bits is dependent on the power-down status of the DAC cores, determined by register POWER DOWN [0x1C3] bits *pdn_daca* and *pdn_dacb*.

1.4 Voltage Reference

A 1.2V bandgap reference is provided on-chip, although this is left unconnected when an external reference is to be used. To use the internal bandgap reference, pins BGAP and VREF should be linked via a 1kΩ resistor. VREF should be decoupled to AVSS with a 100nF capacitor.

For maximum absolute accuracy an external voltage reference should be used. This should be connected to VREF through a 1kΩ resistor and decoupled as described above. The external voltage reference should be powered from the AVD25 pin, which is a regulated 2.5V output with high power supply noise rejection.

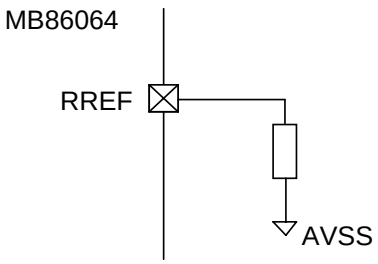


1.5 Analog Output Reference Resistor

From the voltage reference the full scale analog output current is defined by an external reference resistor, R_{ref}, where,

$$R_{ref} \approx \frac{16 \times V_{ref}}{I_{OP}}$$

e.g. With Vref = 1.20V, to give a 20mA full scale output, Rref = 960Ω. Designs that for simplicity use a 1kΩ resistor will result in a marginally lower full scale output current of 19.2mA (-0.35dB) unless using an external reference to provide a higher voltage of 1.25V.



1.6 Analog Outputs

The DAC outputs are differential current type. A termination resistor, or load, should be used appropriate for the recommended output swing. Each DAC may be individually powered down.

Analog output performance benefits from the chosen DAC core architecture, identified in Section 1 as similar to two interleaved DACs running at half rate. The big advantage of this approach compared to a single DAC running at half the rate is much reduced sinx/x roll-off which gives increased output power and better in-band flatness when generating high output frequencies (e.g. 200MHz and above). This is illustrated in Figure 9 as line 1. An alternative approach using a return-to-zero output stage admittedly has the same sinx/x roll off (and switch driver speed) but 6dB lower output power and a large image at Fclk-Fout. See Line 2. For reference, line 3 illustrates a conventional DAC running at half rate.

Another aspect of this comparison which should not be overlooked concerns noise performance, increasingly quoted in units of dBm/Hz. In terms of SNR there is some 7dBs of degradation to consider when comparing a 300MHz test for a standard 400MSa/s DAC with the MB86064 running at 800MSa/s. This is relevant to the Noise floor figures quoted in section 4.5 Dynamic Performance.

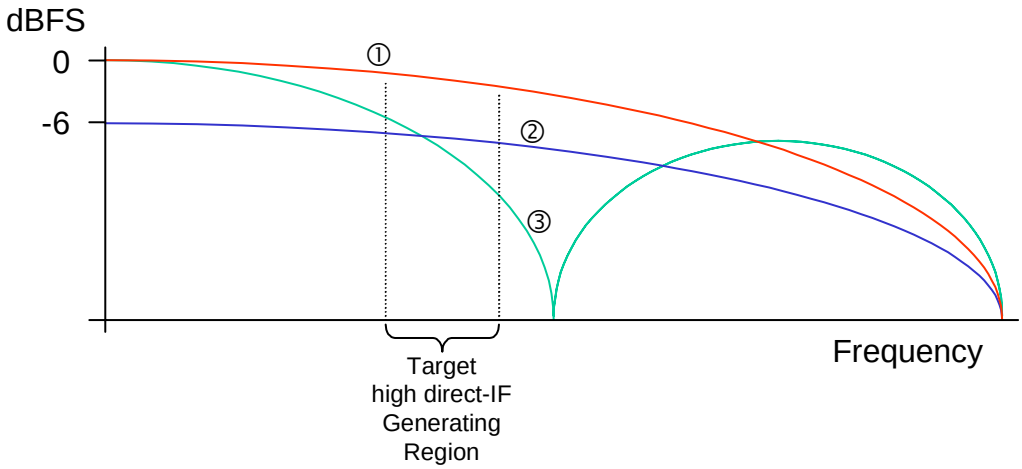


Figure 9 Benefits of DAC core Architecture to Sinx/x Response

1.6.1 Frequency Planning

Systems that require superior dynamic performance should not ignore the DAC from the task of frequency planning. To do so could result in impractical specifications or at worst increase the cost and power of the converter that would need to be selected. The MB86064 is designed to deliver the very best dynamic performance across wide bandwidths, as required for communications systems and in particular for multi-carrier applications. Preferred generating bands can be demonstrated as those centred at 0.2, 0.3 and 0.4 Fdac. In addition, while allowing certain images in-band though at levels unlikely to impact on performance other possible centre frequencies are 0.125 and 0.375 Fdac.

It is important to remember that conventional DACs running at half the rate or those incorporating a return-to-zero output stage are subject to exactly the same frequency planning constraints as these are defined by Nyquist's theorem. However, a key advantage of the MB86064 is its ability to generate wide bandwidth signals in the 2nd Nyquist zone where conventional DACs will be prevented from doing so due to Sinx/x attenuation.

1.7 Reset and Power Down

Pin X_RESET is the device reset pin. On the falling edge of X_RESET the device is reset and all registers are set to their default values. After a reset most parts of the device are powered down. See Table 11, DAC Core Register POWER DOWN. Power to each internal block may be individually controlled through this register.

Table 11: DAC Core Register: POWER DOWN [0x1C3]

POWER DOWN (bit)	Label	Function
0	pdn_reglo	Low voltage (~1.1V) regulator control **0 = Enabled (default)**, 1 = Powered down
1	pdn_regck	1.8V clock regulator control **0 = Enabled (default)**, 1 = Powered down
2	pdn_reg18	1.8V DAC regulator control **0 = Enabled (default)**, 1 = Powered down
3	pdn_reg25	2.5V bandgap regulator control **0 = Enabled (default)**, 1 = Powered down
4	pdn_ckandrefs	DAC common circuit (clocks, references and bias) control **0 = All enabled (default)**, 1 = All powered down
5	pdn_outcks	Divided output clocks **0 = Enabled (default)**, 1 = Powered down
6	pdn_loopcks	Loop clocks 0 = Enabled, **1 = Powered down (default)**
7	pdn_odatb	Access to TEST output pin by DAC B 0 = Enabled, **1 = Disabled (default)**
8	pdn_odata	Access to TEST output pin by DAC A 0 = Enabled, **1 = Disabled (default)**
9	pdn_indatb	DAC B data input power down control 0 = Enabled, **1 = Powered down (default)**
10	pdn_indata	DAC A data input power down control 0 = Enabled, **1 = Powered down (default)**
11	pdn_dacb	DAC B control *N.B. See note below* 0 = Enabled, **1 = Powered down (default)**
12	pdn_daca	DAC A control *N.B. See note below* 0 = Enabled, **1 = Powered down (default)**

The DAC control register bits, *pdn_daca* & *pdn_dacb*, must be set in conjunction with the DAC CONFIG register bits to ensure the correct internal reference current is used. See section 1.3.

Examples of typical settings are:

- 0x0000B80 DAC A enabled for LVDS data
- 0x0001580 DAC B enabled for LVDS data
- 0x0000180 Both DACs enabled for LVDS data

All are based on both the divided clock outputs and loop-clocks being enabled.

2 Serial Control Interface

A simple 4-wire serial control interface is used to control the MB86064. The serial interface uses pins SERIAL_IN, SERIAL_OUT, SERIAL_CLK and SERIAL_EN. Programmed settings are stored in a number of registers which are individually accessible using either an 7-bit (WMM Registers) or 10-bit (DAC Core Registers) address/control word. Data may be written to or read from each of these registers.

The serial interface uses 1.8V LV-CMOS logic levels.

2.1 Programming a Read/Write Cycle

To perform a read or write cycle SERIAL_EN should be taken high on the falling edge of SERIAL_CLK. This will indicate the start of a frame when latched on the next rising edge. At the same time SERIAL_IN should be driven, MSB first, with the address of the register to be accessed. Data is latched into the device on each rising edge of SERIAL_CLK. The register address should be followed with the read/write instruction bit. For a read cycle this bit is ‘0’, for a write cycle this bit is ‘1’. The device is now ready to transfer data in or out of the addressed register.

If the selected register is to be written to, the data should be presented to SERIAL_IN, MSB first. The data packet only needs to be as long as the register that is being written to, with the LSB presented in the final time slot. If the data source has a fixed length packet size, longer than the register, the data packet should be zero-filled at the MSB end. Once the data has been transferred into the register, SERIAL_EN should be taken low on the falling edge of SERIAL_CLK to indicate the end of the read/write cycle and frame. During a write cycle, as data is loaded into the selected register, the previous contents are output on SERIAL_OUT, MSB first.

If the selected register is being read, data will be output on SERIAL_OUT, MSB first, nominally coincident with the falling edge of SERIAL_CLK. Once the register has been read additional clock cycles will produce zero-filled bits until the read cycle is terminated. A read cycle may be terminated by taking the SERIAL_EN low on the falling edge of SERIAL_CLK.

All Waveform Memory Module registers, apart from WMM [EVEN/ODD] RAM DATA, read back as eight bit long registers. All other registers will read back at their true length.

Figure 10 and Figure 11 show the write and read cycles (as functional timing diagrams) in more detail.

In designs where SERIAL_CLK is halted after a Write operation, at least three additional clock cycles should be allowed after SERIAL_EN has return low. This is necessary to complete the internal register programming.

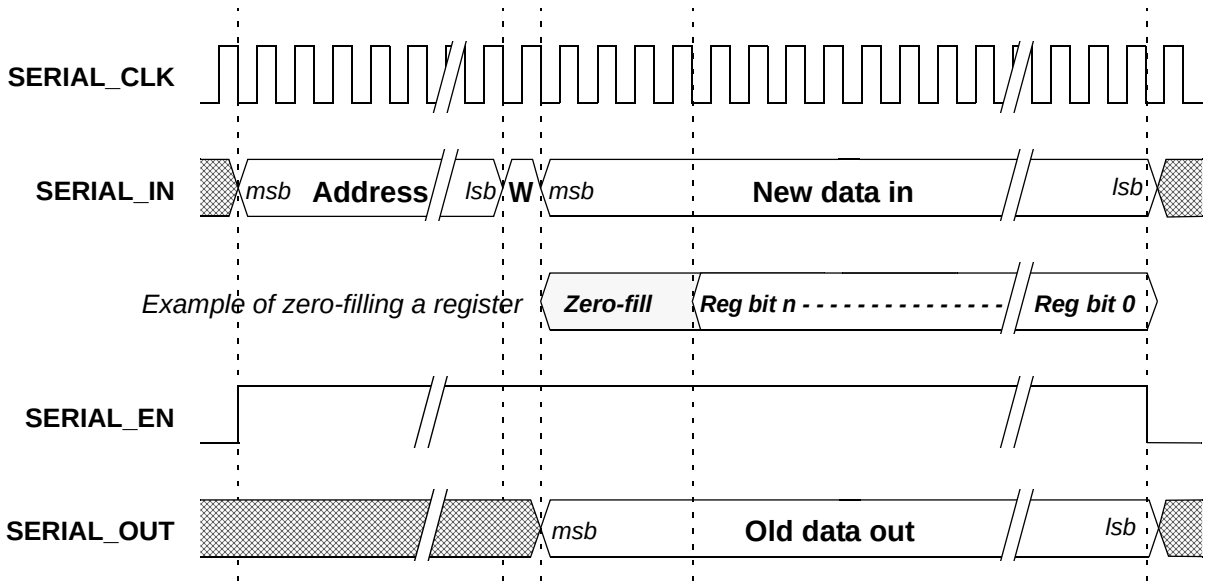


Figure 10 Serial Control Interface 'Write' Operation

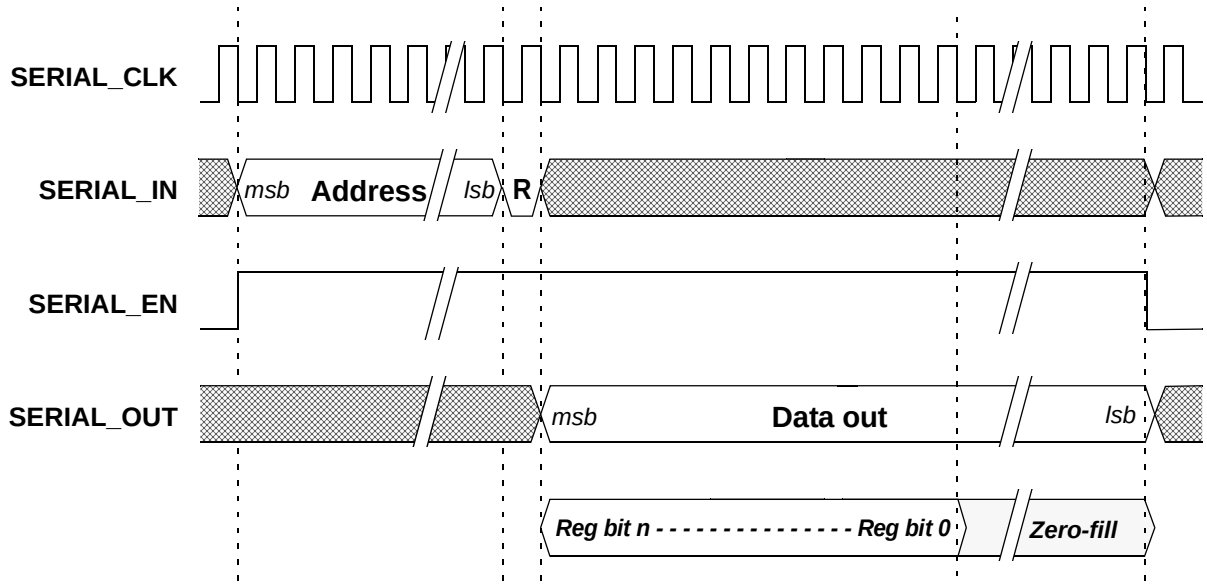


Figure 11 Serial Control Interface 'Read' Operation

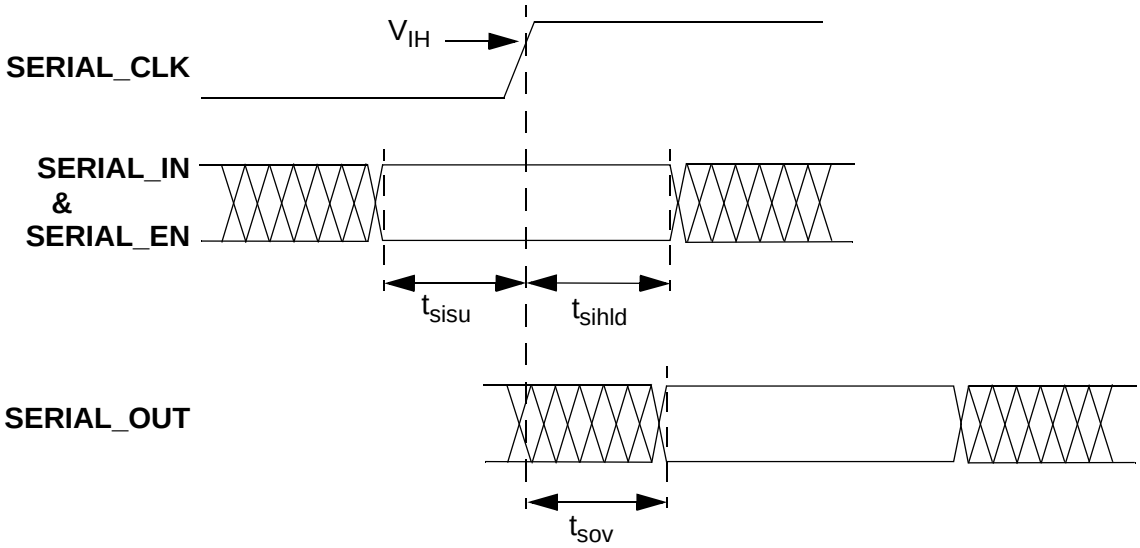


Figure 12 Serial Control Interface Timing Requirements

For initial testing & evaluation it is assumed that customers will use the Fujitsu PC USB Programming cable and software, both with the product development kit and for initial target application debug. See Section 7 for further information.

3 Waveform Memory Module

Enabling the Waveform Memory Module allows interleaving of the LVDS data to drive a single DAC core as well as access to any downloaded waveforms. The on-chip waveform memories allow the DAC cores to be exercised with user programmable waveforms without the need for an external high speed pattern generator. The memories are physically implemented using four 2k x 64-bit static RAMs, assigned as two per DAC for ODD and EVEN samples. The memories can be configured to drive two different waveforms of equal length, up to 16k points each, to be routed to DAC A and DAC B independently. Alternatively, it is possible to download multiple waveforms, totalling 16k points or less, to be selected as required. This last configuration takes advantage of the ability to specify the waveform start address and length.

Data routing within the Waveform Memory Module is determined by three cascaded multiplexers, mux_[a/b/c]_ctrl[0:2], as illustrated in Figure 13.

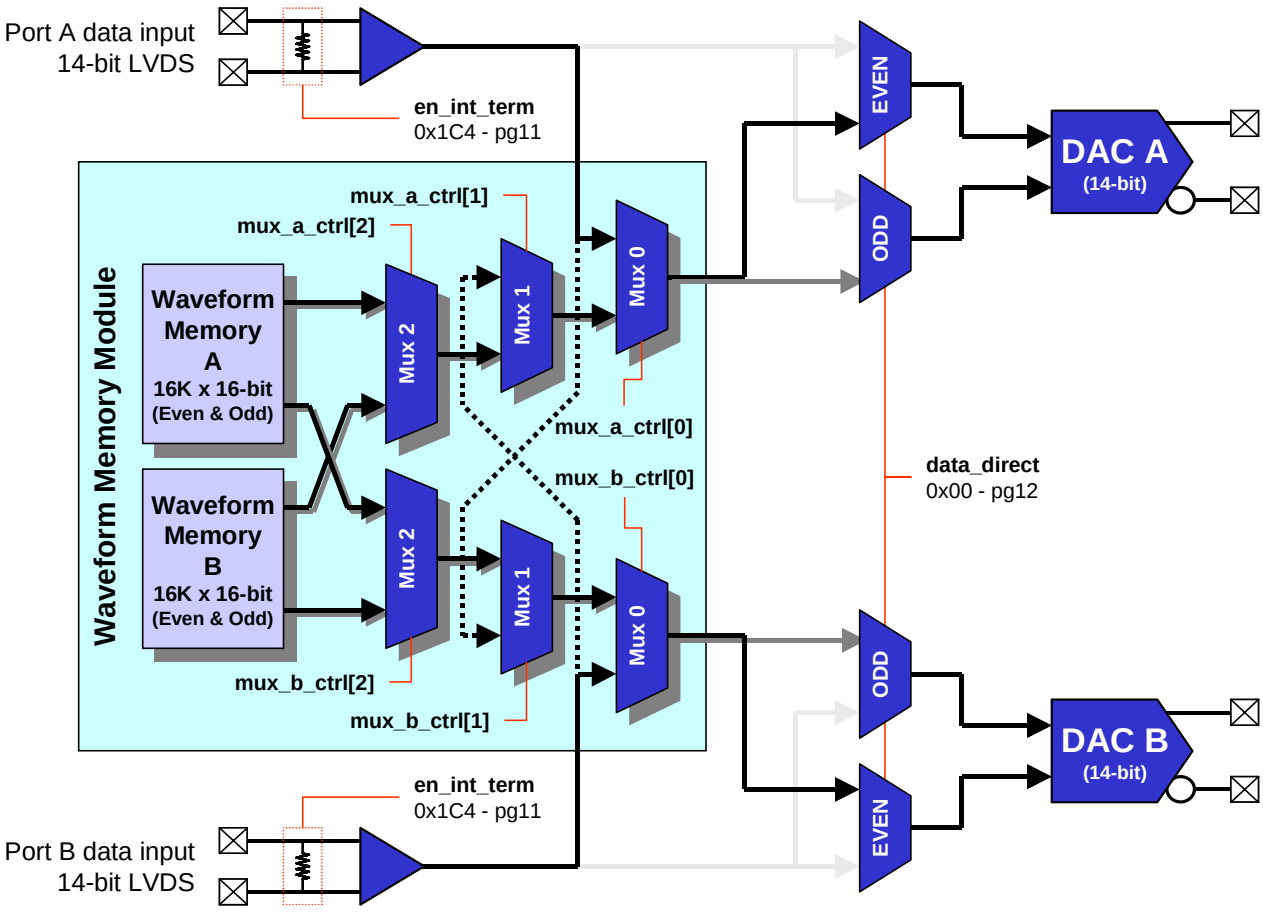


Figure 13 Waveform Memory Module Data Routing

The data multiplexers are controlled by the WMM Registers, WMM [EVEN/ODD] MUX CTRL. Setting of these registers is referred to in the following two sections.

Table 12: Waveform Memory Module Register: WMM [EVEN/ODD] MUX CTRL [0x11/0x21]

WMM [EVEN/ ODD] MUX CTRL (bit)	Label	Function
0	mux_a_ctrl[0]	Mux 0 control bit **0 = Data from LVDS input port A (default)** 1 = Data from Mux 1
1	mux_a_ctrl[1]	Mux 1 control bit **0 = Data from LVDS input port B (default)** 1 = Data from Mux 2
2	mux_a_ctrl[2]	Mux 2 control bit (1). **See also mux_a_ctrl[3] setting.** **0 = Data from RAM A - 16K points mode (default)** 1 = not used
3	mux_a_ctrl[3]	Mux 2 control bit (2) **0 = mux_a_ctrl[2] operates as normal (default)** 1 = When mux_a_ctrl[2] = 0, RAM B is used instead of RAM A
4	mux_b_ctrl[0]	Mux 0 control bit **0 = Data from LVDS input port B (default)** 1 = Data from Mux 1
5	mux_b_ctrl[1]	Mux 1 control bit **0 = Data from LVDS input port A (default)** 1 = Data from Mux 2
6	mux_b_ctrl[2]	Mux 2 control bit (1). **See also mux_b_ctrl[3] setting.** **0 = Data from RAM B - 16k points mode (default)** 1 = not used
7	mux_b_ctrl[3]	Mux 2 control bit (2) **0 = mux_b_ctrl[2] operates as normal (default)** 1 = When mux_b_ctrl[2] = 0, RAM A is used instead of RAM B

To use any of the Waveform Memory Module modes it is necessary to first enable the module's clock through register SYSTEM MISC, bit *en_wmm_clk* (see Table 13).

Table 13: DAC Core Register: SYSTEM MISC [0x1C4] (Part 3 of 3)

SYSTEM MISC (bit)	Label	Function
1	en_wmm_clk	Waveform Memory Module clock control 0 = Enabled, **1 = Disabled (default)**

3.1 Dual Port, Interleaved LVDS Data via the WMM

By routing the external LVDS data through the Waveform Memory Module it is possible to interleave A and B data into one of the DAC cores. To configure the device in this mode EVEN & ODD multiplexers need to be set differently.

Table 14: Configuration for Interleaved Data to DAC A

WMM EVEN MUX CTRL [0x11]	WMM ODD MUX CTRL [0x21]	DAC A	
mux_a_ctrl[0] (bit 0)	**mux_a_ctrl[0] (bit 0)**	**ODD data in**	**EVEN data in**
'1'	**'0' (default)**	Port A	Port B
'0' (default)	'1'	Port B	Port A

Table 15: Configuration for Interleaved Data to DAC B

WMM EVEN MUX CTRL [0x11]	WMM ODD MUX CTRL [0x21]	DAC B	
mux_b_ctrl[0] (bit 4)	**mux_a_ctrl[0] (bit 4)**	**ODD data in**	**EVEN data in**
'1'	**'0' (default)**	Port B	Port A
'0' (default)	'1'	Port A	Port B

Remember to set register WMM CONFIG [0x00] bit *data_direct* to '1' (see Table 9)

The DAC will now sample both input ports, for consecutive DAC samples, as the EVEN and ODD routing through the Waveform Memory Module is not the same.

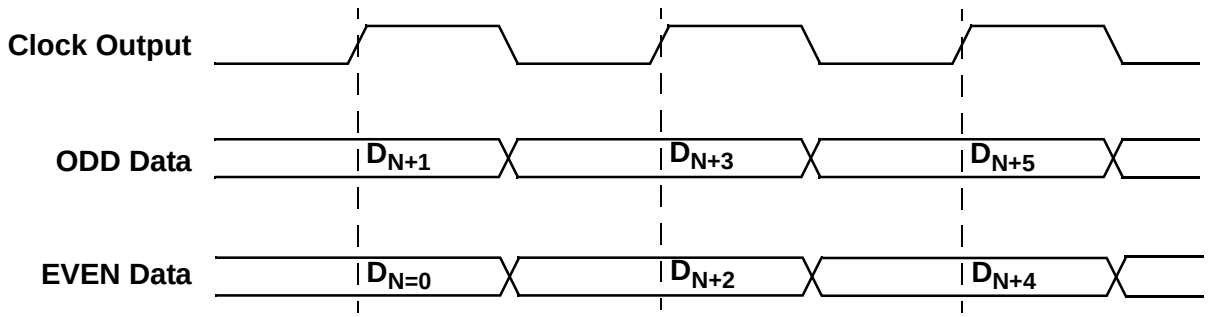


Figure 14 Interleaved Mode ODD and EVEN Data Sampling

3.2 Waveform Memory Module Operation

To make full use of the Waveform Memory Module user waveforms may be downloaded to the on-chip memories. Different waveforms of equal length may be stored in each RAM, totalling up to 16k points (in multiples of eight points). Configuration of the WMM [EVEN/ODD] MUX CTRL registers will determine which vector is routed to which DAC.

Before the waveform memories can be used they must be enabled through register WMM [EVEN/ODD] CONFIG, bit *ram_ih*. See Table 16.

Table 16: WMM Register: WMM [EVEN/ODD] CONFIG [0x10/0x20] (Part 1 of 2)

WMM [EVEN/ ODD] CONFIG (bit)	Label	Function
1	ram_ih	Waveform Memory inhibit control 0 = Memories Enabled **1 = Memories Disabled (default)**

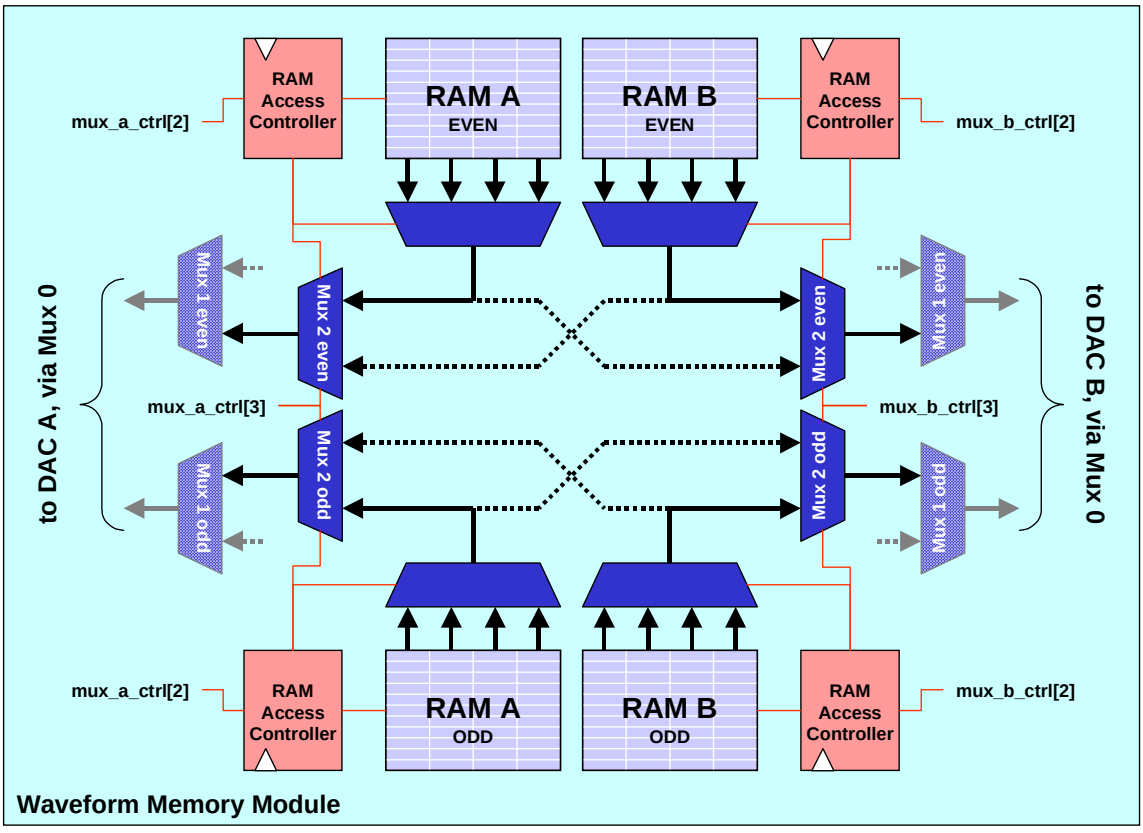


Figure 15 Waveform Memories Routing Diagram

ODD and *EVEN* RAM elements within the module allow data to be routed to the ODD and EVEN phase DAC core data latches, similar to when data is input via the LVDS data interface and double edge clocking is used. As an example, to route data from RAM A to DAC A, and RAM B to DAC B,

- set register WMM [EVEN/ODD] MUX CTRL bits *mux_a_ctrl[1] & [0]* and *mux_b_ctrl[1] & [0]*. Both the EVEN and ODD registers should be set the same. All other bits should be set to their default value.

To swap these data paths,

- set register WMM [EVEN/ODD] MUX CTRL bits *mux_a_ctrl[3]* and *mux_b_ctrl[3].* Both the EVEN and ODD registers should be set the same.

3.2.1 Waveform Memory Access via the Serial Interface

To access the waveform memories the RAM Access Controllers must first be configured. The RAM Access Controllers are configured through registers WMM [EVEN/ODD] RAM CTRL. See Table 17.

Table 17: Waveform Memory Module Registers: WMM [EVEN/ODD] RAM CTRL [0x12/0x22]

WMM [EVEN/ ODD] RAM CTRL (bits)	Label	Function
[10:0]	prog_addr	RAM access start address
[21:11]	prog_burst	RAM access burst size Access burst size should be programmed as ((No. of points/8) - 1) A value of zero indicates a single word access
22	prog_rw	RAM serial interface access mode **0 = Read mode (default)** 1 = Write mode
23	prog_sel(1)	RAM write select (1). **Dependent on prog_sel(2) setting** **0 = Write data to RAM A (default)** 1 = Write data to RAM B
24	prog_sel(2)	RAM write select (2) **0 = prog_sel(1) operates as normal (default)** 1 = Writes the same data to both RAM A and RAM B
25	prog_start	RAM Access Controller control **0 = Cycle through vector address range (default)** 1 = Program RAMs *This bit is self clearing*

When programming the WMM on-chip memories ensure that the Clock Input (f_{Clk}) is greater than 16 times the serial interface clock frequency (f_{sclk}) for correct operation.

The WMM [EVEN/ODD] RAM CTRL registers *prog_addr* fields are used to define the start address of the waveform. These fields should be set to 0 in order to store a full 16k point waveform. For the multiple waveform mode, the number entered into these fields is the start location within the 2k x 64-bit ODD/EVEN RAM element that the waveform is to be stored. One address location in this field translates to eight waveform vector points because four points are stored at each address of the ODD and EVEN RAM blocks.

The WMM [EVEN/ODD] RAM CTRL registers *prog_burst* fields sets the length of the stored waveform, defined as the number of waveform points divided by eight, minus one. Every RAM address in each of the ODD, EVEN, RAM A and RAM B memories corresponds to a 64-bit location. Each location is divided into four 16-bit samples.

Figure 16 shows an example of how a 32 point vector is stored. In this example *prog_addr* is set to 0 and *prog_burst* = 3.

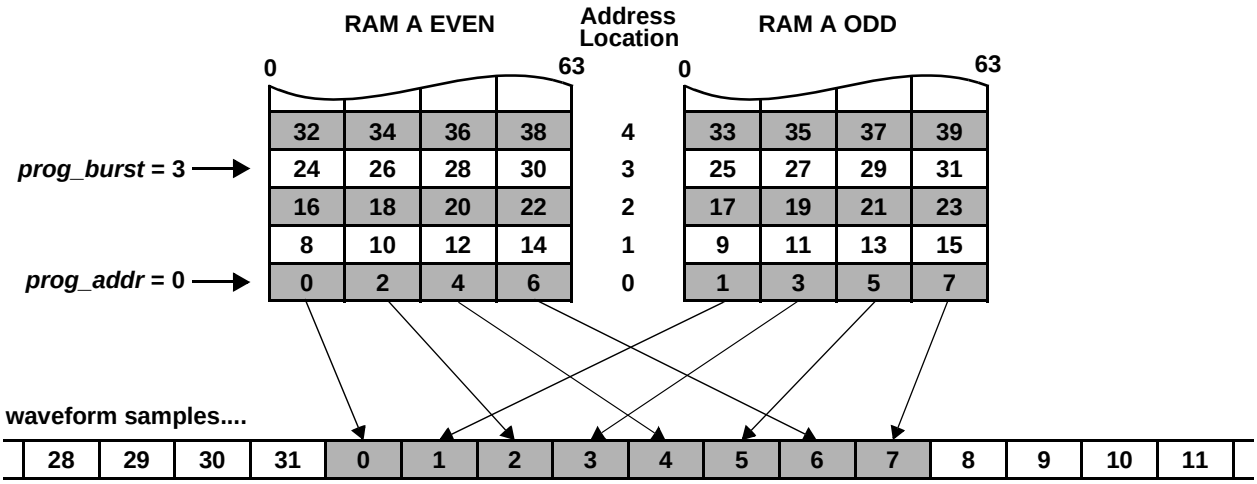


Figure 16 Waveform Vector Storage in on-chip Memories

prog_addr and *prog_burst* must be the same for RAM A and RAM B when routing data to the DACs.

Register bit *prog_rw* is used to select between reading from and writing to the RAMs through the serial interface. This bit should be set to '1' to write data into the RAMs, but does not need to be cleared to route data out to the DACs. Bit *prog_rw* only needs to be cleared if data in the RAMs is to be read out through the serial interface.

Register bit *prog_sel(1)* selects between RAM A and RAM B when data is being written or read via the serial interface. This bit has no function when data is being read out to the DACs. Register bit *prog_sel(2)* allows the data to be written to both RAM A and RAM B simultaneously.

Register bit *prog_start* is used to indicate the start of a write cycle to the RAMs. This bit is self clearing. See section 3.2.2 for details of the write cycle.

3.2.2 Writing Data into the Memories

The process of writing data into the RAMs is controlled by the RAM Access Controllers, which expect data to be presented through the serial interface in a set sequence through the WMM [EVEN/ODD] RAM DATA registers.

The RAM Access Controllers will expect to receive the number of RAM data words specified in the register WMM [EVEN/ODD] RAM CTRL *prog_burst* field. If additional RAM data words are sent, the data will be ignored. However, if less than the specified number of data words is sent, the RAM Access Controller will not return to the idle state until the sequence has been completed by receipt of the correct number of RAM data words. This will corrupt the sequence in the RAM if the next RAM data word received is not intended for that RAM element. A write sequence may be terminated early with a software reset (see section 3.3).

The 64-bit wide WMM [EVEN/ODD] RAM DATA registers are used to transfer pre-formatted data into the RAM address location selected by the RAM Access Controller. See Table 18. The 14-bit DAC data should be MSB aligned to the 15th bit of the waveform sample (DAC data D14 aligned to waveform bit 14 [15:0], i.e. register bits 0, 15, 16, 31, 32, 47, 48, 63 etc. are not used).

Table 18: Waveform Memory Module Registers: WMM [EVEN/ODD] RAM DATA [0x13/0x23]

WMM EVEN RAM DATA (bits)	Label	Function
[15:0]	prog_data	Waveform EVEN sample word ***n***
[31:16]		Waveform EVEN sample word ***n+2***
[47:32]		Waveform EVEN sample word ***n+4***
[63:48]		Waveform EVEN sample word ***n+6***

WMM ODD RAM DATA (bits)	Label	Function
[15:0]	prog_data	Waveform ODD sample word ***n+1***
[31:16]		Waveform ODD sample word ***n+3***
[47:32]		Waveform ODD sample word ***n+5***
[63:48]		Waveform ODD sample word ***n+7***

The following sequence could be followed,

- write the first pre-formatted RAM data word to register WMM EVEN RAM DATA
- write to register WMM EVEN RAM CTRL with bit *prog_start* set
- consecutively write the remaining RAM data words to register WMM EVEN RAM DATA.

Once the RAM Access Controller returns to the idle state, after a successful write sequence, data transfer starts automatically. However, until the other RAM element is programmed and the RAMs are synchronised, the output sequence will be corrupt.

- repeat the above sequence for the ODD RAM element.

The order in which the EVEN/ODD RAMs are programmed is not important.

Once all of the required RAMs have been programmed, the RAM Access Controllers need to be set to 'run' and synchronised by a software reset, see Section 3.3. Finally, ensure that all ODD, EVEN and the WMM/LVDS data multiplexers are set appropriately. A worked example is given in section 6.5.4

Programming the WMM / LVDS data source multiplexer bit '*data_direct*' last will prevent incomplete and unsynchronised data reaching the DAC before it is required.

3.3 Software Reset

The Waveform Memory Module may be reset through a software reset function. This is activated through register BIST [EVEN/ODD] CONFIG bit *swrst*.

Table 19: WMM Register: WMM [EVEN/ODD] CONFIG [0x10/0x20] (Part 2 of 2)

WMM [EVEN/ ODD] CONFIG (bit)	Label	Function
0	swrst	Software reset control bit **0 = Normal operation (default)**, 1 = Software Reset

Two writes to '*swrst*' are required to produce a software reset; first setting (1) and then clearing (0). Writing to both ODD and EVEN registers (0x10 or 0x20) is not necessary as either register will synchronise all memories.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Supply voltage						
Analog supply		V_{AVD33}			3.6	V
Digital Supply		V_{DVDD}			2.0	V
Input Voltage						
LVDS inputs		V_{LVDS}	V_{DVSS}-0.5		V_{DVDD}+0.5	V
Digital control inputs		V_{CON}	V_{DVSS}-0.5		V_{DVDD}+0.5	V
Analog Output Voltage		V_O	V_{DVSS}-1		V_{DVDD}+0.5	V
Analog Output Current	1	I_O			+25	mA
Storage Temperature		T_{ST}	-40		+85	^oC
Junction Temperature		T_J	-40		+125	^oC

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V, I_{FS} = 20mA.
1. IOUT & IOUTB AVSS - 0.5V to AVD18 + 0.5V

4.2 Digital Interface Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
CMOS control inputs						
High-level input voltage		V_{IH}	1.2		V_{DVDD}	V
Low-level input voltage		V_{IL}	V_{DVSS}		0.6	V
CMOS control outputs						
High-level output voltage	1	V_{OH}	V_{DVDD} - 0.275			V
Low-level output voltage	2	V_{OL}			V_{DVSS} + 0.225	V
LVDS data inputs						
Common mode input voltage		V_{CM}	0.9		1.4	V
Differential input voltage		V_{ID}	100	350	600	mV
Setup time	3	t_s	-0.4	-0.6		ns
Hold time	3	t_h		0.9	1.4	ns

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V
1. I_{OH} = +4mA
2. I_{OL} = -4mA
3. Referenced to the input clock (CLKIN) & with dac_clk_dly = 0x00

4.3 DC Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
DC Accuracy						
Integral Non Linearity		INL		1.1	2.0	LSB_{14}
Differential Non Linearity		DNL		0.6	1.0	LSB_{14}
Analog output						
Full scale signal output current		I_{OP}		+20		mA
Current at each output			5	15	25	mA
Load resistance (single ended)		R_L		16.5	50	Ω
Output resistance				330		kΩ
Output capacitance				22		pF
Gain error				0.15		%FS
Output voltage (compliance) - Maximum			-1.0		+0.5	V
Output voltage (compliance) - Best performance			-0.8		+0.2	V
Output Power Supply Rejection Ratio		PSRR				
Due to variation in analog supply (External Vref)	1			0.01		%
Due to variation in analog supply (Internal Vref)	1			0.02		%
Internal Bandgap Reference						
Reference voltage		V_{BG}	1.15	1.2	1.25	V
Reference output current		I_{BG}	0		100	µA
Reference output voltage variation	1			0.01		%
External Reference Input						
Reference voltage		V_{REF}	1.10		1.30	V
Reference input current		I_{BG}	-1		+1	µA
Thermal						
Ambient Temperature		T_A	-40	25	+85	^oC
Storage Temperature		T_S	5		+30	^oC
Package Thermal Resistance						
Junction to PCB (top side)		θ_{J-PCB}		4		$^oC/W$
Junction to Ambient (estimate - PCB dependant)	2	θ_{JA}		20		$^oC/W$

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V, I_{FS} = 20mA.

1. V_{AVD33} (min) to V_{AVD33} (max)
2. Refer to Section 6.1

4.4 AC Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Spurious-Free Dynamic Range		SFDR				
Single tone at -1dBFS, 800MSa/s, DC to 400MHz	1					
20 MHz				75		dBc
40 MHz				72		dBc
70 MHz				66		dBc
140 MHz				62		dBc
300 MHz				58		dBc
Single tone at -1dBFS, 1GSa/s, DC to 500MHz	1					
20 MHz				84		dBc
40 MHz				80		dBc
70 MHz				76		dBc
140 MHz				68		dBc
300 MHz				61		dBc
Single tone at -1dBFS, 800MSa/s, DC to 400MHz	2					
20 MHz				84		dBc
40 MHz				79		dBc
70 MHz				75		dBc
140 MHz			70	76		dBc
300 MHz				72		dBc
Single tone at -1dBFS, 1GSa/s, DC to 500MHz	2					
20 MHz				84		dBc
40 MHz				81		dBc
70 MHz				77		dBc
140 MHz				73		dBc
300 MHz				74		dBc
Single tone at -1dBFS, 800MSa/s, ±100MHz						
300 MHz				79		dBc
Inter-Modulation Distortion	3	IMD				
4 tones, ea. -12dBFS, missing centre tone at						
70MHz				89		dBc
140MHz			75	85		dBc
255MHz				75		dBc

Parameter (Continued)	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Adjacent Channel Leakage Ratio		ACLR				
1 x UMTS carrier, 5MHz channel spacing						
30.72MHz centre frequency, 245.76MSa/s				84		dBc
276.48MHz centre frequency, 737.28MSa/s				76		dBc
4 x UMTS carriers, 5MHz channel spacing						
276.48MHz centre frequency, 737.28MSa/s			69	74		dBc
Images						
Interleaved DAC image		$F_{clk} - F_{sig}$		40	30	dBc
2nd order interleaved DAC image		$F_{clk} - 2.F_{sig}$		57	50	dBc

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V, I_{FS} = 20mA, Differential Transformer coupled output presenting 33Ω effective differential load, Filtered Sinewave clock unless otherwise specified.

1. Excludes f_{clk} & f_{clk}-f_{out} image
2. Excludes f_{clk}, f_{clk}-f_{out} & f_{clk}-2.f_{out} images
3. 240kHz tone spacing with non-aligned phase alignment. Peak to rms = 6.4dB. 800MSa/s

4.5 Dynamic Performance

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Analog Output						
CLK In to Analog Out delay (to 0.1%)		t_o		4.1		ns
Output settling time (to 0.1%)		t_{set}		1.8		ns
Output rise time (10% to 90%)		t_r		0.6		ns
Output fall time (90% to 10%)		t_f		0.6		ns
Noise Floor						
Single tone at -1dBFS, 624MSa/s						
20 MHz tone				-166		dBm/Hz
247 MHz tone				-159		dBm/Hz
300 MHz tone	1			-156		dBm/Hz
Clock feed-through		F_{clkop}		-46	-42	dBm
Crosstalk	2		64	67		dBc

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V, I_{FS} = 20mA, Differential Transformer coupled output presenting 33Ω effective differential load, Filtered Sinewave clock unless otherwise specified.

1. In SNR terms compares to -159dBm/Hz for 500MSa/s DAC or -163dBm/Hz for 400MSa/s.
2. Measured using 4 tone test, each tone at -15dBFS with 1.2MHz spacing, centred at 276MHz ±4MHz

4.6 Clock Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Clock Input						
Maximum clock frequency		F_{clk}	500	600		MHz
Square Wave						
Low time		t_{LO}	0.95	1		ns
High time		t_{HI}	0.95	1		ns
Slew rate for minimum wide-band jitter		t_{SL}	0.5			V/ns
Clock input duty cycle	1			50		%
Low-level input voltage		V_{IL}	V_{DVSS} - 200mV			V
High-level input voltage		V_{IH}			V_{DVDD} + 200mV	V
Sinusoidal (recommended)						
Common mode input voltage		V_{CM}	0.9	1.2	1.8	V
Signal level (f_{Clk} = 312MHz)	2		-2	4	+10	dBm
Clock Outputs (LVDS)						
Common mode output voltage	3	V_{CM}	0.5	1.1	1.2	V
Differential output voltage	3 & 4	V_{OD}	320	350	550	mV
Delay, CLKIN to CLKx_OUT	5	t_{CLKO}		2.9		ns
Jitter added, CLKIN to CLKx_OUT (rms)	6			5		ps
Jitter added, CLKIN to CLKx_OUT (pk-pk)	6			30		ps
Loop Clock (LVDS)						
Delay, LPCLK_IN to LPCLK_OUT	7	t_{LPLCLK}		1.3		ns

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V

1. Ensure clock input symmetry to obtain best performance. Deviation from this will increase Fclk related images.
2. Power into 100R termination.
3. Also applies to Loop Clock Output.
4. R_T = 50Ω (double 100Ω termination) across the LVDS Q and $\overline{Q}$ signals.
5. Assumes 'clkoutx_clk_dly' is set to its minimum (default) setting.
6. At 500MHz. Assumes 'clkoutx_clk_dly' is set to its minimum (default) setting.
7. Assumes 'loop_clk_dly' is set to its minimum (default) setting.

CAUTION

ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

4.7 Serial Interface Timing Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Serial Clock Frequency	1	F_{sclk}	0		10	MHz
Serial Clock Mark or Space			20			ns
Setup, SERIAL_IN to SERIAL_CLK rising edge		t_{sisu}	3			ns
Hold, SERIAL_IN from SERIAL_CLK rising edge		t_{sihld}	3			ns
Delay, SERIAL_CLK to SERIAL_OUT valid		t_{sov}	4		22	ns

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V

1. When programming the WMM on-chip memories $F_{clk} > 16 \times F_{sclk}$ for correct operation.

4.8 Power Consumption

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Power Supply	1					
Analog Supply (AVD33)		V_{AVD33}	3.1	3.3	3.5	V
Single DAC, 500MHz / 1GSa/s, LVDS data	2	I_{AVD33}		83	106	mA
Dual DAC, 500MHz / 1GSa/s, LVDS data	2			140	179	mA
Digital Supply (DVDD)		V_{DVDD}	1.7	1.8	1.9	V
Single DAC, 500MHz / 1GSa/s, LVDS data	2	I_{DVDD}		265	338	mA
Dual DAC, 500MHz / 1GSa/s, LVDS data	2, 3			460	587	mA
Power Dissipation	1, 4	P_D				
Single DAC, 400MHz / 800MSa/s, LVDS data				650	755	mW
Dual DAC, 400MHz / 800MSa/s, LVDS data				1,120	1,300	mW
Single DAC, 500MHz / 1GSa/s, LVDS data				750	870	mW
Dual DAC, 400MHz / 800MSa/s, WMM mode				1,660	1,865	mW

T_A (min) to T_A (max), AVD33 = +3.3V, AVSS = 0V, DVDD = +1.8V, DVSS = 0V, I_{FS} = 20mA.

1. Current consumption and Power dissipation are data related. Maximum figures are by evaluation.
2. See Figure 17.
3. With WMM enabled power consumption is ~ +76mA / 100MHz (Typ.) +86mA / 100MHz (Max.)
4. See Figure 18.

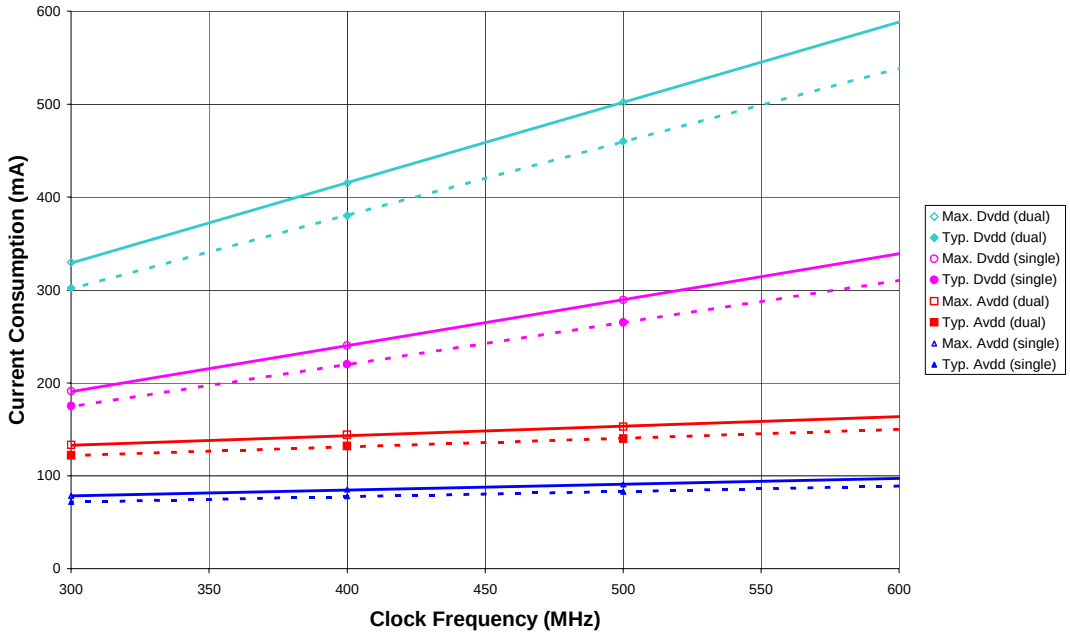


Figure 17 Current Consumption

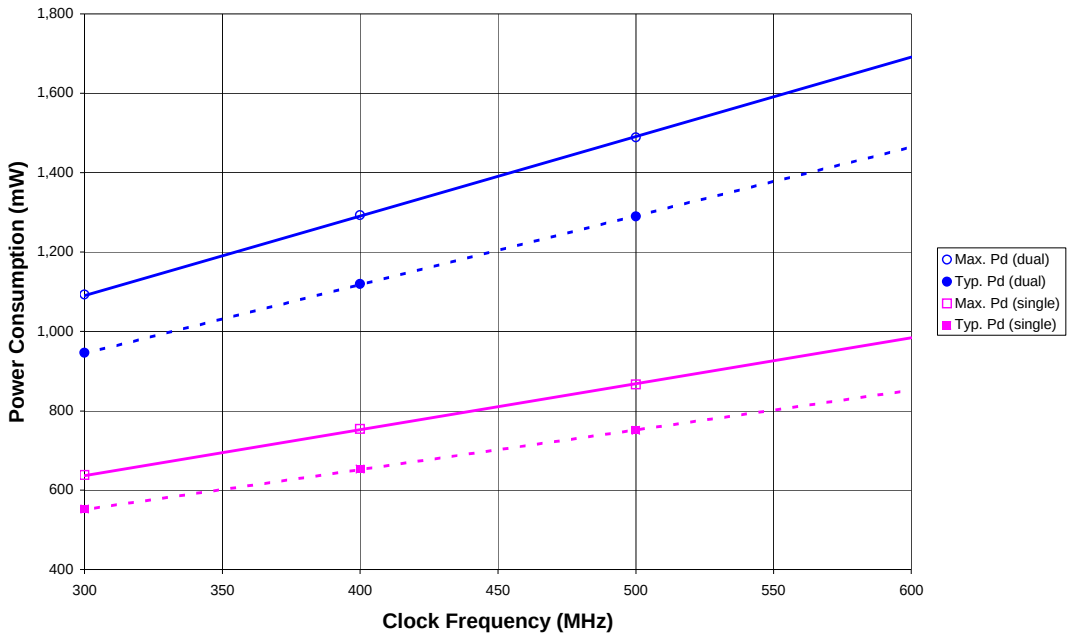
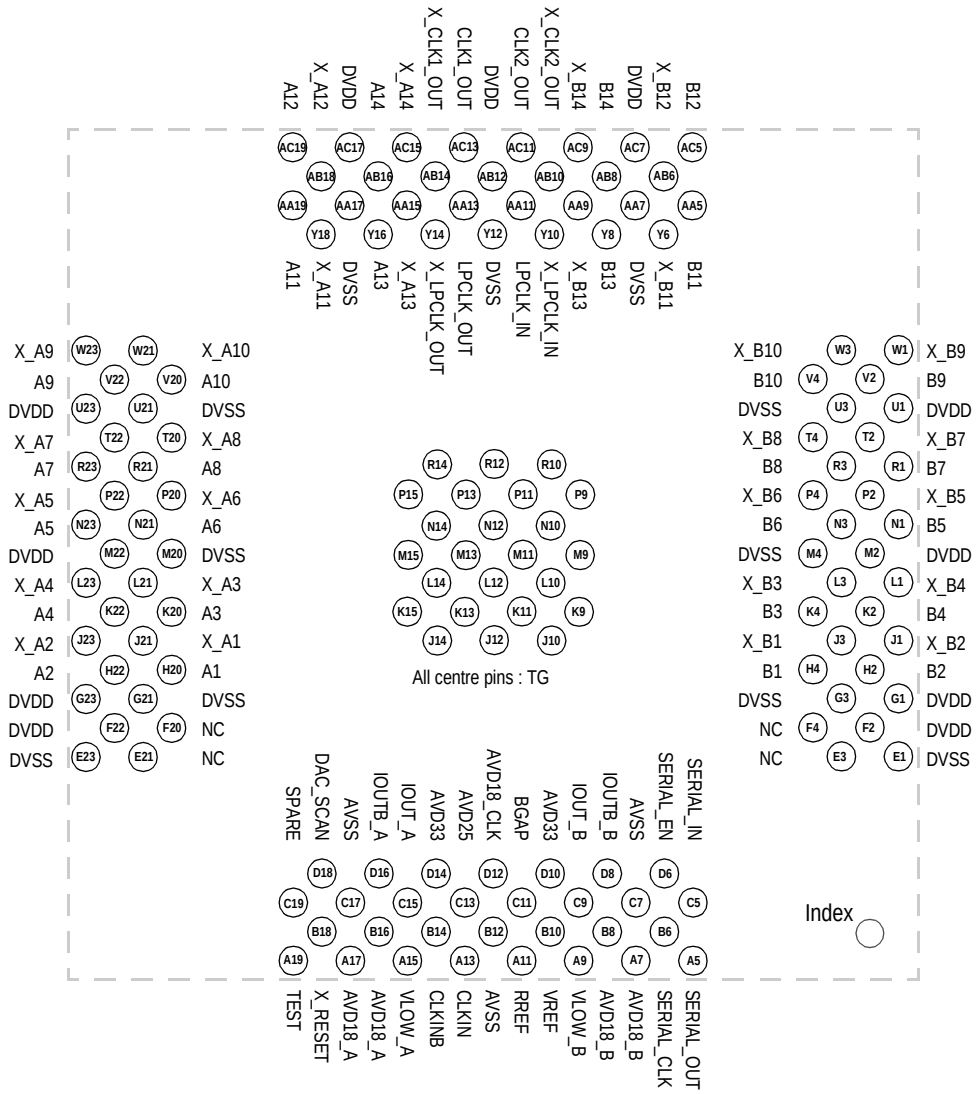


Figure 18 Power Consumption

5 Mechanical Data

5.1 Pin Assignment



Not to scale. Viewed from above.

5.2 Pin Definition

Analog and Clock Interface

Pin Nos.	Pin Name	Input/ Output	Description	Note
D10, D14	AVD33	Power	Analog positive supply, +3.3V	Decouple to AVSS
B16, A17	AVD18_A	O	DAC 'A' internal 1.8V regulator output	Decouple to AVSS
A7, B8	AVD18_B	O	DAC 'B' internal 1.8V regulator output	Decouple to AVSS
D12	AVD18_CLK	O	Input clock internal 1.8V regulator output	Decouple to AVSS
C7, B12, C17	AVSS	Power	Analog ground, 0V	
C15	IOUT_A	O	Positive Analog output, DAC 'A'	
D16	IOUTB_A	O	Negative Analog output, DAC 'A'	
C9	IOUT_B	O	Positive Analog output, DAC 'B'	
D8	IOUTB_B	O	Negative Analog output, DAC 'B'	
C11	BGAP	O	Bandgap reference output	Refer to section 1.4
B10	VREF	I	Voltage reference input	Refer to section 1.4
A11	RREF	O	Analog output current reference resistor	Refer to section 1.5
C13	AVD25	O	Regulated 2.5V output (supply for external voltage reference)	Decouple to AVSS
A15	VLO_A	O	DAC 'A' clock reference level	Decouple to AVD18_A
A9	VLO_B	O	DAC 'B' clock reference level	Decouple to AVD18_B
A13	CLKIN	I	Clock input, positive input	Requires biasing - Refer to section 6.2
B14	CLKINB	I	Clock input, negative input	
AC13	CLK1_OUT	O	LVDS output clock #1, positive output	Use double termination
AB14	X_CLK1_OUT	O	LVDS output clock #1, negative output	
AC11	CLK2_OUT	O	LVDS output clock #2, positive output	Use double termination
AB10	X_CLK2_OUT	O	LVDS output clock #2, negative output	
AA11	LPCLK_IN	I	LVDS calibration loop clock, positive input	
Y10	X_LPCLK_IN	I	LVDS calibration loop clock, negative input	
AA13	LPCLK_OUT	O	LVDS calibration loop clock, positive output	Use double termination
Y14	X_LPCLK_OUT	O	LVDS calibration loop clock, negative output	

Thermal / Ground Array

Pin Nos.	Pin Name	Input/ Output	Description	Note
J10, J12, J14, K9, K11, K13, K15, L10, L12, L14, M9, M11, M13, M15, N10, N12, N14, P9, P11, P13, P15, R10, R12, R14	TG	-	Thermal / Ground array connection	Connect to the DVSS digital ground plane

Digital Data Interface

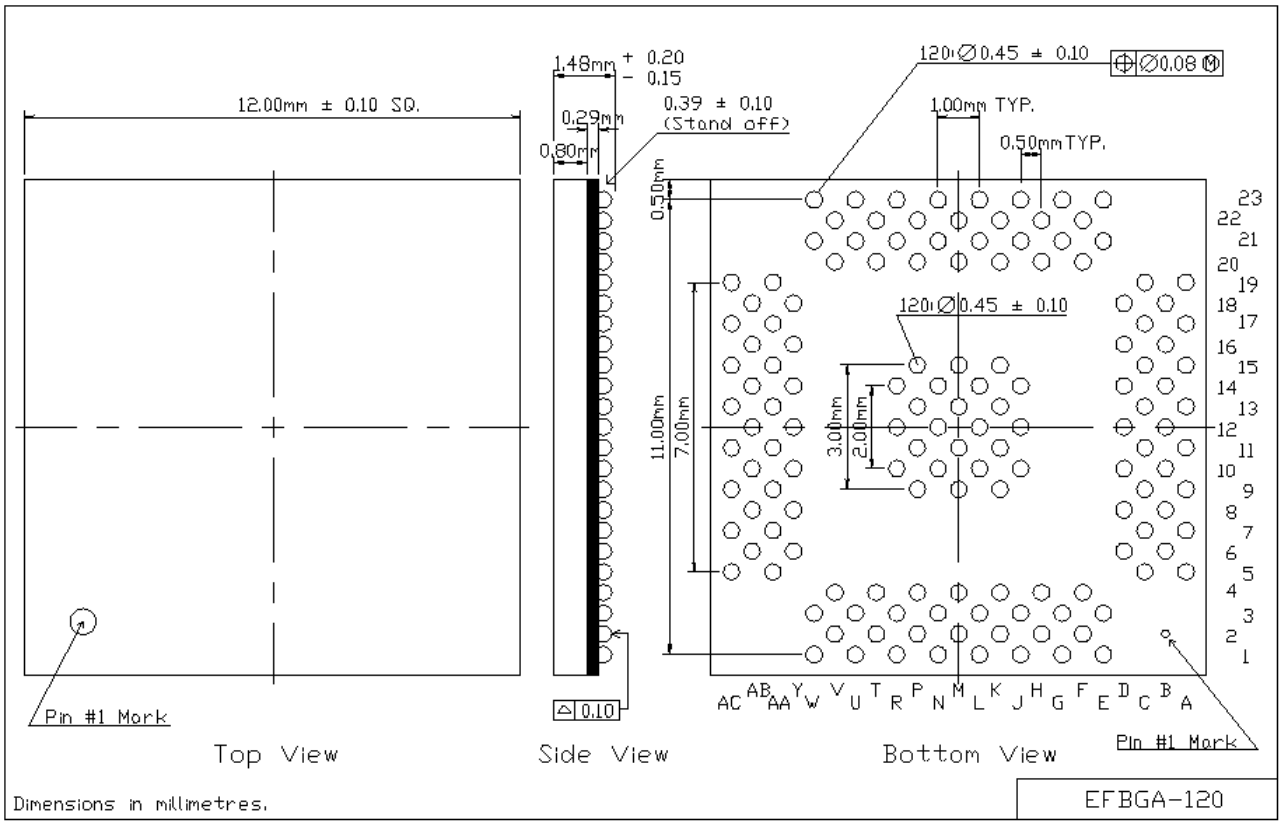
Pin Nos.	Pin Name	Input/ Output	Description	Note
F2, F22, G1, M2, U1, AC7, AB12, AC17, U23, M22, G23	DVDD	Power	Digital positive supply, +1.8V	Decouple to DVSS. N.B. F2 & F22 are not power supplies but should be connected to DVDD.
E1, E23, G3, M4, U3, AA7, Y12, AA17, U21, M20, G21	DVSS	Power	Digital Ground, 0V	N.B. E1 & E23 are not power supplies but should be connected to DVSS.
H20	A1	I	DAC 'A' bit 1 LVDS positive input	LSB
J21	X_A1	I	DAC 'A' bit 1 LVDS negative input	
H22	A2	I	DAC 'A' bit 2 LVDS positive input	
J23	X_A2	I	DAC 'A' bit 2 LVDS negative input	
K20	A3	I	DAC 'A' bit 3 LVDS positive input	
L21	X_A3	I	DAC 'A' bit 3 LVDS negative input	
K22	A4	I	DAC 'A' bit 4 LVDS positive input	
L23	X_A4	I	DAC 'A' bit 4 LVDS negative input	
N23	A5	I	DAC 'A' bit 5 LVDS positive input	
P22	X_A5	I	DAC 'A' bit 5 LVDS negative input	
N21	A6	I	DAC 'A' bit 6 LVDS positive input	
P20	X_A6	I	DAC 'A' bit 6 LVDS negative input	
R23	A7	I	DAC 'A' bit 7 LVDS positive input	
T22	X_A7	I	DAC 'A' bit 7 LVDS negative input	
R21	A8	I	DAC 'A' bit 8 LVDS positive input	
T20	X_A8	I	DAC 'A' bit 8 LVDS negative input	
V22	A9	I	DAC 'A' bit 9 LVDS positive input	
W23	X_A9	I	DAC 'A' bit 9LVDS negative input	
V20	A10	I	DAC 'A' bit 10 LVDS positive input	
W21	X_A10	I	DAC 'A' bit 10 LVDS negative input	
AA19	A11	I	DAC 'A' bit 11 LVDS positive input	
Y18	X_A11	I	DAC 'A' bit 11 LVDS negative input	
AC19	A12	I	DAC 'A' bit 12 LVDS positive input	
AB18	X_A12	I	DAC 'A' bit 12 LVDS negative input	
Y16	A13	I	DAC 'A' bit 13 LVDS positive input	
AA15	X_A13	I	DAC 'A' bit 13 LVDS negative input	
AB16	A14	I	DAC 'A' bit 14 LVDS positive input	MSB
AC15	X_A14	I	DAC 'A' bit 14 LVDS negative input	
H4	B1	I	DAC 'B' bit 1 LVDS positive input	LSB
J3	X_B1	I	DAC 'B' bit 1 LVDS negative input	
H2	B2	I	DAC 'B' bit 2 LVDS positive input	
J1	X_B2	I	DAC 'B' bit 2 LVDS negative input	
K4	B3	I	DAC 'B' bit 3 LVDS positive input	
L3	X_B3	I	DAC 'B' bit 3 LVDS negative input	
K2	B4	I	DAC 'B' bit 4 LVDS positive input	

Pin Nos.	Pin Name	Input/ Output	Description	Note
L1	X_B4	I	DAC 'B' bit 4 LVDS negative input	
N1	B5	I	DAC 'B' bit 5 LVDS positive input	
P2	X_B5	I	DAC 'B' bit 5 LVDS negative input	
N3	B6	I	DAC 'B' bit 6 LVDS positive input	
P4	X_B6	I	DAC 'B' bit 6 LVDS negative input	
R1	B7	I	DAC 'B' bit 7 LVDS positive input	
T2	X_B7	I	DAC 'B' bit 7 LVDS negative input	
R3	B8	I	DAC 'B' bit 8 LVDS positive input	
T4	X_B8	I	DAC 'B' bit 8 LVDS negative input	
V2	B9	I	DAC 'B' bit 9 LVDS positive input	
W1	X_B9	I	DAC 'B' bit 9 LVDS negative input	
V4	B10	I	DAC 'B' bit 10 LVDS positive input	
W3	X_B10	I	DAC 'B' bit 10 LVDS negative input	
AA5	B11	I	DAC 'B' bit 11 LVDS positive input	
Y6	X_B11	I	DAC 'B' bit 11 LVDS negative input	
AC5	B12	I	DAC 'B' bit 12 LVDS positive input	
AB6	X_B12	I	DAC 'B' bit 12 LVDS negative input	
Y8	B13	I	DAC 'B' bit 13 LVDS positive input	
AA9	X_B13	I	DAC 'B' bit 13 LVDS negative input	
AB8	B14	I	DAC 'B' bit 14 LVDS positive input	MSB
AC9	X_B14	I	DAC 'B' bit 14 LVDS negative input	

Digital Control Interface

Pin Nos.	Pin Name	Input/ Output	Description	Note
B18	X_RESET	I	Device reset	'0' = reset
C5	SERIAL_IN	I	Serial interface serial data input	
A5	SERIAL_OUT	O	Serial interface serial data output	
B6	SERIAL_CLK	I	Serial interface serial data clock	
D6	SERIAL_EN	I	Serial interface enable	
D18	DAC_SCAN	I	Fujitsu test pin	Connect to DVSS
C19	SPARE	I	Fujitsu test pin	Connect to DVSS
A19	TEST	I	Fujitsu test pin	Connect to DVSS
E21	NC	-	No connect	
E3	NC	-	No connect	
F4	NC	-	No connect	
F20	NC	-	No connect	

5.3 Package Data



Dimensions in millimetres. **Ball array viewed from below**.

Important: This device requires pre-baking at 125°C (257°F) for 24 hours before mounting unless removed from approved vacuum sealed packaging just prior to assembly.

5.4 Ordering Information

The following reference should be used when ordering devices,

- MB86064PB-G
- MB86064PB-GE1 Lead-free package variant

Shipment is in plastic trays, each capable of holding 168 devices.

For further assistance please contact your Fujitsu Microelectronics' sales representative.

6 Application Notes

6.1 PCB Power & Ground Plane Splits and Decoupling

The following guidelines are suggestions to help obtain best performance from the MB86064. The information may be subject to change.

The ground plane should not be split into the digital and analog regions. The digital and analog power planes must be split as these are different voltages.

Even though a common ground plane is recommended, ‘analog’ and ‘digital’ grounds should not be linked on the top surface of the PCB even where this may appear convenient to do so. Use separate vias to connect directly to the common ground plane.

All supplies should be decoupled using surface mount 100nF to 1µF capacitors, placed as close as possible to the device. For each pair of DVDD/DVSS pins it is recommended that the capacitor is located on the reverse of the PCB, immediately under the device, with vias to the supply and ground planes as close as possible to the device and capacitor. This layout minimizes tracking, including the plated through hole, and hence keeps loop inductance to a minimum. See Figure 19 (0603 size capacitors used).

For the analog supplies, the decoupling scheme in Figure 19 should be used. This scheme uses seven 0603 100nF capacitors. This allows the decoupling capacitors, that also need to be placed close to the device, to be fitted into a small area.

Deviation from the layout in Figure 19 is not recommended as the device pinout has been carefully developed alongside this PCB design to give optimum performance. For single component-sided PCB designs all decoupling capacitors should be placed in a ring around the edge of the device as close as the assembly process will allow. The position of the capacitors should be such as to minimise the distance from the ball, and the tracking must run directly from the supply ball to the capacitor. Positioning the decouplers close to the device is the highest priority layout consideration. Of the analog decouplers, the VREF to AVSS 100nF capacitor has the lowest priority (so is not shown in Figure 19), however this decoupler should be positioned as close as reasonably practical to the device.

Tracking and vias should be excluded from the zone highlighted in Figure 19(a). This recommendation is to maximise separation between LVDS data bits in proximity of the analog outputs.

The central array of thermal/ground balls should be connected directly to the ground plane. This array has two functions. Firstly it connects the substrate to the ground plane that is most able to collect the noise from the mostly digital regions of the die. Secondly, the thermal array is used to conduct heat directly out of the die and into the PCB ground plane for heat spreading. The design of the PCB around the thermal/ground array is critical for maximum heat transfer and ground plane integrity.

A Fujitsu Design Guide, ‘PCB Design Rules for EFBGA Packages’, document number FME/MS/APPS/DG/4568, provides a detailed description of the recommended PCB design principles for this package.

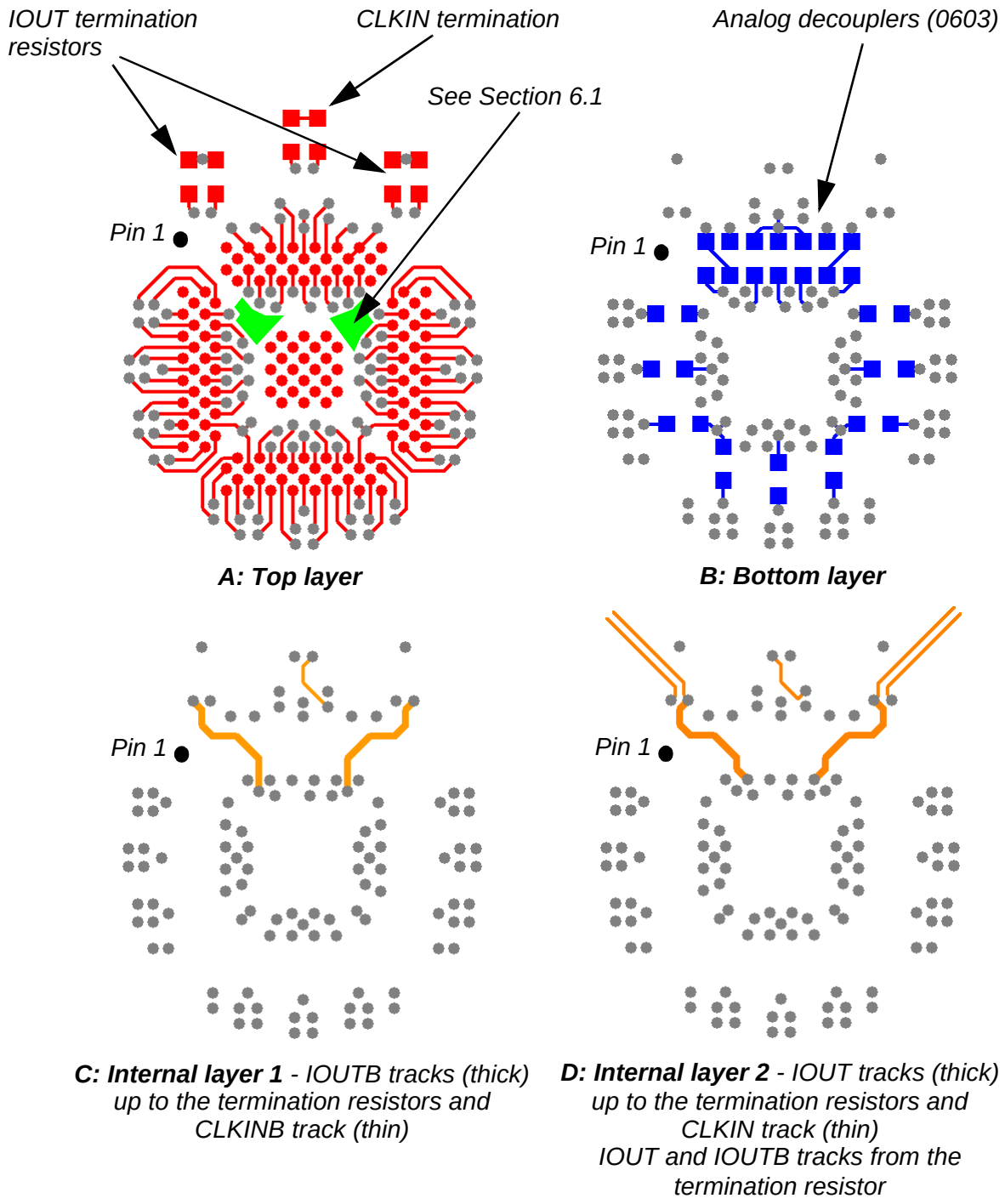


Figure 19 Recommended PCB layout (All plots viewed from above)

6.2 Input Clock Interfacing

The differential clock input to the device needs to be biased about the specified typical common mode input voltage. The exact interface circuitry will depend on the functionality required but an example is illustrated in Figure 20.

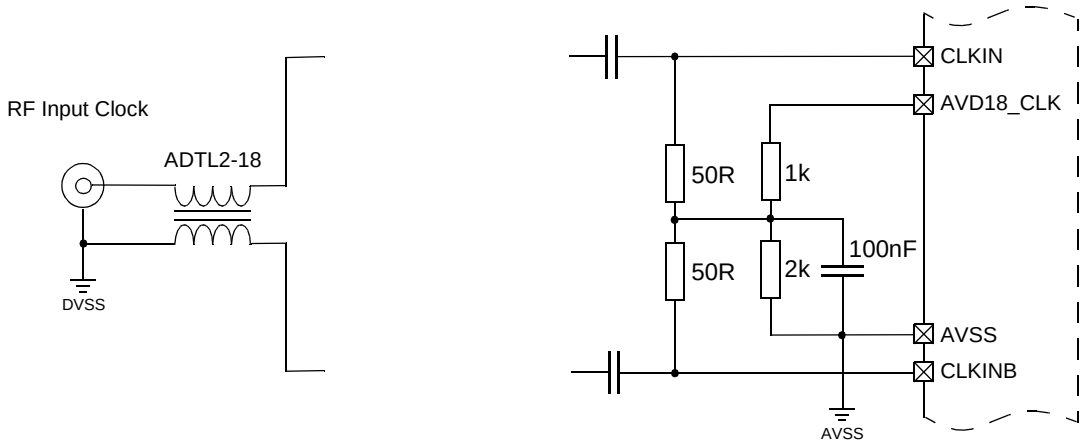


Figure 20 Clock Input Interfacing

In most applications an external single-ended RF clock will not be used and a differential PECL clock could be connected directly to the AC-coupling capacitors.

The above circuit utilises the on-chip regulated 1.8V supply, combined with the 1k/2k resistive divider, to generate a 1.2V common mode voltage. This could easily have been applied to the clock signals through higher value resistors, e.g. 4k7, in place of the 50R termination resistors. In this instance a 100R differential load should be added.

Where adjustment to the clock DC offset is required a trim-pot or trim-DAC could be included as part of the 1k/2k potential divider circuit.

6.3 Clock Duty Cycle Optimisation

Earlier sections of this data sheet document that the DAC core is clocked on both rising and falling edges of the input clock, and that a characteristic of this architecture is suppressed images of the generated signal relating to Fclk. Any duty cycle error in the input clock will exacerbate the Fclk-Fsig image. This can be minimised by using a filtered, sinusoidal clock and if necessary trimming the differential DC offset.

Applications using a square wave clock are unlikely to achieve the 50:50 duty cycle necessary to deliver best wide-band spurious performance. Measurements and calculations show that for an output at 3/8Fdac a duty cycle error of 1% (49:51) gives 32dBc rejection. In cases where maximal suppression of the Fclk-Fsig image is required it is recommended to either filter the clock or implement a tuned circuit as part of the clock routing.

A band-pass filter can be used but a low-pass response allows for some variation in clock frequency to be accommodated. A key target of the filter is to suppress the second harmonic by 40dB. This will reduce the duty cycle error by approximately 100 times, or in other words to a negligible level. For most applications a third order L-C filter should meet these requirements. It is important to ensure that the resultant clock amplitude meets the required specification otherwise phase noise will increase due to reduced slew rate.

An alternative is to construct a tuned circuit by linking CLK to CLKB with two 50Ω delay lines, one at the clock source and the other at the DAC. The delay time required is equivalent to one half of a clock period. The delay line links will need to be AC coupled from the clock source if a DC short is not supported. Similarly, AC coupling with appropriate biassing, prior to the DAC input, would be necessary where trimming of the differential DC offset is required. This approach has also demonstrated a reduction in duty cycle error by approximately 100 times. The two delay lines can be implemented in the PCB tracking. The length of tracking required depends on the PCB signal propagation speed. For example, a delay of 1.35ns would be used in system operating at a clock frequency of about 370MHz, and would be realised with a PCB track length of about 27cm, assuming 5ns/m propagation speed on the PCB. Tracking the delay would be by zig-zagging backwards and forwards on a spare inner layer. The two delay lines must be separated by PCB tracks sufficiently long that a clock edge finishes exiting the first delay line before entering the second, i.e. td > tr, or spacing > 10cm for tr=0.5ns.

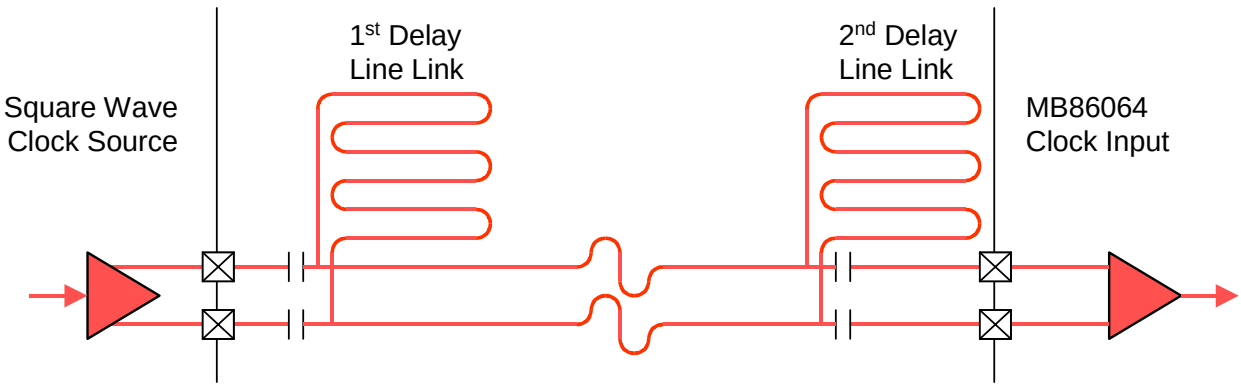


Figure 21 Clock Duty Cycle Optimisation using Delay Line Links

6.4 Analog Output Interfacing

6.4.1 Transformer Coupled Output Circuit

The recommended analog output circuit is a two stage transformer circuit that provides both isolation from the analog ground plane and excellent common-mode rejection, whilst providing the required differential to single-ended conversion. The recommended transformers are a Mini-Circuits (www.minicircuits.com) ADTL1-4-75 transmission line transformer, and an ADT1-1WT balun. See Figure 22. For best performance the DAC output expects to see a low impedance load.

When considering the recommended circuit, it is important to note that transformer ADT1-1WT is not exactly 1:1 turns ratio. Instead, when a 50Ω load is attached to its secondary winding, a primary impedance of approx. 68Ω is exhibited. Hence, each DAC output sees 33Ω/34Ω in parallel with 34Ω, i.e. approx. 16.5Ω/17Ω. See Figure 22.

The primary load can either be two 33Ω precision resistors to ground or a bridged single 68Ω resistor.

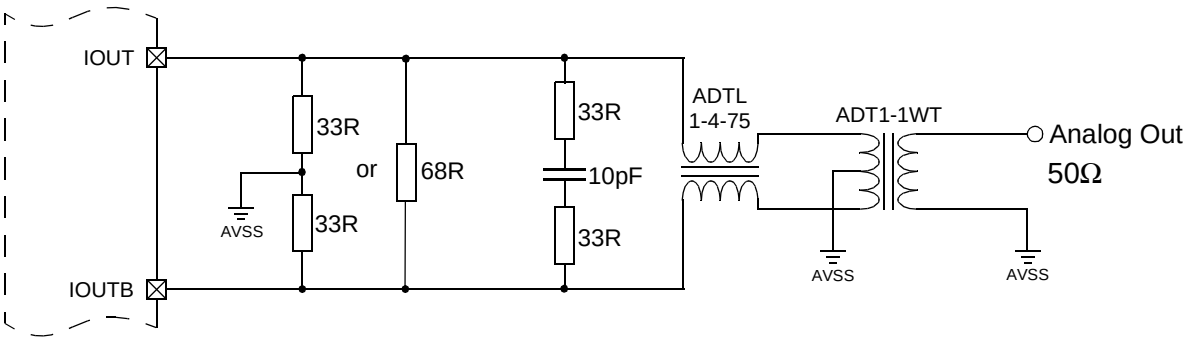


Figure 22 Recommended Transformer Coupled Analog Output Circuit

The primary load resistor(s) should be positioned as close as possible to the IOUT and IOUTB balls, only second in layout priority to the analog decoupling capacitors. The tracking between the DAC and the resistor(s) should be very closely coupled, ideally as a broadside coupled stacked differential pair positioned between two ground planes, with low (approx. 33Ω) differential impedance tracking. Where two single-ended load resistors are used these should be closely matched to maximise CMRR.

The tracking from the termination resistors to the transformer should also be closely coupled, but now routed adjacent to a ground plane as an edge coupled differential pair for best impedance matching. Special attention should be paid to the routing of these tracks. The tracks must always be routed as a matched pair and be equal in length. The routing of these tracks should avoid coming into close proximity to any power or signal tracks, plane edges or even vias that may cause more noise to be induced onto one of the tracks than the other. Switching routing layers should be avoided, but if

necessary, the ground planes that the signals use as a reference plane must be linked together with vias next to the signal vias so that the return currents in the ground plane do not have to travel any distance away from the signal tracks when switching ground layers.

The RCR network, shown in Figure 22, is to compensate for the ADT1-1WT transformer becoming inductive at high frequencies. The 10pF capacitor can be replaced with a variable capacitor to allow optimisation of overshoot at the transformer input. However, this may not be required in all instances, particularly frequency domain applications, since it increases in-band roll-off. For direct-IF, bandpass applications it may be possible to tune out the DAC's output capacitance, Cout, by resonating it with a parallel inductor. For example, about 16nH to GND at each output or 33nH between the outputs for a ~270MHz IF (assuming ideal resistive load). The ADTL1-4-75 transmission line transformer may be removed to simplify the circuit, but this will reduce high frequency rejection of common-mode noise and may reduce system performance in some applications.

For either higher impedance or DC coupled loads it is important to note that the output voltage compliance range for best performance is symmetrical about -0.3V not 0V.

6.4.2 Direct Interface to Quadrature Modulator

Some applications require a DC shift in order to interface the DAC output directly to components such as a quadrature modulator. Traditionally this is not an easy challenge without impacting noise and distortion. However, it may be possible to achieve the optimum operating point of both components by off-setting supply rails/domains. For example, consider a modulator that normally runs on a +5V supply and requires a +1.5V DC bias at its baseband inputs. Whereas the optimum DC bias at the DAC output (for maximum signal swing) is -0.3V.

By shifting the modulator supply to operate between +3.3V (already needed for the DAC) and -1.8V (at all GND pins) supplies, providing a total and acceptable 5.1V supply, all that is needed is appropriate termination resistors at the DAC output, split between 0V and -1.8V, to give the correct -0.3V DC bias at the DAC output and meet the optimal +1.5V DC bias, relative to its VSS pins, at the modulator input.

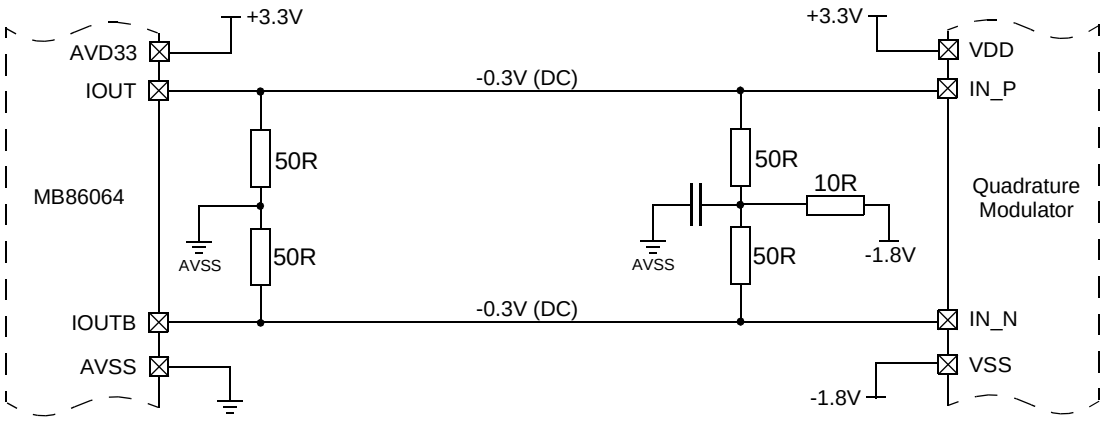


Figure 23 Suggested Direct Interface to Quadrature Modulator

6.5 Example Setup Register Settings

The following sections provide examples of typical configurations for the MB86064 and required register settings. In all cases other registers are assumed to be at their default values, following a device reset.

6.5.1 Dual DAC, LVDS data, Clock Outputs enabled

	Address	Data	Note
•	0x1B2	0x0000000	set recommended DAC core delay settings
•	0x1C3	0x00001C0	power up device and enable clock outputs

6.5.2 Single DAC, LVDS data port A, driving DAC A

	Address	Data	Note
•	0x1B2	0x0000000	set recommended DAC core delay settings
•	0x1C0	0x0000002	set Iref for DAC A only configuration
•	0x1C3	0x0000BC0	power up DAC A and enable clock outputs

6.5.3 Multiplexed LVDS data into DAC A (A=EVEN, B=ODD)

	Address	Data	Note
•	0x00	0x10	set WMM/LVDS data mux to WMM
•	0x21	0x01	set ODD Mux0 = Mux1 data
•	0x1B2	0x0000000	set recommended DAC core delay settings
•	0x1C0	0x0000002	set Iref for DAC A only configuration
•	0x1C3	0x00009C0	power up data ports, DAC A and clock outputs
•	0x1C4	0x0000080	enable WMM clock (bit #1 to ‘0’)

6.5.4 Waveform Memory Module, Different A & B Waveforms

	Address	Data	Note
•	0x10	0x00	enable EVEN memory
•	0x20	0x00	enable ODD memory
•	0x1B2	0x0000000	set recommended DAC core delay settings
•	0x1C3	0x00007E0	power up both DACs, disable LVDS ports
•	0x1C4	0x0000081	enable WMM clock, disable clock outputs

```
• {load waveform data into memories, start addr=0 length=2047(0x7FF)}
• {this length corresponds to a vector length of 16k points}
• 0x13      0xXXXXXXX    {write first data word}
• 0x12      0x27FF800    program RAM controller: RAM A, EVEN, write
• 0x13      0xXXXXXXX    {write next data word}
• {repeat above instruction 2045 times}
• 0x13      0xXXXXXXX    {write last data word}

• 0x23      0xXXXXXXX    {write first data word}
• 0x22      0x27FF800    program RAM controller: RAM A, ODD, write
• 0x23      0xXXXXXXX    {write next data word}
• {repeat above instruction 2045 times}
• 0x23      0xXXXXXXX    {write last data word}

• {Repeat for RAM B}

• 0x12      0x07FF800    program RAM controller: RAM A, EVEN, run
• 0x12      0x0FFF800    program RAM controller: RAM B, EVEN, run
• 0x22      0x07FF800    program RAM controller: RAM A, ODD, run
• 0x22      0x0FFF800    program RAM controller: RAM B, ODD, run

• 0x11      0x33         set EVEN Mux0 = Mux1 = RAM data
• 0x21      0x33         set ODD Mux0 = Mux1 = RAM data
• 0x10      0x01         set software reset to sync RAMs
• 0x10      0x00         clear software reset to sync RAMs
• 0x00      0x10         set WMM/LVDS data mux to WMM
```

6.6 Technical Support

Requests for technical support on the MB86064 may be e-mailed to:

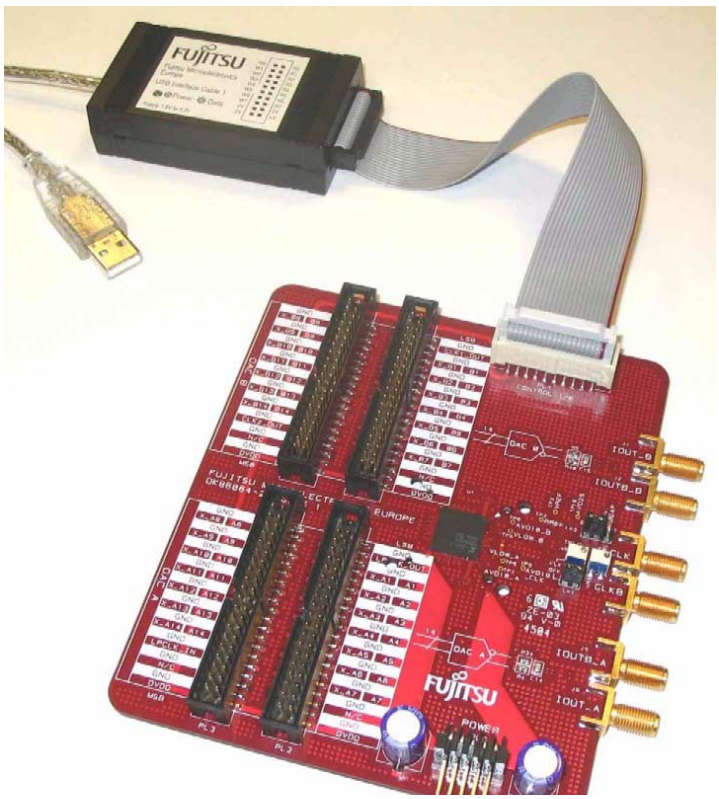
- msd.support@fme.fujitsu.com

7 Development Kit

A development kit, reference DK86064-2, is available for the MB86064 Dual 14-bit 1GSa/s DAC. This comprises an evaluation board for the MB86064 and a PC programming cable with associated software. Connections for all analog signals are via SMA connectors, allowing instruments to be connected using standard cables. All digital I/O signals are routed to four 2-row 0.1” headers, allowing the board to be connected to a suitably designed customer’s board if required.

The DK86064-2 Development Kit includes,

- Evaluation board with MB86064 device fitted
- USB programming cable for control of the DAC from a host PC
- Windows PC based control software
- Shielded power supply cable
- User manual



To convert the 2-row 0.1” data headers on to SMA style connectors, an optional adaptor kit is available,

- DK86064-1-SMA

In addition to the complete development kit, key modules are available individually,

- DKUSB-1
    - PC USB Programming cable and control software

For further assistance, including price and availability of the development kits, please contact your Fujitsu sales representative.

7.1 Using DKUSB-1 in Target Applications

It is expected that customers can benefit from using Fujitsu's PC USB Programming cable and accompanying PC software, DKUSB-1, for debug of prototype target applications. To facilitate this it is recommended that an appropriate connector is fitted to the target board, providing connections to the following signals as a minimum,

- DVDD (+1.8V)
- DVSS
- SERIAL_IN
- SERIAL_OUT
- SERIAL_CLK
- SERIAL_EN
- X_RESET

An interface cable will need to be assembled to connect from the board to the 10 x 2 row 0.1" header on the PC USB cable control box.

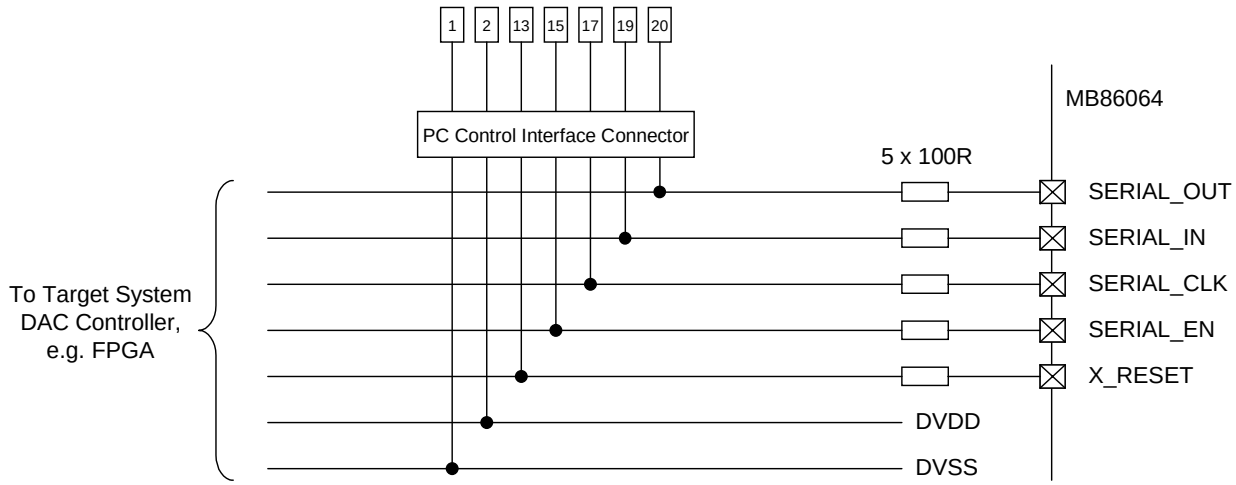


Figure 24 Recommended Application PC Control Interface Connector

This will allow full control of the MB86064 either prior to implementation of the target system DAC controller or to assist with initial debug of the DAC circuitry. Full access to configuration registers as well as the WMM is possible.

Appendix A Default Register Settings

Appendix A.1 DAC Core Registers

Register	Address	Register Bits																											
		27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC A	190_{16}																					[7:0]							
THOLD	01 1001 0000																					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
DAC A	191_{16}	[27:21]							[20:14]							[13:7]						[6:0]							
SEED	01 1001 0001	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
DAC B	$1A0_{16}$																					[7:0]							
THOLD	01 1010 0000																					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
DAC B	$1A1_{16}$	[27:21]							[20:14]							[13:7]						[6:0]							
SEED	01 1010 0001	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
DAC CORE	$1B2_{16}$																			9	8	[7:4]				[3:0]			
CLOCK DELAYS	01 1011 0010																			0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**
DAC A & B	$1B3_{16}$																								4	3	2	1	0
CORE	01 1011 0011																								**0**	**0**	**0**	**0**	**0**
DAC	$1C0_{16}$																										2	1	0
CONFIG	01 1100 0000																										**X**	**0**	**0**
SYSTEM CLOCK	$1C1_{16}$													[15:12]				[11:8]				[7:4]				[3:0]			
DELAYS	01 1100 0001													**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
DAC	$1C2_{16}$																										[2:0]		
TEST	01 1100 0010																										**X**	**0**	**0**
POWER	$1C3_{16}$																12	11	10	9	8	7	6	5	4	3	2	1	0
DOWN	01 1100 0011																**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
SYSTEM	$1C4_{16}$																					7	[6:2]					1	0
MISC	01 1100 0100																					**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

R	Read-only bit
X	Don’t care
	Not used
	Reserved. Set to defined value

Appendix A.2 Waveform Memory Module Registers

Register	Address	Register Bits																											
		27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WMM	00_{16}																					7	6	5	4	[3:2]		[1:0]	
CONFIG	000 0000																					0	0	**0**	**0**	**0**	**0**	**0**	**0**
WMM EVEN	10_{16}																					7	6	5	4	3	2	1	0
CONFIG	001 0000																					0	0	0	**R**	**R**	**0**	**1**	**0**
WMM EVEN	11_{16}																					[7:6]			5	4	[3:2]		1	0
MUX CTRL	001 0001																					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
WMM EVEN	12_{16}			25	[24:23]		22	[21:11]											[10:0]										
RAM CTRL	001 0010			**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
WMM EVEN	13_{16}	**63**	**62**	**61**	**60**	**59**	***Note: 64 bit register***																		**4**	**3**	**2**	**1**	**0**
RAM DATA	001 0011																												
WMM ODD	20_{16}																					7	6	5	4	3	2	1	0
CONFIG	010 0000																					0	0	0	**R**	**R**	**0**	**1**	**0**
WMM ODD	21_{16}																					[7:6]			5	4	[3:2]		1	0
MUX CTRL	010 0001																					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
WMM ODD	22_{16}			25	[24:23]		22	[21:11]											[10:0]										
RAM CTRL	010 0010			**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
WMM ODD	23_{16}	**63**	**62**	**61**	**60**	**59**	***Note: 64 bit register***																		**4**	**3**	**2**	**1**	**0**
RAM DATA	010 0011																												

R	Read-only bit
X	Don't care
	Not used
	Reserved. Set to defined value

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