DENSE-PAC MICROSYSTEMS

M-Densus
High Density Memory Device

128 Megabit Synchronous DRAM
DPSD8MX16RKY5

DESCRIPTION:

The ***M-Densus*** series is a family of interchangeable memory modules. The 128 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 4 Meg x 16 SDRAMs.

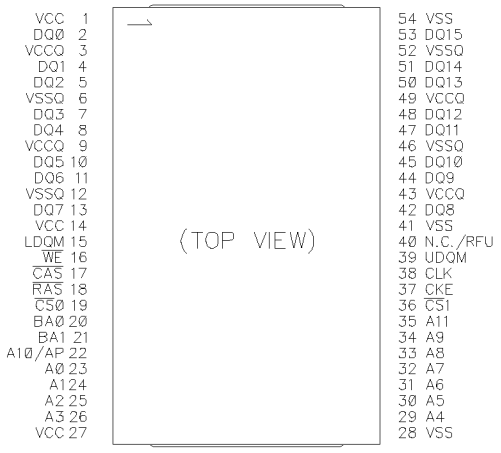
This 64 Megabit based ***M-Densus*** module, the DPSD8MX16RKY5 has been designed to fit in the same footprint as the 4 Meg x 16 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of ***M-Densus*** modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

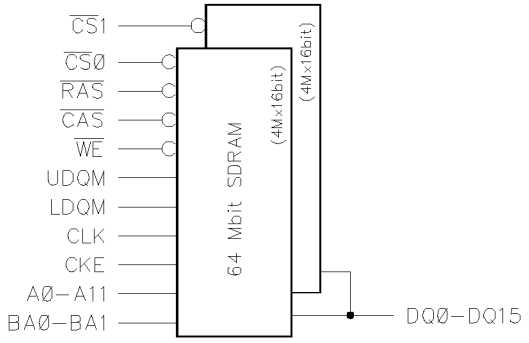
- Configuration Available:
  8 Meg x 16 bit (with two Chip Selects)
- Clock Frequency:
- 66[1], 83[1], 100, 125[2] MHz (max.)
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack with Transposer

NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
[2] Available in Commercial Temperature Range Only.

PIN-OUT DIAGRAM

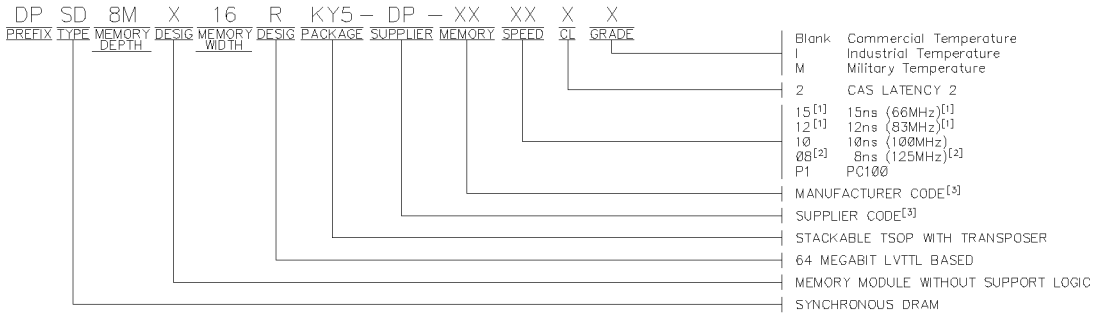


FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A7
BA0, BA1	Bank Select Address
DQ0 - DQ15	Data In / Data Out
$\overline{CAS}$	Column Address Strobes
$\overline{RAS}$	Row Address Enables
$\overline{WE}$	Data Write Enable
UDQM, LDQM	Upper & Lower Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
$\overline{CS0}$-$\overline{CS1}$	Chip Selects
V_{CC}/V_{SS}	Power Supply/Ground
V_{CCQ}/V_{SSQ}	Data Output Power/Ground
N.C./RFU	No Connect Reserved for Future Use

PART NUMBER DESCRIPTION



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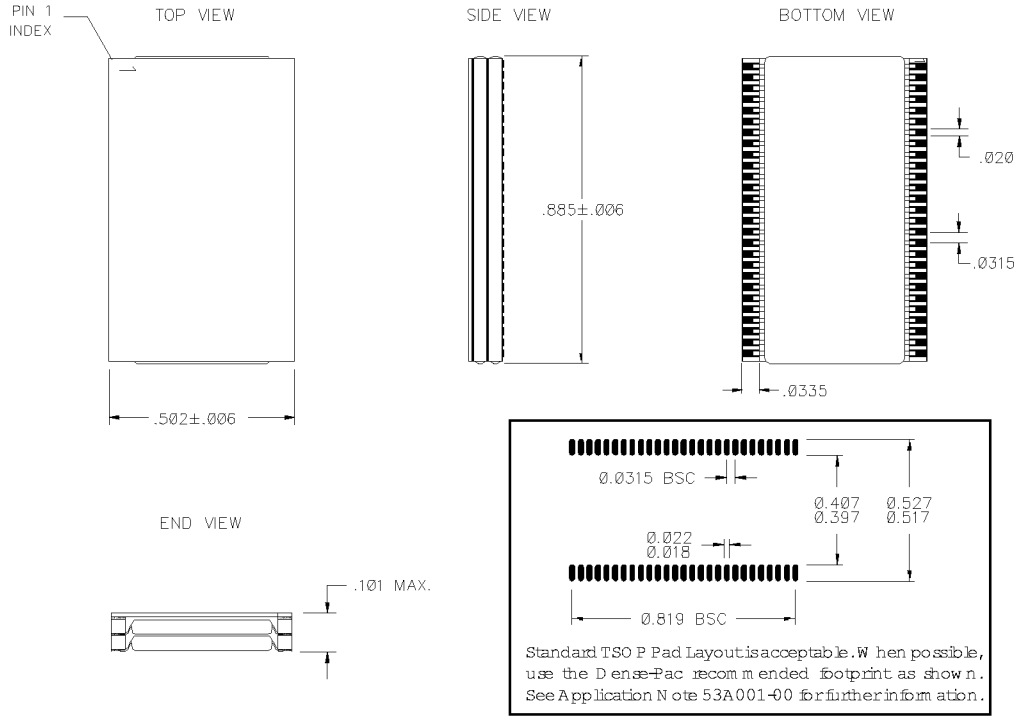
[2] Available in Commercial Temperature Range Only.
[3] Contact your sales representative for supplier and manufacturer codes.

MECHANICAL DRAWING



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