DENSE-PAC
MICROSYSTEMS

64 Megabyte SDRAM SODIMM
DPSD8MX64RSW

DESCRIPTION:

The JEDEC compatible DPSD8MX64RSW is a high speed 64 Megabyte CMOS Synchronous DRAM Small Outline DIMM consisting of eight 2Mx8x4 SDRAM devices.

These modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during a burst.

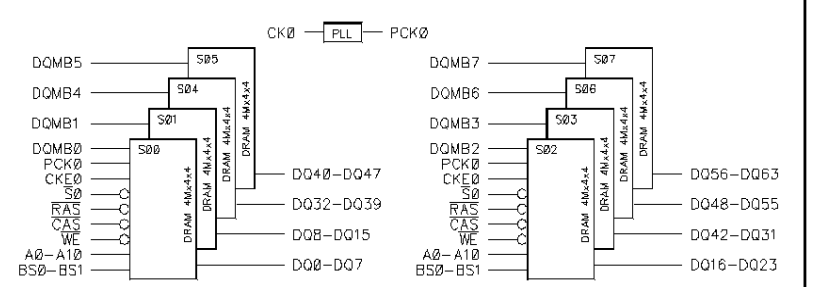
The DPSD8MXRSW is designed to operate in 3.3V, low power memory systems. An Auto Refresh Mode is provided along with a power saving Power-Down Mode. All inputs, outputs and clocks are LVTTL-compatible.

FEATURES:

- Configuration: 8 Meg x 64
- 10ns(100MHz)/12ns(83MHz) Devices
- 3.3±0.3 Volt Power Requirement
- Fully Synchronous;
  All signals registered on positive edge of system clock
- LVTTL Compatible I/O and Clock
- Internal Pipeline Operation;
  Column address can be changed every clock cycle
- PLL Clock Buffer
- Program Burst Lengths:
  1, 2, 4, 8 or Full Page
- Programmable Burst Type,
  Burst Length, and CAS Latency
- 4096 Cycles / 64 ms Refresh
- Auto Precharge and
  Auto Refresh Modes
- Serial Presence-Detect (SPD)
- Package:
  JEDEC Standard 144-Pin SODIMM

PIN NAMES	
A0 - A13	Row Address: A0 - A11 Column Address: A0 - A8 Auto Precharge: A10 Bank Select: A12, A13
DQ0 - DQ63	Data In / Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Enable
$\overline{WE}$	Data Write Enable
DQMB0-DQMB7	Data Input/Output Mask
CKE0, CKE1	Clock Enables
CK0, CK1	System Clocks
$\overline{S0}$, $\overline{S1}$	Chip Select
SDA	Serial Presence-Detect Data
SCL	Serial Clock for Presence-Detect
VDD	Power Supply
Vss	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM

VSS	1		2	VSS
DQ0	3		4	DQ32
DQ1	5		6	DQ33
DQ2	7		8	DQ34
DQ3	9		10	DQ35
VDD	11		12	VDD
DQ4	13		14	DQ36
DQ5	15		16	DQ37
DQ6	17		18	DQ38
DQ7	19		20	DQ39
VSS	21		22	VSS
DQMB0	23		24	DQMB4
DQMB1	25		26	DQMB5
VDD	27		28	VDD
A0	29		30	A3
A1	31		32	A4
A2	33		34	A5
VSS	35		36	VSS
DQ8	37		38	DQ40
DQ9	39		40	DQ41
DQ10	41		42	DQ42
DQ11	43		44	DQ43
VDD	45		46	VDD
DQ12	47		48	DQ44
DQ13	49		50	DQ45
DQ14	51		52	DQ46
DQ15	53		54	DQ47
VSS	55		56	VSS
N.C.	57		58	N.C.
N.C.	59		60	N.C.
CK0	61		62	CKE0
VDD	63		64	VDD
RAS	65		66	CAS
WE	67		68	CKE1
S0	69		70	A12
S1	71		72	A13
N.U.	73		74	CK1
VSS	75		76	VSS
N.C.	77		78	N.C.
N.C.	79		80	N.C.
VDD	81		82	VDD
DQ16	83		84	DQ48
DQ17	85		86	DQ49
DQ18	87		88	DQ50
DQ19	89		90	DQ51
VSS	91		92	VSS
DQ20	93		94	DQ52
DQ21	95		96	DQ53
DQ22	97		98	DQ54
DQ23	99		100	DQ55
VDD	101		102	VDD
A6	103		104	A7
A8	105		106	BA0
VSS	107		108	VSS
A9	109		110	BA1
A10/AP	111		112	A11
VDD	113		114	VDD
DQMB2	115		116	DQMB6
DQMB3	117		118	DQMB7
VSS	119		120	VSS
DQ24	121		122	DQ56
DQ25	123		124	DQ57
DQ26	125		126	DQ58
DQ27	127		128	DQ59
VDD	129		130	VDD
DQ28	131		132	DQ60
DQ29	133		134	DQ61
DQ30	135		136	DQ62
DQ31	137		138	DQ63
VSS	139		140	VSS
SDA	141		142	SCL
VDD	143		144	VDD

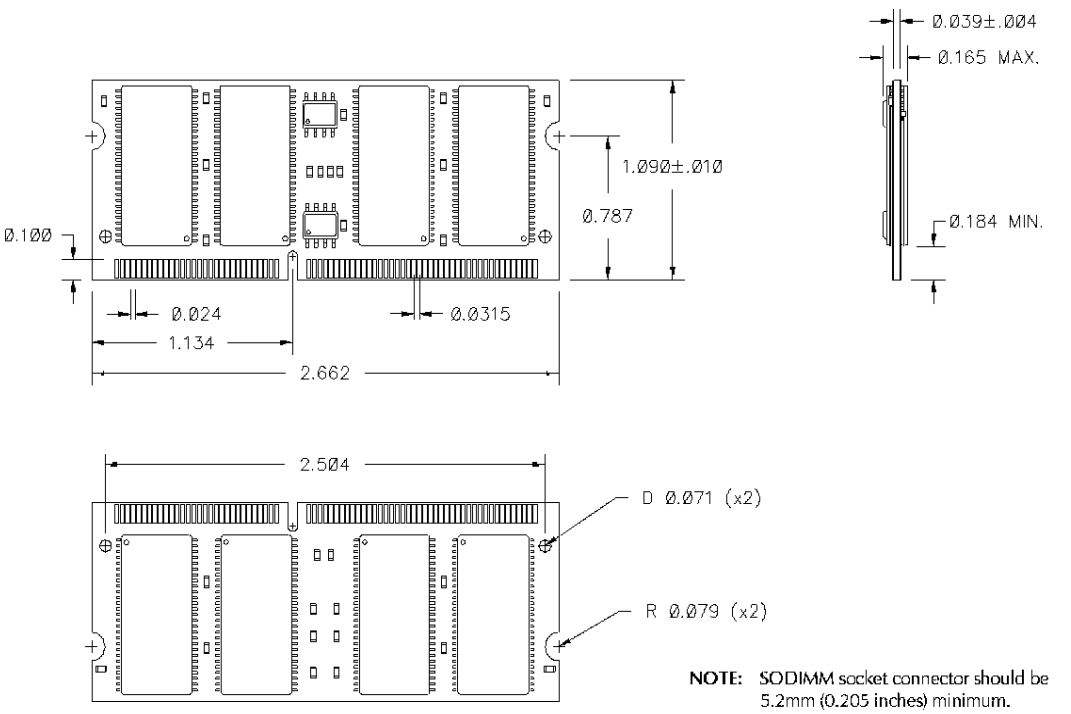
This document contains information on a product that is currently released to production at Dense-Pac Microsystems, Inc. Dense-Pac reserves the right to change products or specifications herein without prior notice.

ORDERING INFORMATION

DP	SD	8M	X	64	R	SW	– XX	C	T
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE	SPEED	GRADE	DESIG

- Blank GOLD CONTACTS
- T TIN CONTACTS
- C COMMERCIAL 0°C to +70°C
- 10 10ns, 100MHz
- 12 12ns, 83MHz
- } 66MHz BUS SPEED
- 144–PIN SMALL OUTLINE DIMM
- 64 MEGABIT BASED
- MEMORY MODULE WITHOUT SUPPORT LOGIC
- SYNCHRONOUS DRAM

MECHANICAL DRAWING



NOTE: SODIMM socket connector should be 5.2mm (0.205 inches) minimum.

Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove , California 92841-1431
(714) 898-0007 (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com