Data Sheet
January 1992

AT&T Microelectronics

# ATT7C168
# ATT7C170

# High-Speed CMOS SRAM
# 16 Kbits (4K x 4), Common I/O

## Features

- High speed — 10 ns maximum access time
- Output enable (ATT7C170 only)
- Automatic powerdown during long cycles
- Advanced CMOS technology
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT6168 and CY7C168/170
- Low-power operation
  — Active: 325 mW typical at 25 ns
  — Standby: 100 µW typical
- Package styles available:
  — 20-/22-pin, plastic DIP
  — 20-/24-pin, plastic SOJ (J-lead)

## Description

The ATT7C168 and ATT7C170 devices are high-performance, low-power, CMOS static RAMs organized as 4,096 words by 4 bits per word. The data-in and data-out signals share I/O pins. The ATT7C170 device adds an active-low output enable control. Parts are available in four speeds with worst-case access times from 10 ns to 20 ns.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power consumption is 325 mW (typical) at 25 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (enable is high).

Two standby modes are available. Automatic powerdown during long cycles reduces power consumption when the memory is deselected, or during read or write accesses that are longer than the minimum access time. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C168 and ATT7C170 devices consume only 15 µW at 3 V (typical), thereby allowing effective battery backup operation.

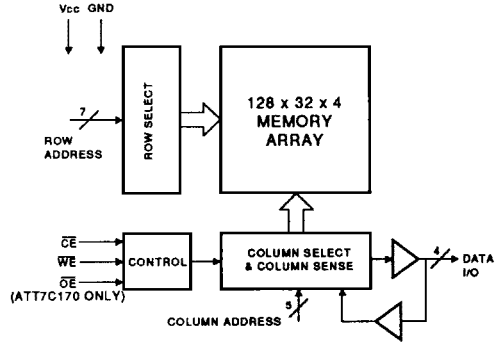



**Figure 1. Block Diagram**

## Pin Information

**Table 1. ATT7C168 Pin Descriptions**

| Pin | Name/Function |
|---|---|
| A0—A11 | Address |
| I/O0—I/O3 | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{WE}$ | Write Enable |
| GND | Ground |
| Vcc | Power |

**Table 2. ATT7C170 DIP Pin Descriptions**

| Pin | Name/Function |
|---|---|
| A0—A11 | Address |
| I/O0—I/O3 | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| GND | Ground |
| Vcc | Power |
| NC | No Connect |

**Table 3. ATT7C170 SOJ Pin Descriptions**

| Pin | Name/Function |
|---|---|
| A0—A11 | Address |
| I/O0—I/O3 | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{WE}$ | Write Enable |
| GND | Ground |
| Vcc | Power |
| NC | No Connect |

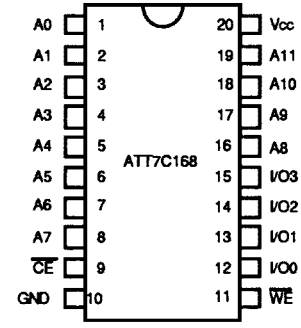



**Figure 2. Pin Diagram**

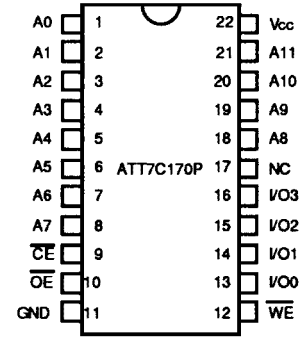



**Figure 3. Pin Diagram**

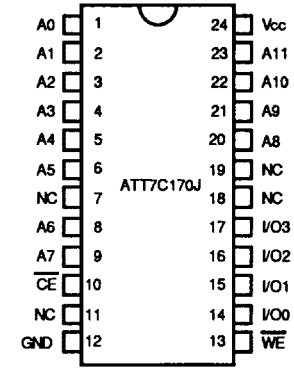



**Figure 4. Pin Diagram**

## Functional Description

The ATT7C168 and ATT7C170 devices provide asynchronous (unclocked) operation with matching access and cycle times. An active-low chip enable and a 3-state I/O bus simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A11. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location then appears on the data-out pin within one access time. When $\overline{CE}$ or $\overline{OE}$ is high or $\overline{WE}$ is low, the I/O pins stay in a high-impedance state.

Writing to an addressed location is accomplished when the $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal can be used to terminate the write operation. Data-in and data-out signals have the same polarity.

Latch-up and static discharge protection are provided on-chip. The ATT7C168 and ATT7C170 devices can withstand an injection of up to 200 mA on any pin without damage.

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_{stg}$ | −65 | 150 | °C |
| Operating Ambient Temperature | $T_A$ | −55 | 125 | °C |
| Supply Voltage with Respect to Ground | $V_{CC}$ | −0.5 | 7.0 | V |
| Input Signal with Respect to Ground | — | −3.0 | 7.0 | V |
| Signal Applied to High-impedance Output | — | −3.0 | 7.0 | V |
| Output Current into Low Outputs | — | — | 25 | mA |
| Latch-up Current | — | >200 | — | mA |

## Recommended Operating Conditions

| Mode | Temperature Range (Ambient) | Supply Voltage |
|---|---|---|
| Active Operation | 0 °C to 70 °C | 4.5 V ≤ $V_{CC}$ ≤ 5.5 V |
| Data Retention | 0 °C to 70 °C | 2.0 V ≤ $V_{CC}$ ≤ 5.5 V |

## Truth Tables

**Table 4. Truth Table for the ATT7C168**

| $\overline{CE}$ | $\overline{WE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|
| H | X | High Z | Powerdown | Standby ($I_{CC2}$ and $I_{CC3}$) |
| L | H | Data Out | Read | Active ($I_{CC1}$) |
| L | L | Data In | Write | Active ($I_{CC1}$) |

## Truth Tables (continued)

**Table 5. Truth Table for the ATT7C170**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Powerdown | Standby ($I_{CC2}$ and $I_{CC3}$) |
| L | H | H | High Z | Output Disabled | Active ($I_{CC1}$) |
| L | H | L | Data Out | Read | Active ($I_{CC1}$) |
| L | L | X | Data In | Write | Active ($I_{CC1}$) |

## Electrical Characteristics

Over all Recommended Operating Conditions

**Table 6. General Electrical Characteristics**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage: | | | | | | |
| High | $V_{OH}$ | $I_{OH}$ = –4.0 mA, $V_{CC}$ = 4.5 V | 2.4 | — | — | V |
| Low | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | — | 0.4 | V |
| Input Voltage: | | | | | | |
| High | $V_{IH}$ | — | 2.2 | — | $V_{CC}$ + 0.3 | V |
| Low[1] | $V_{IL}$ | — | –3.0 | — | 0.8 | V |
| Input Current | $I_{IX}$ | Ground ≤ $V_I$ ≤ $V_{CC}$ | –10 | — | 10 | µA |
| Output Leakage Current | $I_{OZ}$ | Ground ≤ $V_O$ ≤ $V_{CC}$, $\overline{CE}$ = $V_{CC}$ | –10 | — | 10 | µA |
| Output Short Current | $I_{OS}$ | $V_O$ = Ground, $V_{CC}$ = Max[2] | — | — | –350 | mA |
| $V_{CC}$ Current: | | | | | | |
| Inactive[3] | $I_{CC2}$ | — | — | 15 | 30 | mA |
| Standby[4] | $I_{CC3}$ | — | — | 20 | 100 | µA |
| DR Mode | $I_{CC4}$ | $V_{CC}$ = 2.0 V[5] | — | 5 | 50 | µA |
| Capacitance: | | | | | | |
| Input | $C_I$ | $T_A$ = 25 °C, $V_{CC}$ = 5.0 V | — | — | 5 | pF |
| Output | $C_O$ | Test frequency = 1 MHz[6] | — | — | 7 | pF |

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short-circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ $V_{IH}$.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = $V_{CC}$. Input levels are within 0.2 V of $V_{CC}$ or ground.
5. Data retention operation requires that $V_{CC}$ never drops below 2.0 V. $\overline{CE}$ must be ≥ $V_{CC}$ – 0.2 V. For all other inputs, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V or $V_{IN}$ < 0.2 V is required to ensure full powerdown.
6. This parameter is not 100% tested.

**Table 7. Electrical Characteristics by Speed**

| Parameter | Symbol | Test Condition | Speed (ns) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | 25 | 20 | 15 | 12 | 10 | |
| Max $V_{CC}$ Current, Active | $I_{CC1}$ | * | 65 | 85 | 110 | 135 | 150 | mA |

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE}$ and $\overline{WE}$ ≤ $V_{IL}$. Input pulse levels are 0 V to 3.0 V.
Max Icc shown applies over the active operating temperature range.

# Timing Characteristics

**Table 8. Read Cycle[1, 2, 3, 4]**

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified $I_{OL}$ and $I_{OH}$ +30 pF (see Figure 10A).

| Symbol | Parameter | Speed | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 25 | | 20 | | 15 | | 12 | | 10 | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| tADXADX, tCELCEH | Read-cycle Time | 25 | — | 20 | — | 15 | — | 12 | — | 10 | — |
| tADXDOV | Address Change to Output Valid[5, 6] | — | 25 | — | 20 | — | 15 | — | 12 | — | 10 |
| tADXDOX | Address Change to Output Change | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — |
| tCELDOV | Chip Enable Low to Output Valid[5, 7] | — | 25 | — | 20 | — | 15 | — | 12 | — | 10 |
| tCELDOZ | Chip Enable Low to Output Low-Z[8, 9] | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — |
| tCEHDOZ | Chip Enable High to Output High-Z[8, 9] | — | 10 | — | 8 | — | 8 | — | 5 | — | 4 |
| tOELDOV | Output Enable Low to Output Valid | — | 12 | — | 10 | — | 8 | — | 6 | — | 4 |
| tOELDOZ | Output Enable Low to Output Low-Z[8, 9] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tOEHDOZ | Output Enable High to Output High-Z[8, 9] | — | 10 | — | 8 | — | 5 | — | 5 | — | 4 |
| tCELICH, tADXICH | Chip Enable Low or Address Change to Powerup[10, 11] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tICHICL | Powerup to Powerdown[10, 11] | — | 25 | — | 20 | — | 20 | — | 20 | — | 18 |

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH (Table 9) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. $\overline{WE}$ is high for the read cycle.
6. The chip is continuously selected ( $\overline{CE}$ low).
7. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.
8. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
9. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 10B. This parameter is sampled and not 100% tested.
10. This parameter is not 100% tested.
11. Powerup from $I_{CC2}$ to $I_{CC1}$ occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ( $\overline{CE}$ active), (3) transition on any address line ( $\overline{CE}$ active), or (4) transition on any data line ( $\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from $I_{CC1}$ to $I_{CC2}$ after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

## Timing Characteristics (continued)

**Table 9. Write Cycle[1, 2, 3, 4]** (See Figures 7, 8, and 9.)

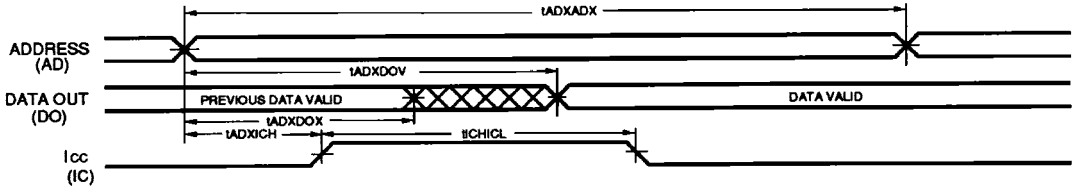
Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified $I_{OL}$ and $I_{OH}$ +30 pF (see Figure 10A).

| Symbol | Parameter | Speed | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 25 | | 20 | | 15 | | 12 | | 10 | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| tADXADX | Write-cycle Time | 20 | — | 20 | — | 15 | — | 12 | — | 10 | — |
| tCELWEH | Chip Enable Low to End of Write | 15 | — | 15 | — | 12 | — | 10 | — | 8 | — |
| tADXWEX, tADXWEL | Address Change to Beginning of Write | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tADXWEH | Address Change to End of Write | 15 | — | 15 | — | 12 | — | 10 | — | 8 | — |
| tWEHADX | End of Write to Address Change | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tWELWEH | Write Enable Low to End of Write | 15 | — | 15 | — | 12 | — | 10 | — | 8 | — |
| tDIVWEH, tDIXCEH | Data Valid to End of Write | 10 | — | 10 | — | 7 | — | 6 | — | 5 | — |
| tWEHDIV, tWEHDIX | End of Write to Data Change | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tWEHDOZ | Write Enable High to Output Low-Z[5, 6] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | |
| tWELDOZ | Write Enable Low to Output High-Z[5, 6] | — | 7 | — | 7 | — | 5 | — | 4 | — | 4 |
| tCELICH | Chip Enable Low to Powerup[7, 8] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tWELICH | Write Enable Low to Powerup[7, 8] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tCEHVCL | Chip Enable High to Data Retention[7] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — |
| tICHICL | Powerup to Powerdown | — | 25 | — | 20 | — | 20 | — | 20 | — | 18 |

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
6. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 10B. This parameter is sampled and not 100% tested.
7. This parameter is not 100% tested.
8. Powerup from $I_{CC2}$ to $I_{CC1}$ occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from $I_{CC1}$ to $I_{CC2}$ after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

## Timing Characteristics (continued)

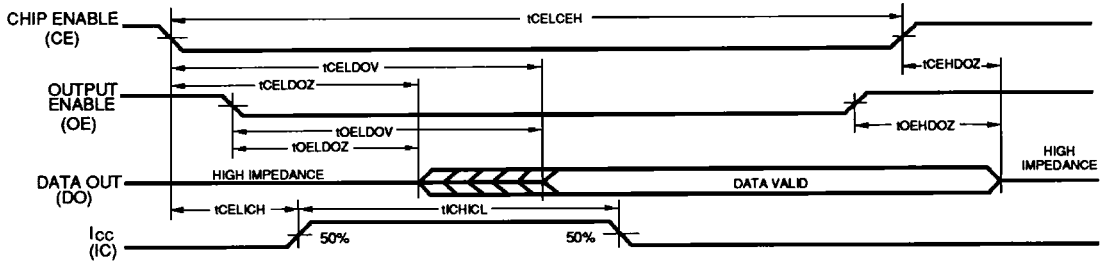
### Timing Diagrams




Notes:
$\overline{WE}$ is high for the read cycle.

The chip is continuously selected ( $\overline{CE}$ low).

**Figure 5. Read Cycle — Address-Controlled**

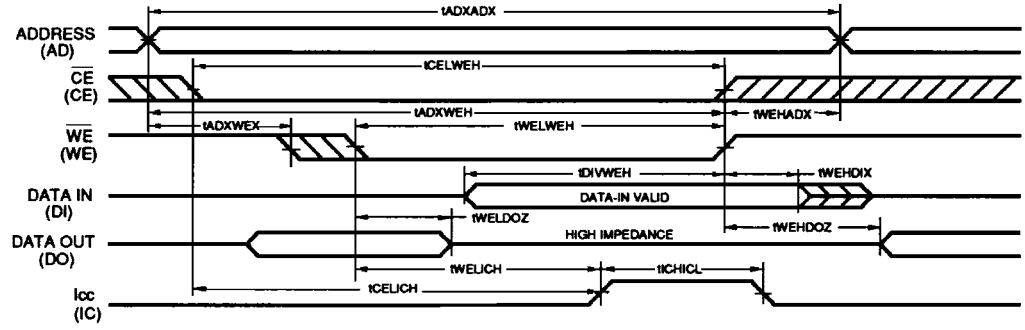



Notes:
$\overline{WE}$ is high for the read cycle.

All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

**Figure 6. Read Cycle — $\overline{CE}$ / $\overline{OE}$ -Controlled**

## Timing Characteristics (continued)



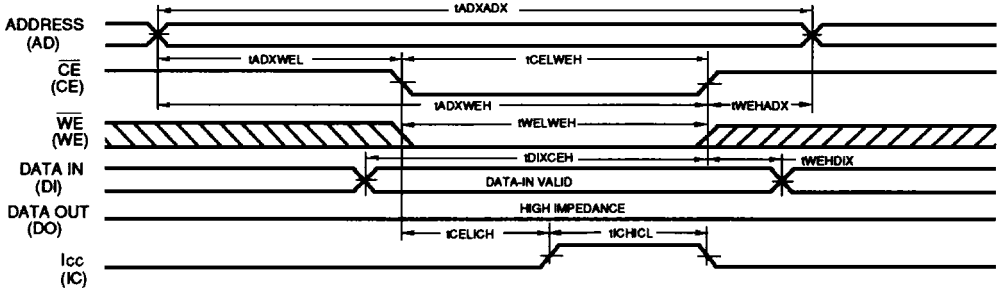

Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.

If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from $I_{CC2}$ to $I_{CC1}$ occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from $I_{CC1}$ to $I_{CC2}$ after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

**Figure 7. Write Cycle — $\overline{WE}$-Controlled**




Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.

If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from $I_{CC2}$ to $I_{CC1}$ occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from $I_{CC1}$ to $I_{CC2}$ after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

**Figure 8. Write Cycle — $\overline{CE}$-Controlled**

## Timing Characteristics (continued)

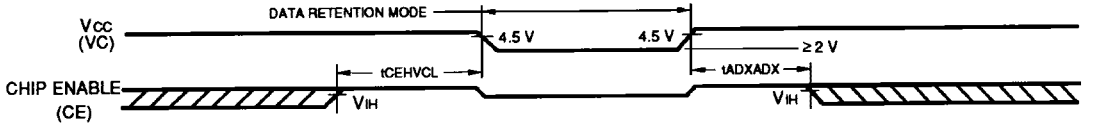



**Figure 9. Data Retention**

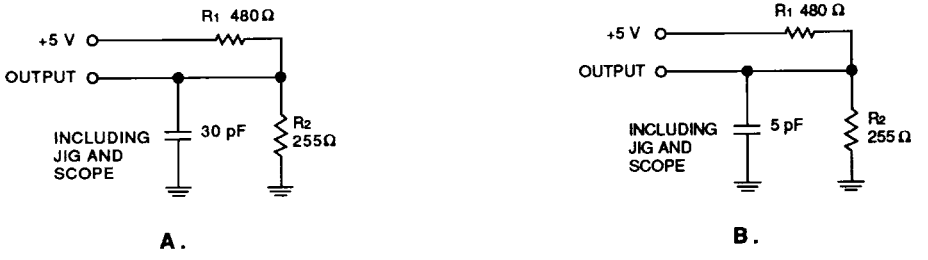



**Figure 10. Test Loads**

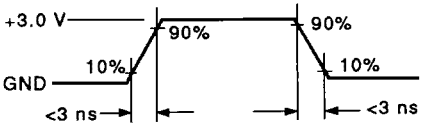
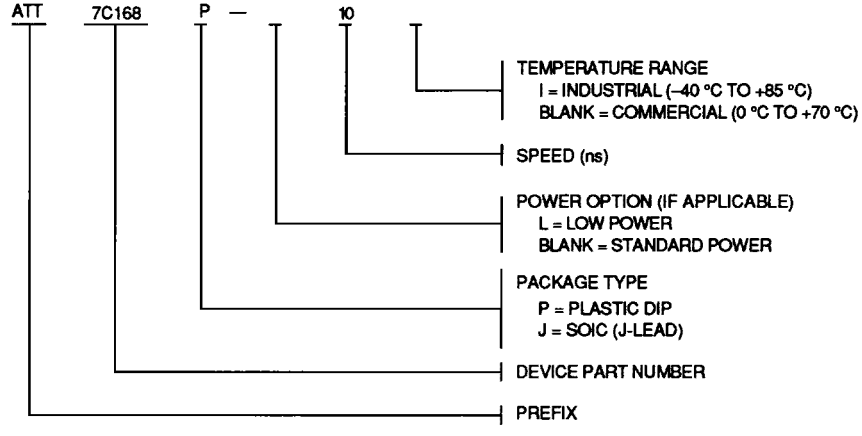



**Figure 11. Transition Times**

## Ordering Information




### ATT7C168

Operating Range 0 °C to 70 °C

| Package Style | Performance Speed | | | | |
|---|---|---|---|---|---|
| | 25 ns | 20 ns | 15 ns | 12 ns | 10 ns |
| 20-Pin, Plastic DIP | ATT7C168P–25 | ATT7C168P–20 | ATT7C168P–15 | ATT7C168P–12 | ATT7C168P–10 |
| 20-Pin, Plastic SOJ | ATT7C168J–25 | ATT7C168J–20 | ATT7C168J–15 | ATT7C168J–12 | ATT7C168J–10 |

### ATT7C170

Operating Range 0 °C to 70 °C

| Package Style | Performance Speed | | | | |
|---|---|---|---|---|---|
| | 25 ns | 20 ns | 15 ns | 12 ns | 10 ns |
| 22-Pin, Plastic DIP | ATT7C170P–25 | ATT7C170P–20 | ATT7C170P–15 | ATT7C170P–12 | ATT7C170P–10 |
| 24-Pin, Plastic SOJ | ATT7C170J–25 | ATT7C170J–20 | ATT7C170J–15 | ATT7C170J–12 | ATT7C170J–10 |