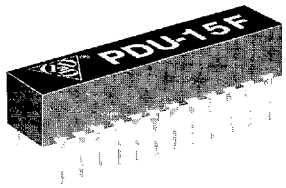
Fast Logic

Programmable Delay Units

SERIES: PDU-15F (5 Bit) TTL Interfaced

data delay devices, inc.



Features:

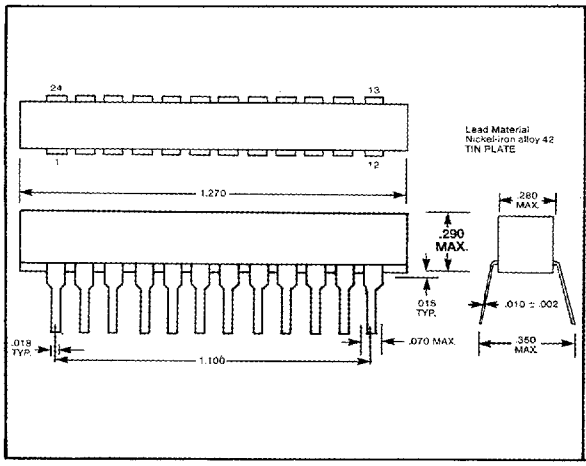
- **Input & Output TTL buffered**
- **5-Bit TTL programmable delay line**
- **Two (2) Separate outputs; inverting and non-inverting.**
- **Completely interfaced**
- **Compact & low profile**

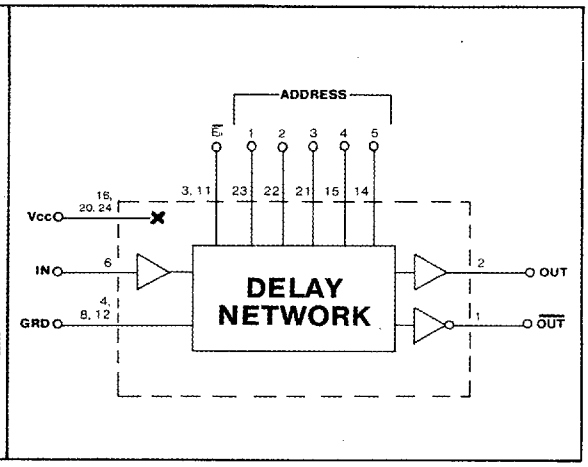
Specifications:

- **Propagation delay:**
  Address to output (T_{SUA}) = 7 ns typ.
  Enable to output (T_{SUE}) = 6 ns typ.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ± 5% or 2 ns whichever is greater.
- **Inherent delay (T_{DO}):** 9 ns on pin 2 } typical
  8 ns on pin 1 }
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.
- **Supply current:** I_{CCH} = 70 ma.
  I_{CCL} = 30 ma.
- **Minimum pulse-width** = 10% of total delay.

Test Conditions:

- **Input pulse-width:** > 150% of Max. delay.
- **Input pulse spacing:** > 3 times of Max. delay.
- **Input pulse voltage:** TTL logic.
- **Measurements taken @** $T_a = 25°C$; $V_{CC} = 5V$.





TRUTH TABLE

Enable (E_0)	Address 5	4	3	2	1	Delay Out
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{31}
1	ϕ	ϕ	ϕ	ϕ	ϕ	0

0 = Logic 0 1 = Logic 1 ϕ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{31}$ Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-15F-0.5	0.5 ± 0.3	15.5
PDU-15F-1	1 ± 0.5	31
PDU-15F-2	2 ± 0.5	62
PDU-15F-3	3 ± 1.0	93
PDU-15F-4	4 ± 1.0	124
PDU-15F-5	5 ± 1.0	155
PDU-15F-6	6 ± 1.0	186
PDU-15F-8	8 ± 1.0	248
PDU-15F-10	10 ± 1.5	310
PDU-15F-12	12 ± 1.5	372
PDU-15F-15	15 ± 1.5	465
PDU-15F-20	20 ± 2.0	620

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