

# NTP45N06L, NTB45N06L

## Power MOSFET 45 Amps, 60 Volts, Logic Level N-Channel TO-220 and D<sup>2</sup>PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Higher Current Rating
- Lower  $R_{DS(on)}$
- Lower  $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter  $V_{SD}$  Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 10\text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage	$V_{GS}$		Vdc
– Continuous	$V_{GS}$	$\pm 15$	
– Non-Repetitive ( $t_p \leq 10\text{ ms}$ )	$V_{GS}$	$\pm 20$	
Drain Current			
– Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	45	A dc
– Continuous @ $T_A = 100^\circ\text{C}$	$I_D$	30	
– Single Pulse ( $t_p \leq 10\text{ }\mu\text{s}$ )	$I_{DM}$	150	A pk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	125	W
Derate above $25^\circ\text{C}$		0.83	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1.)		3.2	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2.)		2.4	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	$-55$ to $+175$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50\text{ Vdc}$ , $V_{GS} = 5.0\text{ Vdc}$ , $L = 0.3\text{ mH}$ $I_L(\text{pk}) = 40\text{ A}$ , $V_{DS} = 60\text{ Vdc}$ , $R_G = 25\text{ }\Omega$ )	$E_{AS}$	240	mJ

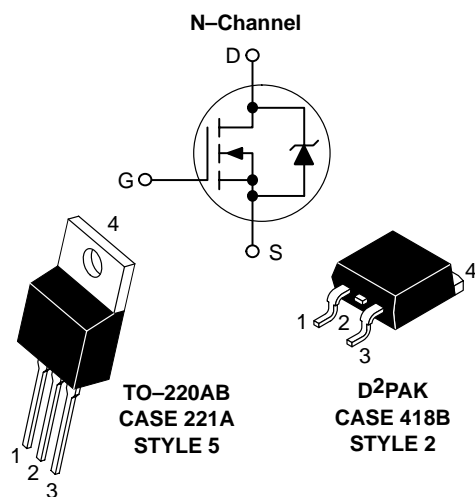
1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).



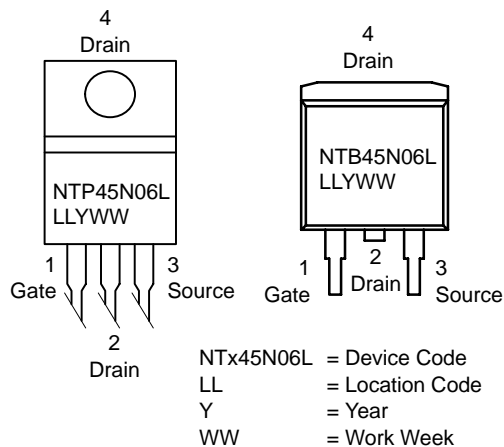
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**45 AMPERES**  
**60 VOLTS**  
 **$R_{DS(on)} = 28\text{ m}\Omega$**



### MARKING DIAGRAMS & PIN ASSIGNMENTS



### ORDERING INFORMATION

Device	Package	Shipping
NTP45N06L	TO-220AB	50 Units/Rail
NTB45N06L	D <sup>2</sup> PAK	50 Units/Rail
NTB45N06LT4	D <sup>2</sup> PAK	800/Tape & Reel

# NTP45N06L, NTB45N06L

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Thermal Resistance – Junction-to-Case – Junction-to-Ambient (Note 3.) – Junction-to-Ambient (Note 4.)	R <sub>θJC</sub> R <sub>θJA</sub> R <sub>θJA</sub>	1.2 46.8 63.2	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4.) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 –	67 67.2	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

### ON CHARACTERISTICS (Note 5.)

Gate Threshold Voltage (Note 5.) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.8 4.7	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 5.) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 22.5 Adc)	R <sub>DS(on)</sub>	–	23	28	mOhm
Static Drain-to-Source On-Voltage (Note 5.) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 45 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 22.5 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	– –	1.03 0.93	1.51 –	Vdc
Forward Transconductance (Note 5.) (V <sub>DS</sub> = 8.0 Vdc, I <sub>D</sub> = 12 Adc)	g <sub>FS</sub>	–	22.8	–	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	–	1212	1700	pF
Output Capacitance		C <sub>oss</sub>	–	352	480	
Transfer Capacitance		C <sub>rss</sub>	–	90	180	

### SWITCHING CHARACTERISTICS (Note 6.)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 45 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 5.)	t <sub>d(on)</sub>	–	13	30	ns
Rise Time		t <sub>r</sub>	–	341	680	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	36	75	
Fall Time		t <sub>f</sub>	–	158	320	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 45 Adc, V <sub>GS</sub> = 5.0 Vdc) (Note 5.)	Q <sub>T</sub>	–	23	32	nC
		Q <sub>1</sub>	–	4.6	–	
		Q <sub>2</sub>	–	14.1	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 45 Adc, V <sub>GS</sub> = 0 Vdc) (Note 5.) (I <sub>S</sub> = 45 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	– –	1.01 0.92	1.15 –	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 45 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 5.)	t <sub>rr</sub>	–	56	–	ns
		t <sub>a</sub>	–	30	–	
		t <sub>b</sub>	–	26	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.09	–	μC

3. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).

4. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

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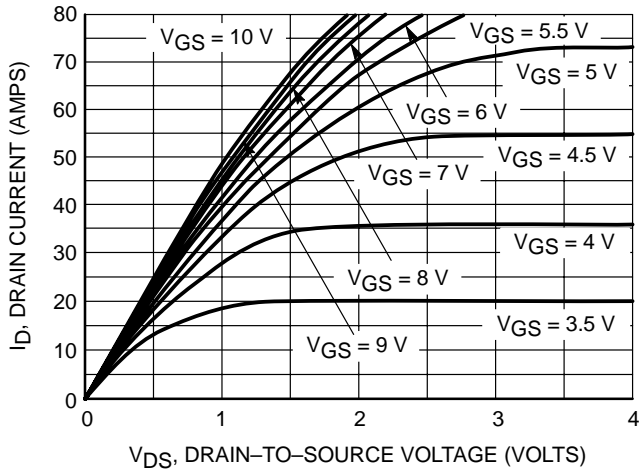


Figure 1. On-Region Characteristics

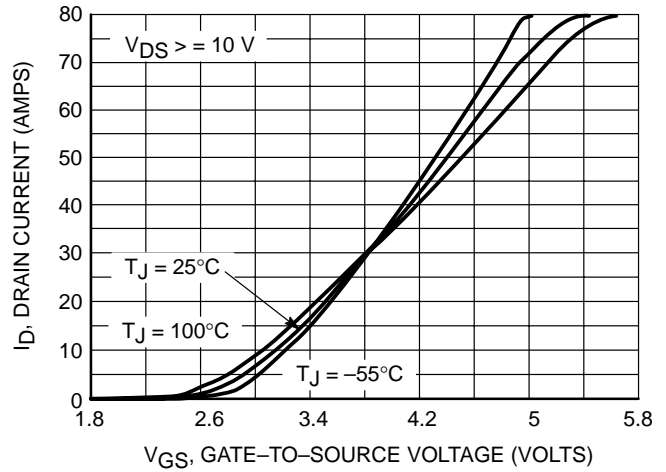


Figure 2. Transfer Characteristics

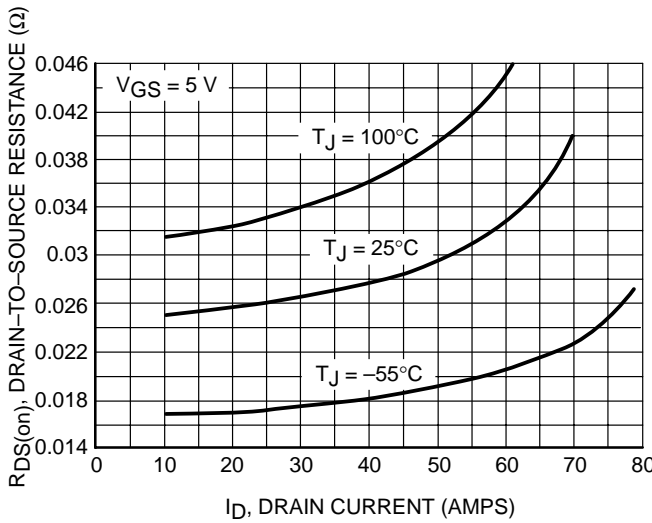


Figure 3. On-Resistance vs. Gate-to-Source Voltage

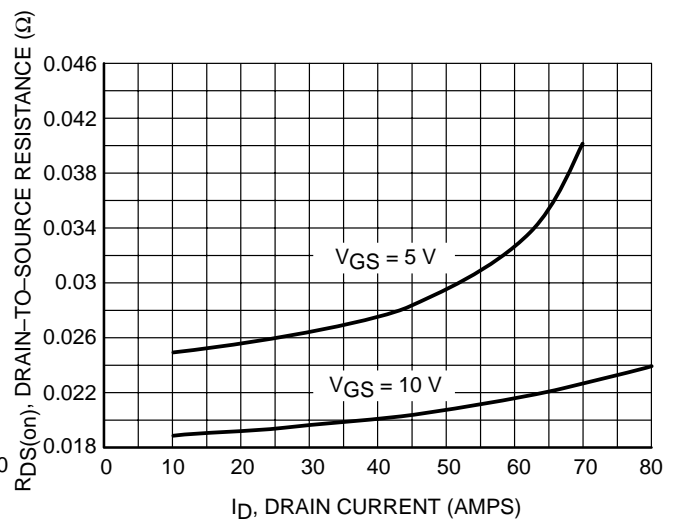


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

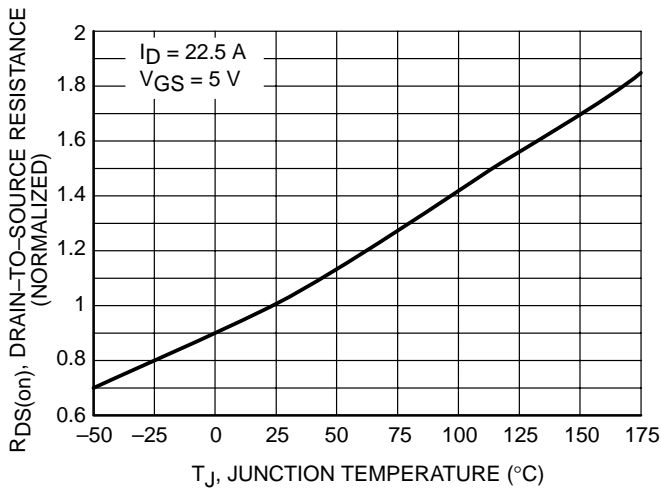


Figure 5. On-Resistance Variation with Temperature

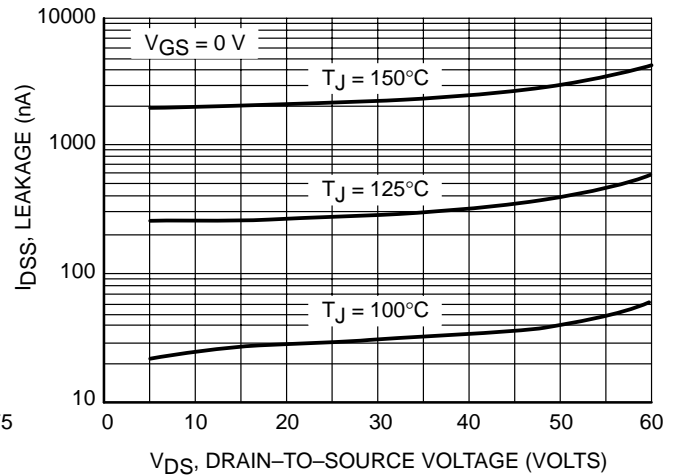
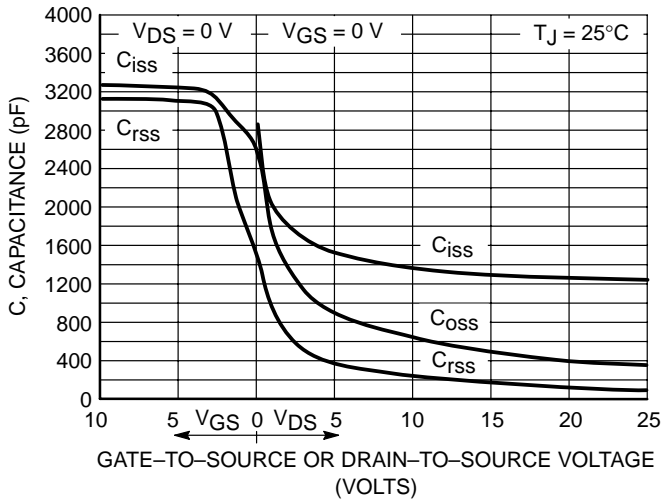
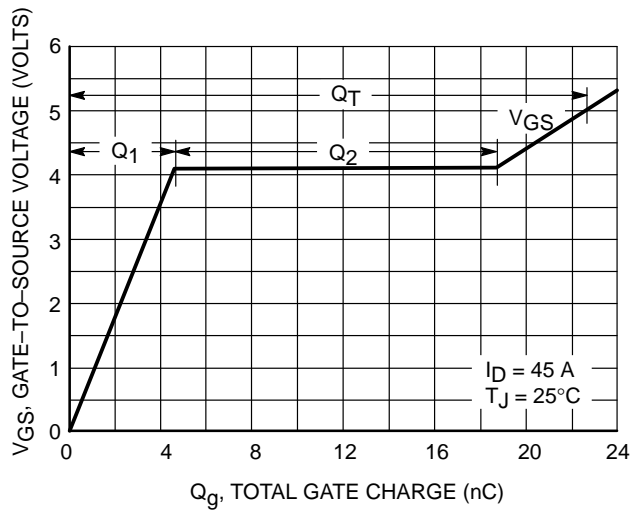


Figure 6. Drain-to-Source Leakage Current vs. Voltage

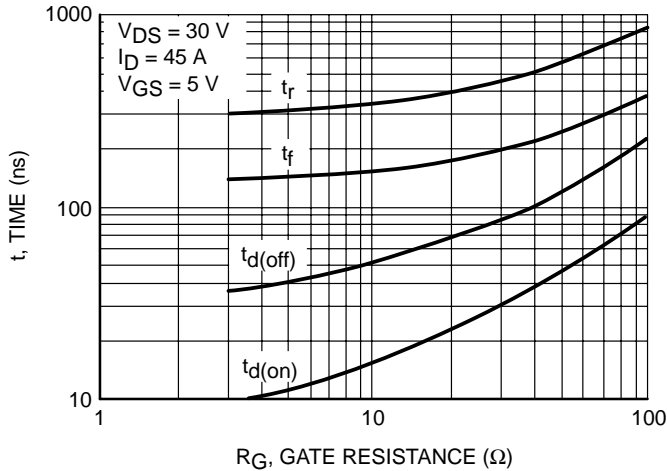
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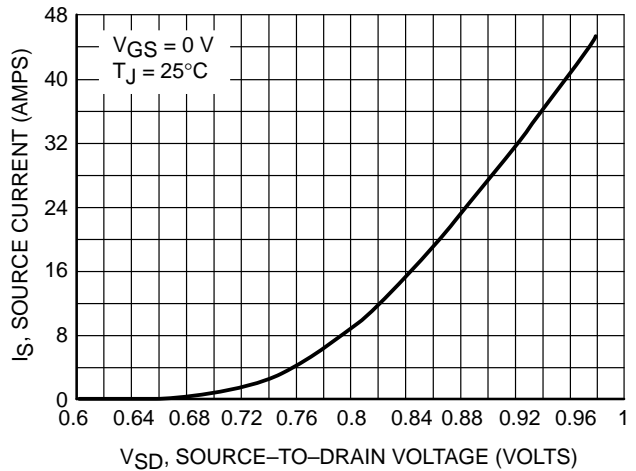
**Figure 7. Capacitance Variation**



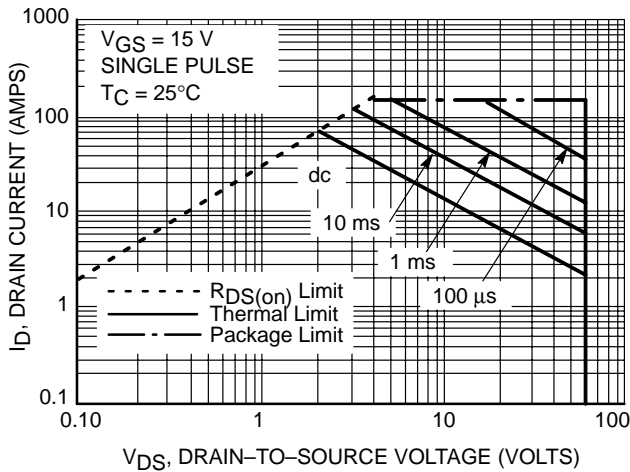
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



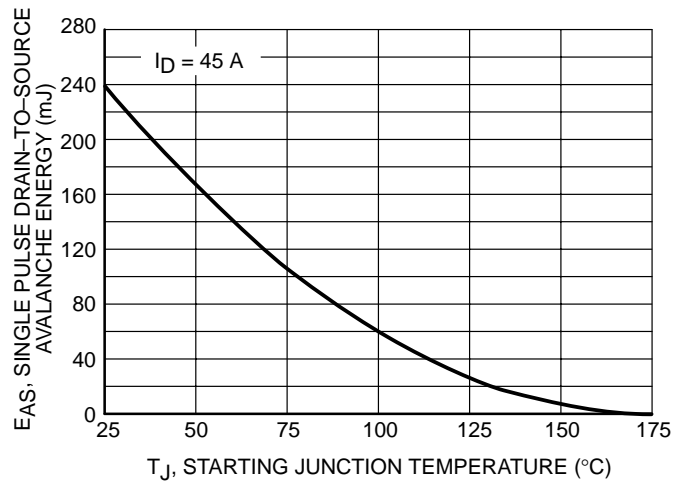
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

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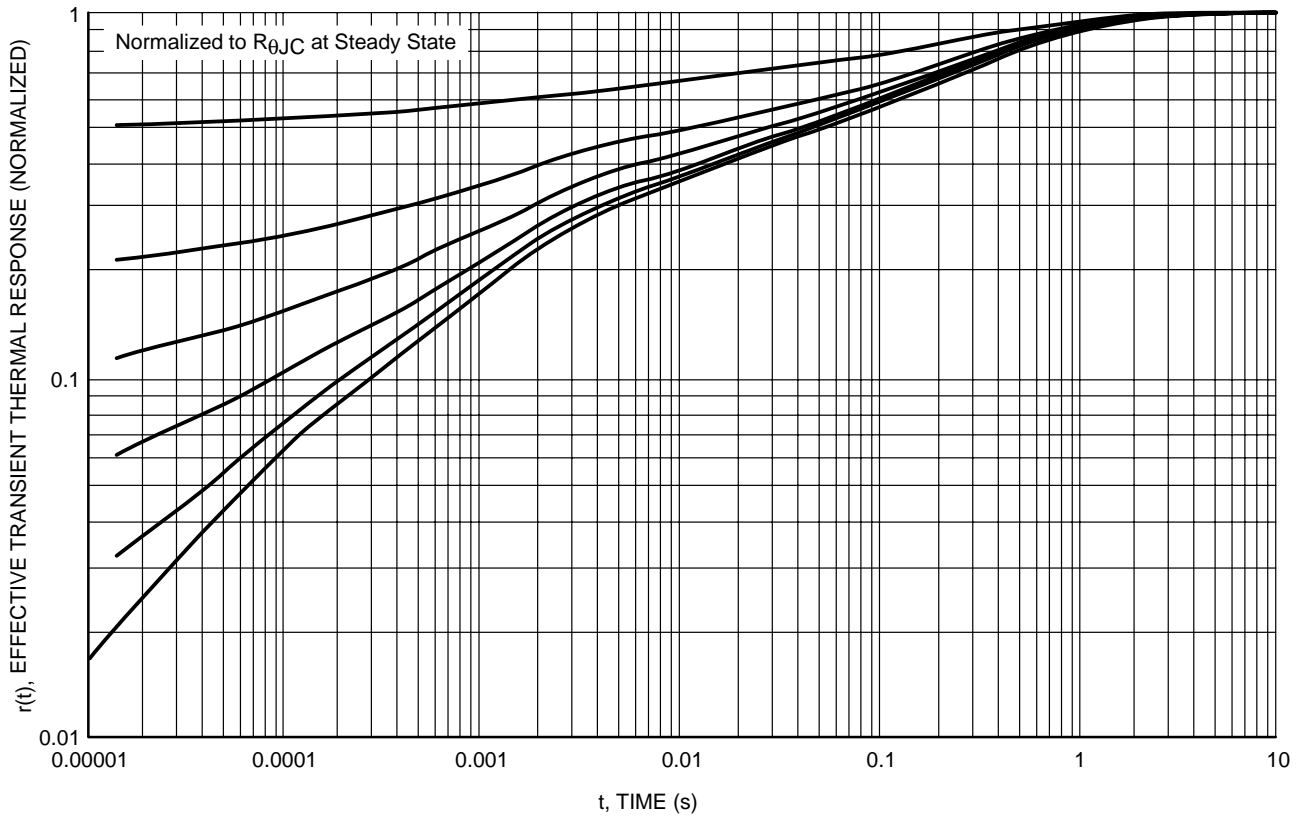


Figure 13. Thermal Response

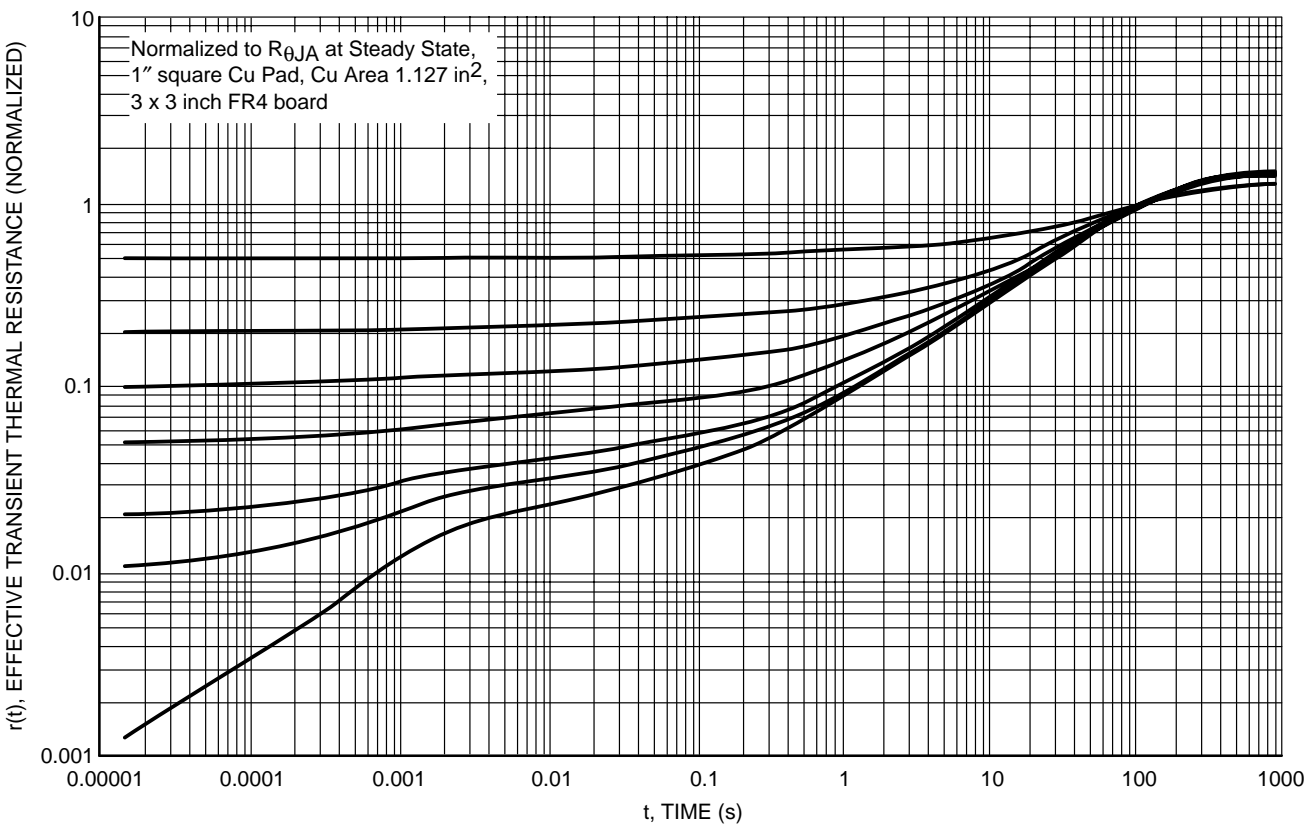


Figure 14. Thermal Response

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## PACKAGE DIMENSIONS

TO-220 THREE-LEAD  
TO-220AB  
CASE 221A-09  
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

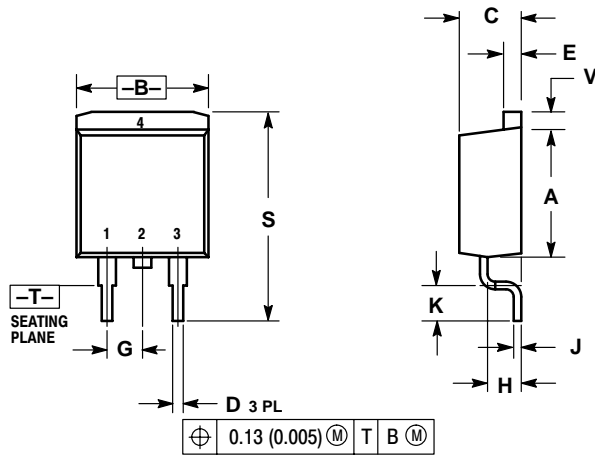
STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

# NTP45N06L, NTB45N06L

## PACKAGE DIMENSIONS

**D2PAK**  
CASE 418B-03  
ISSUE D



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

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