

Complementary Power Darlington

For Isolated Package Applications

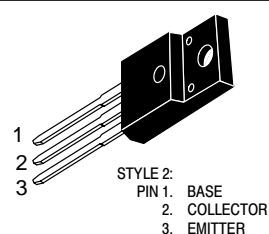
Designed for general-purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Isolated Overmold Package, TO-220 Type
- Electrically Similar to the Popular 2N6388, 2N6668, TIP102 and TIP107
- 100 V_{CEO(sus)}
- 10 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 1000 (Min) @ I_C = 5.0 Adc
- High Isolation Voltage (up to 4500 VRMS)
- Case 221D is UL Recognized at 3500 VRMS: File #E69369

NPN
MJF6388*
PNP
MJF6668*

*ON Semiconductor Preferred Devices

**COMPLEMENTARY
SILICON
POWER DARLINGTONS**
10 AMPERES
100 VOLTS
40 WATTS



CASE 221D-02
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	100	Vdc
Collector-Base Voltage	V _{CB}	100	Vdc
Emitter-Base Voltage	V _{EB}	5.0	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T _A = 25°C)	V _{ISOL}	4500 3500 1500	V
Collector Current — Continuous — Peak(2)	I _C	10 15	Adc
Base Current	I _B	1.0	Adc
Total Power Dissipation* @ T _C = 25°C Derate above 25°C	P _D	40 0.31	Watts W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	P _D	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	R _{θJC}	3.2	°C/W
Thermal Resistance, Junction to Ambient	R _{θJA}	62.5	°C/W
Lead Temperature for Soldering Purpose	T _L	260	°C

(1) Proper strike and creepage distance must be provided.

(2) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied and a mounting torque of 6 to 8 in•lbs.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) ($I_C = 30\text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ($V_{CE} = 80\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	10	μAdc
Collector Cutoff Current ($V_{CE} = 100\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 100\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	—	10 3.0	μAdc mAdc
Collector Cutoff Current ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc

ON CHARACTERISTICS (1)

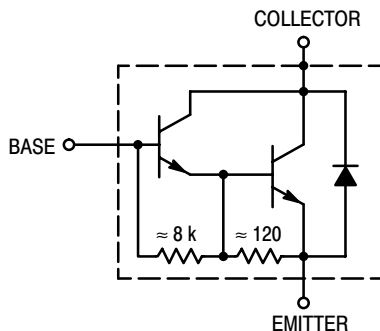
DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) ($I_C = 8.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	h_{FE}	3000 1000 200 100	15000 — — —	—
Collector–Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 6.0\text{ mAdc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.01\text{ Adc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 80\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 0.1\text{ Adc}$)	$V_{CE(sat)}$	— — — —	2.0 2.0 2.5 3.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.01\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 0.1\text{ Adc}$)	$V_{BE(sat)}$	— —	2.8 4.5	Vdc
Base–Emitter On Voltage ($I_C = 8.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	—	2.5	Vdc

DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	$ h_{fe} $	20	—	—
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	MJF6388 MJF6668 C_{ob}	—	200 300	pF
Insulation Capacitance (Collector–to–External Heatsink)	C_{C-hs}	—	3.0 Typ	pF
Small–Signal Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 1.0\text{ kHz}$)	h_{fe}	1000	—	—

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

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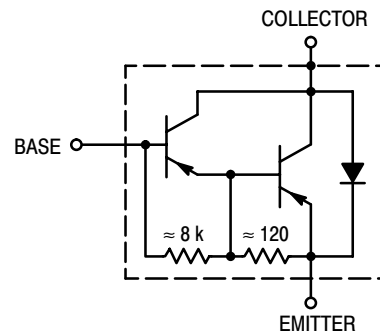


Figure 1. Darlington Schematic

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R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
 D_1 , MUST BE FAST RECOVERY TYPES, e.g.,
 MUR110 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA

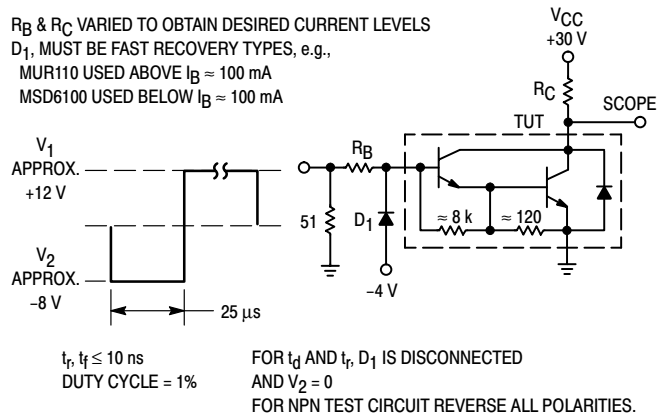


Figure 2. Switching Times Test Circuit

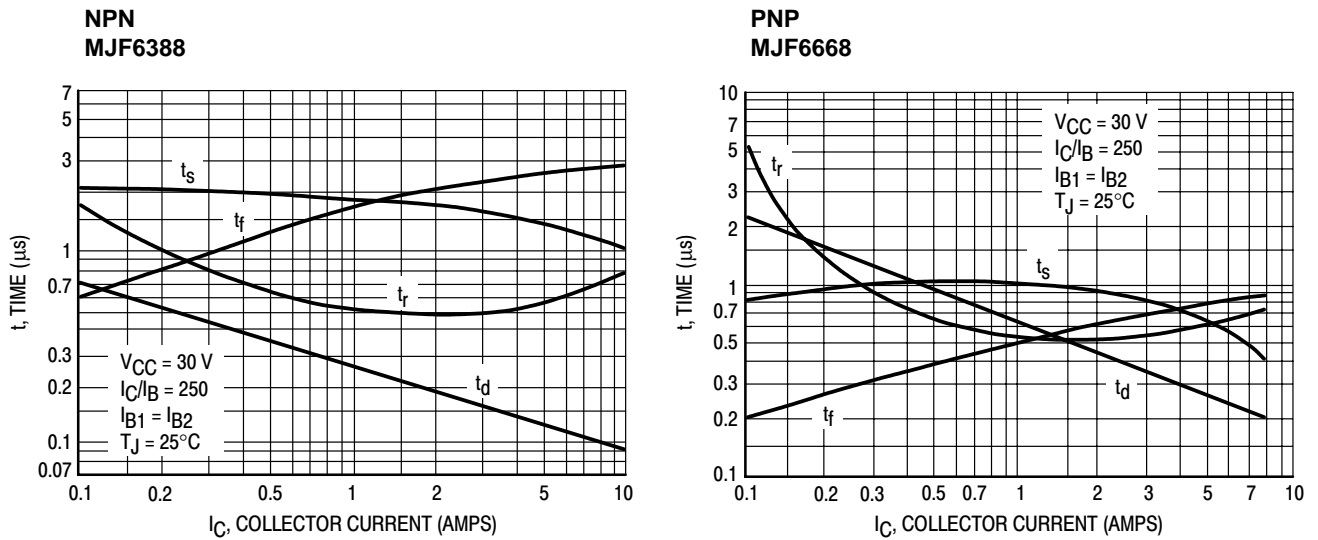


Figure 3. Typical Switching Times

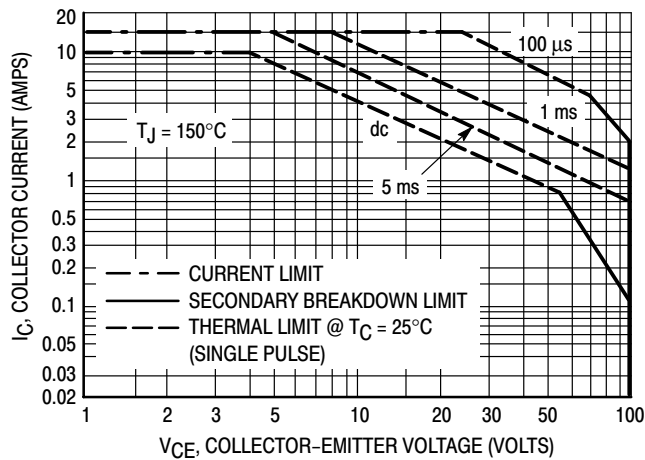


Figure 4. Maximum Forward Bias Safe Operating Area

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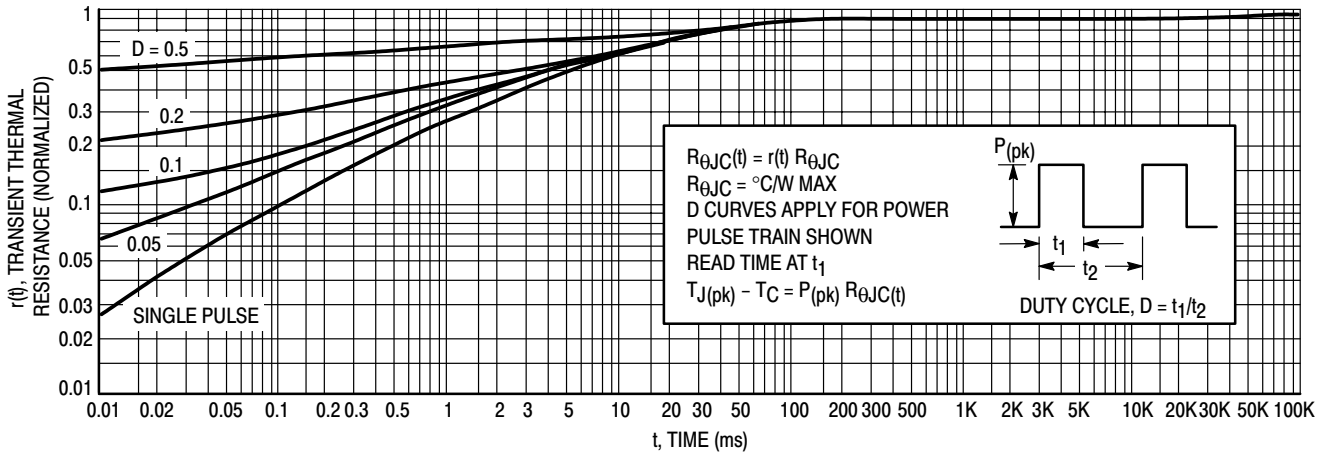


Figure 5. Thermal Response

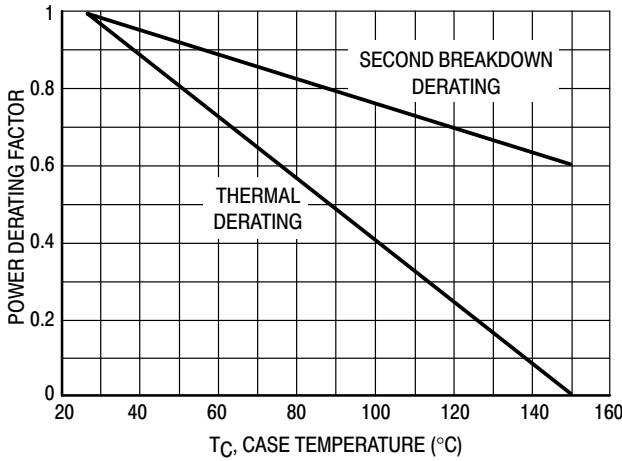


Figure 6. Maximum Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

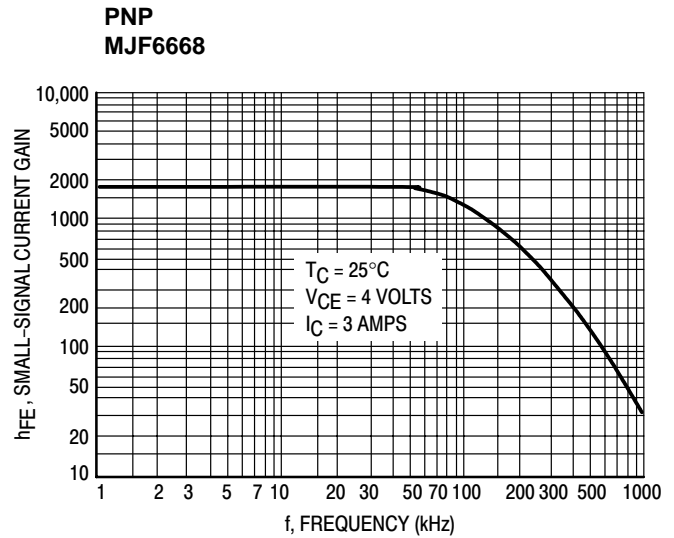
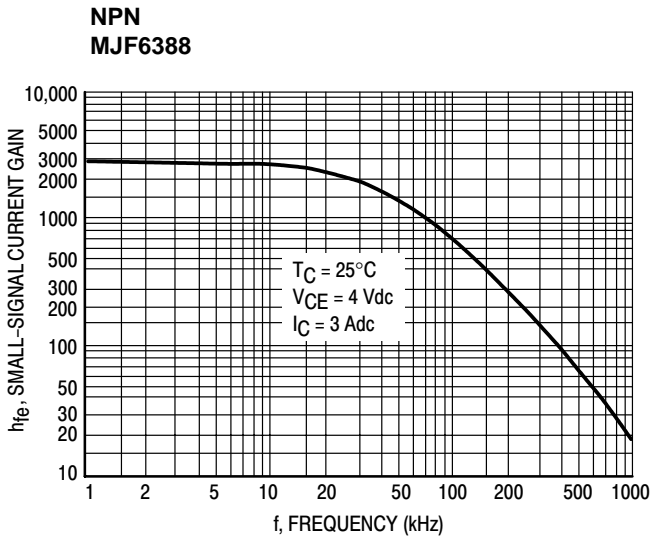
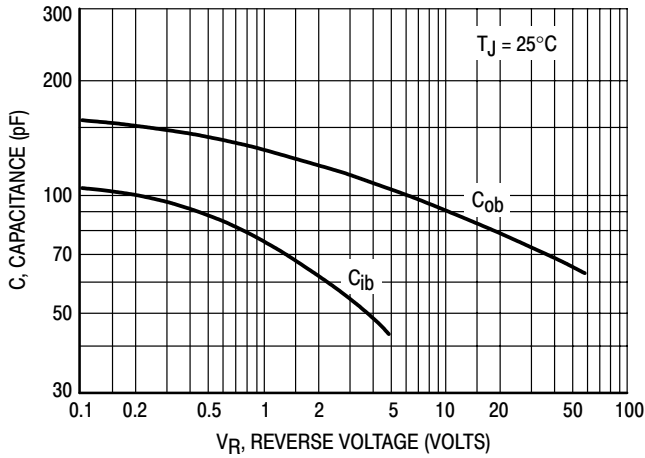


Figure 7. Typical Small-Signal Current Gain

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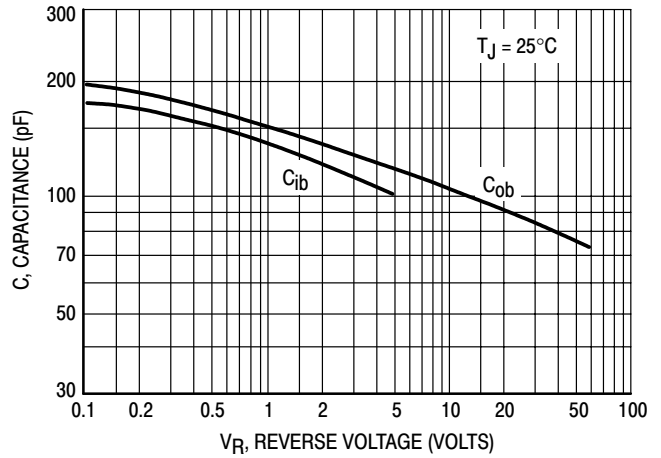


Figure 8. Typical Capacitance

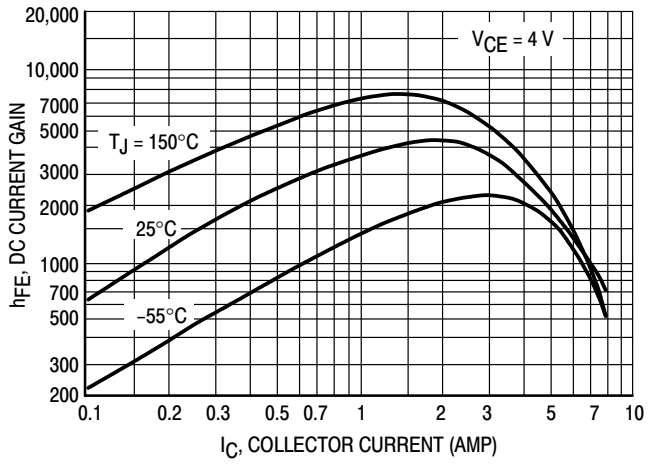
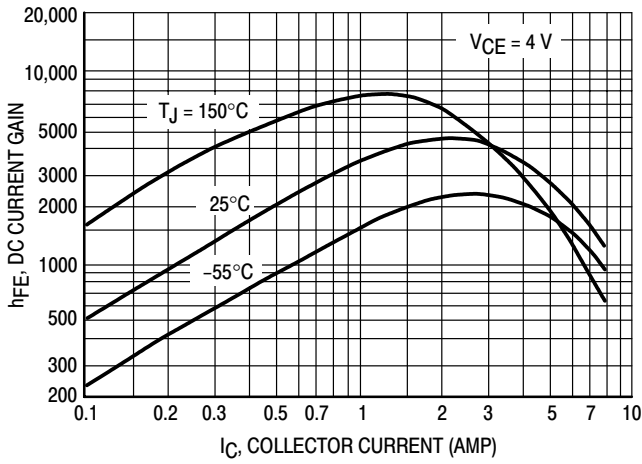


Figure 9. Typical DC Current Gain

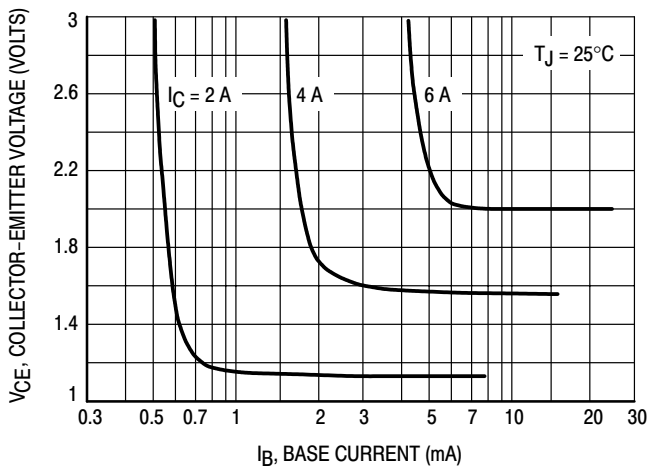
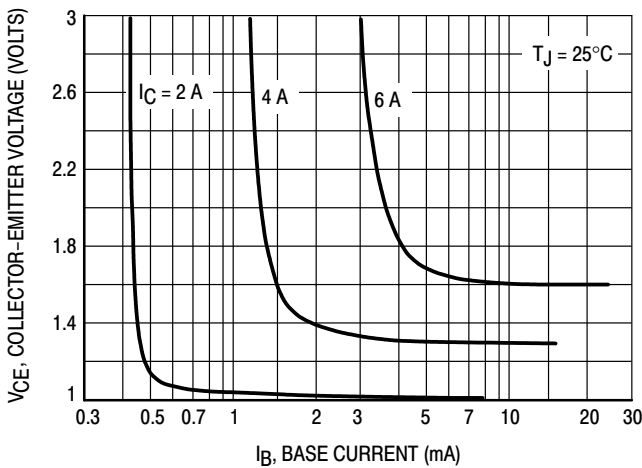


Figure 10. Typical Collector Saturation Region

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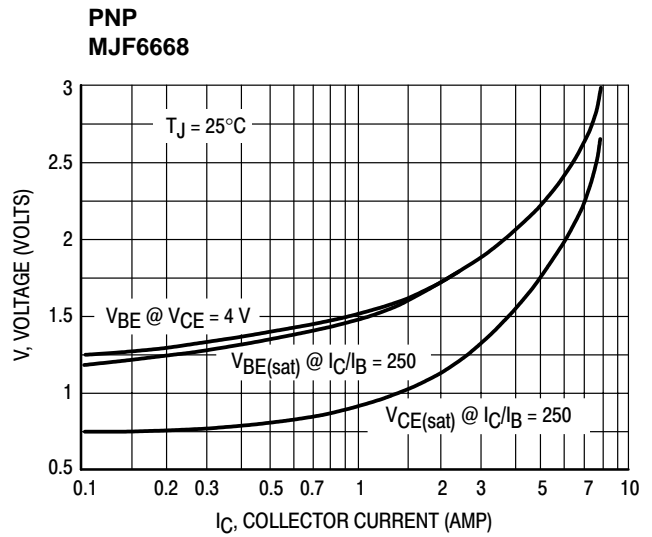
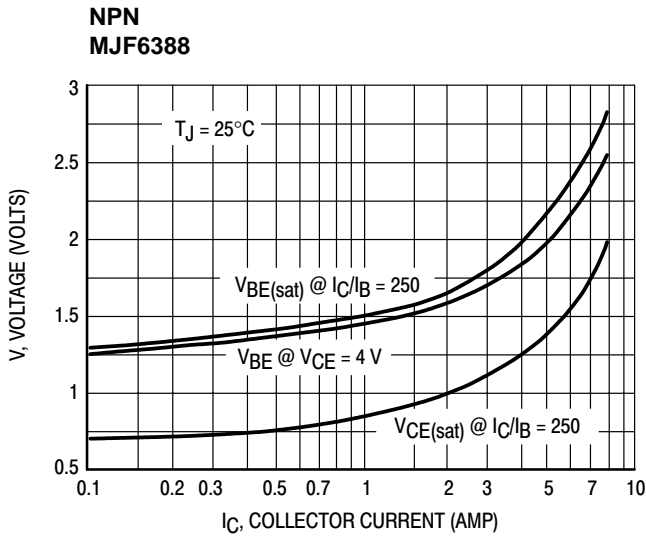


Figure 11. Typical "On" Voltages

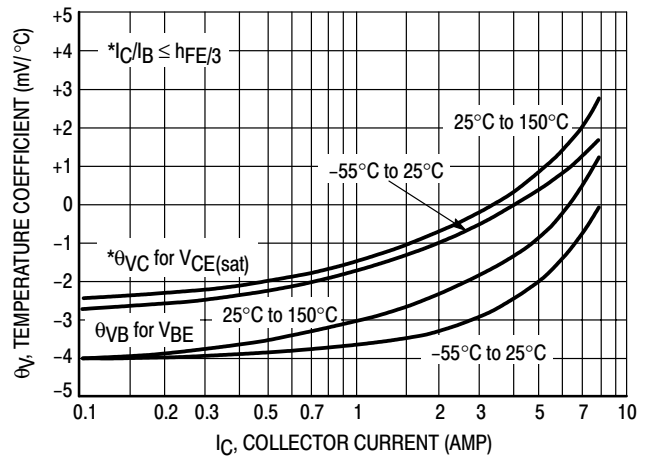
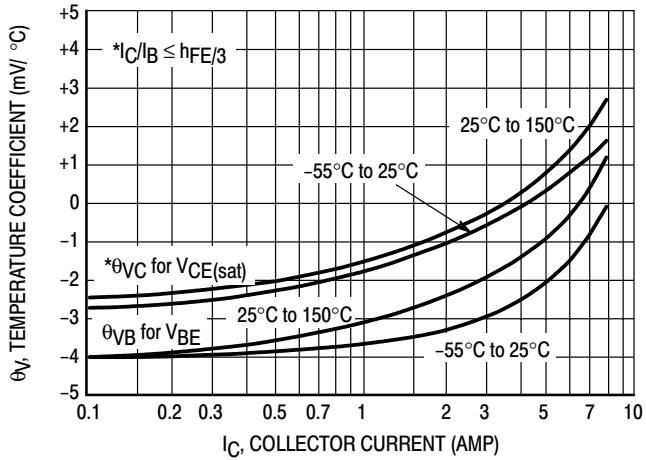


Figure 12. Typical Temperature Coefficients

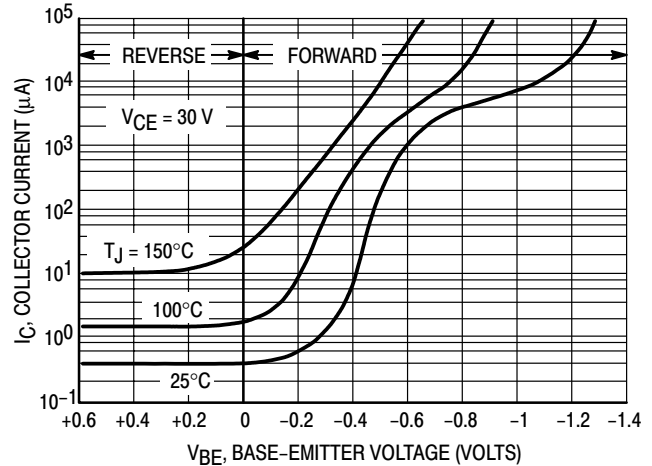
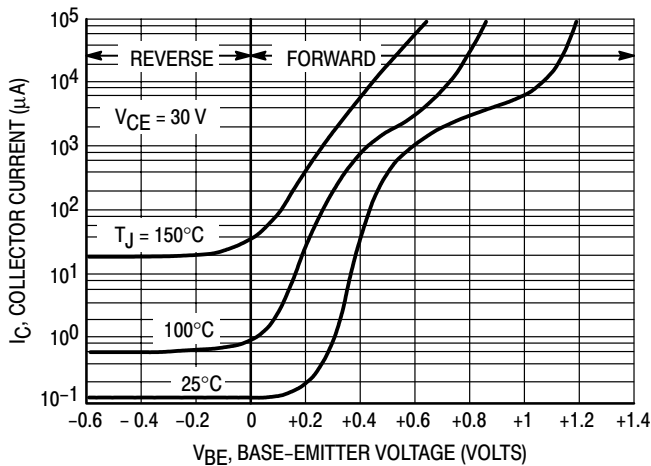


Figure 13. Typical Collector Cut-Off Region

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TEST CONDITIONS FOR ISOLATION TESTS*

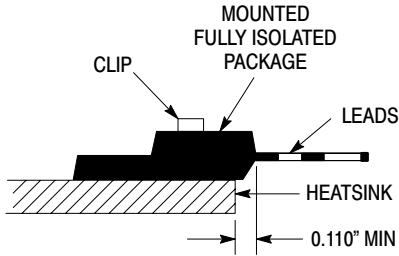


Figure 14. Clip Mounting Position for Isolation Test Number 1

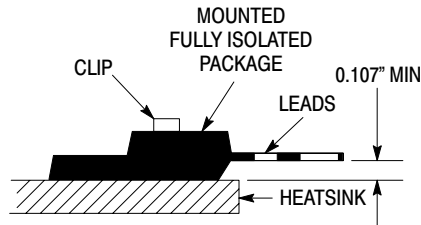


Figure 15. Clip Mounting Position for Isolation Test Number 2

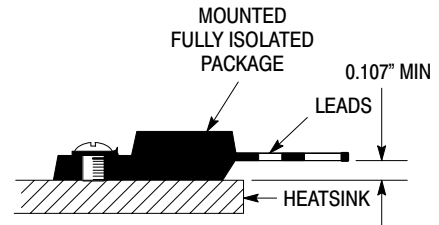


Figure 16. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

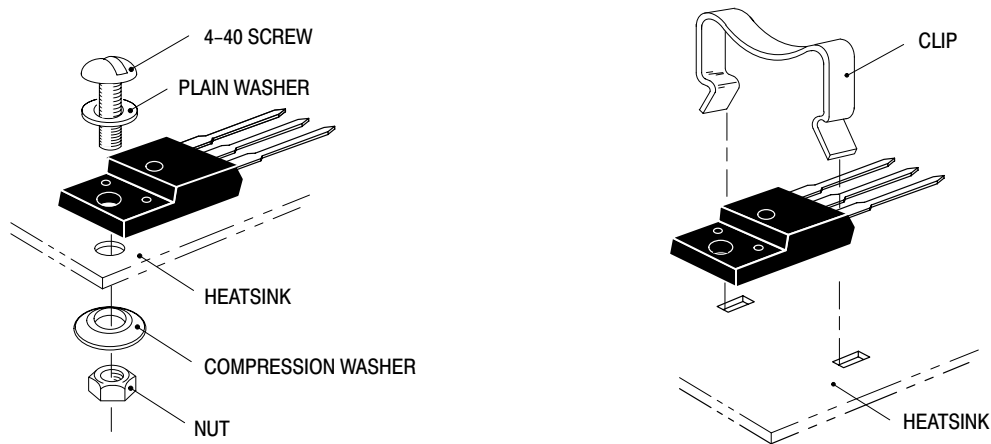


Figure 17. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

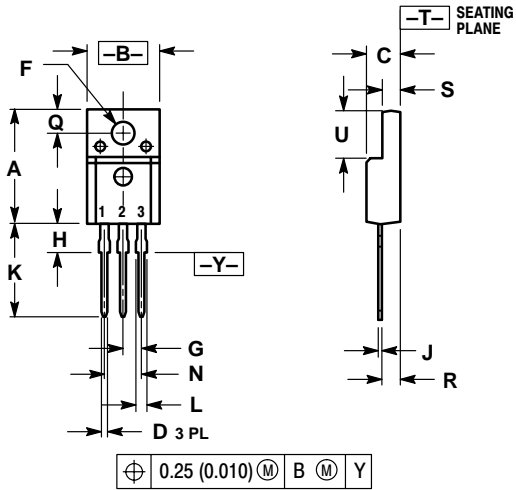
Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

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PACKAGE DIMENSIONS

CASE 221D-02 TO-220 TYPE ISSUE D




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

STYLE 2:

- PIN 1. BASE
- COLLECTOR
- EMITTER

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