PulseCre Giving you the edge

PCS1P2859A

rev 0.2

Multi-Output Clock Synthesizer

Features

- Generates multiple clock outputs from an inexpensive 25MHz crystal or external reference clock
- Frequency outputs:
 - 25MHz Reference clock
 - 33MHz
 - 48MHz (2 outputs)
 - 127MHz (2 outputs)
- · Zero ppm frequency synthesis error for all CLK outputs
- Supply Voltage :3.3V ± 5%V
- Low jitter design
- Packaged in 16 pin TSSOP
- Industrial Temperature range
- Compatible with CY22393XC-F12
- Advanced low-power CMOS process

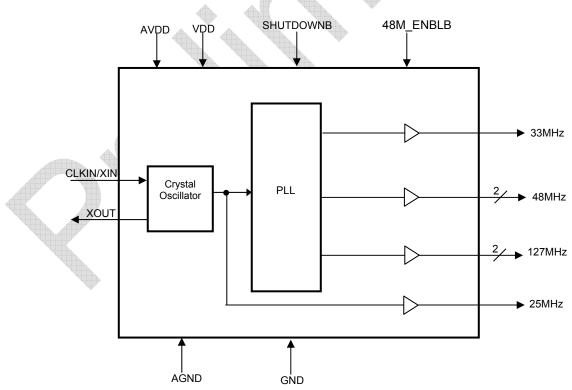
Block Diagram

Product Description

The PCS1P2859A is a Precision multi-PLL based frequency synthesizer. The six Clock outputs are generated using an inexpensive 25MHz Crystal. The outputs consist of 25 MHz reference clock, 33 MHz, two 127MHz and two 48MHz clocks. The SHUTDOWNB tristates all the clocks when enabled. The device operates from a Supply Voltage of 3.3V±5%V. The device is available in a 16-pin TSSOP JEDEC package for Industrial temperature range.

Application

PCS1P2859A is targeted for use in high-end multimedia, communications and consumer applications.



PulseCore Semiconductor Corporation 1715 S. Bascom Ave Suite 200, Campbell, CA 95008 • Tel: 408-879-9077 • Fax: 408-879-9018 www.pulsecoresemi.com

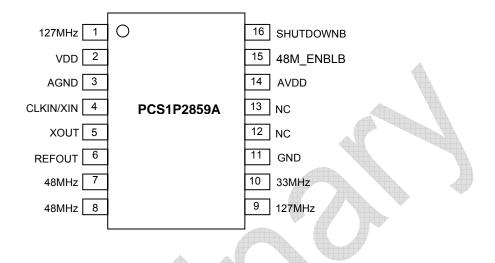


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Pin Diagram



Pin Description

Pin #	Pin Name	Pin Type	Pin Description		
1	127MHz	Output	127MHz Clock Output		
2	VDD	Power	Connect to +3.3V		
3	AGND	Power	Connect to ground		
4	CLKIN / XIN	Input	External reference Clock or Input Crystal connection.		
5	XOUT	Output	Connection to crystal. If using an external reference clock, this pin must be left unconnected		
6	REFOUT	Output	25MHz Reference Clock output		
7	48MHz	Output	48MHz Clock Output		
8	48MHz	Output	48MHz Clock Output		
9	127MHz	Output	127MHz Clock Output		
10	33MHz	Output	33MHz Clock Output		
11	GND	Power	Connect to ground		
12	NC		No connection		
13	NC		No connection		
14	AVDD	Power	Connect to +3.3V		
15		Innut	48MHz Output Enable bit. When this pin is made LOW, the 48MHz clocks		
15	48M_ENBLB	Input	are enabled. Tri-states 48MHz clocks when this pin is HIGH.		
16	SHUTDOWNB	Input	Output Enable bit. When this pin is made HIGH, all clocks are enabled.		
.0		input	Tri-states all clocks when this pin is LOW.		



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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Power Supply Voltage relative to Ground	-0.5 to +4.6	V
V _{IN}	Input Voltage relative to Ground (Input Pins)	-0.5 to VDD+0.3	v
T _{STG}	Storage temperature	-65 to +150	°C
Ts	Max. Soldering Temperature (10 sec)	260	°C
TJ	Junction Temperature	125	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV
Note: These are s device reli	tress ratings only and are not implied for functional use. Exposure to absolute maximum ratings fability.	for prolonged periods of time i	may affect

Operating Conditions

Parameter	Description		Тур	Max	Unit
VDD /AVDD	Operating Voltage	3.135	3.3	3.465	V
T _A	Operating Temperature (Ambient Temperature)	-40	T	+85	°C
CL	Load Capacitance			15	рF
C _{IN}	Input Capacitance		5		рF

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Units
VDD /AVDD	Operating Voltage	ϕ	3.135	3.3	3.465	V
VIH	Input High Voltage		2.2		VDD+0.3	V
VIL	Input Low Voltage		GND-0.3		1.0	V
Vон	Output High Voltage	VDD=3.135,Iон= -12mA	2.4			V
Vol	Output Low Voltage	VDD=3.135, IoL= 12mA			0.4	V
loz	Output Leakage Current	Three-state outputs			10	μA
Icc	Static Current	CLKIN and SHUTDOWN Pins pulled low			5.5	μA
IDD	Dynamic Current	No Load, All Clocks on			35	mA
Ζουτ	Nominal output impedance			30		Ω



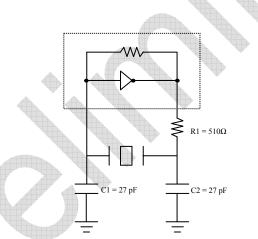
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AC Electrical Characteristics

Symbol	Par	Min	Тур	Max	Unit	
CLKIN/XIN	Input Clock Frequency	Input Clock Frequency				MHz
		Pin 10		33		MHz
CLK OUT	Output Clock Frequency	Pin 7,8		48		
		Pin 1,9		127		
		Pin 6		25		
t _{LH} 1	Rising edge slew rate (Meas	Rising edge slew rate (Measured from 20% to 80%)				V/nS
t _{HL} 1	Falling edge slew rate (Meas	1.3	2		V/nS	
T _{PJ} 1	Peak-to-peak Period Jitter @	Peak-to-peak Period Jitter @ VDD/2				pS
	Synthesis Error (Output Free	Synthesis Error (Output Frequency)				ppm
t _D 1	Output Duty Cycle	45	50	55	%	
tlock	PLL Lock Time from Power-	PLL Lock Time from Power-Up			3	mS
NOTE: 1. Measured with 15pF capacitive load						

Typical Crystal Oscillator Circuit



Typical Crystal Specifications

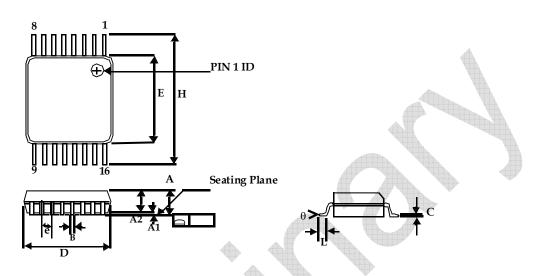
Fundamental AT cut parallel resonant crystal				
Nominal frequency	25MHz			
Frequency tolerance	± 50 ppm or better at 25°C			
Operating temperature range	-25°C to +85°C			
Storage temperature	-40°C to +85°C			
Load capacitance	18pF			
Shunt capacitance	7pF maximum			
ESR	25Ω			



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Package Information

16-lead Thin Shrunk Small Outline Package (4.40-MM Body)



	Dimensions				
Symbol	Inch	ies	Millimeters		
	Min	Max	Min	Мах	
А		0.043	V	1.20	
A1	0.002	0.006	0.05	0.15	
A2	0.031	0.041	0.80	1.05	
В	0.007	0.012	0.19	0.30	
с	0.004	0.008	0.09	0.20	
D	0.193	0.201	4.90	5.10	
E	0.169	0.177	4.30	4.50	
е	0.026 BSC		0.65 BSC		
н	0.252 BSC		6.40	BSC	
L	0.020	0.030	0.50	0.75	
θ	0°	8°	0°	8°	



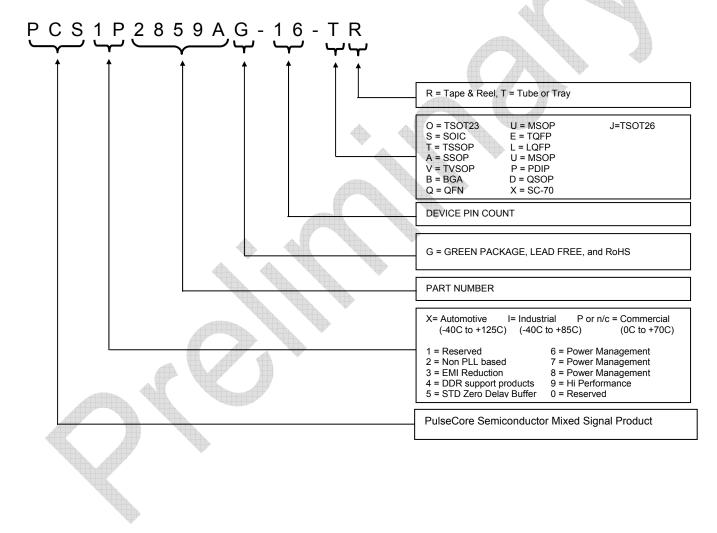
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Ordering Code

Part Number	Marking	Package	Temperature
PCS1P2859AG-16TR	1P2859AG	16-Pin TSSOP, TAPE & REEL, Green	Commercial
PCS1P2859AG-16TT	1P2859AG	16-Pin TSSOP, TUBE, Green	Commercial
PCS1I2859AG-16TR	112859AG	16-Pin TSSOP, TAPE & REEL, Green	Industrial
PCS1I2859AG-16TT	112859AG	16-Pin TSSOP, TUBE, Green	Industrial

Device Ordering Information



Licensed under US patent Nos 5,488,627 and 5,631,920.

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PulseCore Semiconductor Corporation 1715 S. Bascom Ave Suite 200 Campbell, CA 95008 Tel: 408-879-9077 Fax: 408-879-9018 www.pulsecoresemi.com

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003 Many PulseCore Semiconductor products are protected by issued patents or by applications for patent

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