



μPD72111
Small Computer System
Interface Controller

T-52-33-27

Description

The μPD72111 is a small computer system interface controller (SCSIC) conforming to ANSI X3T9.2/82-2 Rev.17B. The μPD72111 SCSI controller offers a true 16-bit CPU data bus but also can be interfaced to an 8-bit CPU data bus.

The μPD72111 contains functions for controlling the sequence between bus phases so that host processor overhead can be reduced. In addition, single-ended type bus drivers/receivers are internally provided on the SCSI bus side so that system size can be reduced.

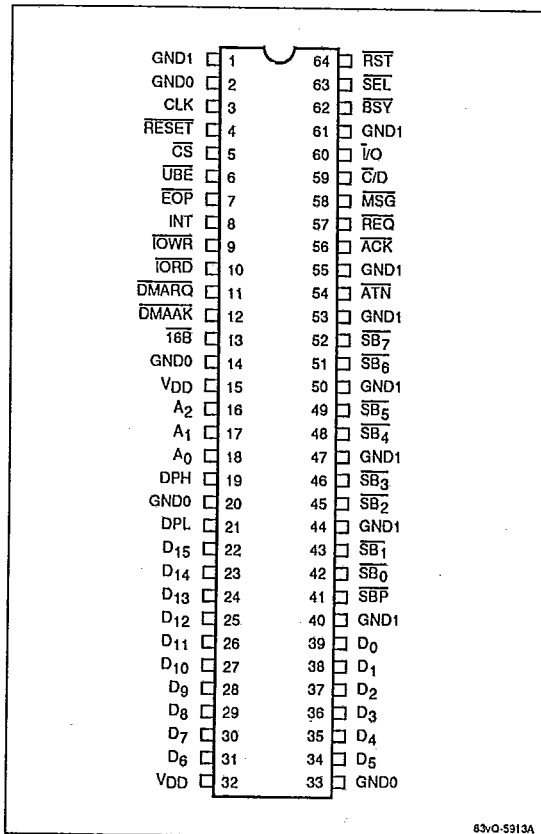
The μPD72111 was developed utilizing NEC's 1.2-μm CMOS process technology for low power consumption. It operates from a single 5-volt supply and is available in plastic DIP, PLCC, and miniflat packages.

Features

- Conforms to ANSI X3T9.2 Rev.17B
 - Arbitration function
 - Disconnection/reconnection function
 - Parity generation and check function
- Two different data transfer modes
 - Synchronous: 4.0 Mbytes/second max; offset value selectable from 1 to 8
 - Asynchronous: 4.0 Mbytes/second max target
- 16 commands reduce host CPU load; automatic execution of standard operation as SCSI controller can be performed by a single command
- Operates as initiator or target
- Internal single-ended type SCSI bus drivers (48-mA) and Schmitt-type receivers
- CPU data bus width selectable (16 bits or 8 bits)
- Programmed transfer or DMA transfer selectable
- Internal 24-bit transfer counter
- FIFO-type data buffers on SCSI bus side and CPU bus side

Pin Configurations

64-Pin Plastic Shrink DIP (750 mil)



83vQ-5913A

Ordering Information

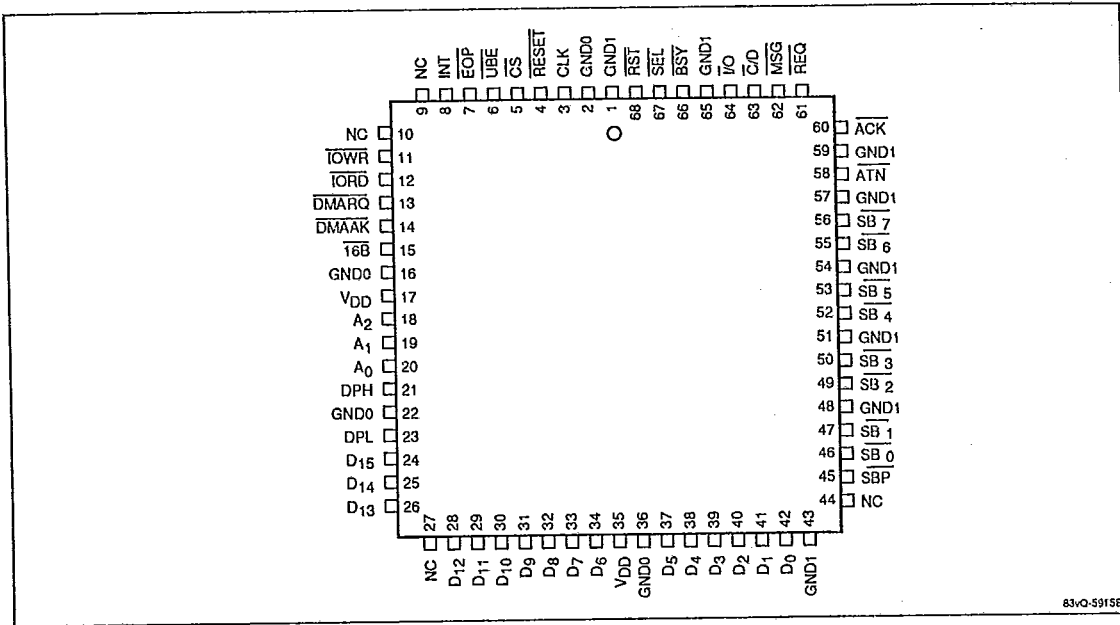
Part No.	Package
μPD72111CW	64-pin plastic shrink DIP (750 mil)
μPD72111L	68-pin PLCC
μPD72111GJ-5BJ	74-pin plastic miniflat



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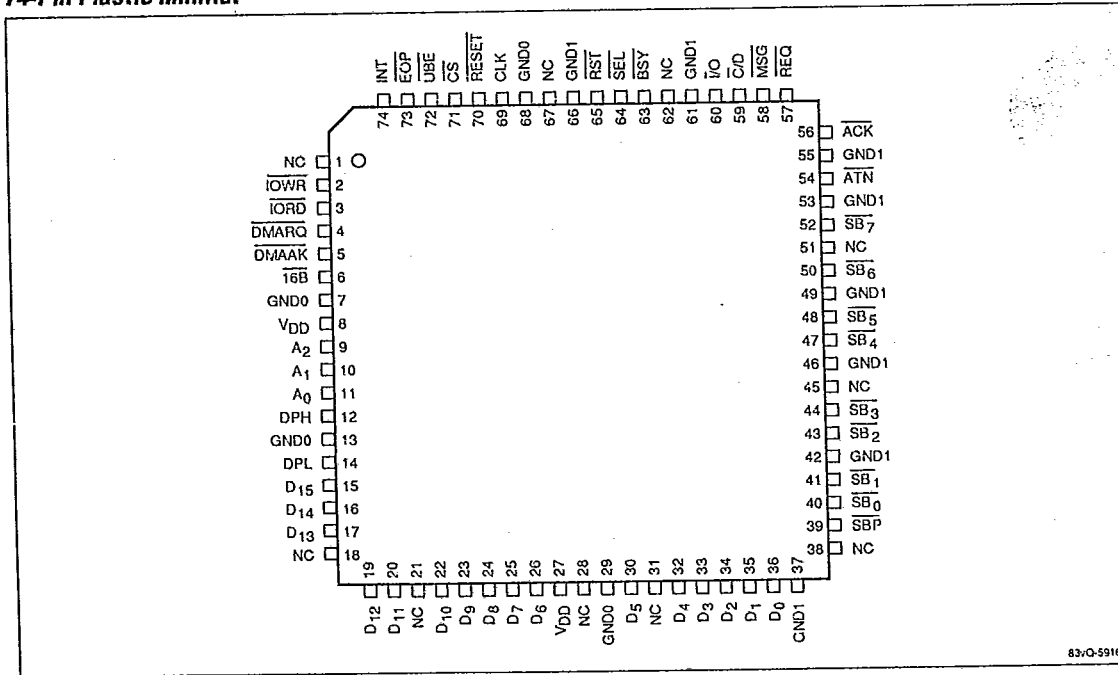
μPD72111

68-Pin PLCC



83/O-59158

74-Pin Plastic Miniflat



83/O-59168



μPD72111

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Pin Identification

Symbol	I/O	Signal Function
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CPU Interface Pins

A ₀ -A ₂	In	Address bus, bits 0-2. Specifies direct access register to be accessed.															
CS	In	Chip Select. Enables internal register accessing.															
D ₀ -D ₁₅	I/O	Data bus, bits 0-15. Function depends on bus mode. 16-Bit Bus Mode D ₀ -D ₇ Lower 8 data bits D ₈ -D ₁₅ Upper 8 data bits. 8-Bit Bus Mode D ₀ -D ₇ 8 data bits D ₈ -D ₁₅ High-impedance state															
DMAAK	In	DMA Acknowledge. DMA service enable signal input.															
DMARQ	Out	DMA Request. DMA service signal output.															
DPH	I/O	Data Parity High. In 16-bit bus mode, parity bit for data bits D ₈ -D ₁₅ . In 8-bit bus mode, this pin becomes high impedance.															
DPL	I/O	Data Parity Low. Parity bit for data bits D ₀ -D ₇ .															
EOP	Out	End of Process. Open-drain output that terminates DMA service data transfer.															
INT	Out	Interrupt Request. Open-drain output to CPU.															
IOR _D	In	I/O Read. Enables CPU to read contents of μPD72111 internal register.															
IOW _R	In	I/O Write. Enables CPU to write data to μPD72111 internal register.															
UBE	In	Upper Byte Enable. In 16-bit bus mode, indicates that upper 8 bits of data bus are valid; \overline{UBE} and address A ₀ determine how internal register is accessed. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A₀</th> <th>\overline{UBE}</th> <th>Register Access</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>16-bit units (D₀-D₁₅)</td> </tr> <tr> <td>0</td> <td>1</td> <td>8-bit units (D₀-D₇)</td> </tr> <tr> <td>1</td> <td>0</td> <td>8-bit units (D₈-D₁₅)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not allowed</td> </tr> </tbody> </table>	A ₀	\overline{UBE}	Register Access	0	0	16-bit units (D ₀ -D ₁₅)	0	1	8-bit units (D ₀ -D ₇)	1	0	8-bit units (D ₈ -D ₁₅)	1	1	Not allowed
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0	1	8-bit units (D ₀ -D ₇)															
1	0	8-bit units (D ₈ -D ₁₅)															
1	1	Not allowed															
16B	In	16-Bit Bus. Selects bus mode: 0 = 16-bit; 1 = 8-bit.															

SCSI Interface Pins

ACK	I/O	Acknowledge. Indicates that initiator has accepted the target information transfer request.
ATN	I/O	Attention. Indicates that initiator is requesting the message-out phase.
BSY	I/O	Busy. Indicates that another SCSI device is currently using the bus.
C/D	I/O	Command/Data.
I/O	I/O	Input/Output.

Symbol	I/O	Signal Function
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MSG	I/O	Message. Combinations of these signals determine the SCSI bus phase. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MSG</th> <th>C/D</th> <th>I/O</th> <th>Bus Phase</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Data-out</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Data-in</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Command</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Status</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Message-out</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Message-in</td> </tr> </tbody> </table>	MSG	C/D	I/O	Bus Phase	1	1	1	Data-out	1	1	0	Data-in	1	0	1	Command	1	0	0	Status	0	0	1	Message-out	0	0	0	Message-in
MSG	C/D	I/O	Bus Phase																											
1	1	1	Data-out																											
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1	0	1	Command																											
1	0	0	Status																											
0	0	1	Message-out																											
0	0	0	Message-in																											
REQ	I/O	Requests transfer of target information.																												
RST	I/O	Reset. When RST signal is detected, μPD72111 immediately releases SCSI bus, sets INT pin active, and then enters idle state.																												
SB ₀ -SB ₇	I/O	SCSI data bus, bits 0-7.																												
SBP	I/O	Parity bit for SCSI data bus.																												
SEL	I/O	Indicates that the select/reselect operation is being executed.																												

Other Pins

CLK	In	External clock.
RESET	In	System reset.
GND0	-	Ground (0 V).
GND1	-	Driver/receiver ground (0 V).
V _{DD}	In	+5-volt power supply.

Notes:

- Each SCSI Interface pin has an open-drain driver and a Schmitt receiver so that the μPD72111 can be directly connected to a single-end SCSI bus.
- After reset, the status of each output pin and each I/O pin is high-impedance except:

DMARQ	High level
EOP	High level
INT	Low level

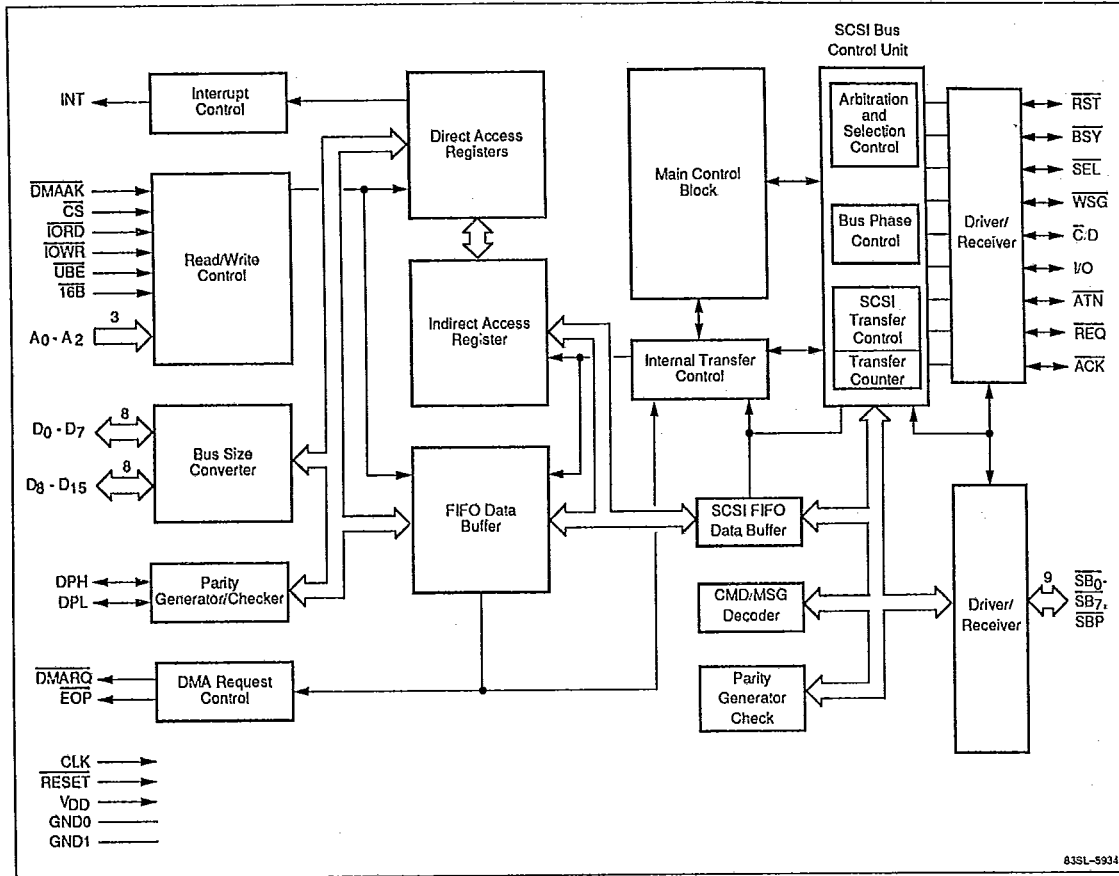




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μPD72111

μPD72111 Block Diagram

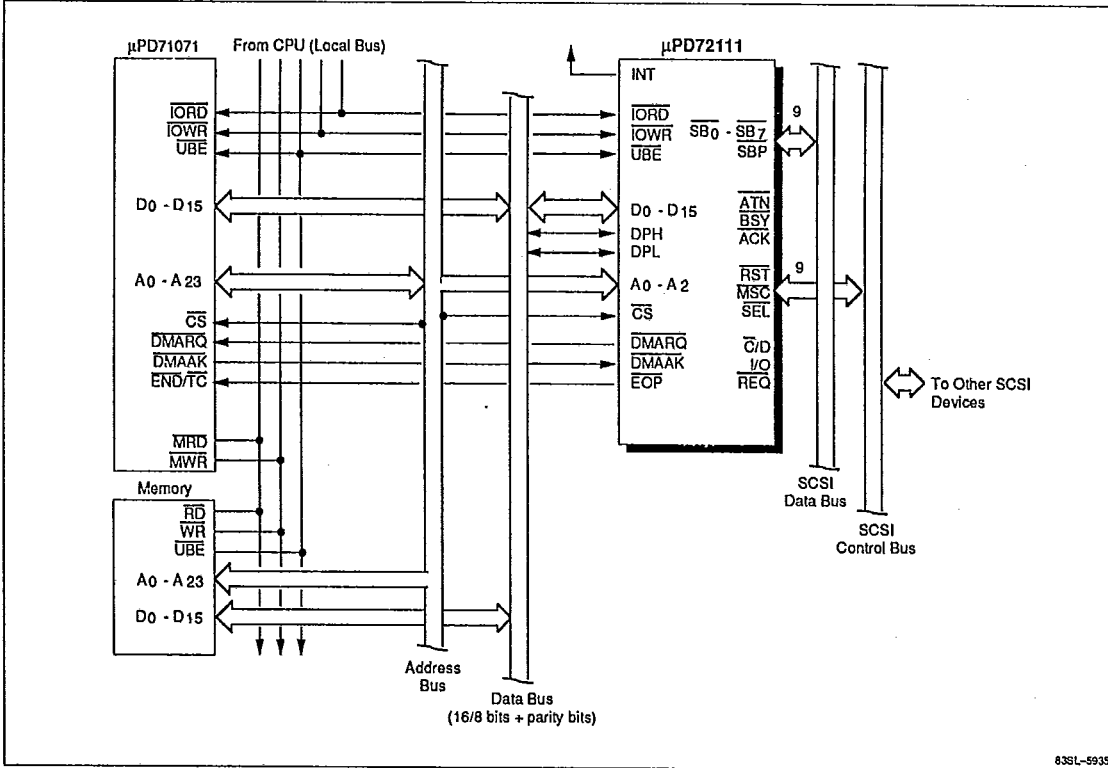




μPD72111

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Typical System Configuration





μPD72111

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Internal Blocks

Name	Description
SCSI bus driver/receiver	Open-drain driver for a single-end SCSI bus and a Schmitt-type receiver.
Arbitration/selection control	Controls execution sequence of arbitration, selection, and reselection phases; consists of a timing generator and a sequencer.
Bus phase control	Outputs a signal that specifies bus phase type; also monitors bus phase to detect a transition.
SCSI transfer control	Controls data transfer operation on the SCSI bus in each data transfer phase: data-in, data-out, status, message-in, and message-out. Controls SCSI protocol according to \overline{REQ} and ACK signals. Controls data transfer execution/termination according to SCSI FIFO status. Contains a 24-bit transfer counter that manages the amount of transfer data on the SCSI bus.
SCSI FIFO data buffer	Eight-bit, eight-stage asynchronous FIFO that adjusts difference between data transfer timing of internal and external SCSI buses; also used for queuing received data for synchronous data transfer.
Command/message decoder	Decodes received command and message; generates decoded signal that specifies the next sequence.
SCSI parity generator/checker	Generates parity that will be attached to data output to SCSI data bus; or checks parity attached to data read out from SCSI data bus.
Main control	Sequencer that controls microprogram, operation of each block, and control sequence.
Internal transfer control	Controls data transfer between SCSI FIFO and FIFO or between registers in the indirect access register block. Controls 8-bit/16-bit conversion when host CPU is set to 16-bit bus mode.
Direct access registers	Comprises registers that can be directly accessed from host CPU, such as command register, status register, etc.
Indirect access registers	Comprises registers that cannot be directly accessed from host CPU, but that can be accessed through the window in the direct access register.
FIFO data buffer	This 16-bit, eight-stage asynchronous FIFO increases usage rate of host bus. In 8-bit mode, only the lower 8 bits are used; in 16-bit mode, accessing in 8-bit units is not possible.
Interrupt control	Sets/resets interrupt request signal.
Read/write control	Controls read/write operation of various internal registers; also controls 8-bit accessing in 16-bit mode.
Bus-size converter	Converts bus size according to bus mode.

Name	Description
Host parity generator/checker	Generates parity that will be attached to data output to CPU data bus; or checks parity attached to data read out from CPU data bus.
DMA request control	Generates DMA service request signal (\overline{DMARQ}) according to FIFO status; also controls termination of command operation by \overline{EOP} signal.

Absolute Maximum Ratings

$T_A = +25^\circ\text{C}$

Supply voltage, V_{DD}	-0.5 to +7.0 V
Input voltage, V_I	-0.5 to $V_{DD} + 0.5$ V
Output voltage, V_O	-0.5 to $V_{DD} + 0.5$ V
Operating temperature, T_{OPT}	-10 to +70°C
Storage temperature, T_{STG}	-65 to +150°C

DC Characteristics

$T_A = -10$ to $+70^\circ\text{C}$; $V_{DD} = +5.0$ V $\pm 10\%$

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL1}	0	0.8	V	Other than CLK
	V_{IL2}	0	0.6	V	CLK
High-level input voltage	V_{IH1}	2.2		V	CPU bus
	V_{IH2}	2.0		V	SCSI bus
	V_{IH3}	3.9		V	CLK
Input hysteresis	V_{HI}	0.2		V	SCSI bus
Low-level output voltage	V_{OL1}	0.4		V	$I_{OL1} = 2.5$ mA; CPU bus
	V_{OL2}	0.4		V	$I_{OL2} = 48.0$ mA; SCSI bus
High-level output voltage	V_{OH}	2.4		V	$I_{OH} = -400$ μA ; CPU bus
Low-level input leakage current	I_{LIL1}	-10		μA	$V_I = 0$ V; CPU bus
	I_{LIL2}	-1.0		mA	$V_I = 0$ V; SCSI bus
High-level input leakage current	I_{LIH1}	10		μA	$V_I = V_{DD}$; CPU bus
	I_{LIH2}	0.1		mA	$V_I = V_{DD}$; SCSI bus
Low-level output leakage current	I_{LOL}	-10		μA	$V_I = 0$ V; CPU bus



DC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
High-level output leakage current	I_{LOH1}	10		μA	$V_O = V_{DD}$; CPU bus
Low-level output leakage current	I_{LOH2}	0.25		mA	$V_O = V_{DD}$; SCSI bus
Supply current	I_{DD}	100		mA	At 16 MHz

Capacitance

$T_A = +25^\circ\text{C}$; $V_{DD} = 0\text{ V}$; $f = 1\text{ Mhz}$

Item	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_i	20		pF	CPU bus; unmeasured pins at 0 V.
Output capacitance	C_o	20		pF	
Input/output capacitance	C_{IO1}	20		pF	
	C_{IO2}	100		pF	SCSI bus; unmeasured pins at 0 V.

Figure 1. Voltage Thresholds for Timing Measurements

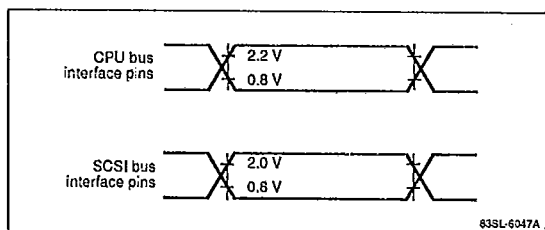


Figure 2. Clock Timing

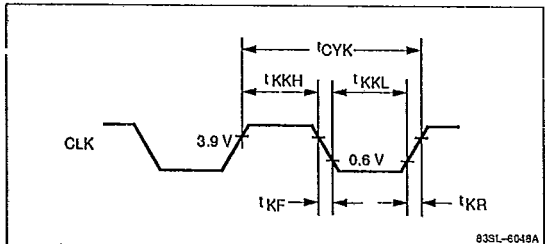
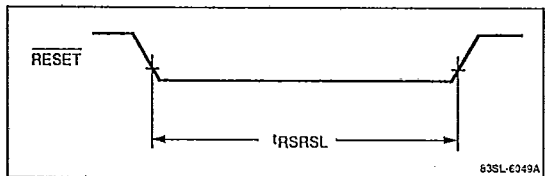


Figure 3. RESET Waveform



AC Characteristics; CPU Bus Interface

$T_A = -10\text{ to }+70^\circ\text{C}$; $V_{DD} = +5.0\text{ V} \pm 10\%$; see figure 1 for timing measurement voltage thresholds

Parameter	Symbol	Min	Max	Unit	Conditions
Clock (figure 2)					
CLK input cycle time	t_{CYK}	60		ns	
CLK input high-level width	t_{KKH}	25		ns	
CLK input low-level width	t_{KKL}	25		ns	
CLK input rise time	t_{KR}	10		ns	
CLK input fall time	t_{KF}	10		ns	

Reset (figure 3)

RESET low-level width	t_{RSRL}	16		t_{CYK}	
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CPU Bus Read (figure 4)

\overline{CS} set time to $\overline{IORD} \downarrow$	t_{SCSR}	20		ns	
\overline{CS} hold time from $\overline{IORD} \uparrow$	t_{HRCS}	0		ns	
Address set time to $\overline{IORD} \downarrow$	t_{SAR}	20		ns	
Address hold time from $\overline{IORD} \uparrow$	t_{HRA}	0		ns	
DMAAK set time to $\overline{IORD} \downarrow$	t_{SDAR}	20		ns	
DMAAK hold time from $\overline{IORD} \uparrow$	t_{HRDA}	0		ns	
\overline{IORD} low-level width	t_{RRL}	80		ns	
$\overline{IORD} \uparrow$ to data output delay time	t_{ORD}	50		ns	
$\overline{IORD} \uparrow$ to data float time	t_{FRD}	0	50	ns	
$\overline{IORD} \uparrow$ to $\overline{DMARQ} \uparrow$ delay time	t_{DRDQ}	80		ns	

CPU Bus Write (figure 5)

\overline{CS} set time to $\overline{IOWR} \downarrow$	t_{SCSW}	20		ns	
\overline{CS} hold time from $\overline{IOWR} \uparrow$	t_{HWCS}	0		ns	
Address set time to $\overline{IOWR} \downarrow$	t_{SAW}	20		ns	
Address hold time from $\overline{IOWR} \uparrow$	t_{HWA}	0		ns	
DMAAK set time to $\overline{IOWR} \downarrow$	t_{SDAW}	20		ns	
DMAAK hold time from $\overline{IOWR} \uparrow$	t_{HWDA}	0		ns	
\overline{IOWR} low-level width	t_{WWL}	80		ns	
Data set time to $\overline{IOWR} \uparrow$	t_{SDW}	20		ns	
Data hold time from $\overline{IOWR} \uparrow$	t_{HWD}	0		ns	
$\overline{IOWR} \uparrow$ to $\overline{DMARQ} \uparrow$ delay time	t_{DWDQ}	80		ns	

Other CPU Bus (figure 6)

$\overline{IOWR} \uparrow$ to $\overline{IORD} \downarrow$ or $\overline{IOWR} \uparrow$ recovery time	t_{RWV}	80		ns	
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AC Characteristics; CPU Bus Interface (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
\overline{IORD} ↑ to \overline{IORD} ↓ or \overline{IOWR} ↓ recovery time	t_{RVR}	80		ns	
\overline{IORD} ↑ to \overline{EOP} ↓ delay time	t_{DREP}	40		ns	
\overline{IOWR} ↑ to \overline{EOP} ↓ delay time	t_{DWEP}	40		ns	
\overline{IORD} ↑ to INT ↓ delay time	t_{DRI}	40		ns	
\overline{IOWR} ↑ to INT ↓ delay time	t_{DWI}	40		ns	
INT low-level width	t_{IIL}	2		t_{CYK}	

AC Characteristics; SCSI Bus Interface

$T_A = -10$ to $+70^\circ\text{C}$; $V_{DD} = +5.0\text{ V} \pm 10\%$; see figure 1 for timing measurement voltage thresholds

Parameter	Symbol	Min	Max	Unit	Conditions
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Arbitration (figure 7)

Bus free detection to \overline{BSY} response time	t_{DBFBY}	14		t_{CYK}	
\overline{BSY} ↓ to ID output delay time	t_{DBYID}	0		ns	
\overline{BSY} ↓ to \overline{SEL} ↓ delay time	t_{DBYSL}	36		t_{CYK}	

Selection as initiator (figure 8)

\overline{SEL} ↓ to ID output delay time	t_{DSLID1}	20		t_{CYK}	
\overline{SEL} ↓ to \overline{ACK} , \overline{ATN} output delay time	t_{DSLAK}	20		t_{CYK}	
\overline{ACK} , \overline{ATN} output to \overline{BSY} ↑ delay time	t_{DAKBY}	2		t_{CYK}	
\overline{BSY} ↑ to \overline{BSY} ↓ input valid delay time	t_{DBYBY1}	8		t_{CYK}	
\overline{BSY} ↓ to \overline{SEL} ↑ output delay time	t_{DBYSL1}	2		t_{CYK}	

Selection as target (figure 9)

\overline{BSY} hold time from \overline{SEL} ↓	t_{HSLBY1}	0		ns	
ID set time from \overline{BSY} ↑	t_{SIDBY}	0		ns	
\overline{BSY} ↑ to \overline{BSY} ↓ output delay time	t_{DBYBY2}	10		t_{CYK}	
ID hold time from \overline{BSY} ↓	t_{HBYID1}	0		ns	
\overline{SEL} hold time from \overline{BSY} ↓	t_{HEYSL1}	0		ns	
\overline{ATN} set time to \overline{SEL} ↑	t_{SATSL}	0		ns	
\overline{SEL} ↑ to target output delay time	t_{DSLTD}	2		t_{CYK}	

Reselection as initiator (figure 10)

\overline{BSY} hold time from \overline{SEL} ↓	t_{HSLBY2}	0		ns	
ID set time to \overline{BSY} ↑	t_{SIDBY}	0		ns	
I/O set time to \overline{BSY} ↑	t_{SIOBY}	0		ns	

Parameter	Symbol	Min	Max	Unit	Conditions
\overline{SEL} ↑ to \overline{ATN} output delay time	t_{DSLAT}	2		t_{CYK}	
\overline{BSY} ↑ to \overline{BSY} ↓ output delay time	t_{DBYBY3}	10		t_{CYK}	
ID hold time from \overline{BSY} ↓	t_{HBYID2}	0		ns	
\overline{SEL} hold time from \overline{BSY} ↓	t_{HBYSL2}	0		ns	
\overline{SEL} ↑ to \overline{BSY} ↑ output delay time	t_{DSLBY}	2		t_{CYK}	

Reselection as target (figure 11)

\overline{SEL} ↑ to ID output delay time	t_{DSLID2}	20		t_{CYK}	
\overline{SEL} ↓ to target output delay time	t_{DSLTD}	0		ns	
ID output to I/O output delay time	t_{DIDIO}	0		ns	
I/O input to \overline{BSY} ↑ output delay time	t_{DIOBY}	2		t_{CYK}	
\overline{BSY} ↑ to \overline{BSY} ↓ input valid delay time	t_{DBYBY4}	8		t_{CYK}	
\overline{BSY} ↓ to \overline{SEL} ↑ output delay time	t_{DBYSL2}	2		t_{CYK}	

Reception as initiator in asynchronous mode; data-in, status, and message-in phases (figure 12)

\overline{SEL} ↑ to phase input valid delay time	t_{DSLPH1}	0		ns	
I/O ↓ to data float delay time	t_{FIOD1}	0		ns	
Phase set time to \overline{REQ} ↓	t_{SPHRQ1}	400		ns	
Data set time to \overline{REQ} ↓	t_{SDRQ1}	5		ns	
\overline{REQ} ↓ to \overline{ACK} ↓ output delay time	t_{DRQAK1}	0		ns	
Data hold time from \overline{ACK} ↓	t_{HAKD1}	0		ns	
\overline{REQ} hold time from \overline{ACK} ↓	t_{HAKRQ1}	0		ns	
\overline{REQ} ↑ to \overline{ACK} ↑ output delay time	t_{DRQAK2}	1		t_{CYK}	
Phase hold time from \overline{ACK} ↑	t_{HAKPH1}	0		ns	

Transfer as target in asynchronous mode; data-in, status, and message-in phases (figure 13)

\overline{SEL} ↑ to phase output delay time	t_{DSLPH2}	2		t_{CYK}	
I/O ↓ to data output delay time	t_{DIOD1}	0		ns	
Phase set time to \overline{REQ} ↓	t_{SPHRQ2}	500		ns	
Data hold time to \overline{REQ} ↓	t_{SDRQ2}	55		ns	
\overline{REQ} ↓ to \overline{ACK} ↓ input valid delay time	t_{DRQAK3}	0		ns	
\overline{ACK} ↓ to \overline{REQ} ↑ output delay time	t_{DAKRQ1}	1		t_{CYK}	
Data hold time from \overline{ACK} ↓	t_{HAKD2}	0		ns	



AC Characteristics; SCSI Bus Interface (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
ACK hold time from REQ ↑	t _{HRQAK1}	0		ns	
ACK ↑ to REQ ↓ output delay time	t _{DAKRQ2}	1		t _{CYK}	
Phase hold time from ACK ↑	t _{HAKPH2}	1		t _{CYK}	

Transfer as initiator in asynchronous mode; data-out, command, and message-in phases (figure 14)

SEL ↑ to phase input delay time	t _{DSLPH3}	0		ns	
I/O ↑ to data output delay time	t _{DIOD2}	0		ns	
Phase set time to REQ ↓	t _{SPHRQ3}	400		ns	
Data set time to ACK ↓	t _{SDAK1}	55		ns	
REQ ↓ to ACK ↓ output delay time	t _{DRQAK4}	1		t _{CYK}	
Data hold time from REQ ↑	t _{HRQD1}	0		ns	
REQ hold time from ACK ↓	t _{HAKRQ2}	0		ns	
REQ ↑ to ACK ↑ output delay time	t _{DRQAK5}	1		t _{CYK}	
Phase hold time from ACK ↑	t _{HAKPH3}	0		ns	

Reception as target in asynchronous mode; data-out, command, and message-out phases (figure 15)

SEL ↑ to phase output delay time	t _{DSLPH4}	2		t _{CYK}	
I/O ↑ to data float delay time	t _{FIOD2}	0		ns	
Phase set time to REQ ↓	t _{SPHRQ4}	500		ns	
Data set time to ACK ↓	t _{SDAK2}	5		ns	
REQ ↓ to ACK ↓ input valid delay time	t _{DRQAK6}	0		ns	
ACK ↓ to REQ ↑ output delay time	t _{DAKRQ3}	1		t _{CYK}	
Data hold time from REQ ↑	t _{HRQD2}	0		ns	
ACK hold time from REQ ↑	t _{HRQAK2}	55		ns	
ACK hold time from REQ ↑	t _{HRQAK2}	55		ns	
ACK ↑ to REQ ↓ output delay time	t _{DAKRQ4}	1		t _{CYK}	
Phase hold time from ACK ↑	t _{HAKPH4}	1		t _{CYK}	

Reception as initiator in synchronous mode; data-in phase (figure 16)

SEL ↑ to phase input delay time	t _{DSLPH5}	0		ns	
I/O ↓ to data float delay time	t _{FIOD3}	0		ns	
Phase set time to REQ ↓	t _{SPHRQ5}	400		ns	
Data set time to REQ ↓	t _{SDRQ3}	5		ns	
Data hold time from REQ ↓	t _{HRQD3}	5		ns	
REQ input low-level width	t _{RQRQL1}	50		ns	
REQ ↑ to REQ ↓ recovery time	t _{RVRQ1}	2		t _{CYK}	
ACK output low-level width	t _{AKAKL1}	2		t _{CYK}	

Parameter	Symbol	Min	Max	Unit	Conditions
Phase hold time from ACK ↑	t _{HAKPH5}	0		ns	

Transfer as target in synchronous mode; data-in phase (figure 17)

SEL ↑ to phase output delay time	t _{DSLPH6}	2		t _{CYK}	
I/O ↓ to data output delay time	t _{DIOD3}	0		ns	
Phase set time to REQ ↓	t _{SPHRQ6}	500		ns	
Data set time to REQ ↓	t _{SDRQ4}	55		ns	
Data hold time from REQ ↓	t _{HRQD4}	125		ns	
REQ output low-level width	t _{RQRQL2}	2		t _{CYK}	
ACK input low-level width	t _{AKAKL2}	50		ns	
ACK ↑ to ACK ↓ recovery time	t _{RAK1}	2		t _{CYK}	
Phase hold time from ACK ↑	t _{HAKPH6}	1		t _{CYK}	

Transfer as initiator in synchronous mode; data-out phase (figure 18)

SEL ↑ to phase input valid delay time	t _{DSLPH7}	0		ns	
I/O ↓ to data output delay time	t _{DIOD4}	0		ns	
Phase set time to REQ ↓	t _{SPHRQ7}	400		ns	
Data set time to ACK ↓	t _{SDAK3}	55		ns	
Data hold time from ACK ↓	t _{HAKD3}	125		ns	
REQ input low-level width	t _{RQRQL3}	50		ns	
REQ ↑ to REQ ↓ recovery time	t _{RVRQ2}	2		t _{CYK}	
ACK output low-level width	t _{AKAKL3}	2		t _{CYK}	
Phase hold time from ACK ↑	t _{HAKPH7}	0		ns	

Reception as target in synchronous mode; data-out phase (figure 19)

SEL ↑ to phase output delay time	t _{DSLPH8}	2		t _{CYK}	
I/O ↓ to data float delay time	t _{FIOD4}	0		ns	
Phase set time to REQ ↓	t _{SPHRQ8}	500		ns	
Data set time to ACK ↓	t _{SDAK4}	5		ns	
Data hold time from DAK ↓	t _{HAKD4}	5		ns	
REQ output low-level width	t _{RQRQL4}	2		t _{CYK}	
ACK input low-level width	t _{AKAKL4}	50		ns	
ACK ↑ to ACK ↓ recovery time	t _{RAK2}	125		ns	
Phase hold time from ACK ↑	t _{HAKPH8}	1		t _{CYK}	

Arbitration; bus free (figure 20)

SEL ↓ to ID float delay time	t _{FSLID}			4t _{CYK} ns +50	
------------------------------	--------------------	--	--	-----------------------------	--

Selection/reselection; bus free (figure 21)

ID float to SEL ↑ delay time	t _{DIDSL}	3200		t _{CYK}	
SEL ↑ to control float delay time	t _{FSLCTL}	0		ns	





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Figure 4. CPU Bus Read

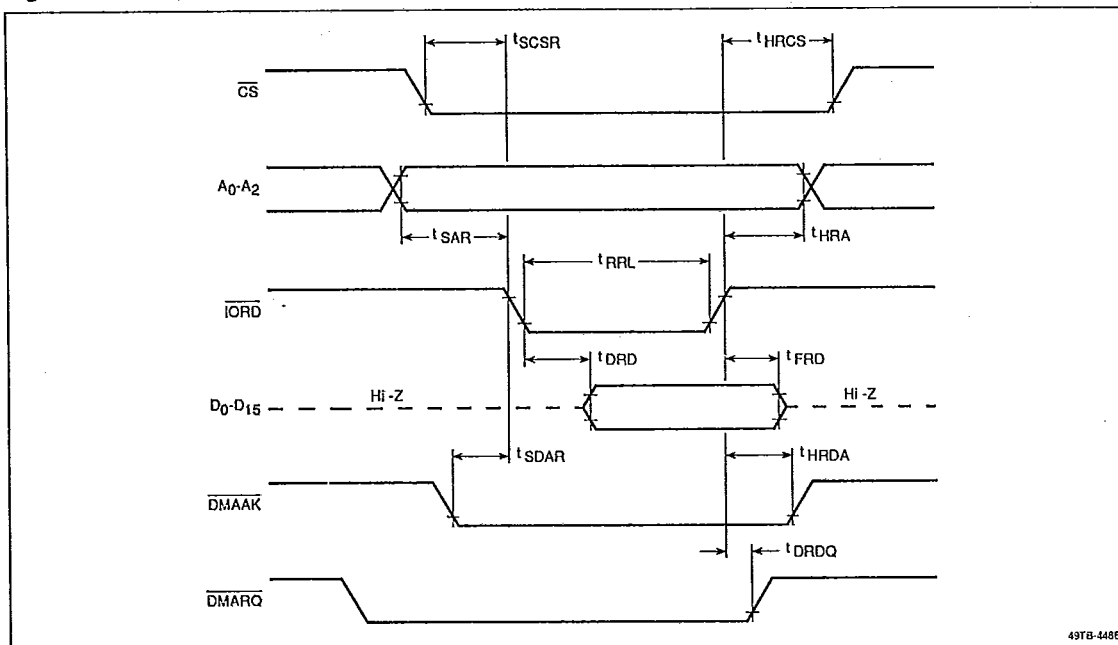


Figure 5. CPU Bus Write

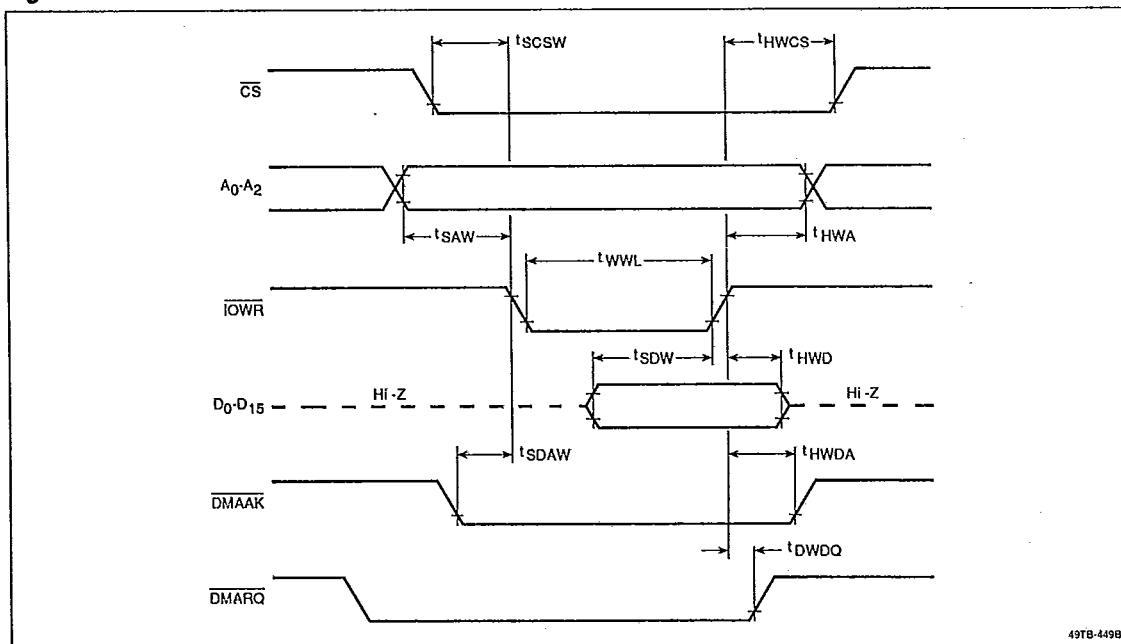




Figure 6. Other CPU Bus Timing

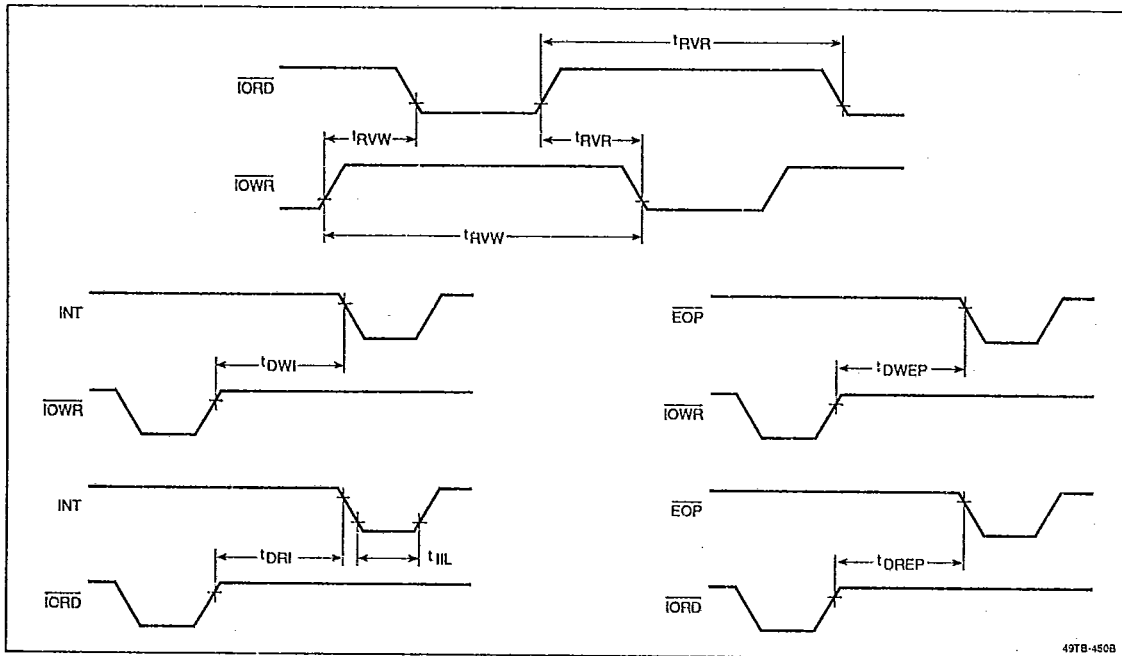
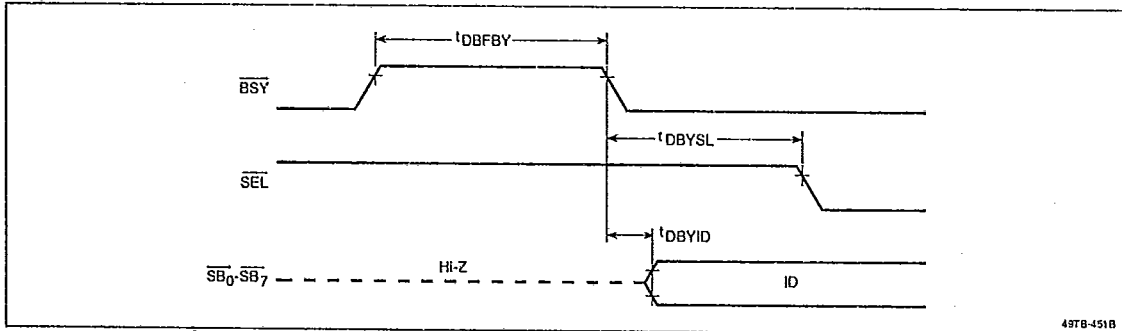


Figure 7. SCSI Bus; Arbitration

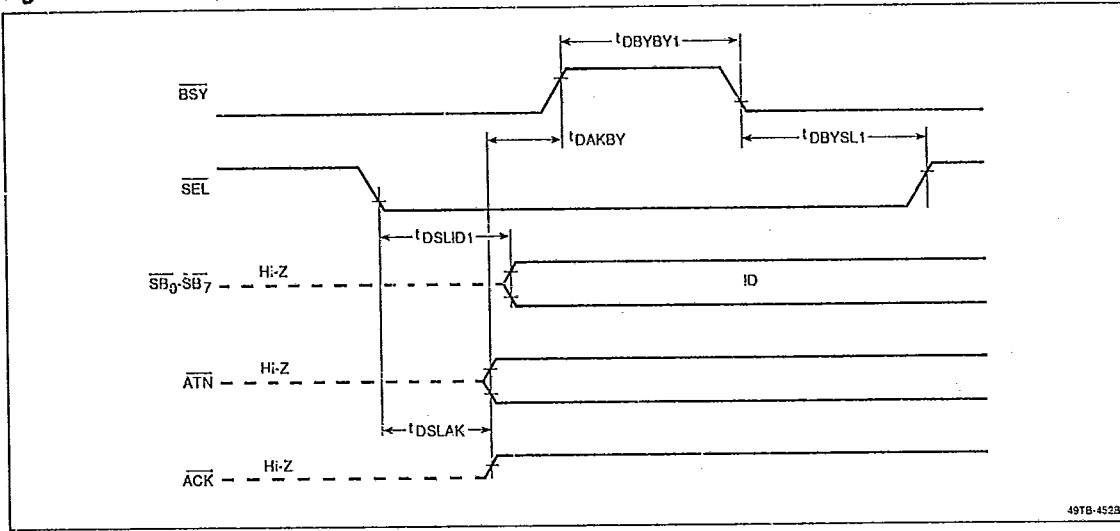


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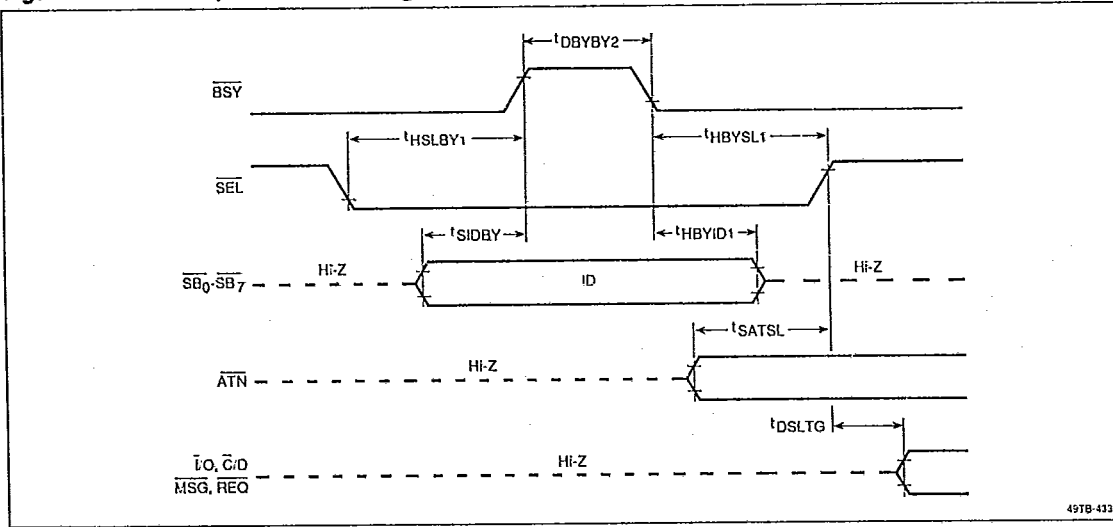
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Figure 8. SCSI Bus; Selection as Initiator



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Figure 9. SCSI Bus; Selection as Target



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Figure 10. SCSI Bus; Reselection as Initiator

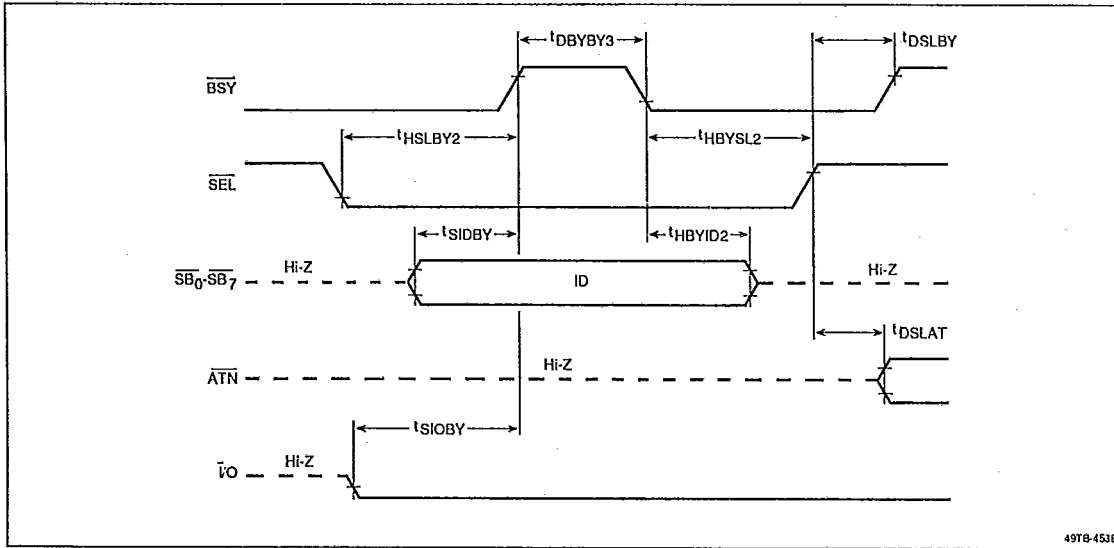
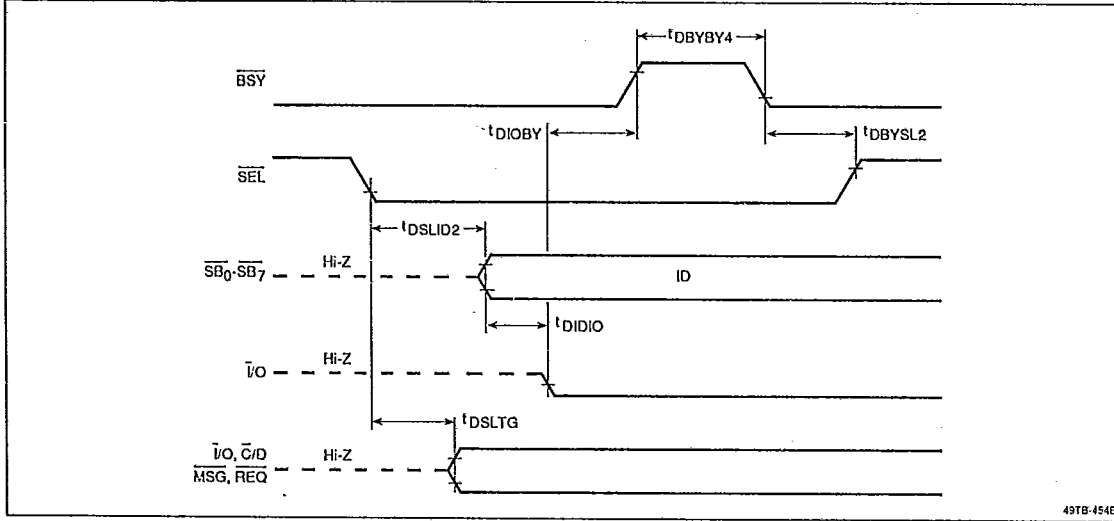
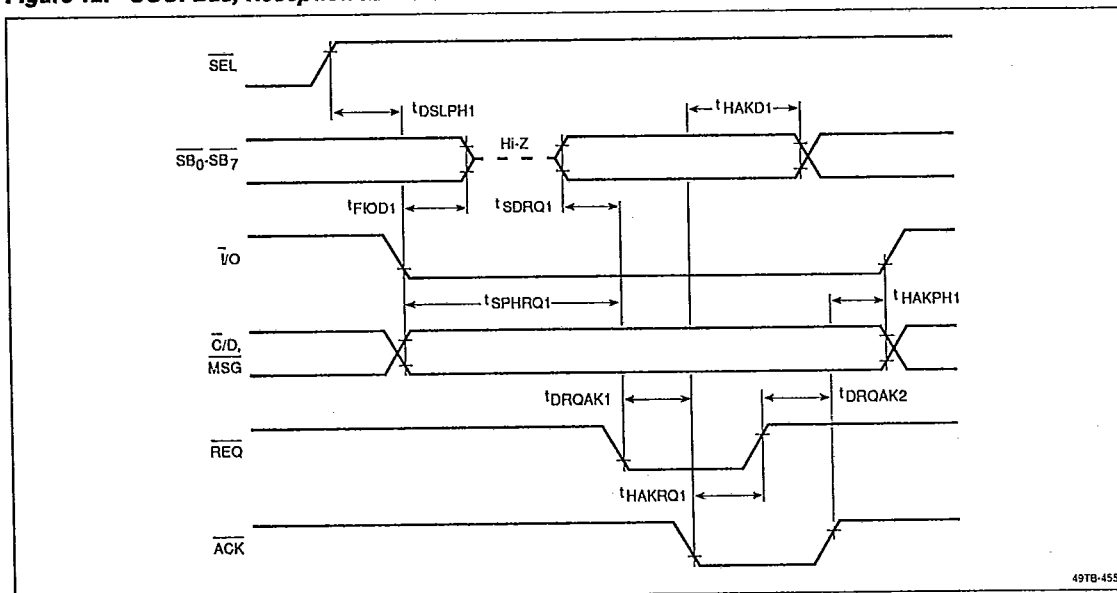


Figure 11. SCSI Bus; Reselection as Target



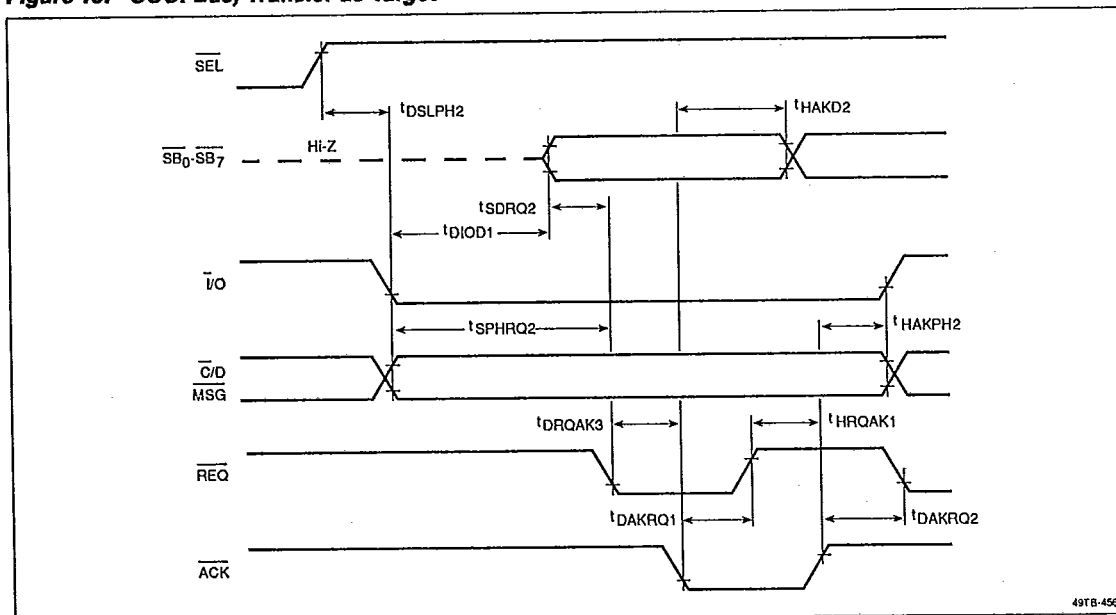
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Figure 12. SCSI Bus; Reception as Initiator



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Figure 13. SCSI Bus; Transfer as Target



49TB-455B

Figure 14. SCSI Bus; Transfer as Initiator in Async Mode

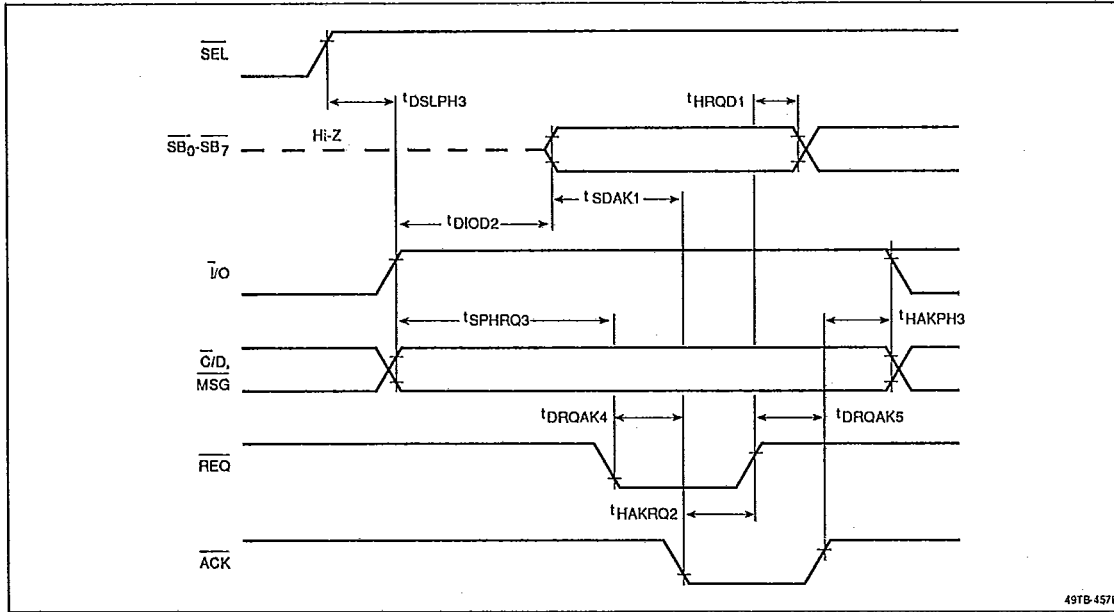


Figure 15. SCSI Bus; Reception as Target in Async Mode

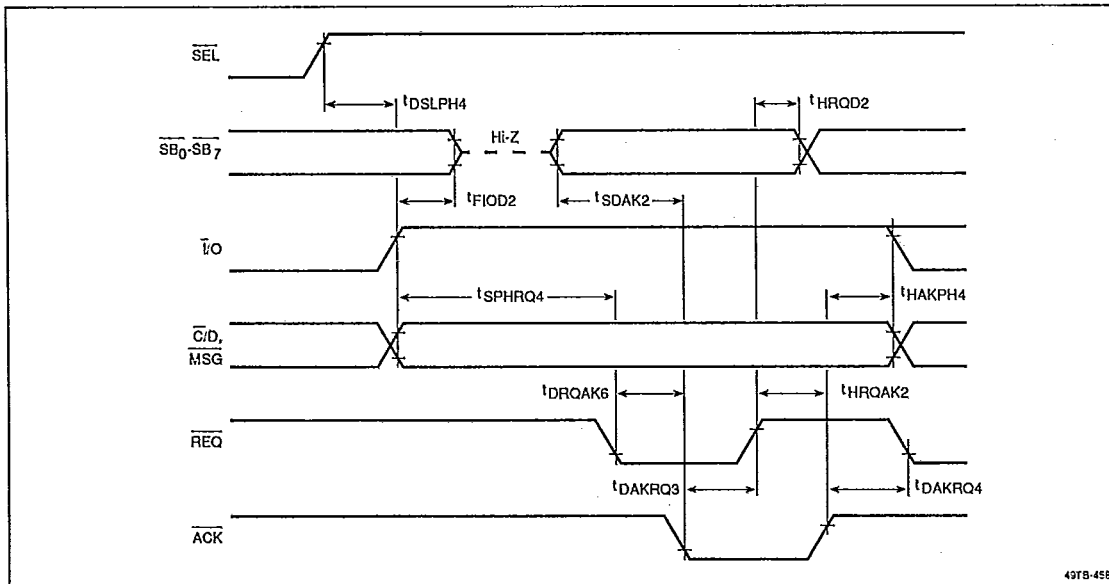


Figure 16. SCSI Bus; Reception as Initiator in Sync Mode

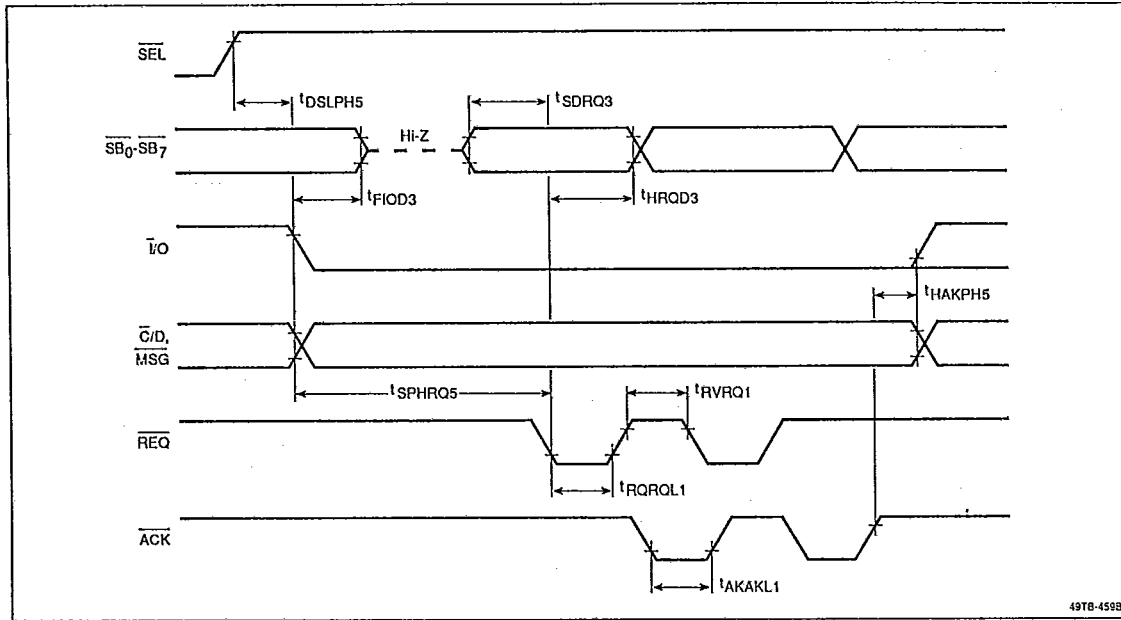
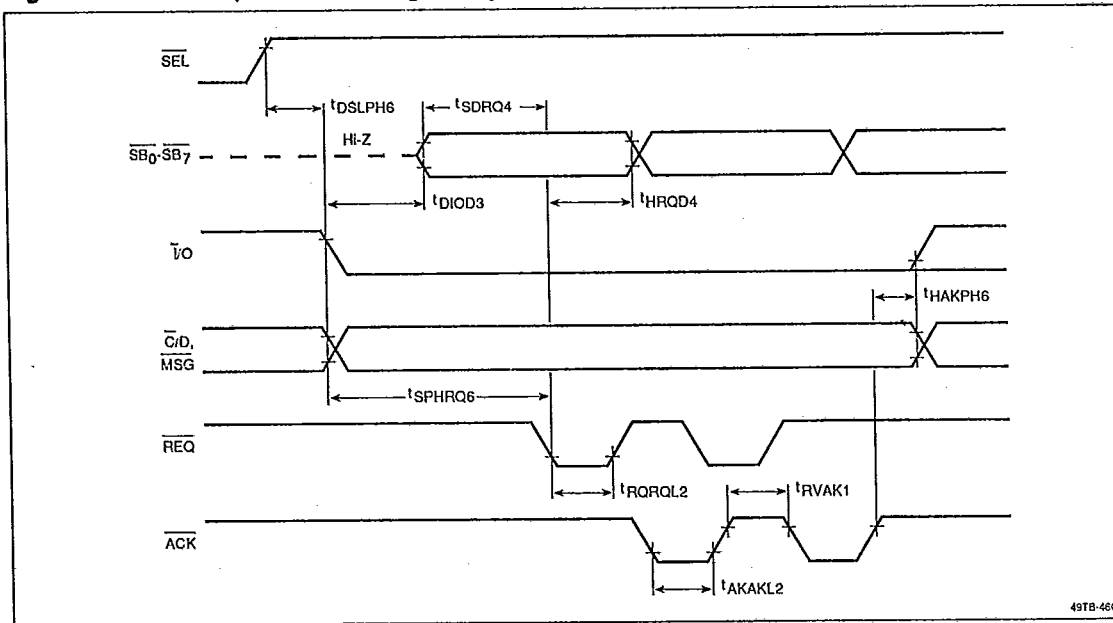


Figure 17. SCSI Bus; Transfer as Target in Sync Mode

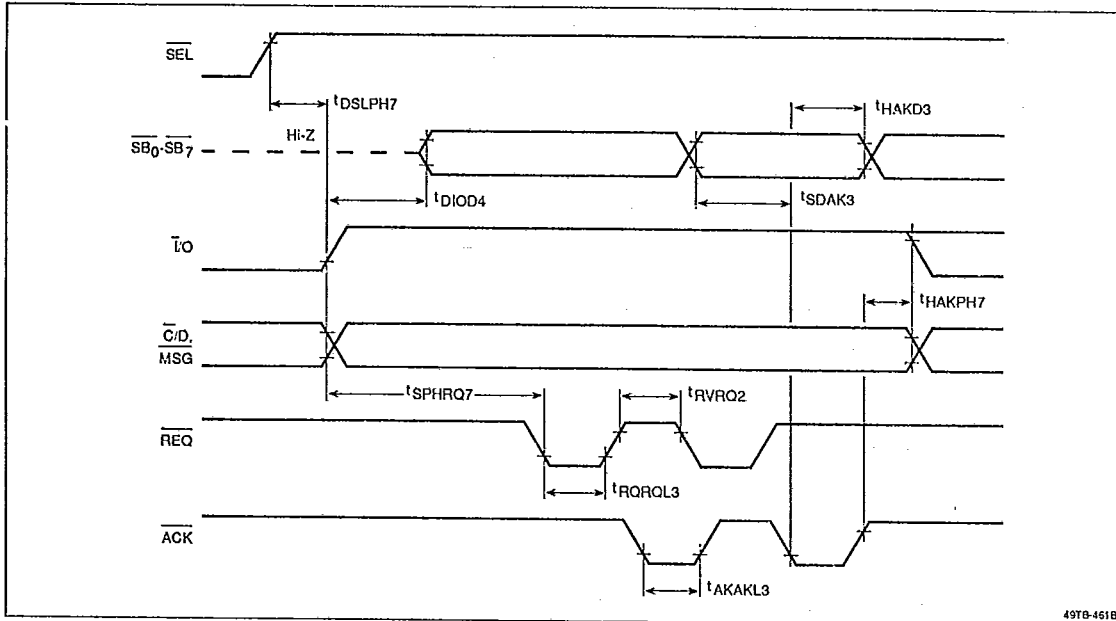




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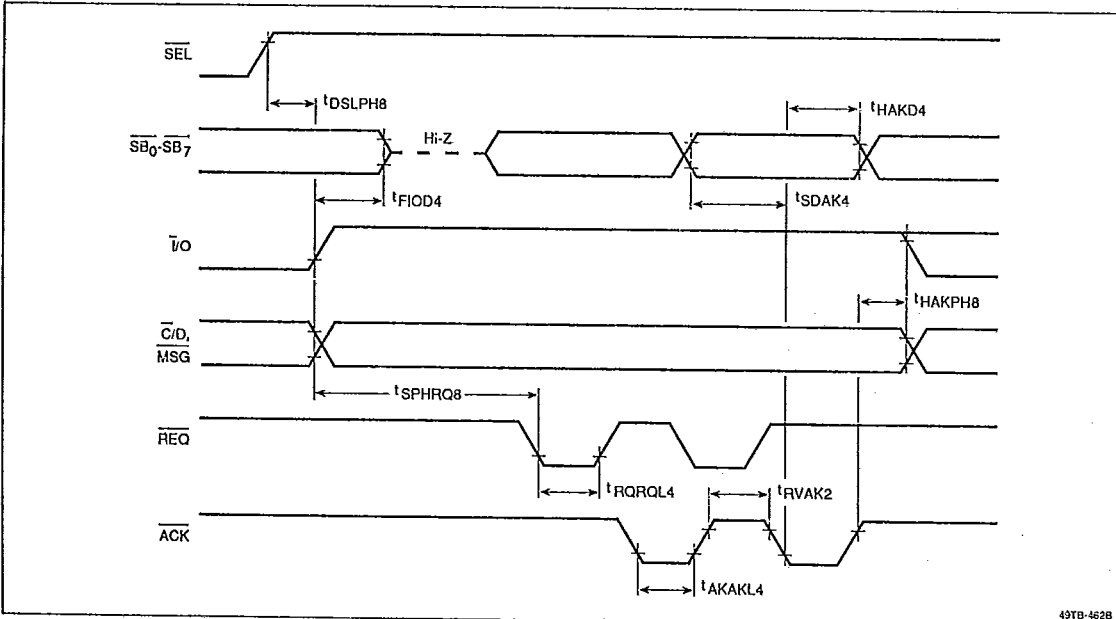
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Figure 18. SCSI Bus; Transfer as Initiator in Sync Mode



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Figure 19. SCSI Bus; Reception as Target in Sync Mode

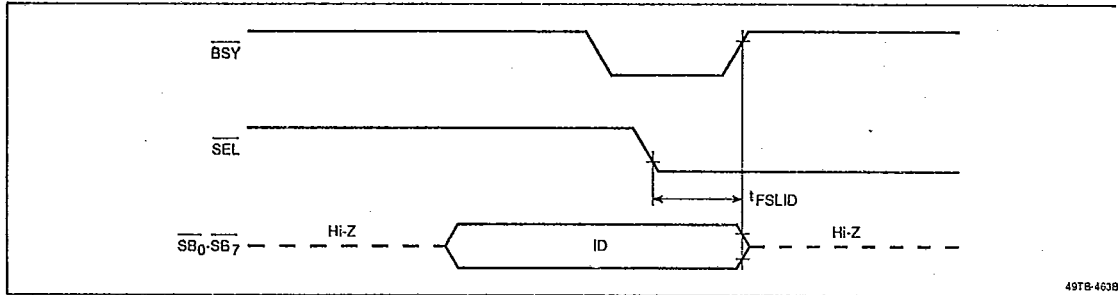


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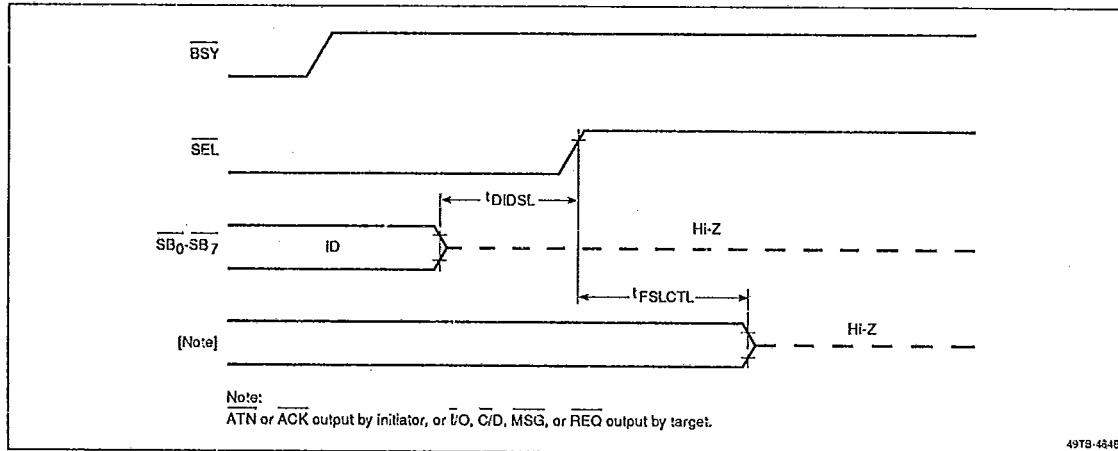
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Figure 20. SCSI Bus; Arbitration, Bus Free



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Figure 21. SCSI Bus; Selection/Reselection, Bus Free



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DIRECT ACCESS REGISTERS

Table 1 lists the 10 internal registers that can be directly accessed from the host CPU. The register address is specified by pins A₂-A₀.

Table 1. Direct Access Registers

Address A ₂ -A ₀	R/W	Symbol	Register Name
000	R/W	DFL	Data FIFO
001	R/W	DFH	
010	R	CST	Controller status
011	R/W	ADR	Address
100	R/W	WIN1	Window
101	R/W	WIN2	
110	R	TP	Terminated phase
	W	DID	Destination ID

Table 1. Direct Access Registers (cont)

Address A ₂ -A ₀	R/W	Symbol	Register Name
111	R	IST	Interrupt status
	W	CMD	Command

Data FIFO Register

The 16-bit data FIFO register (figure 22) is used to write or read data (including command, status, and message data) accessed through the SCSI bus.

In the 8-bit mode, only the lower 8-bit DFL register at address 0H is used. The contents of the upper 8-bit DFH register at address 1H are fixed to 00H.

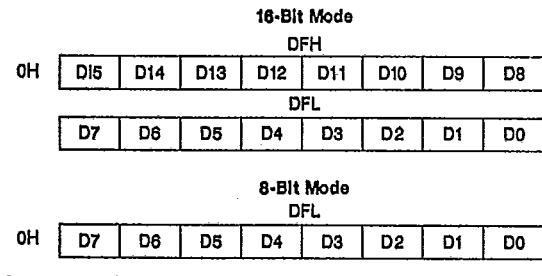
In the 16-bit mode, the register is accessed to/from address 0H with signals A₀ = 0 and \overline{UBE} = 0. When data is sent to the SCSI data bus, the DFL contents are output



first, followed by the DFH contents. When data is sent, the first byte fills DFL and the second byte fills DFH.

The data FIFO register empties when a RESET signal is input, the CHIP RESET command is executed, or the CLEAR FIFO command is executed.

Figure 22. DFL and DFH Registers



Controller Status Register

The 8-bit CST register (figure 23) indicates the operating condition of the μPD72111. This is a read-only register; data written to CST becomes invalid.

The value of the CST register becomes 82H when a RESET signal is input or the CHIP RESET command is executed.

Address Register

When accessing an indirect access register, the address should be set to the 8-bit ADR register and the window register (WIN1, WIN2) accessed. Bit 7 of ADR (figure 24) specifies the mode and bits 5-0 specify the address of the indirect access register.

In the auto-increment mode, each access automatically increments the contents of the lower 6 bits of ADR (+1 for the 8-bit bus mode, +2 for the 16-bit bus mode).

The ADR register is reset to 00H by a RESET signal or by execution of the CHIP RESET command.

Figure 23. CST Register

	7	DFH						0
2H	CBSY	INTRQ	CST1	CST0	ATNC	FFUL	FEMP	DRQ
CBSY		μPD72111 Command Execution Status						
0	Idle (waiting for a command or executing a type A command)							
1	Busy (executing type B or C command)							
INTRQ		CPU Interrupt Request						
0	Not generated							
1	Generated							
CST1, CST0		μPD72111 Operating Condition						
0	0	Disconnected state						
0	1	Initiator state						
1	0	Target state						
ATNC		ATN Pin Status						
0	Inactive (high level)							
1	Active (low level)							
FFUL, FEMP		FIFO State						
0	0	Neither full nor empty						
0	1	Empty						
1	0	Full						
DRQ		DFL/DFH Register						
0	Accessing DFL/DFH is disabled							
1	Writing to or reading from DFL/DFH is requested							

Figure 24. ADR Register

	7	Read/Write						0
3H	AINC	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
AINC		Mode for Accessing an Indirect Access Register						
0	Normal mode (address is not automatically updated)							
1	Auto-Increment mode (address is automatically updated)							
ADR5-ADR0		Indirect Access Register Address						
000000	00H							
:	:							
111111	3FH							



Window Register

The window register (figure 25) comprises two 8-bit registers used as a window for accessing the indirect access registers. With the μPD72111 in the 8-bit mode, WIN1 and WIN2 are accessed to/from addresses 4H and 5H, respectively.



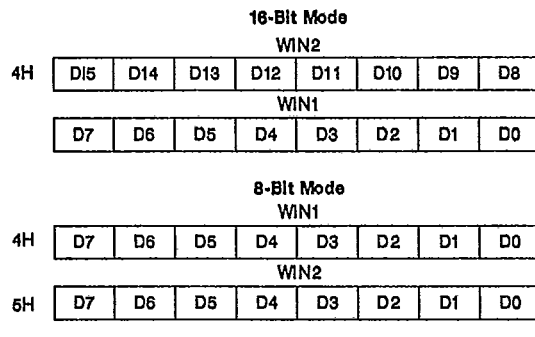
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In the 16-bit mode, WIN1 and WIN2 function as one 16-bit register accessed to/from address 4H. WIN1 and WIN2 hold the least- and most-significant bytes of the word, respectively. According to the settings of signals A₀ and UBE, either or both registers can be accessed.

A ₀	UBE	Address	Register Accessed
0	0	4H	WIN1, WIN2
0	1	4H	WIN1
1	0	5H	WIN2

Figure 25. WIN1 and WIN2 Registers



Terminated Phase Register

The 8-bit TP register (figure 26) indicates the phase executed when a command execution is terminated.

The TP register is reset to 00H by a RESET signal or by execution of the CHIP RESET command.

Destination ID Register

Bits 2-0 of the DID register (figure 27) set the ID of the target to be selected or the Initiator to be reselected. Bit 7 of DID can be set to mask the interrupt request signal (INT). The INTRQ bit of the CST register (figure 23) indicates whether the INT signal was generated or not.

Zeros must be written to bits 6-3 of the DID register.

Figure 26. TP Register

		Read Only							
		7							0
6H		TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
TP7-TP0	Command	Execution Phase							
0000	0001	SCSI RESET SCSI reset							
0001	0001	SELECT Arbitration							
0001	0010	Target selection							
0010	0001	TRANSFER Information transfer							
0011	0001	AUTO Arbitration							
0011	0010	INITIATOR Target selection							
0011	0011	Identify message transmit							
0011	0100	Command transmit							
0011	0101	Data transmit/receive							
0011	0110	Status receive							
0011	0111	Command complete message receive							
0100	0001	RESELECT Arbitration							
0100	0010	Initiator reselection							
0101	0001	RECEIVE Information receive							
0110	0001	SEND Information transmit							
0111	0001	AUTO Selected waiting							
0111	0010	TARGET Identify message receive							
0111	0011	Command receive							
1000	0001	RE-RECEIVE Arbitration							
1000	0010	Initiator reselection							
1000	0011	Identify message transmit							
1000	0100	Data receive							
1001	0001	RE-SEND Arbitration							
1001	0010	Initiator reselection							
1001	0011	Identify message transmit							
1001	0100	Data transmit							

Figure 27. DID Register

		Write Only							
		7					0		
6H		INTM	0	0	0	0	DID2	DID1	DID0
INTM	Interrupt Request Signal Mask Function								
0	Does not mask Interrupt request (INT signal is output when Interrupt is generated)								
1	Masks Interrupt request (INT signal is not output even if interrupt request is generated)								
DID2-DID0	Setting ID of SCSI Device To Be Selected								
000	0								
:	:								
111	7								

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Interrupt Status Register

The read-only IST register (figure 28) indicates the cause of the interrupt request. If the current contents of IST are not read out, they are retained and IST is not updated for new interrupt generation.

Similarly, if the previous contents were not read out, IST would not have been dated for the current interrupt; however, the current interrupt data would be retained elsewhere internally.

Bit 7 of the IST register indicates the group of the interrupt request generation source. The contents of bits 6-0 depend on the value of bit 7.

The IST register is reset to 00H by a $\overline{\text{RESET}}$ signal or by execution of the CHIP RESET command.

Command Register

The 8-bit CMD register (figure 29) is used by the CPU to write commands to the μ PD72111. Commands are described later in table 3.

INDIRECT ACCESS REGISTERS

The 27 registers listed in table 2 can be directly accessed by the CPU through a window in a direct access register. The register address is specified by the lower 6 bits of the ADR register (figure 24).

Table 2. Indirect Access Registers

Address	R/W	Symbol	Register Name
00H	R	TST	Target status
01H	R	SBST	SCSI bus status
02H	R	SID	Source ID
03H	R/W	MSG	Message
04H thru 0FH	R/W	CDB00 thru CDB11	Command descriptor block
10H	R/W	TMOD	Transfer mode
11H	R	CTCL	Current counter (lower 8 bits)
	W	BTCL	Base counter (lower 8 bits)
12H	R	CTCM	Current counter (middle 8 bits)
	W	BTM	Base counter (middle 8 bits)
13H	R	CTCH	Current counter (upper 8 bits)
	W	BTCH	Base counter (upper 8 bits)
14H thru 1FH			Reserved
20H	R/W	BFTOUT	Bus free timeout
21H	R/W	SRTOUT	Selection/reselection timeout
22H	R/W	RATOUT	REQ/ACK handshake timeout
23H	R/W	CDBL	Command descriptor block length

Table 2. Indirect Access Registers (cont)

Address	R/W	Symbol	Register Name
24H	R/W	MOD	Mode
25H	R/W	PID	Physical ID
26H thru 3FH			Reserved

R = Read only; W = Write only; R/W = Read/Write

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Figure 28. IST Register

		Write Only								
7H		SRI	IST6	IST5	IST4	IST3	IST2	IST1	IST0	0
SRI		Interrupt Request Type								
0		Interrupt request caused by command termination (normal termination or abort)								
1		Interrupt request caused by service request issued to CPU								
SRI	IST6-IST0	Interrupt Request Generation Source								
0	000	AT	000	Command normal termination						
0	000	AT	001	Command break						
0	001	AT	000	Invalid command						
0	010	AT	000	FIFO overrun/underrun						
0	010	AT	001	Synchronous offset error						
0	010	AT	010	SCSI bus parity error						
0	010	AT	011	CPU bus parity error						
0	010	AT	100	Bus free time-out error						
0	010	AT	101	Selection/reselection timeout error						
0	010	AT	110	REQ/ACK timeout error						
0	011	0	000	Data-out phase error						
0	011	0	001	Data-in phase error						
0	011	0	010	Command phase error						
0	011	0	011	Status phase error						
0	011	0	110	Message-out phase error						
0	011	0	111	Message-in phase error						
0	100	AT	000	Unsupported SCSI command group						
1	000	0	000	Reset						
	000	0	001	SCSI reset condition occurred						
1	001	0	000	Disconnected						
1	001	0	001	Reselected						
1	001	AT	010	Selected						
1	010	0	000	Data-out phase started						
1	010	0	001	Data-in phase started						
1	010	0	010	Command phase started						
1	010	0	011	Status phase started						
1	010	0	110	Message-out phase started						
1	010	0	111	Message-in phase started						
1	100	AT	000	Message received						

AT bit is valid in target mode only. It shows whether attention condition has occurred (AT = 1) or not (AT = 0).

Figure 29. CMD Register

		Write Only								
7H		CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	0

Target Status Register

The TST register (figure 30) stores the status byte of the target received in the status phase during execution of the AUTO INITIATOR command.

Figure 30. TST Register

		Read Only								
00H		TST								

SCSI Bus Status Register

The SBST register (figure 31) indicates the status of each signal on the SCSI control bus.

Figure 31. SBST Register

		Read Only								
01H		BSY	SEL	REQ	ACK	ATN	MSG	C/D	I/O	0

Status of Each Pin

0	Inactive (high level)
1	Active (low level)

Source ID Register

The read-only SID register (figure 32) stores the ID of the last SCSI device that selected the μPD72111. Bits 6-3 are always read out as zeros.

Figure 32. SID Register

		Read Only								
02H		S/R	0	0	0	0	SID2	SID1	SID0	0

S/R μPD72111 Select/Reselect Operation

0	Has neither been selected nor reselected (contents of SID2-SID0 are invalid)
1	Has been selected or reselected (contents of SID2-SID0 are valid)

SID2- SID0 ID No. of Last SCSI Device That Selected μPD72111

000	0
:	:
111	7



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Message Register

The MSG register (figure 33) sets transmit messages or stores receive messages when the μPD72111 is transmitting or receiving.

Figure 33. MSG Register

7	Read/Write	0
03H	MSG	

Command Descriptor Block

The 12 CDB registers (figure 34) set/store the command descriptor blocks of SCSI commands.

Figure 34. CDB Registers

7	Read/Write	0
04H	CDB00	
05H	CDB01	
06H	CDB02	
07H	CDB03	
08H	CDB03	
09H	CDB04	
0AH	CDB06	
0BH	CDB07	
0CH	CDB08	
0DH	CDB09	
0EH	CDB10	
0FH	CDB11	

Transfer Mode Register

The TMOD register (figure 35) sets the mode for data transfer. Zero must be written to bit 3.

Current Counter

The 24-bit CTC register (figure 36) counts the number of data bytes transferred in the information transfer phase. This is a read-only register; data cannot be written to it.

During execution of an information transfer command, the CTC counter is loaded with the values in the BTC base counter. The values loaded from BTC to CTC are controlled by count select bits C1 and C0 of the command code (table 5).

Figure 35. TMOD Register

7	Read/Write							0
10H	SYNC	TPD2	TPD1	TPD0	0	TOF2	TOF1	TOF0
SYNC Data Transfer Mode								
0 Asynchronous mode								
1 Synchronous mode								
TPD2-TPD0 Cycles for Sync Mode Transfer Rate (at 16 MHz)								
0 0 0 16 clock cycles 1.00 Mbytes/s								
0 0 1								
0 1 0 4 clock cycles 4.00 Mbytes/s								
0 1 1 6 clock cycles 2.67 Mbytes/s								
1 0 0 8 clock cycles 2.00 Mbytes/s								
1 0 1 10 clock cycles 1.60 Mbytes/s								
1 1 0 12 clock cycles 1.33 Mbytes/s								
1 1 1 14 clock cycles 1.14 Mbytes/s								
TOF2-TOF0 REQ, ACK Pulse Offset Value for Sync Mode								
0 0 0 1								
:								
1 1 1 8								

Figure 36. CTC Register

7	Read Only	0
11H	CTCL	
12H	CTCM	
13H	CTCH	



Base Counter

The 24-bit BTC register (figure 37) sets the number of data transfer bytes to be loaded into the CTC current counter. This is a write-only register; the contents cannot be read out. The count values written to BTC are controlled by count select bits C1 and C0 of the command code. (table 5).

Bus Free Timeout Register

The BFTOUT register (figure 38) sets the bus free timeout. If 00H is written to this register, the timeout detection function will not operate.



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Figure 37. BTC Register

7	Write Only	0
11H	BTCL	
12H	BTCM	
13H	BTCH	

BTCH	BTCM	BTCL	Number of Data Transfer Bytes
00H	00H	00H	0
:	:	:	:
00H	00H	FFH	255
00H	01H	00H	256
:	:	:	:
00H	FFH	FFH	65,535
01H	00H	00H	65,536
:	:	:	:
FFH	FFH	FFH	16,777,215

Figure 38. BFTOUT Register

7	Read/Write	0
20H	BFTOUT	

BFTOUT	Bus Free Timeout (at 16 MHz)
00H	No timeout detection is performed
01H	8.192 ms
:	:
FFH	2088.928 ms

Selection/Reselection Timeout Register

The SRTOUT register (figure 39) sets the timeout for the selection or reselection operation. If 00H is written to this register, the timeout detection function will not operate.

Figure 39. SRTOUT Register

7	Read/Write	0
21H	SRTOUT	

SRTOUT	Selection/Reselection Timeout (at 16 MHz)
00H	No timeout detection is performed
01H	8.192 ns
:	:
FFH	2088.928 ms

REQ/ACK Handshake Timeout Register

The RATOUT register (figure 40) sets the timeout for handshake operation of REQ and ACK signals during information transfer. If 00H is written to this register, the timeout detection function will not operate.

Figure 40. RATOUT Register

7	Read/Write	0
22H	RATOUT	

RATOUT	REQ/ACK Timeout (at 16 MHz)
00H	No timeout detection is performed
01H	128 μs
:	:
FFH	32,640 μs

Command Descriptor Block Length Register

The CDBL register (figure 41) sets parameters for the group 6 and group 7 SCSI commands (vendor unique) of the SCSI specifications by using the AUTOINITIATOR command and the AUTO TARGET command.

Figure 41. CDBL Register

7	Read/Write	0
23H	CL73 CL72 CL71 CL70 CL63 CL62 CL61 CL60	

CL73-CL70	Group 7 SCSI Command; CDB Length
0001	1 byte
:	:
1100	12 bytes
1101	Does not support group 7 SCSI commands (generates unsupported group command error)
:	:
1111	
0000	
CL63-CL60	Group 6 SCSI Command; CDB Length
0001	1 byte
:	:
1100	12 bytes
1101	Does not support group 6 SCSI commands (generates unsupported group command error)
:	:
1111	
0000	



Mode Register

The MOD register (figure 42) sets the μPD72111 operation mode.

Figure 42. MOD Register

		Read/Write							
		7							0
24H		DMA	HPS	DHP	DSP	NAM	SIM	RAEN	SAEN
DMA	Data Transfer Mode (In data-In/data-out phase)								
0	Program I/O mode								
1	DMA mode								
HPS	DHP	CPU Bus Parity							
0	0	Odd parity							
1	0	Even parity							
x	1	Disable parity							
DSP	SCSI Bus Parity								
0	Enable (even parity only)								
1	Disable parity								
NAM	SIM	Bus Arbitration Execution							
0	x	Arbitration mode							
1	0	Non-arbitration mode (non-single-initiator mode)							
1	1	Non-arbitration mode (single-initiator mode)							
RAEN	Response (when reselected as Initiator by target)								
0	Does not respond								
1	Responds								
SAEN	Response (when reselected as target by Initiator)								
0	Does not respond								
1	Responds								

Physical ID Register

The PID register (figure 43) sets the μPD72111's own physical ID on the SCSI system. Zeros must be written to bits 6-3.

Figure 43. PID Register

		Read/Write							
		7						0	
25H		FEN	0	0	0	0	PID2	PID1	PID0
FEN	Controller Operation								
0	Does not operate as Initiator								
1	Operates as Initiator								
PID2- PID0	μPD72111's Own ID Number								
000	0								
:	:								
111	7								

COMMANDS

Descriptions

The CPU controls the μPD72111 with the 16 commands described in table 3. Commands are listed in groups according to mode—initiator/target, initiator, and target.

Command Code

Table 4 gives the command code, status, and type for each command.

Command Bits. Symbols for command bits in table 4 are explained below.

Symbol	Function
C1, C0	Count select bits
AT	ATN signal status selection bit. (1 means the initiator is requesting the message-out phase.)
MG, CD	Transfer information specification bits

The function of count select bits C1 and C0 is to specify the value loaded to the current transfer counter. This can reduce the overhead of modifying the transfer counter. See table 5.

Status. Table 4 specifies the status in effect when the command is issued. Symbols are explained below.

Symbol	Status
D	Disconnect
I	Initiator
T	Target

Type. Table 4 classifies commands as type A, B, or C according to the execution status defined under "μPD72111 Processing" below.





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Table 3. Command Functions

Mode	Command Name	Mnemonic	Function
Initiator or Target	CHIP RESET	CRST	Resets μPD72111 using software.
	BREAK	BRK	Discontinues command execution.
	DISCONNECT	DIS	Releases SCSI bus.
	CLEAR FIFO	CLRF	Clears FIFO
	SCSI RESET	SRST	Resets SCSI bus.
Initiator	SET ATN	SETAT	Sets \overline{ATN} signal.
	RESET ACK	RSTAK	Resets \overline{ACK} signal.
	SELECT	SEL	Selects a target.
	TRANSFER	TFR	Sends/receives data (in Initiator mode).
	AUTO INITIATOR	AIN	Automatically executes Initiator standard operation.
Target	RESELECT	RSEL	Reselects Initiator
	RECEIVE	REC	Receives data (in target mode).
	SEND	SND	Sends data (in target mode).
	AUTO TARGET	ATG	Automatically executes target standard operation.
	RE-RECEIVE	RREC	Reselects → Continuous execution of data-recvle operation (in target mode)
	RE-SEND	RSND	Reselects → Continuous execution of data-send operation (in target mode)

Table 4. Command Codes

Command Name	Command Code	Status	Type
CHIP RESET	0 0 0 0 0 0 0 0	D, I, T	A
BREAK	0 0 0 0 0 0 0 1	D, I, T	A
DISCONNECT	0 0 0 0 0 0 1 0	D, I, T	A
CLEAR FIFO	0 0 0 0 0 1 0 1	D, I, T	A
SCSI RESET	0 0 0 0 1 0 0 0	D, I, T	B
SET ATN	0 0 0 0 0 0 1 1	I	A
RESET ACK	0 0 0 0 0 1 0 0	I	A
SELECT	0 0 0 1 AT 0 0 0	D	B
TRANSFER	C1 C0 0 1 0 0 1 0	I	B
AUTO INITIATOR	C1 C0 0 1 AT 1 0 0	D	C
RESELECT	0 0 1 0 0 0 0 0	D	B
RECEIVE	C1 C0 1 0 1 MG CD 0	T	B
SEND	C1 C0 1 0 1 MG CD 1	T	B
AUTO TARGET	0 0 1 1 0 0 0 0	D	C
RE-RECEIVE	C1 C0 1 1 1 0 0 0	D	C
RE-SEND	C1 C0 1 1 1 0 0 1	D	C

Table 5. Loading the Current Transfer Counter

C1	C0	Load Operation	Counting Range
1	0	CTCH/M CTCL ← 0000H ← BTCL	0 to 256 bytes in 1-byte units
1	1	CTCH/M/L ← 000001H	Single-byte only

μPD72111 PROCESSING

Processing by the μPD72111 is in either of two categories:

- Command processing initiated by a command from the CPU
- Response processing executed by the SCSI bus status transition

Command Processing

Command processing operations differ depending on the command executed.

Type A Command. Except for CHIP RESET, the command is immediately executed. Then, a new command is awaited.

CHIP RESET Command. The μPD72111 is immediately reset, after which an interrupt request is generated.

Type B and C Commands. The issued command is synchronized with the system clock and executed. After the command is executed, an interrupt is generated.



Response Processing

When selected or reselected by another device, response processing for the device is executed. If the bus status changes during information transfer, the bus phase after the transition is detected and reported. The μPD72111 generates an interrupt upon completing the response processing.

HOST CPU PROCESSING

Processing by the host CPU for the μPD72111 is in either of two categories.

- Command issuance processing by request from the CPU side. See figure 44.
- Interrupt processing generated when the operation specified by the command is completed, or the SCSI bus status changes. See figure 45.

Figure 44. Command Issuance Processing Flow

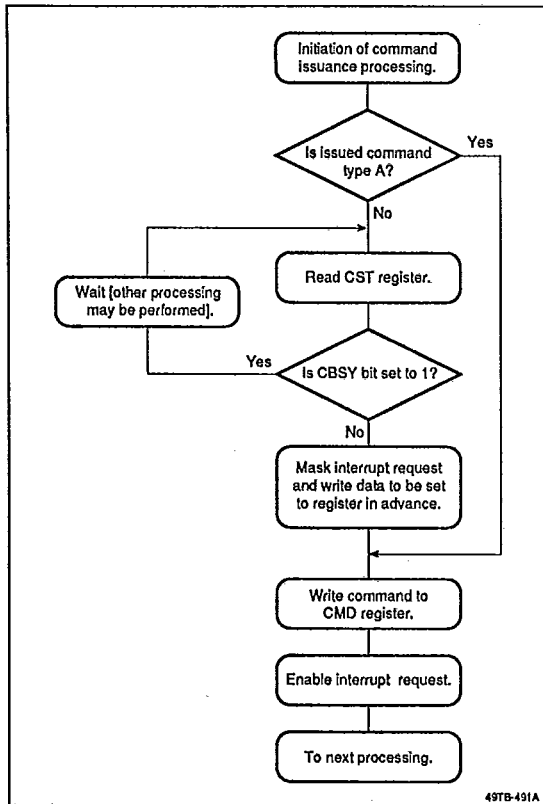


Figure 45. Interrupt Processing Flow

