JANSR2N7395

HARRIS SEMICONDUCTOR

Formerly Available As FSL130R4, Radiation Hardened, SEGR Resistant, N-Channel Power MOSFET

August 1997

Features

- **8A, 100V, $r_{DS(ON)} = 0.230\Omega$**
- **Total Dose**
  - **Meets Pre-RAD Specifications to 100K RAD (Si)**
- **Single Event**
  - **Safe Operating Area Curve for Single Event Effects**
  - **SEE Immunity for LET of 36MeV/mg/cm^2 with V_{DS} up to 80% of Rated Breakdown and V_{GS} of 10V Off-Bias**
- **Dose Rate**
  - **Typically Survives 3E9 RAD (Si)/s at 80% BV_{DSS}**
  - **Typically Survives 2E12 if Current Limited to I_{DM}**
- **Photo Current**
  - **1.5nA Per-RAD(Si)/s Typically**
- **Neutron**
  - **Maintain Pre-RAD Specifications for 3E13 Neutrons/cm^2**
  - **Usable to 3E14 Neutrons/cm^2**

Ordering Information

PART NUMBER	PACKAGE	BRAND
JANSR2N7395	TO-205AF	JANSR2N7395

Die Family TA17636.

MIL-PRF-19500/631.

Description

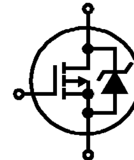
The Discrete Products Operation of Harris Semiconductor has developed a series of Radiation Hardened MOSFETs specifically designed for commercial and military space applications. Enhanced Power MOSFET immunity to Single Event Effects (SEE), Single Event Gate Rupture (SEGR) in particular, is combined with 100K RADS of total dose hardness to provide devices which are ideally suited to harsh space environments. The dose rate and neutron tolerance necessary for military applications have not been sacrificed.

The Harris portfolio of SEGR resistant radiation hardened MOSFETs includes N-Channel and P-Channel devices in a variety of voltage, current and on-resistance ratings. Numerous packaging options are also available.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

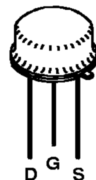
Reliability screening is available as either commercial, TXV equivalent of MIL-S-19500, or Space equivalent of MIL-S-19500. Contact Harris Semiconductor for any desired deviations from the data sheet.

Symbol



Package

TO-205AF



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		JANSR2N7395	UNITS
Drain-Source Voltage	V_{DS}	100	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	V_{DGR}	100	V
Continuous Drain Current			
$T_C = 25^oC$	I_D	8	A
$T_C = 100^oC$	I_D	5	A
Pulsed Drain Current	I_{DM}	24	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
$T_C = 25^oC$	P_T	25	W
$T_C = 100^oC$	P_T	10	W
Derated Above 25^oC		0.20	$W/^oC$
Single Pulsed Avalanche Current, L = 100µH, (See Test Figure)	I_{AS}	24	A
Continuous Source Current (Body Diode)	I_S	8	A
Pulsed Source Current (Body Diode)	I_{SM}	24	A
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Lead Temperature (During Soldering) (Distance >0.063in (1.6mm) from Case, 10s Max)	T_L	300	^oC
Weight (Typical)		1.0	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1mA$, $V_{GS} = 0V$		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1mA$	$T_C = -55^oC$	-	-	5.0	V
			$T_C = 25^oC$	1.5	-	4.0	V
			$T_C = 125^oC$	0.5	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V$, $V_{GS} = 0V$	$T_C = 25^oC$	-	-	25	µA
			$T_C = 125^oC$	-	-	250	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	$T_C = 25^oC$	-	-	100	nA
			$T_C = 125^oC$	-	-	200	nA
Drain-Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12V$, $I_D = 8A$		-	-	1.93	V
On Resistance	$r_{DS(ON)12}$	$I_D = 5A$, $V_{GS} = 12V$	$T_C = 25^oC$	-	0.170	0.230	Ω
			$T_C = 125^oC$	-	-	0.361	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 50V$, $I_D = 8A$, $R_L = 6.25\Omega$, $V_{GS} = 12V$, $R_{GS} = 7.5\Omega$		-	-	70	ns
Rise Time	t_r			-	-	220	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	100	ns
Fall Time	t_f			-	-	90	ns
Total Gate Charge (Not on Slash Sheet)	$Q_{g(TOT)}$	$V_{GS} = 0V$ to 20V	$V_{DD} = 50V$, $I_D = 8A$,	-	-	64	nC
Gate Charge at 12V	$Q_{g(12)}$	$V_{GS} = 0V$ to 12V		-	33	43	nC
Threshold Gate Charg (Not on Slash Sheet)	$Q_{g(TH)}$	$V_{GS} = 0V$ to 2V		-	-	2.4	nC
Gate Charge Source	Q_{gs}			-	6.5	8.7	nC
Gate Charge Drain	Q_{gd}			-	17	22	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	175	$^oC/W$

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Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 8A	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	I_{SD} = 8A, dI_{SD}/dt = 100A/µs	-	-	330	ns

Electrical Specifications up to 100K RAD $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain-Source Breakdown Volts	(Note 3)	BV_{DSS}	V_{GS} = 0, I_D = 1mA	100	-	V
Gate-Source Threshold Volts	(Note 3)	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA	1.5	4.0	V
Gate-Body Leakage	(Notes 2, 3)	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	100	nA
Zero-Gate Leakage	(Note 3)	I_{DSS}	V_{GS} = 0, V_{DS} = 80V	-	25	µA
Drain-Source On-State Volts	(Notes 1, 3)	$V_{DS(ON)}$	V_{GS} = 12V, I_D = 8A	-	1.93	V
Drain-Source On Resistance	(Notes 1, 3)	$r_{DS(ON)12}$	V_{GS} = 12V, I_D = 5A	-	0.230	Ω

NOTES:

1. Pulse test, 300µs max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both V_{GS} = 12V, V_{DS} = 0V and V_{GS} = 0V, V_{DS} = 80% BV_{DSS}.

Single Event Effects (SEB, SEGR) Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)			APPLIED V_{GS} BIAS (V)	(NOTE 6) MAXIMUM V_{DS} BIAS (V)
		ION SPECIES	TYPICAL LET (MeV/mg/cm)	TYPICAL RANGE (µ)		
Single Event Effects Safe Operating Area	SEESOA	Ni	26	43	-20	100
		Br	37	36	-10	100
		Br	37	36	-15	80
		Br	37	36	-20	50

NOTES:

4. Testing conducted at Brookhaven National Labs; sponsored by Naval Surface Warfare Center (NSWC), Crane, IN.
5. Fluence = 1E5 ions/cm^2 (typical), T = 25°C.
6. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

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Typical Performance Curves Unless Otherwise Specified

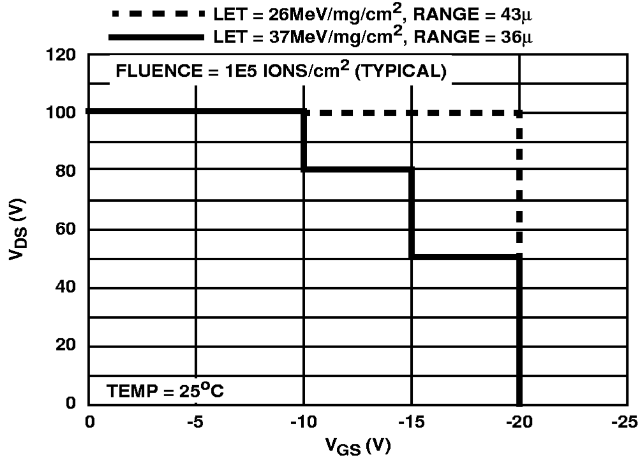

FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

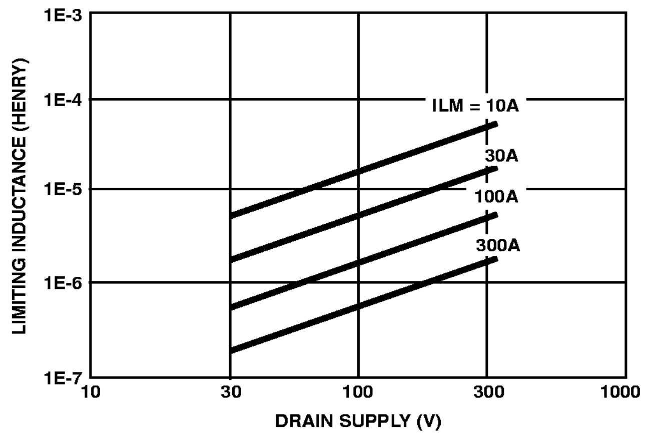

FIGURE 2. DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO I_{AS}

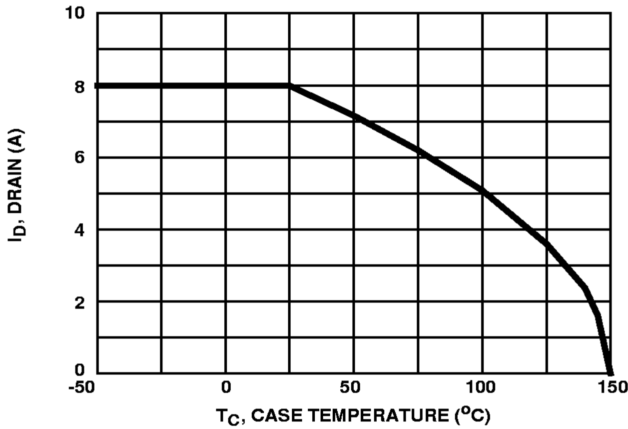

FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

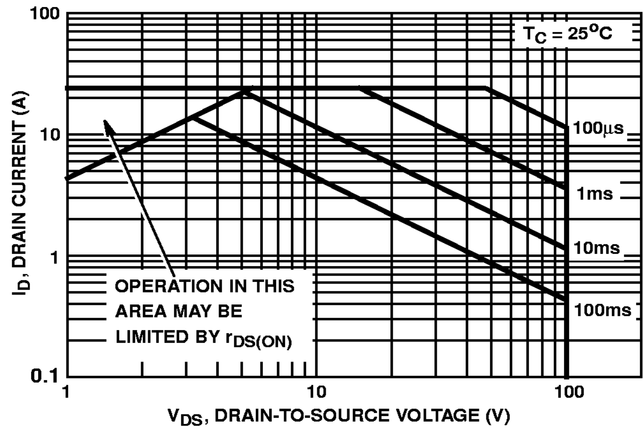

FIGURE 4. FORWARD BIAS SAFE OPERATING CURVE

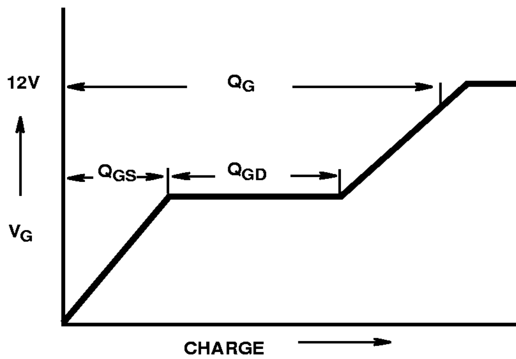

FIGURE 5. BASIC GATE CHARGE WAVEFORM

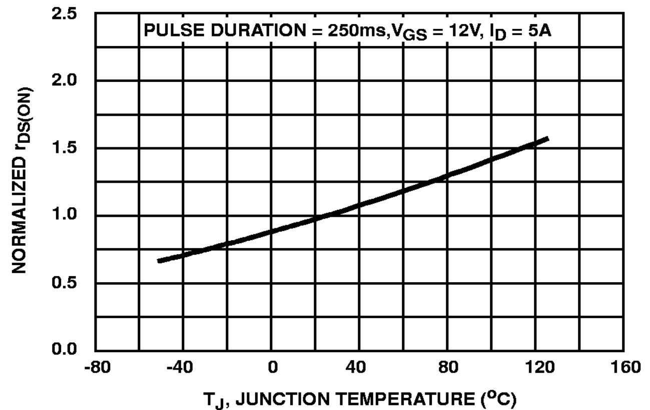

FIGURE 6. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

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Typical Performance Curves Unless Otherwise Specified (Continued)

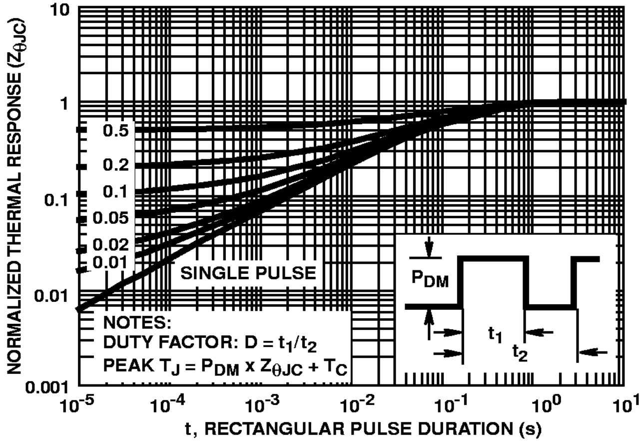

FIGURE 7. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

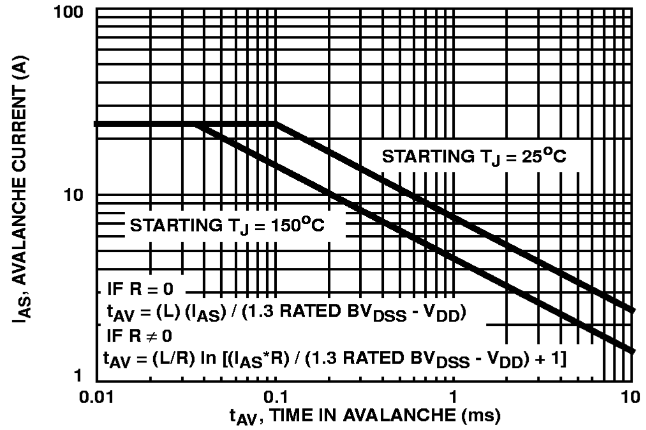

FIGURE 8. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

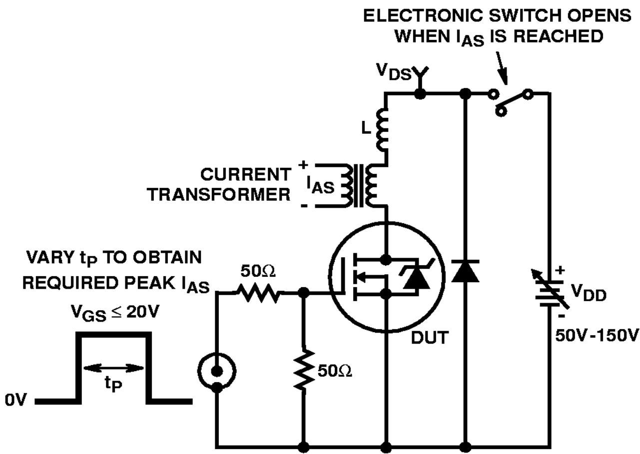

FIGURE 9. UNCLAMPED ENERGY TEST CIRCUIT

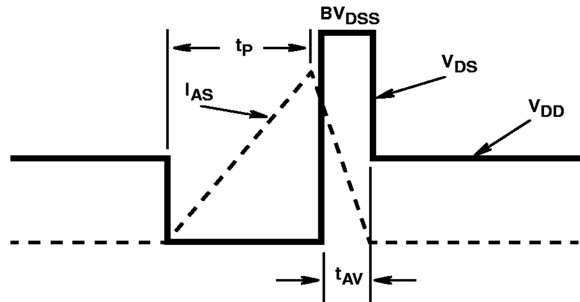

FIGURE 10. UNCLAMPED ENERGY WAVEFORMS

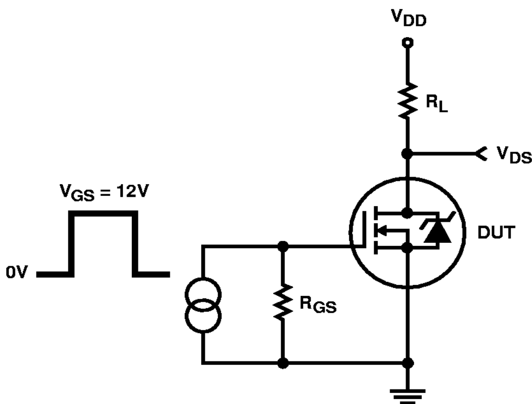

FIGURE 11. RESISTIVE SWITCHING TEST CIRCUIT

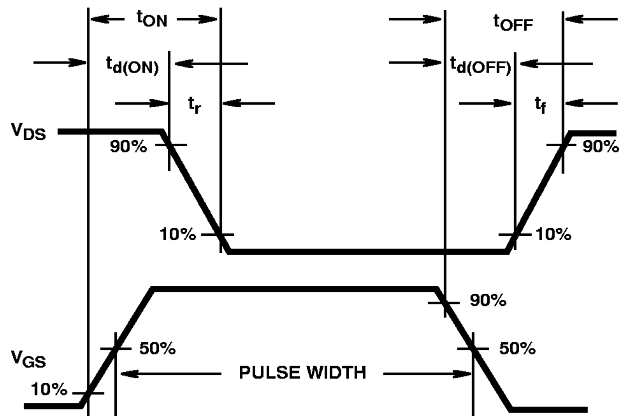

FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Screening Information

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Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANS) $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	±20 (Note 7)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value	±25 (Note 7)	μA
On Resistance	$r_{DS(ON)}$	$T_C = 125^oC$ at Rated I_D	±20% (Note 8)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0mA$	±20% (Note 8)	V

NOTES:

7. Or 100% of Initial Reading (whichever is greater).
8. Of Initial Reading.

Screening Information

TEST	JANS
Gate Stress	$V_{GS} = 30V$, t = 250μs
Pind	Required
PDA	5%
Pre Burn-In Tests (Note 9)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25^oC)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, $T_A = 150^oC$, Time = 48 hours
Interim Electrical Tests (Note 9)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, $T_A = 150^oC$, Time = 240 hours
Final Electrical Tests (Note 9)	MIL-S-19500, Group A, Subgroups 2 and 3

NOTE:

9. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 80V$, t = 10ms	1.5	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)} = 15V$, L = 0.1mH	24	A
Thermal Response	ΔV_{SD}	$t_H = 10ms$; $V_H = 25V$; $I_H = 2A$	125	mV
Thermal Impedance	ΔV_{SD}	$t_H = 500ms$; $V_H = 25V$; $I_H = 1A$	250	mV

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Rad Hard Data Packages - Harris Power Transistors

1. JANS Rad Hard - Standard Data Package
   - A. Certificate of Compliance
   - B. Serialization Records
   - C. Assembly Flow Chart
   - D. SEM Photos and Report
   - E. Preconditioning
     - Attributes Data Sheet
     - Hi-Rel Lot Traveler
     - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
     - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
   - F. Group A - Attributes Data Sheet
   - G. Group B - Attributes Data Sheet
   - H. Group C - Attributes Data Sheet
   - I. Group D - Attributes Data Sheet

2. JANS Rad Hard - Optional Data Package
   - A. Certificate of Compliance
   - B. Serialization Records
   - C. Assembly Flow Chart
   - D. SEM Photos and Report
   - E. Preconditioning
     - Attributes Data Sheet
     - Hi-Rel Lot Traveler
     - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
     - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
     - X-Ray and X-Ray Report
   - F. Group A
     - Attributes Data Sheet
     - Hi-Rel Lot Traveler
     - Subgroups A2, A3, A4, A5 and A7 Data
   - G. Group B
     - Attributes Data Sheet
     - Hi-Rel Lot Traveler
     - Subgroups B1, B3, B4, B5 and B6 Data
   - H. Group C
     - Attributes Data Sheet
     - Hi-Rel Lot Traveler
     - Subgroups C1, C2, C3 and C6 Data
   - I. Group D
     - Attributes Data Sheet
     - Hi-Rel Lot Traveler
     - Pre and Post Radiation Data

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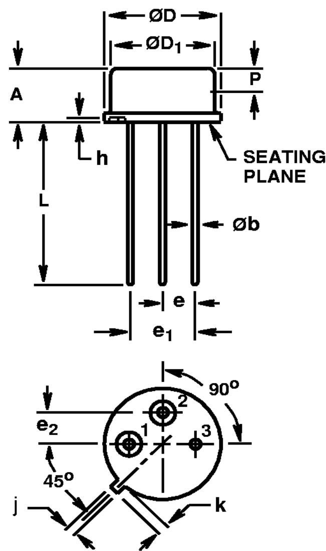
TO-205AF

3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
$ØD_1$	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e_1	0.190	0.210	4.83	5.33	4
e_2	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.075	-	1.91	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Lead no. 3 butt welded to stem base.
7. Controlling dimension: Inch.
8. Revision 3 dated 6-94.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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