Introduction

The EG&G Reticon RA0256B is a two-dimensional self-scanned optical sensor array with perfected characteristics. 65,536 discrete photodiodes are geometrically arranged into 256 x 256 matrix. In contrast to comparable CCD devices, the discrete photodiode sensors require no surface electrode so there is no interference pattern or light loss and the full inherent sensitivity is obtainable.

The scanning method permits pixel rates up to 5 MHz. Each line of pixel information is parallel-loaded into a high-speed bucket-brigade analog shift register and sequentially shifted out. All 256 lines may be sequentially accessed to give a 256-line frame, or alternate odd or even lines may be selected to produce 128 lines per field in an odd and even field pattern. The integration time is nominally one frame period, giving maximum sensitivity.

Features

- 65,536 light-sensitive elements in a high-resolution 256 x 256 matrix
- 40 µm center-to-center element spacing in both X and Y directions
- Frame storage–each diode integrates photocurrent for the entire frame
- Self-scanned in both X and Y directions by high-speed on-chip circuitry to provide either single frame or interlaced odd/even field multiplexed serial video output
- Nonburning sensors
- Solid-state reliability
- Low power dissipation
- 28-pin dual-inline package with scratch-resistant quartz window

General Description

The RA0256B is packaged in a 28-pin dual-inline pin package with a ground and polished window covering the mask-defined active area. Figure 1 is the device's pinout configuration. The device, fabricated on a monolithic silicon chip, contains the matrix diode array with access and reset switches in addition to both the X and Y readout shift registers. Figure 2 is a schematic representation.

A MOS dynamic shift register sequentially selects the diode rows while two bucket brigades connect to each column. Each position of the shift register selects two diode rows through two multiplexing gates, ϕ_A and ϕ_B, one for the odd and the other for the even, providing the user the choice of selecting the odd or even fields.

Together the shift register and the bucket brigade process the signal in the following sequence: The shift register selects two rows, one of which is selected by the ϕ_A or ϕ_B clock. The transfer gates parallel-transfer the selected diode in each column into the bucket brigade.

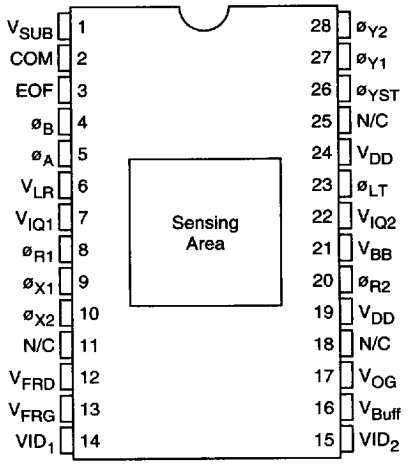

Figure 1. Pinout Configuration

One bucket brigade obtains information from odd and the other from even diode columns and each then shifts that information sequentially to the output. On the output side, there are three extra buckets on the even video transport and two extra buckets on the odd video. Therefore, the even video is delayed an extra 1/2 cycle of the shift frequency, ϕ_{X1}, to obtain the desired time sequence. The alternating odd and even signals are then transferred to corresponding output ports, VID_1 and VID_2.

The integration times are determined by the time interval between accesses for a given diode. This interval can be controlled through the special frame reset clock or through the normal sequential readout. The difference between the two reset processes lies in the integration time for each diode. Frame reset initializes all diodes simultaneously and hence allows each diode to increase the integration time monotonically as the diodes are sequentially read-out–while in the array's normal scanning mode, each diode is accessed periodically with a constant time interval. Hence, in this mode each diode has the same integration time.

Input/Output Definitions and Functional Description

The area array has functional elements which serve to control the timing sequences for diode access, to transport the pixel information to the output, to control integration time, to control the odd and even fields, to provide for interlace, and to buffer each video output. The external circuit provides the timing and the bias to these functional elements as well as clocks to control ϕ_A, ϕ_B, LT, V_{BUFF}, ϕ_{YST}, EOF, FRD, ϕ_{R1}, ϕ_{R2}, V_{IQ1},V_{IQ2}.

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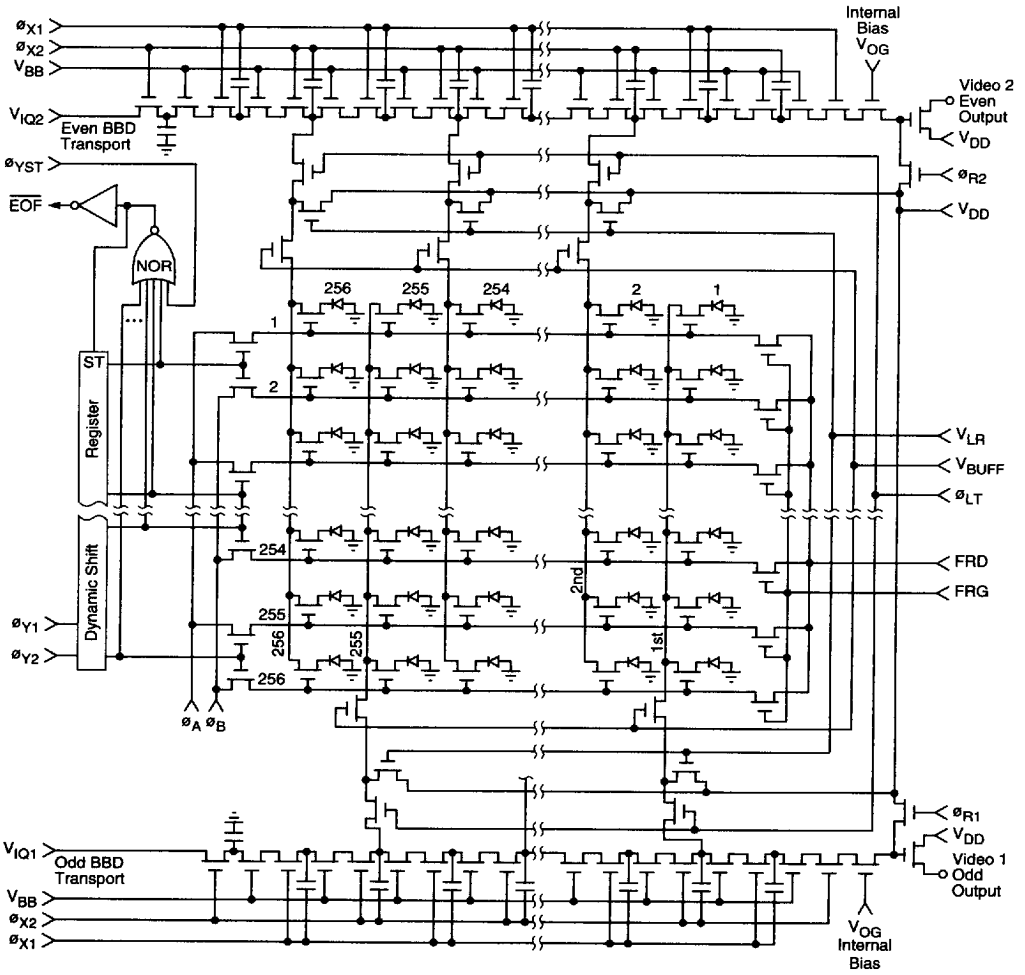


Figure 2. Schematic RA0256B

1. The Odd and Even Bucket Brigade Transports and Their Clocks, ϕ_{X1}-ϕ_{X2}.

Figure 2 shows two bucket brigade analog shift registers located on each side of the device. These are the odd and even transport registers which accept the pixel information in parallel from their respective odd and even video diode columns and shift the pixel information sequentially to the output amplifier. Each bucket brigade must be provided with a two-phase clock as shown in Figure 3. Note: To ensure high transfer efficiency, it is important that the clock waveforms cross at or below the 50% level. The two limits on clock crossing are shown in Figure 3. Normally these clocks swing from a low of 0.4V to a high of 15V.

As evident from Figures 2 and 4, the transfer into both shift registers takes place simultaneously while the ϕ_{X2} is held high. However, the odd bucket brigade produces a pixel first, since it reads out on the second low-going ϕ_{X2} clock after the transfer period. The second pixel is produced by the even shift register. This pixel must transfer through an extra half-stage which is controlled by the ϕ_{X1} clock; thus, even pixels are produced 1/2 cycle out of phase with the odd pixels to provide an easily multiplexed signal by means of a simple adder amplifier.

The multiplexing increases the pixel rate to 2 times the transport clock frequency. See Figure 4 for the clock timing diagram. Figure 5 shows the detailed relationship between ϕ_{X1} and ϕ_{LT}, the line transfer clock. Figure 6 shows the detailed relationship between ϕ_A, and ϕ_B, the vertical multiplexing clocks, and ϕ_Y, the shift register clock.

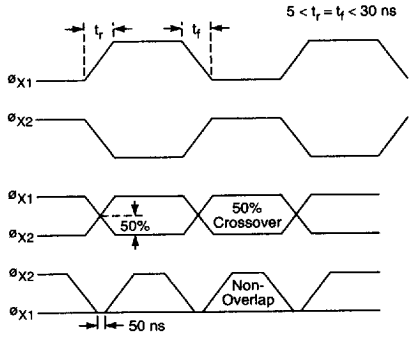


Figure 3. Illustration of $ø_{X1}$ and $ø_{X2}$ Clock Crossover and Time Tolerance

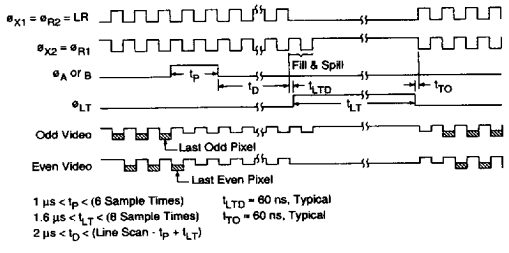
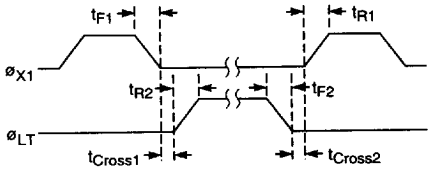


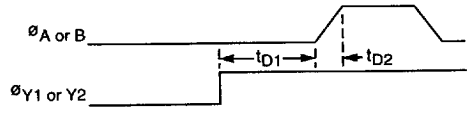
Figure 4. Overall Relationship



0 < t_{F1} < 30 ns
0 < t_{R2} < 30 ns
50% Crossing < $t_{Cross\ 1}$ < 50 ns
$t_{Cross\ 1}$ = $t_{Cross\ 2}$

t_{F1} = t_{F2}
t_{R1} = t_{R2}

Figure 5. Detailed Timing Between $ø_{X1}$ and $ø_{LT}$



t_{D1} > 1.0 µs
t_{D2} > 10 ns

Figure 6. Detailed Timing Between $ø_A$ or $ø_B$, $ø_{Y1}$ or $ø_{Y2}$

2. The Y Dynamic Shift Register

This shift register is shown in Figure 2 as a block with 128 outputs, each connected to two multiplexing gates plus one extra stage at each end. The gates are connected to two rows of photodiodes and select those rows in accordance to the multiplex clocks, $ø_A$ and $ø_B$. If $ø_A$ and $ø_B$ are alternately clocked, the rows will be sequentially accessed, each selected diode connected to its respective column's video line. Then the photodiode information on each column line is transferred to the bucket brigade. Tied to each stage of the shift register are inputs to a NOR gate which provides for the self-loading feature. When there is a "1" in any of the 130 stages the NOR gate keeps the shift register from loading. Once the bit has been clocked out of the last stage, the NOR gate's output goes high and the shift register loads with the falling edge of $ø_{Y1}$. Note that $ø_{YST}$ is connected to the NOR gate. It can be used to inhibit the register from loading by pulling $ø_{YST}$ to V_{DD}. The register requires a two-phase clock which typically swings from a low of 0.4V to V_{DD}.

Note there are two extra stages, one in the first and another in the last position. The purpose of the stages is to minimize the interference caused by the starting and terminating process of the shift register.

3. Line Select Controls, $ø_A$ and $ø_B$

As evident from the schematic diagram, Figure 2, the $ø_A$ input terminal controls the gates that switch all of the odd-numbered rows from the Y shift register, and the $ø_B$ terminal controls the gates that switch the even-numbered rows. These gates, $ø_A$ and $ø_B$, select the rows of diodes as discussed under Section 2. The time relationship is shown in Figure 6.

4. Line Reset, LR

The LR maintains the potential of the column video line between line transfers by bleeding off the excess charges collected under excess illumination. It will require adjustment when the frame reset function is used. This adjustment is discussed under Optimum Relation Between Clocks and Bias.

5. Line Transfer, LT, and Line Buffer, V_{BUFF}

The LT pulse input controls the period during which the row of diode information is transferred into the bucket-brigade transport registers. This pulse must occur while LR is off (low). Normally this LT input is clocked as seen in Figures 4 and 5 with rise and fall as shown. The line buffer control, V_{BUFF}, is normally held at approximately 0.8 V_{DD} and adjusted to optimize blooming control.

6. Y Shift Register Start, $ø_{YST}$

The $ø_{YST}$ input provides access to one of the inputs to the Y shift register's NOR gate (Figure 2). When this input is held high, the output of the NOR gate is held low and inhibits loading of the shift register; however, when the $ø_{YST}$ input is pulled low, the NOR output rises and a bit is loaded into the register with the falling edge of $ø_{Y1}$ clock. The first two rows are then accessed on the next $ø_{Y1}$ rising edge.

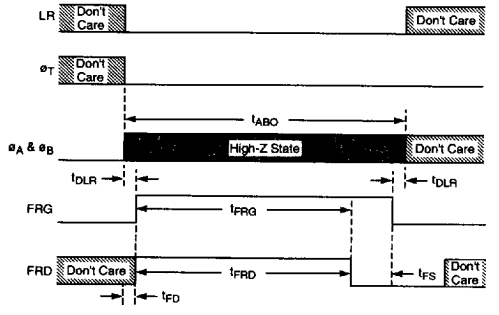
7. End of Frame, EOF

As discussed under ϕ_{YST}, the Y shift register has a NOR gate which provides control for the self-starting feature. The NOR gate output is connected to an external pin through an open-drain inverter. This output is normally tied to V_{DD} through an 8.6 KΩ resistor; therefore, when there is a bit in any row, or if ϕ_{YST} is active, EOF will remain high. It goes immediately low on the rising edge of ϕ_{Y2}, when the bit leaves the last stage of the shift register. This point will sink a maximum of 1.5 ma.

8. Frame Reset, FRG

This input controls access switches to every diode in the matrix and provides simultaneous resetting of all diodes. Since the diodes in each line are automatically reset when the line is accessed, the frame reset control is not normally used, and, as such, is held low. However, when a particular exposure is desired, this control may be used to clear the diodes to start a fresh integration cycle.

The minimum timing requirements for the frame operation are shown in Figure 7. ϕ_A and ϕ_B are held in a high-impedance state during the entire procedure. FRG and FRD are pulsed as shown to connect all photodiodes to their respective video lines. During this connection, the array is taken through at least three line-transfer-and-readout sequences. This resets the video lines and photodiodes through the BBD output registers (the LR function could be used, too, at the expense of more fixed-pattern-noise (FPN). This FPN can be reduced by going through one line readout sequence after the line reset is done). After the reset is finished, FRD is taken low to turn off the multiplex switches. It is important to wait the indicated time, t_{FS}, to make sure the multiplex switches are not left with their gates floating "on."



	Min	Typ	Max	Remark
t_{DLR}	200 ns			
t_{ABO}				To be consistant with t_{FRG}
t_{FRG}	2.5 ms		3.5 ms	
t_{FRD}	2.5 ms			
t_{FS}	4.0 µs			
t_{FD}	0.2 µs			

Note: Clock rise and fall times are not critical. However it is recommended not to exceed 0.5 µs. While frame reset is active, the reset takes place by performing at least 3 line scans using the BBD registers. If no bit is in the Y-register (i.e., between frames), ϕ_A and ϕ_B need not be taken to a high-Z state during frame reset.

Figure 7. Timing Sequence for Frame Reset. This is only performed before or after a line transfer sequence.

9. Reset Clocks for the Gated-Charge Amplifiers, ϕ_{R1} and ϕ_{R2}

These terminals provide reset voltages for the gated-charge amplifiers which are shown in the schematic diagram, Figure 2, at the outputs of both bucket brigades. On the even side, the signal appears at the gate of the output source follower when ϕ_{X1} drops to a low potential. While ϕ_{X1} is high, before the next sample appears, this node is cleared by charging it to a reset voltage. Thus, reset is accomplished when this terminal is clocked synchronously with ϕ_{X1}. The complementary situation applies to the odd output, with signal appearing while ϕ_{X2} is low and reset while ϕ_{X2} is high. The extra half-stage in the even side allows the alternating sequence desired. Normally, the synchronous relationship is obtained by direct connection of ϕ_{X1} to ϕ_{R2}, and direct connection of ϕ_{X2} to ϕ_{R1}. The timing sequence for the output signal is shown in Figure 4 relative to the transfer pulse time.

10. Video Output Terminals, VID_1 and VID_2

The video output is that of a source follower. Normally, the output of each source follower is connected to 1KΩ which is referenced to ground. This configuration provides the proper bias current for the source follower. Figure 8 shows the output voltage across such a load resistor, showing the relationship of the video pixel information relative to the superimposed reset clock amplitude.

Figure 9 shows the output impedance of the source follower as a function of the bias current. This graph can be used to design a desired interface circuit with suitable DC bias translation (e.g., an emitter-coupled transistor with the base biased up near the video output line potential).

11. Input Bias, V_{IQ1} and V_{IQ2}

Bias voltages are connected to the inputs of both bucket-brigade transports: V_{IQ1} to the odd and V_{IQ2} to the even. These inputs control the bias level in the dark. Nominally, these terminals are biased to approximately 10V.

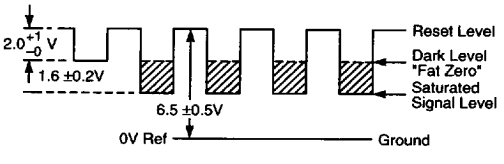


Figure 8. Typical Video Signal Across a 1 KΩ Output Load

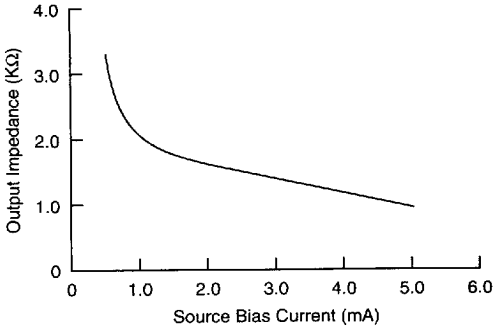


Figure 9. Output Impedance vs. Output Source Current

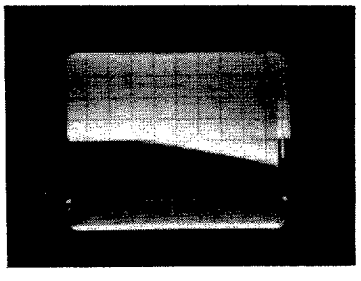


Figure 10a. Scope Output

An example of worst case adjustment. Single frame scan of video output after frame reset. Horizontal 0.5V/div, Vertical 0.002 sec/div.

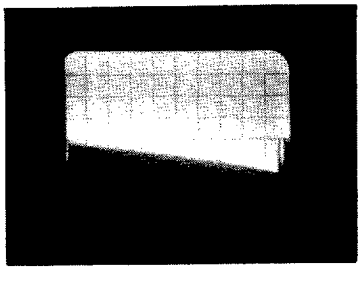


Figure 10b. Scope Output

An example of properly biased output. Single frame scan of video output after frame reset. Horizontal 0.5V/div, Vertical 0.002 sec/div.

Adjustment of V_{IQ1} and V_{IQ2}

Since V_{IQ1} and V_{IQ2} bias the internal operating levels of the bucket brigade, they affect the output signal level. Since there are two bucket brigade outputs, when the two are summed together, an odd and even imbalance may be experienced. One easy method to balance out the odd and even patterns in the summed video is to make one of the V_{IQ} inputs adjustable.

Typically these voltages are set to 10V and they will produce an output bias condition as seen in Figure 8 where the difference between the "fat zero" (or the dark level) and the reset level will maintain a magnitude of approximately 2V. However, when V_{BB} is reduced, the "fat zero" level reduces proportionally. In this case, V_{IQ1} and V_{IQ2} may be reduced to maintain the "fat zero" level. In any case, both V_{IQ} voltages and V_{BB} must be limited according to $7<V_{IQ}<10V$ and $8.5<V_{BB}<V_{DD}-0.5$.

Optimum Relation Between Clocks and Bias

Greatest performance from the device is normally obtained with the ϕ_{X2} and LT clocks interleaved as shown in Figure 4. In this mode of operation the optical to electrical transfer function is given in Figure 11. The dynamic range is in excess of 100:1 with an rms noise-equivalent exposure of less than $.5 \times 10^{-3}$ $\mu J/cm^2$.

The important relationships that must be observed are timing of the clock transitions of ϕ_{X1}, ϕ_{X2}, ϕ_{Y1} and ϕ_{Y2}; the zero level of LT; and the relative timing relationship between LT and ϕ_{X2} (this creates a fill-and-spill phenomenon to improve transfer efficiency). Furthermore, when FR is employed, both the LR and FR voltage level will require adjustment (see Frame Reset Adjustment).

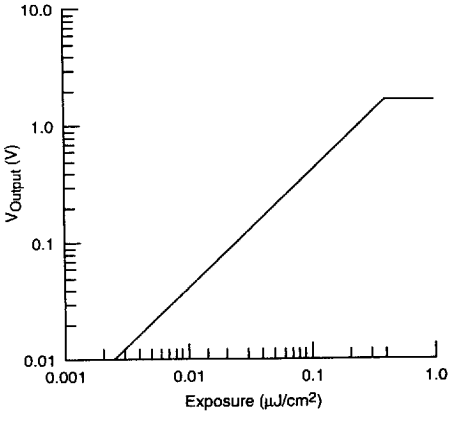


Figure 11. Exposure Chart

$ø_{X1}$ and $ø_{X2}$ are complementary clocks with crossover of the transition edge taking place at or below 50% of the clock amplitude. Rise and fall times preferably are on the order of 20 nanoseconds. If an MH0026 or equivalent is employed, place a 50Ω resistor in series between the driver output and the clock input pins. This edge control is required to obtain the optimum efficiency from the bucket-brigade transport (refer to Figure 3 for $ø_X$ clock shapes).

$ø_{Y1}$ and $ø_{Y2}$ also are complementary and should cross approximately at the 50% level at the transition edges and should have rise and fall times the same as the $ø_X$ clocks. The transition-edge spacing of the interleaving clocks $ø_{LT}$ and $ø_{X2}$ should be kept as shown in the detailed timing diagram of Figure 4.

Frame Reset Adjustment

When FR is employed, FRD and V_{LR} voltages may require adjustment. With the application of the voltage as given in the specification table, the array will provide operation suitable for most applications. However, to obtain the best balance between low noise, high sensitivity, and antiblooming control, the following adjustment procedure is recommended.

With the array operating with the voltages as specified in the specification table, make the following adjustment: Apply a uniform light across the array surface to provide an output which is approximately 1/4 of the total saturated output. Apply the frame reset clock as specified in Figure 7 and the specification table. Operate the array atapproximately 2 MHz sampling rate. With the Frame Reset pulse synchronized to the scope, the frame scan as shown in Figure 10A will be seen. Lower LR amplitude to approximately 12V then lower FRD voltage towards 10V until a linear output as seen in Figure 10B is achieved.

Transfer Function and Spectral Response

Figure 11 is a transfer function graph which shows a linear optical-to-electrical relationship with dynamic range exceeding 100:1. This linear relationship depends on the proper electrode potentials, especially those for V_{BUFF} and the line reset level, LR. Improper potentials can cause substantial nonlinearity.

The array spectral response is shown in Figure 12.

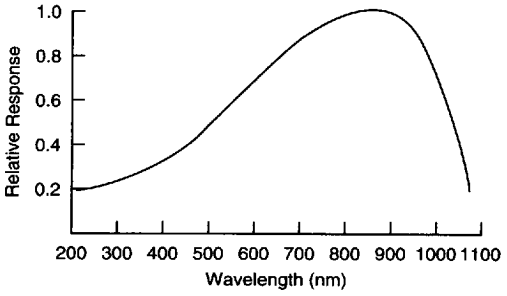


Figure 12. Photodiode Response

Table 1. Array Mechanical Characteristics

		Units
Number of diodes	65,536	
Diode X, Y center-to-center spacing	40/1.57	µm/mils
Diode sensing area	912 µm²	
Package size (28-pin)	0.8 x 1.4	inch

Table 2. Terminal Input Capacitance

Typical Capacitance with 10V Bias		
Pin	**Sym**	**Capacitance (pF)**
3	End of frame	5
4	$ø_B$	21
5	$ø_A$	21
6	V_{LR}	48
7	V_{IQ1}	5
8	V_{R1}	6
9	$ø_{X1}$	150
10	$ø_{X2}$	150
12	$ø_{FRD}$	50
13	$ø_{FRG}$	29
14	VID_1	6
15	VID_2	6
16	V_{BUFF}	64
17	V_{OG}	6
20	V_{R2}	4
21	V_{BB}	101
22	V_{IQ2}	5
23	$ø_{LT}$	43
26	$ø_{YST}$	4
27	$ø_{Y1}$	28
28	$ø_{Y2}$	28

Table 3. Array Performance Characteristics (T_A = 23°C)

Sym	Parameter	Typ	Max	Units
DR	Dynamic range (P-P) [1]	100:1		—
E_{NE}	Peak-to-peak noise equivalent exposure [2]	2.5 x 10^{-3}		μJ/cm²
E_{Sat}	Saturation exposure [2]	0.4		μJ/cm²
R	Responsivity [2]	4		V/(μJ/cm²)
PRNU	Photoresponse nonuniformity [1,2]	±10	±15	%
V_{Dark}	Average dark signal [3]	1	2	%
V_{Sat}	Saturation output voltage [4]	1.6	2	V
R_O	Output impedance [5]	1		KΩ
f_s	Video sample rate [6]		5	MHz

Notes:
1 Ignoring lines 1, 2 and 256 as well as the first and last two diodes of each line
2 2870°K tungsten lamp with a Fish Schurman HA-11 visible spectrum filter was used as the source
3 Integration time 20 ms. Dark signal changes by a factor of 2 every 7°C
4 Voltage measured across 1.5KΩ load resistor
5 See Figure 9
6 Odd and even video outputs combined

Table 4. Electrical Specifications

Definition	Parameter				
	Sym	Min	Typ	Max [3]	Dimension
X-register clock amplitudes [2]	$ø_{X1}$	11.5	14	V_{DD}	V
	$ø_{X2}$	11.5	14	V_{DD}	V
Y-register clock amplitudes [2]	$ø_{Y1}$	11.5	14	V_{DD}	V
	$ø_{Y2}$	11.5	14	V_{DD}	V
Y shift register reset amplitude	$ø_{YST}$	11.5	14	V_{DD}	V
Line transfer amplitude	$ø_{LT}$	11.5	14	V_{DD}	V
Line reset amplitude	V_{LR}	9	12	V_{DD}	V
X-register input bias odd	V_{IQ1}		10		V
X-register input bias even	V_{IQ2}		10		V
Video reset 1 (odd)	VR_1		V_{DD}-0.5	V_{DD}	V
Video reset 2 (even)	VR_2		V_{DD}-0.5	V_{DD}	V
Frame reset gate [1]	FRG		V_{DD}-0.5	V_{DD}	V
Frame reset drain [1]	FRD		10	V_{DD}	V
Isolation gate	V_{Buff}	11	12.75	13	V
DC supply	V_{DD}	11.8	15	16	V
DC current	I_{DD}	6	8	10	mA
X-register tetrode gate bias	V_{BB}	8	12.5	V_{DD}-.5V	V
Multiplex clock amplitude	$ø_A$	11.5	14	V_{DD}	V
Multiplex clock amplitude	$ø_B$	11.5	14	V_{DD}	V
Substrate bias	V_{Sub}	-2.95	-3.3	-3.65	V

Notes:
1 See text
2 All voltages measured with reference to common (ground). See text
3 For optimum performance use typical value. Other in-spec voltages will operate the array but with reduction in performance

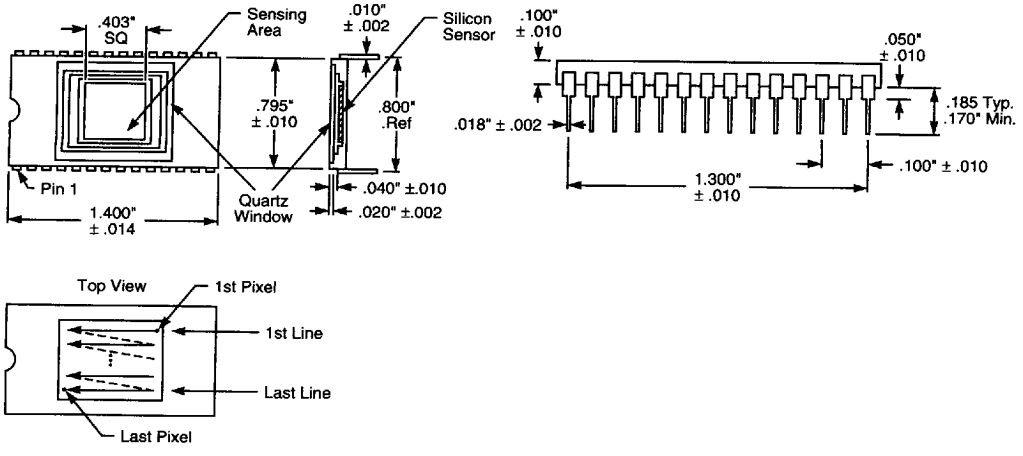


Figure 13. Package Dimensions and Scanning Sequence

Ordering Information

Part Number	Evaluation Circuit (Current Amplifier)	Adjacent Defects Forming a Group
RA0256BAQ-011 (1-12 defects)	RC0503ANC-011	up to 2
RA0256BAQ-020 (13-50 defects)	RC0503ANC-011	up to 4