

T-50-09



# NJ88C25

## FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated on the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered Band 0 and Band 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although thirty bits of data are initially required to program all counters, subsequent updating can be abbreviated to nineteen bits when only the 'A', 'M' and 'B' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

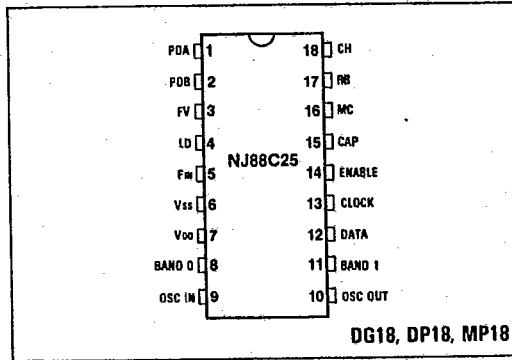


Fig.1 Pin connections - top view

### FEATURES

- 3.0V to 5.0V Supply Range
- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- > 20MHz Input Frequency

### ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD - Vss)	-0.5V to 7V
Input voltage	
Open drain O/Ps (pins 3 & 4)	7V
All other pins	Vss - 0.3V to VDD + 0.3V
Storage temperature	-65°C to +150°C

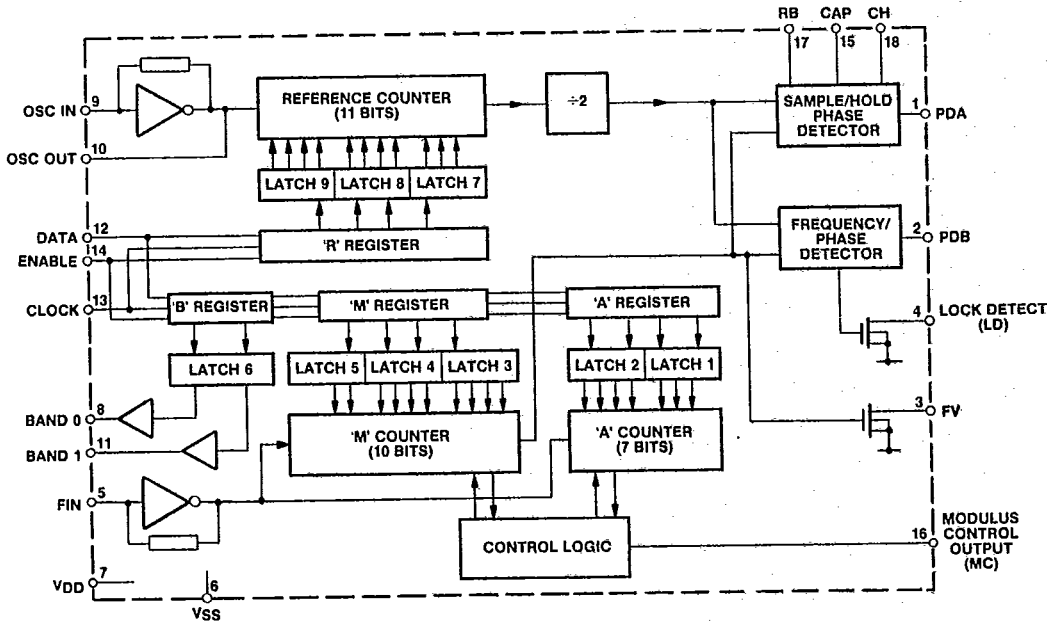


Fig.2 Block Diagram

NJ88C25

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):

V<sub>DD</sub> - V<sub>SS</sub> 2.7V to 5.5V, Temperature Range -30°C to +70°C

T-50-09

**DC Characteristics at V<sub>DD</sub> = 5.0V**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.5	TBA	mA	FOSC, FIN = 20MHz } 0 to 5V FOSC, FIN = 1MHz } square FOSC, FIN = 10MHz } wave
		0.7	TBA	mA	
		3.7	TBA	mA	
<b>Modulus Control out, BAND 0, BAND 1</b>					
High level	V <sub>DD</sub> -0.4			V	I <sub>source</sub> 1mA
Low level			0.4	V	I <sub>sink</sub> 1mA
<b>Lock Detect Out, FV</b>					
Low level			0.4	V	I <sub>sink</sub> 4mA
Open drain pull-up voltage			7	V	
<b>PDB output</b>					
High level	4.6			V	I <sub>source</sub> 4mA
Low level			0.4	V	I <sub>sink</sub> 4mA
3-state leakage			±0.1	μA	

**AC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC outputs	200			mV RMS	20MHz AC coupled sinewave V <sub>DD</sub> = 5V, 0 to 5V square wave Note 2
Max. operating freq. OSC/FIN inputs	20			MHz	
Propagation delay, clock to modulus control		30	50	ns	
<b>Programming Inputs</b>					
Clock high time, t <sub>CH</sub>	0.5			μs	Note 5
Clock low time, t <sub>CL</sub>	0.5			μs	
Enable set-up time, t <sub>ES</sub>	0.2		t <sub>CH</sub>	μs	
Enable hold time, t <sub>EH</sub>	0.2			μs	
Data set-up time, t <sub>DS</sub>	0.2			μs	
Data hold time, t <sub>DH</sub>	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V <sub>T+</sub>	3			V	TTL compatible
Negative going threshold, V <sub>T-</sub>			2	V	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	Note 3
Hold capacitor, CH			1	nF	
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

**NOTES**

- Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
- All counters have outputs directly synchronous with their respective clock rising edges.
- The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time constant of 5 microseconds.
- The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.
- Clock to enable set up time is variable, dependent on frequency of OSC. IN, it needs to be specified in terms of OSC. IN frequency, clock high time (t<sub>CH</sub>) and clock low time (t<sub>CL</sub>). Enable set-up time, t<sub>ES</sub> must meet following conditions:  $4 \times 1/\text{OSC. IN} \leq t_{ES} < (t_{CH} + t_{CL})$ .

NJ88C25

T-50-09

## PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	FV	This pin is an open drain output from the 'M' counter.
4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
6	V <sub>SS</sub>	Negative supply (ground).
7	V <sub>DD</sub>	Positive supply (normally 5V).
9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
8,11	BAND 0/1	Two latch outputs, providing an output of the data from the register 'B'.
12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are four data words which control the NJ88C25, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'B' (2 bits) and 'R' (11 bits).
13	CLOCK	Data is clocked in on the negative transition of the clock waveform. If less than 30 negative clock transitions have been received when the enable line goes low (ie only 'B', 'M' and 'A' have been clocked in) then the 'R' counter latch will remain unchanged and only 'B', 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'B', 'M' and 'A' have been loaded. If 30 negative transitions have been counted then the 'R' counter will be loaded with the new data.
14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions are only allowed when CLK is high.
15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V <sub>SS</sub> .)
16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of $M \cdot N + A$ where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $\div 128/129$ . The programming range of the 'M' counter is 3-1023 and for correct program operation $M \geq A$ . Wherever possible channels is required, the minimum division ratio should be $N^2 - N$ .
17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V <sub>SS</sub> .
18	CH	An external hold capacitor should be connected between this pin and V <sub>SS</sub> .

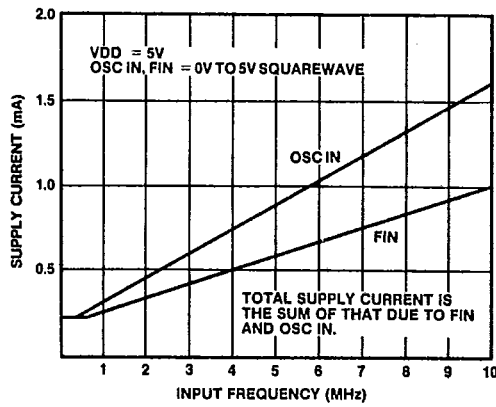


Fig.3 Typical supply current versus input frequency

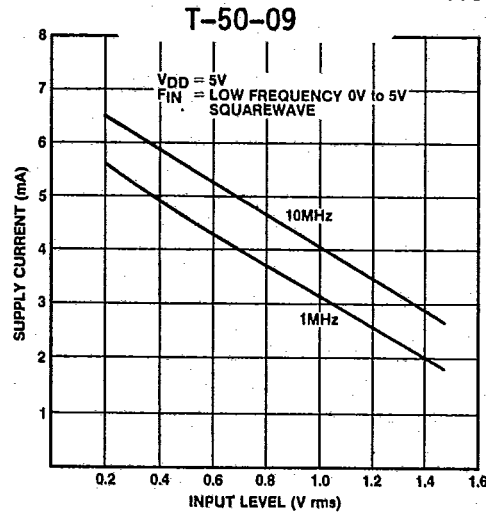


Fig.4 Typical supply current versus input level, Osc In

**PROGRAMMING**

**Reference Divider Chain**

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{f_{osc}}{2 \times f_{comp}}$$

ie where  $f_{comp}$  = comparison frequency  
 $f_{osc}$  = oscillator frequency  
 $R$  = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.  
 NB The total divider range is from 6 to 4094 in steps of 2.

**VCO Divider Chain**

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ( $N/N + 1$ ) and the value of the comparison frequency  $f_{comp}$ .

The division ratio  $P = NM + A$   
 where  $M$  is the ratio of the M counter in the range 3 to 1023 and  $A$  is the ratio of the A counter in the range 1 to 127  
 Note  $M \geq A$

$$\text{Also } P = \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of  $\div 64/65$  is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now  $P = NM + A$   
 which can be rearranged to be  $P/N = M + A/N$   
 In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64} \text{ therefore } 343.75 = M + \frac{A}{64}$$

$M$  is programmed to the integer part = 343 and  $A$  is programmed to the fractional part times 64  
 ie  $A = 0.75 \times 64 = 48$   
 NB The minimum ratio that can be used is  $N^2 - N$   
 To check  $P = 343 \times 64 + 48 = 22000$  which is the required dividers ratio.

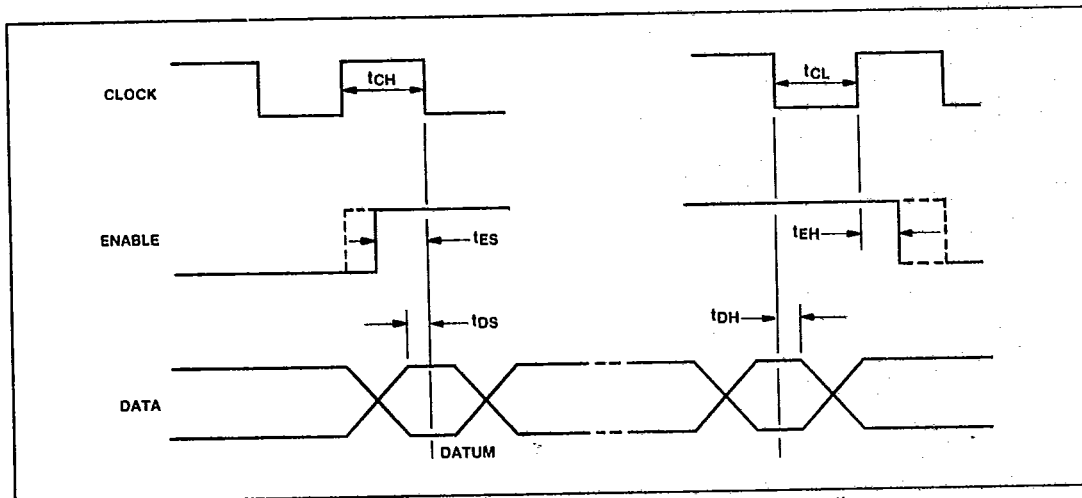


Fig.5 Timing diagram showing timing periods required for correct operation

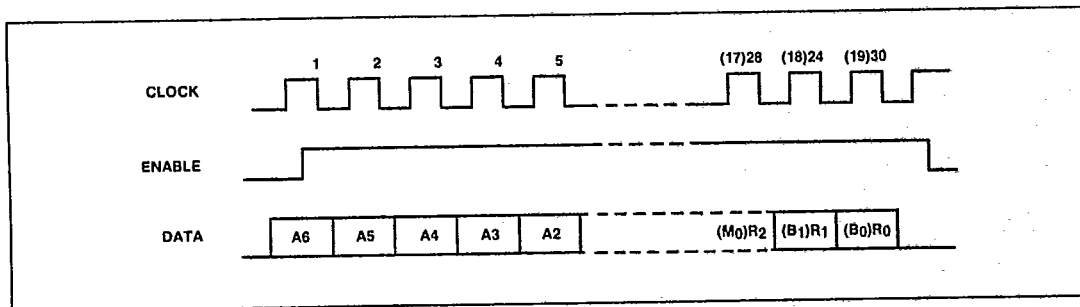


Fig.6 Timing diagram showing programming details

**PHASE COMPARATORS**

Noise output from a synthesiser loop is related to loop gain  $K\Phi K_V/P$ , where  $K\Phi$  is phase detector constant (volts/rad),  $K_V$  is the VCO constant (rad-secs/volt) and  $P$  is the overall loop division ratio. When  $P$  is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ88C25 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically

be at  $(V_{DD}-V_{SS})/2$  and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor,  $R_B$  and a capacitor,  $CAP$ .

An internal 50pF capacitor is used in the sample and hold comparator.

The gain is typically

$$GAIN = \frac{10 |V_{DD} - V_{SS} - 0.7 - 89(R_B^{-1/2})|}{2\pi [CAP + 50 \times 10^{-12}] \times R_B \times FR}$$

The value of  $R_B$  and  $CAP$  should be chosen to give the required gain at the reference frequency used.

Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires  $R_B$  to be approximately 39k $\Omega$ ,  $CAP$  is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to  $V_{SS}$ . A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

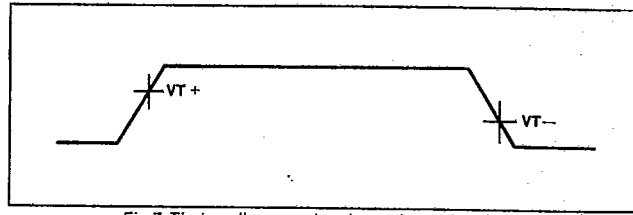


Fig.7 Timing diagram showing voltage thresholds

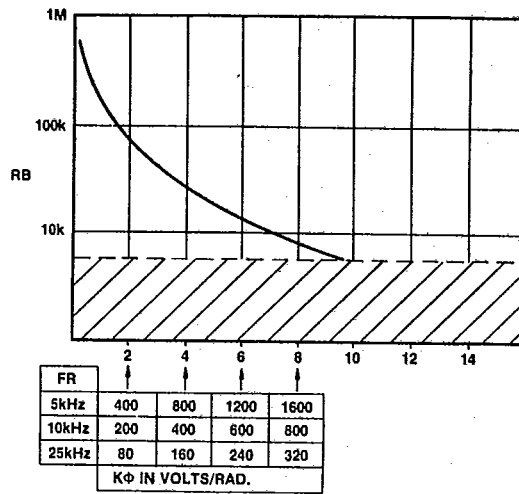


Fig.8 RB versus gain and reference frequency