To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M62500P/FP

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

DESCRIPTION

The M62500 is a semiconductor integrated circuit designed and developed as a deflection control of the CRT display monitor.
The built-in trigger mode oscillator allows stable PWM control to be gained against a wide range of change of external signals.
The M62500 provides a low supply voltage output malfunction preventive circuit (UVLO) and software start function optimum to horizontal output correction of monitor, high voltage drive and high voltage regulator.

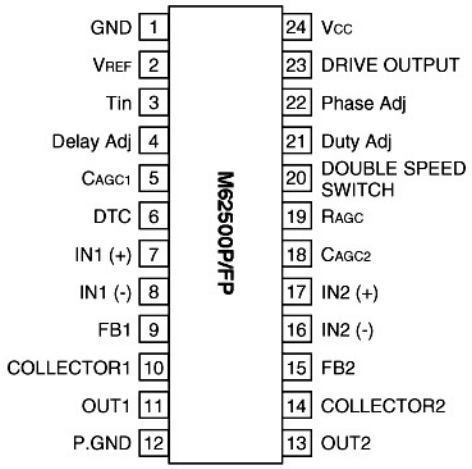
FEATURES

- PWM output in synchronization with external signals
- Wide range of PWM control frequency
  15kHz to 150kHz
- The PWM output phase is adjustable against external signals
- Soft start
- Built-in low voltage output malfunction prevention circuit
  Start V_{CC}>9V
  Stop V_{CC}<6V

APPLICATION

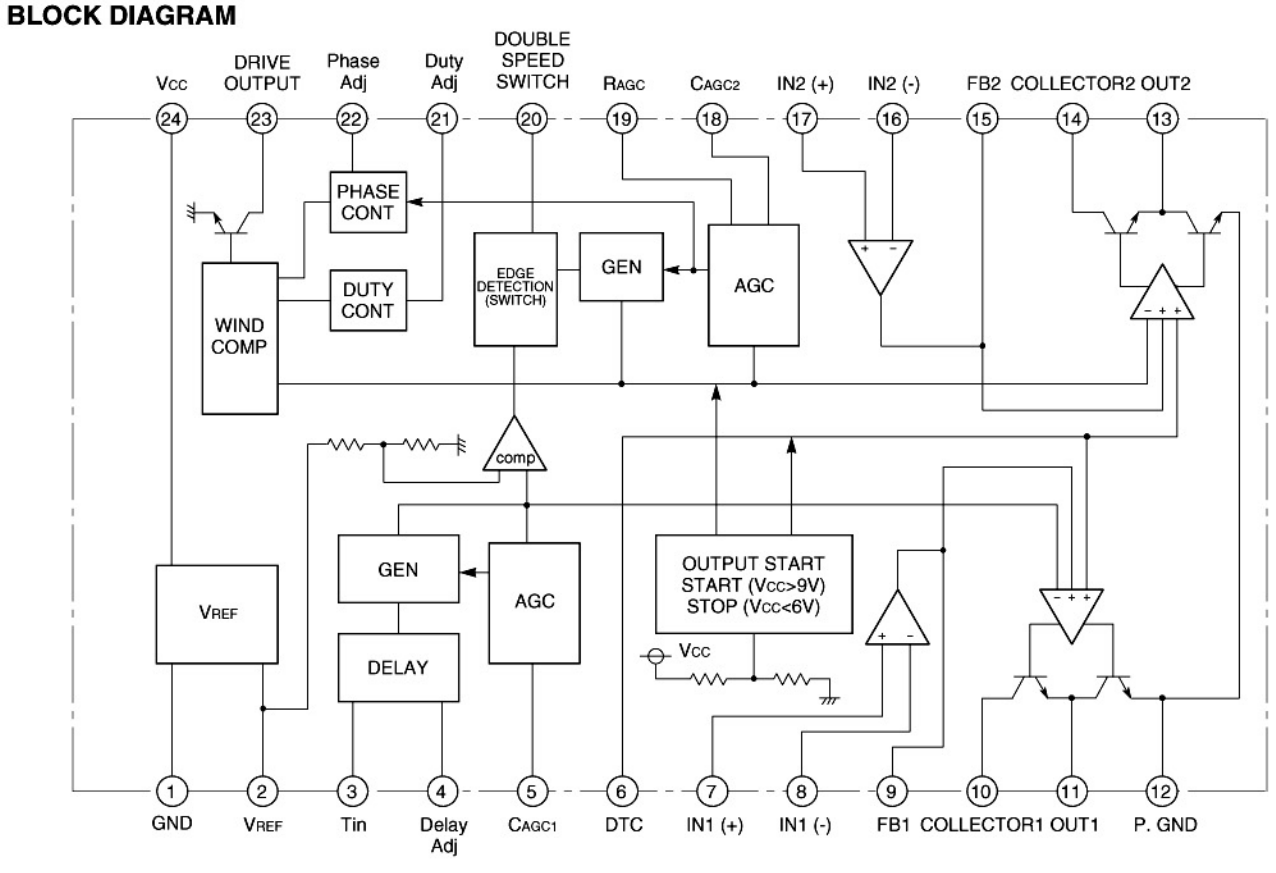
CRT display monitor

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D (P)
24P2V-A (FP)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings		Unit
V_{CC}	Supply voltage	15		V
V_{OUT}	Output voltage	15		V
I_{OUT}	Output current	±150		mA
V_d	Drive output voltage	15		V
I_d	Drive output current	20		mA
V_{ICM}	Common mode input voltage range of error amplifier	-0.3 to V_{CC}		V
V_{ID}	Common mode differential input voltage of error amplifier	V_{CC}		V
P_d	Power dissipation	P	FP	mW
		1400	1000	
K_Θ	Thermal derating	P	FP	mW/°C
		11.2	8	
T_{opr}	Operating temperature	-20 to +75		°C
T_{stg}	Storage temperature	-40 to +125		°C

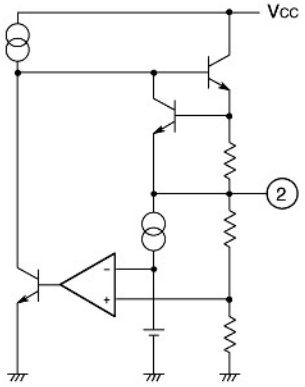
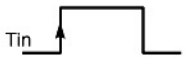
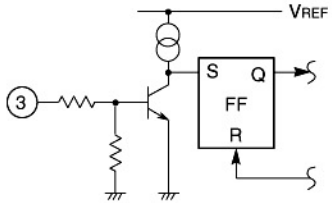
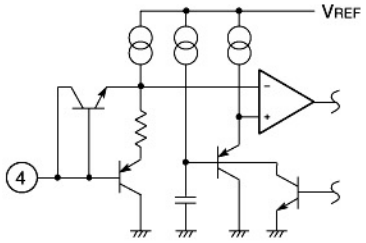
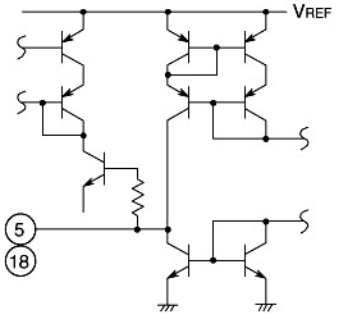
Note. For the polarity of current, the direction in which current flows to the IC is specified positive (+), while the direction in which current flows out from the IC is specified to be negative (-).

ELECTRICAL CHARACTERISTICS (V_{CC}=12V, f_{IN}=40kHz, Ta=25°C, unless otherwise noted)

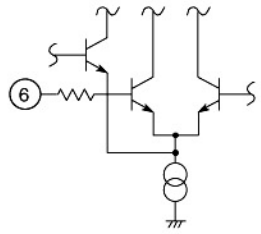
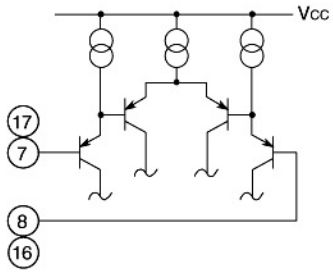
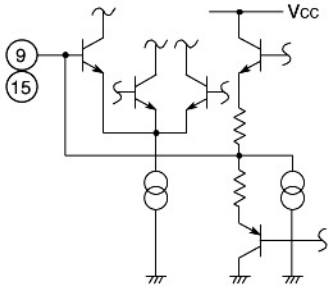
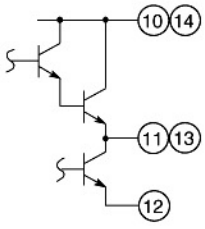
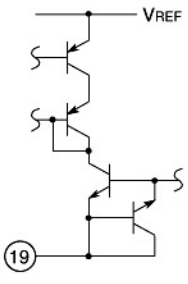
Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Supply voltage	V_{CC}	Range of power supply voltage		V_{CC} off		14	V
	I_{CC}	Dissipation current	Without signal	20	40	70	mA
	V_{CC} ON	Activation start voltage		8	9	10	V
	V_{CC} OFF	Activation stop voltage		5.4	6.0	6.6	V
Error amp. section	V_{IO}	Input offset voltage				7	mV
	I_{Ib}	Input bias voltage		-100			nA
	I_{IO}	Input offset current		-100		100	nA
	V_{ICM}	Common mode input range		-0.3		V_{CC}-2	V
	AV	Open loop gain		70	110		dB
	SR	Through rate			4		V/μs
	V_{OR}	Output voltage range 1)		0.3		V_{REF}-1.5	V
	I_{sink}	Output sink current		10			mA
	I_{source}	Output source current				-10	mA
PWM output section	V_{satL}	Output saturation voltage L	I_O=100mA		0.7	1.4	V
	V_{satH}	Output saturation voltage H	I_O=-100mA	9.5	10.5		V
Std. voltage section	V_{REF}	Reference voltage	I_{REF}=-5mA	4.80	5.00	5.20	V
	R_{eg-in}	Input stability	V_{CC}=7 to 14V I_{REF}=-5mA		1	10	mV
	R_{eg-L}	Load voltage	I_{REF}=0 to -5mA		2	20	mV
	TC_{VREF}	Temperature coefficient of reference voltage	Ta=-20 to +75°C		0.01		%/°C
	$I_{REF\ MAX}$	Maximum reference current			-40		mA
	IS	Short-circuit current			-70		mA
Delay adj section	I_{IN}	Input current	V_{IN}=5V	—	140	200	μA
	$V_{IN\ L}$	"L" input voltage		—	—	0.6	V
	$V_{IN\ H}$	"H" input voltage		2.0	—	—	V
	I_{Delay}	Input current		-0.6	-0.1	—	μA
	$T_{D\ min}$	Minimum delay time	$V_{Delay\ adj}$=0V	—	0.8	1	μs
	$T_{D\ max}$	Maximum delay time	$V_{Delay\ adj}$=3.0V	10	15	—	μs
PWM comp section	I_{DTC}	Input current		—	0.5	2.0	μA
	$V_{th\ U}$	Upper limit voltage of saw tooth wave		0.65V_{REF}	0.7V_{REF}	0.75V_{REF}	V
	$V_{th\ L}$	Lower limit voltage of saw tooth wave		0.28V_{REF}	0.3V_{REF}	0.32V_{REF}	V
	T_{Duty}	PWM output duty	V_{DTC}=2.5V	45	50	55	%
Duty adj section	I_{Duty}	Input current	$V_{Duty\ adj}$=2.5V	-6.5	-1.3	—	μA
	$Duty_{min}$	Minimum duty		—	10	20	%
	$Duty_{max}$	Maximum duty		80	95	—	%
	Duty	Duty	$V_{Duty\ adj}$=2.5V	45	50	55	%
Phase adj section	I_{Phase}	Input current	$V_{Phase\ adj}$=2.5V	-3.5	-0.7	—	μA
	$T_{2\ min}$	Minimum leading time of drive output		—	0.7	1.6	μs
	$T_{2\ max}$	Minimum leading time of drive output		9	9.4	—	μs
	T_2	Leading time of drive output	$V_{Phase\ adj}$=1.0V	4.5	5.5	7.0	μs
Drive output section	$V_{sat\ D}$	Output saturation voltage	I_d=10mA			0.4	V
	I_{LD}	Output leak current	V_{DO}=12V			1	μA
fh switch sectio	I_{fh}	fh pin current	V_{fh}=5V	—	330	430	μA
n	V_{fh}	fh switching voltage		0.4V_{REF}	0.5V_{REF}	0.6V_{REF}	V

Note 1. Output must not be reversed with input of 0.

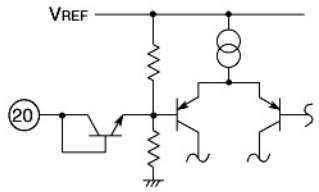
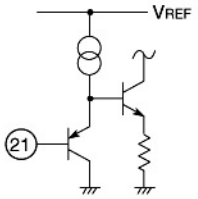
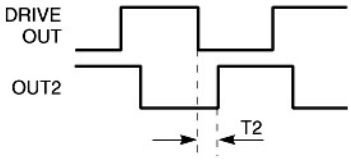
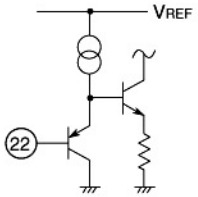
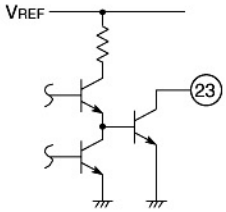
EXPLANATION OF TERMINALS

Pin No.	Symbol	Function and peripheral circuit of pins
①	GND	GND
②	V_{REF}	5.0V reference voltage External load of about 5mA can be taken out. 
③	T_{in}	Trigger input Read at the rising edge  
④	Delay Adj	Delay adjustment Delay of read trigger signal V_{Delay} : 0 to 3.0V T_{Delay} : 1μ to 10μsec 
⑤ ⑱	C_{AGC1} C_{AGC2}	AGC capacitance Connects capacitance between each pin and GND and sets up AGC sensitivity 

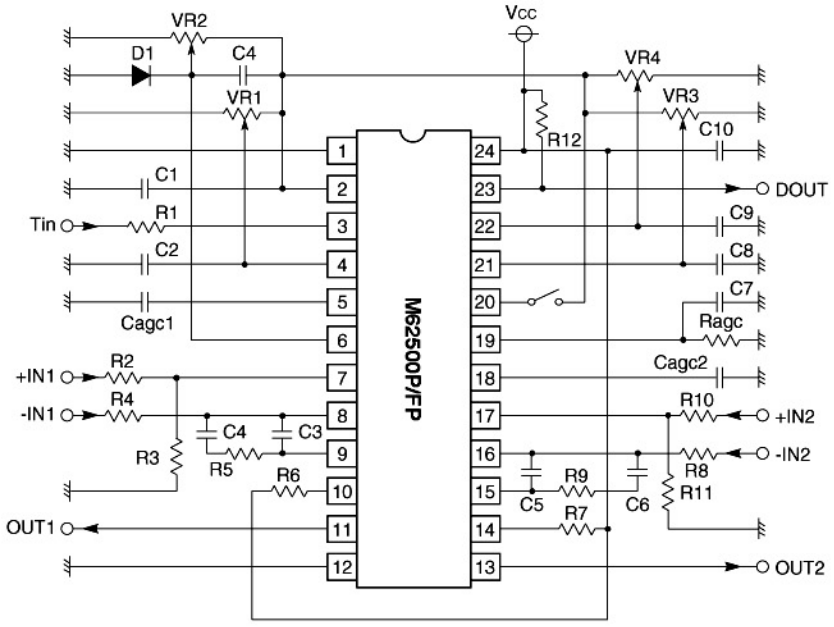
EXPLANATION OF TERMINALS (Cont.)

Pin No.	Symbol	Function and peripheral circuit of pins
⑥	DTC	Dead time control (PWM comparator ⊕ pin) 
⑦ ⑧ ⑯ ⑰	IN1 (+) IN1 (-) IN2 (-) IN2 (+)	Air amplifier input pin 
⑨ ⑮	FB1 FB2	Air amplifier output (PWM comparator ⊕ input pin) 
⑩ ⑪ ⑫ ⑬ ⑭	COLLECTOR1 OUT1 P.GND OUT2 COLLECTOR2	PWM output section 
⑲	RAGC	AGC current setup Connects resistance between pin ⑲ and GND and sets up AGC current on the OUT2 side. 

EXPLANATION OF TERMINALS (Cont.)

Pin No.	Symbol	Function and peripheral circuit of pins
⑳	fh/2fh	Double speed switch Switches frequency of OUT2 and drive output to the double frequency. OPEN, GND → fh VREF → 2fh 
㉑	Duty Adj	Duty adjustment of drive output 
㉒	Phase Adj	Phase adjustment of drive output against OUT2 (T2)  
㉓	DRIVE OUTPUT	Open collector output 
㉔	Vcc	Supply terminal

APPLICATION EXAMPLE



C1, C10 : Is required for stabilization of Vcc and V_{REF}. Is normally set to tens of μF to hundreds of μF.

VR 1, 2, 3, 4 : Is determined taking into account the load capability of V_{REF}. (External load capability of approx. 5mA) Shall be normally set to approx. 10kΩ.

C2, C8, C9 : Is added to high impedance pin of voltage control for improvement in noise margin. Depends on the device installation environment. Shall be normally set to approx. 0.1μF.

C4, D1 : Is added for the execution of software start. Set a time constant, taking into account the set value of VR2.

R1 : Is added to reduce interference by Tin and outputs. With VIN=approx. 2.5V to 5V, the resistance value of approx. 22kΩ is recommended.

Cagc 1, 2 : Capacitance necessary for stabilization of AGC. As the capacitance is larger, the stability is larger, but the characteristic of answering becomes worse. The capacitance value of 1μF is recommended.

R2, R3, R10, R11 : A gain setup constant of error Amp. To
R4, R5, R8, R9 assure the stability of feedback, R4 and R8
C3, C4, C5, C6 shall be set to several kΩ to tens of kΩ to set the gain to approx. 20dB to 40dB with f=1 kHz. If the gain is too low, jitter may take place. It is therefore recommended to set C3 and C5 to tens of pF to hundreds of pF, C4 and C6 to thousands of pF to tens of thousands of pF, and R5 and R9 to tens of kΩ to hundreds of kΩ.

Ragc : Resistance for setting AGC on the OUT2 side. Is set with Ragc=27kΩ.

C7 : If f to be input into Tin suddenly changes, addition of C7 shortens non-control time of Dout (output of "H"). As a capacitance value, it is recommended to adopt 2.2μF. In the case of adding C7, however, Cagc2≥0.68μF is recommended.

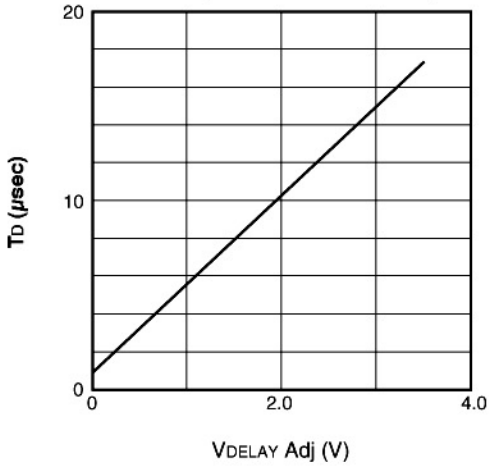
R6, R7 : Current limit resistance of OUT1/2. Is normally set to several Ω. Insertion of direct limit resistance into OUT1/2 pin is also effective.

R12 : Pull-up resistance of DOUT output. DOUT is an open collector output and requires R12. Is normally set to several kΩ.

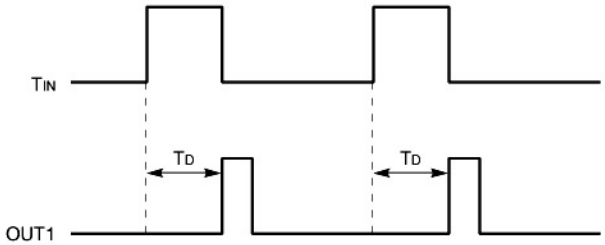
* Note: To reduce interference in the signal system, pins ① GND and ⑫ P.GND shall be grounded at a point in the power supply block.

SETUP OF VOLTAGE CONTROL BLOCK

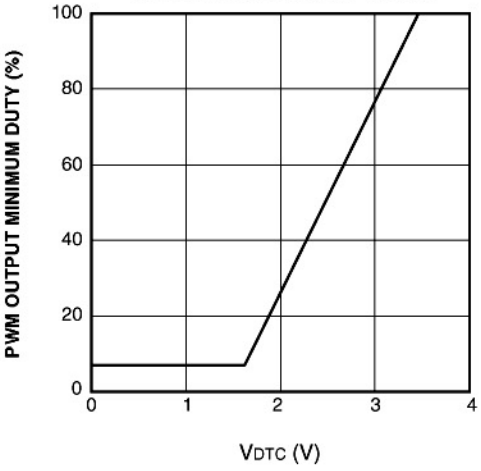
TD vs. VDELAY Adj CHARACTERISTICS (f=40kHz)



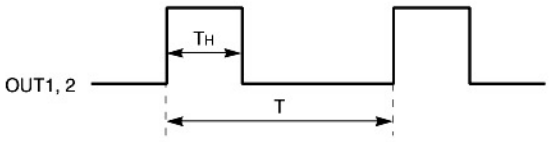
Applying a voltage to the DELAY Adj pin can control the delay time of OUT1 to TIN.



PWM OUTPUT MINIMUM DUTY vs. VDTC CHARACTERISTICS (f=40kHz)



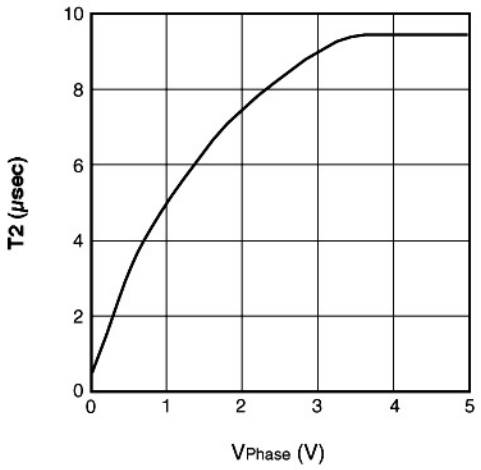
Applying a voltage to the DTC pin can control the dead time of PWM output.



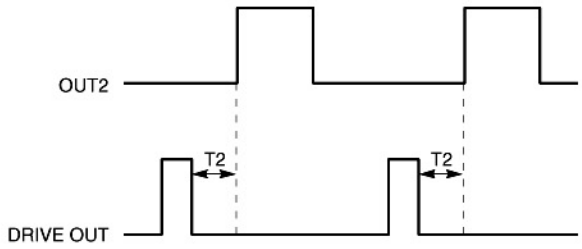
PWM output minimum duty

$$T_{DUTY} = \frac{T_H}{T} \times 100\ (\%)$$

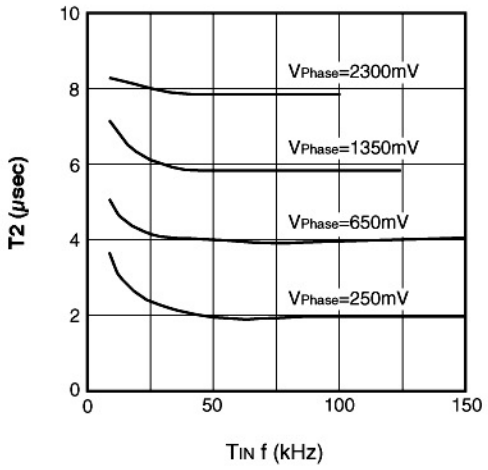
T2 vs. VPhase CHARACTERISTICS (f=40kHz)



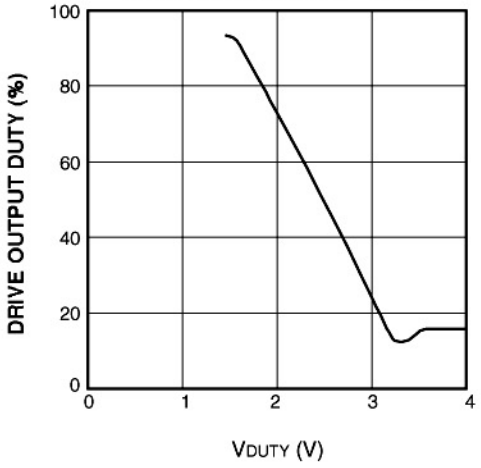
Applying a voltage to the Phase Adj pin can control a leading time of drive output to OUT2.



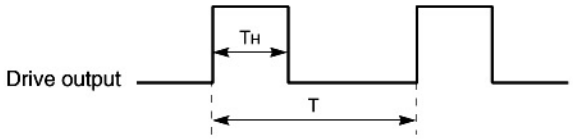
T2 vs. f CHARACTERISTICS



DRIVE OUTPUT DUTY vs. VDUTY CHARACTERISTICS (f=40kHz)



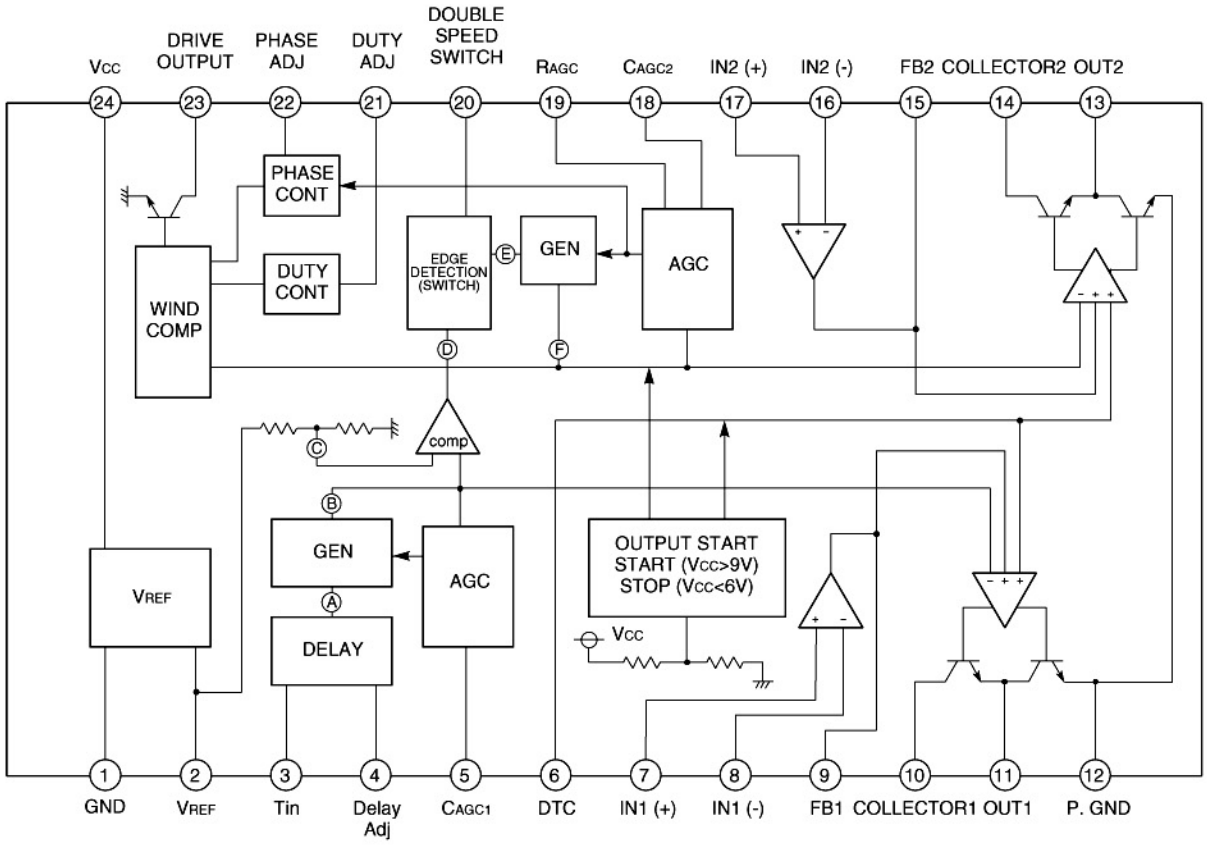
Applying a voltage to the DUTY Adj pin can control drive output duty.



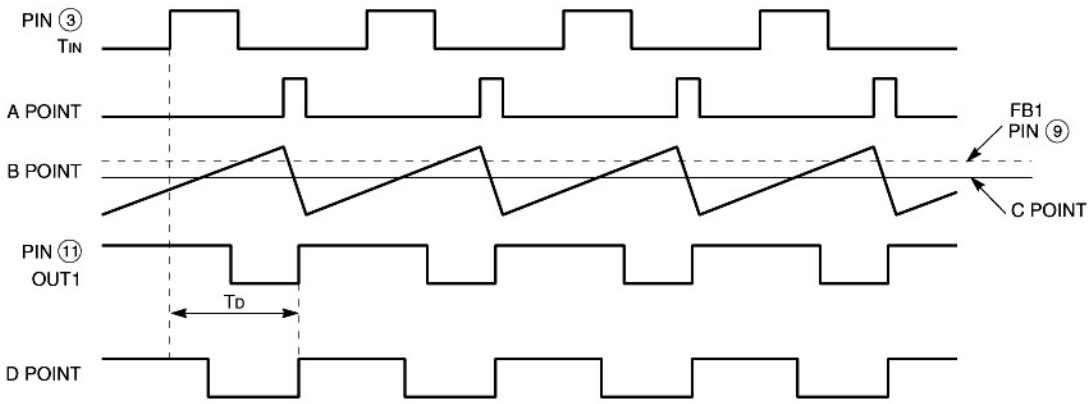
Drive output duty

$$T_{DUTY} = \frac{T_H}{T} \times 100\ (\%)$$

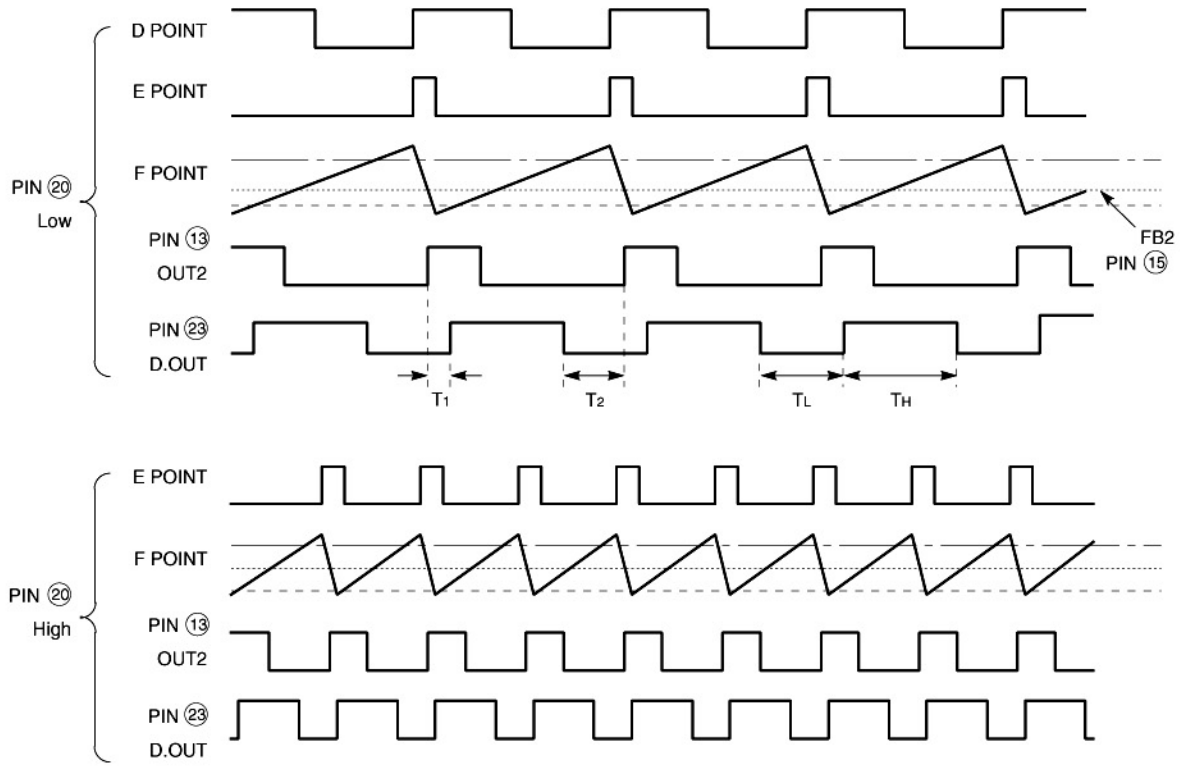
TIME CHART



PIN WAVE

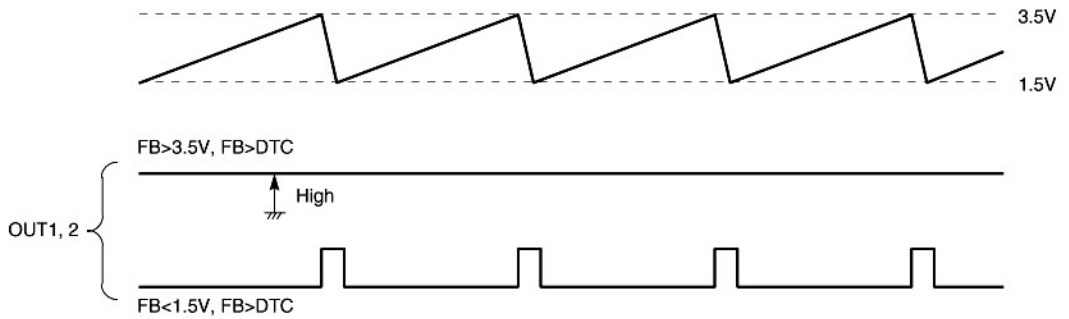


PIN WAVE (Cont.)



PWM OUT NON-CONTROL STATUS

With trigger input at pin③



Without trigger at pin③ (in case of GND)