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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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RJK6011DJE

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1577-0300

Rev.3.00

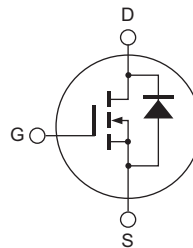
Oct 03, 2008

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSS0003DC-A
(Package name: TO-92 Mod)



1. Source
2. Drain
3. Gate

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	0.1	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	0.4	A
Body-drain diode reverse drain current	I_{DR}	0.1	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note1}	0.4	A
Channel dissipation	Pch	0.9	W
Channel to ambient thermal impedance	θ_{ch-a}	139	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

Electrical Characteristics

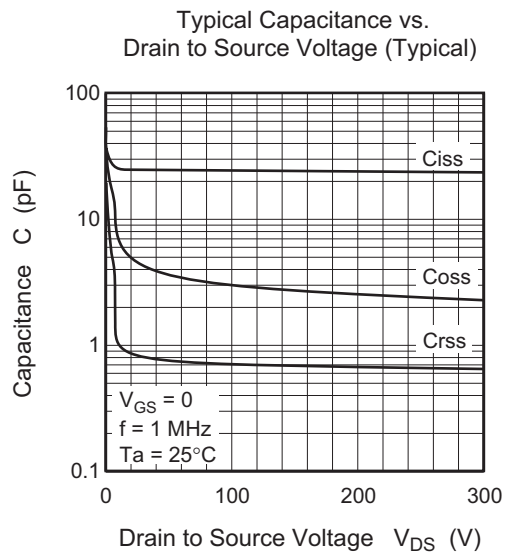
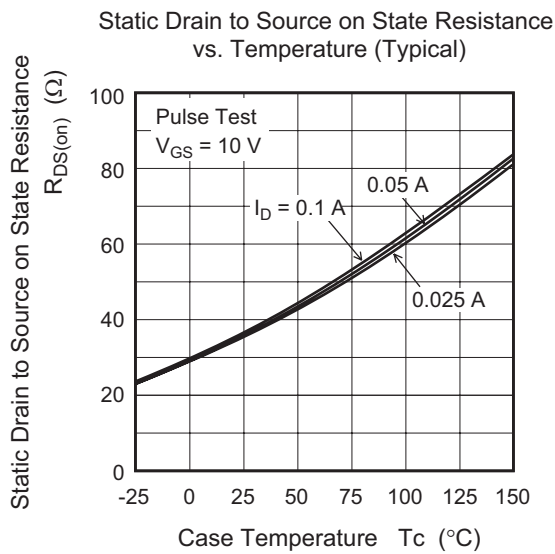
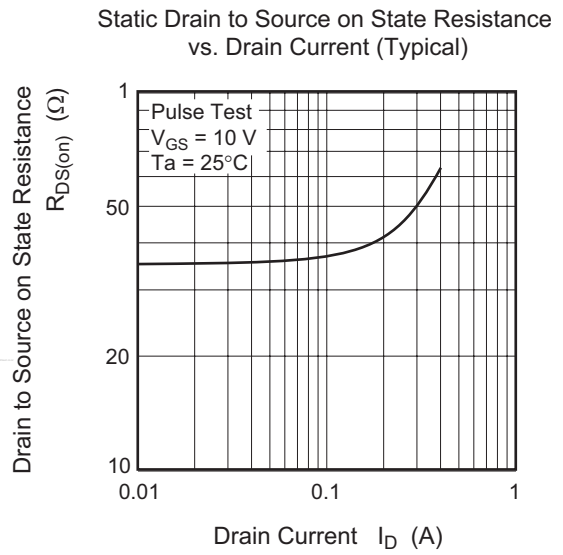
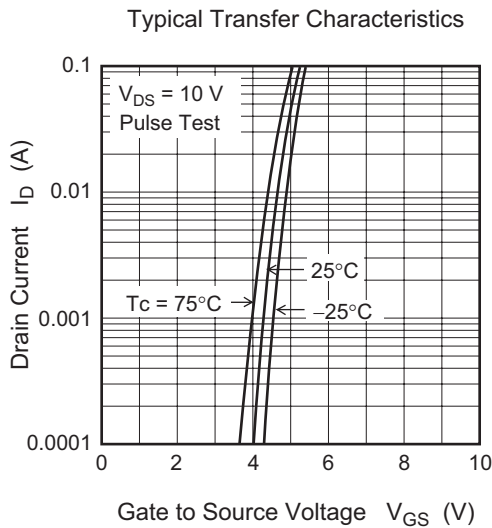
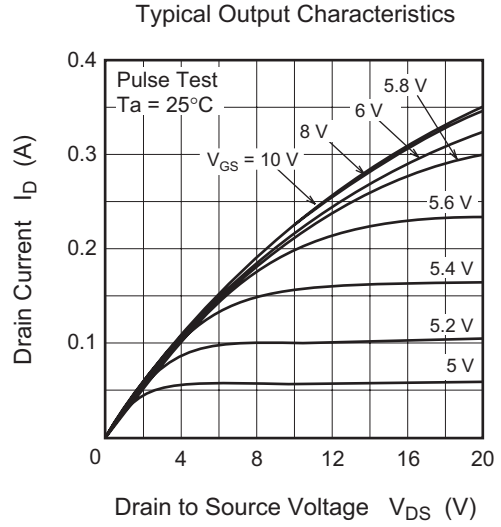
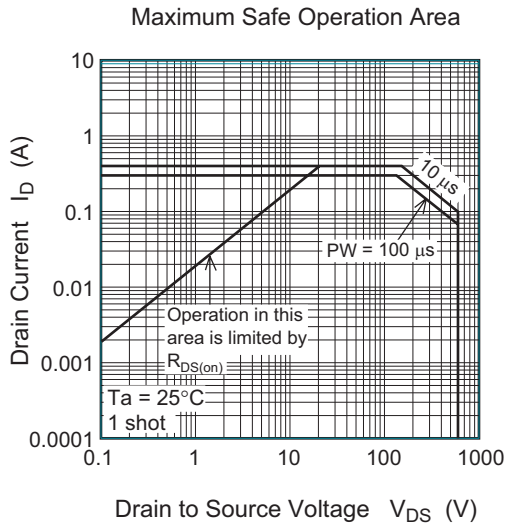
(Ta = 25°C)

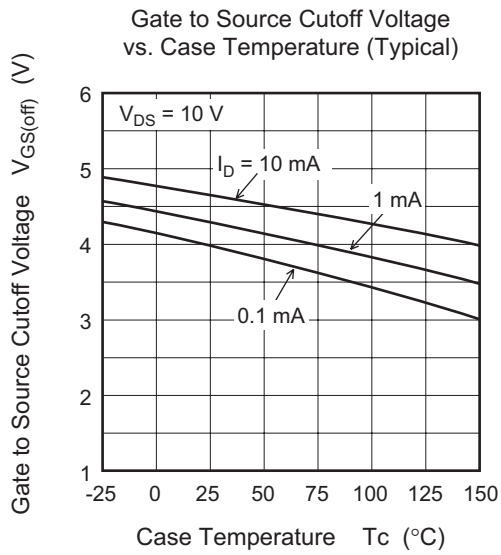
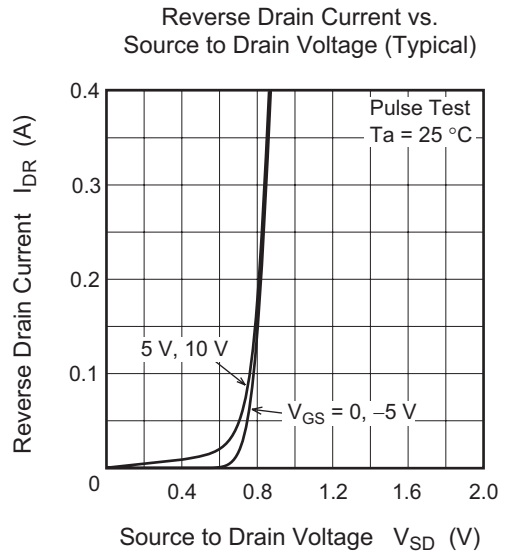
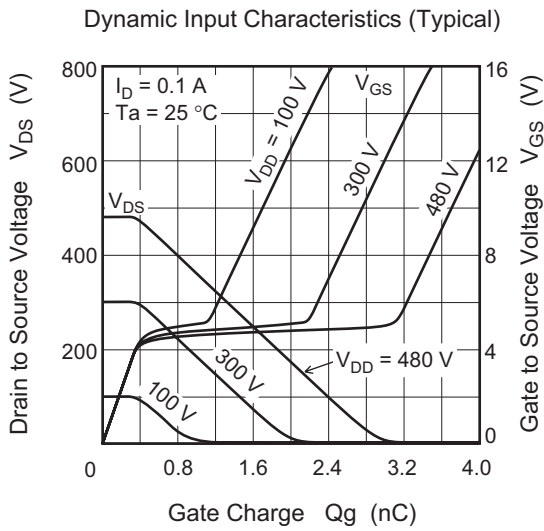
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 600 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	35	52	Ω	$I_D = 0.05 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note2}
Input capacitance	C_{iss}	—	25	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	4.7	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	0.9	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	33	—	ns	$I_D = 0.05 \text{ A}$
Rise time	t_r	—	16	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	54	—	ns	$R_L = 6000 \Omega$
Fall time	t_f	—	300	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	3.7	—	nC	$V_{DD} = 480 \text{ V}$
Gate to source charge	Q_{gs}	—	0.4	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.7	—	nC	$I_D = 0.1 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.80	1.35	V	$I_F = 0.1 \text{ A}$, $V_{GS} = 0$ ^{Note2}

Notes: 2. Pulse test

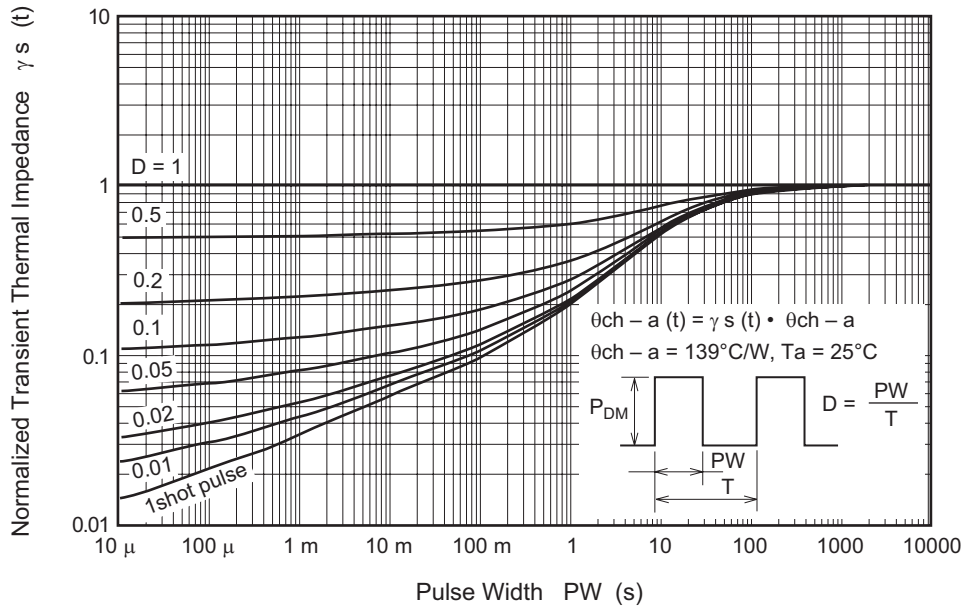
3. Since this device is equipped with high voltage FET chip ($V_{DSS} \geq 600 \text{ V}$), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.

Main Characteristics

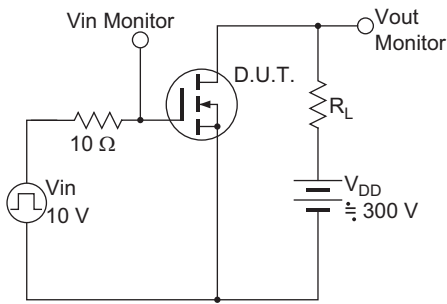




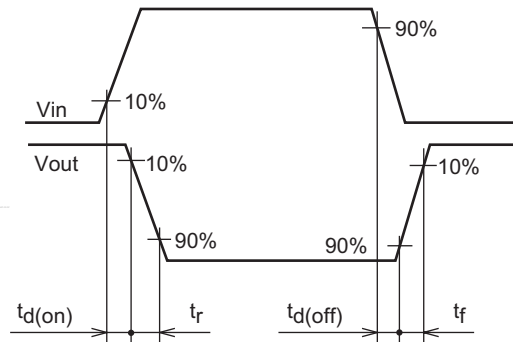
Normalized Transient Thermal Impedance vs. Pulse Width



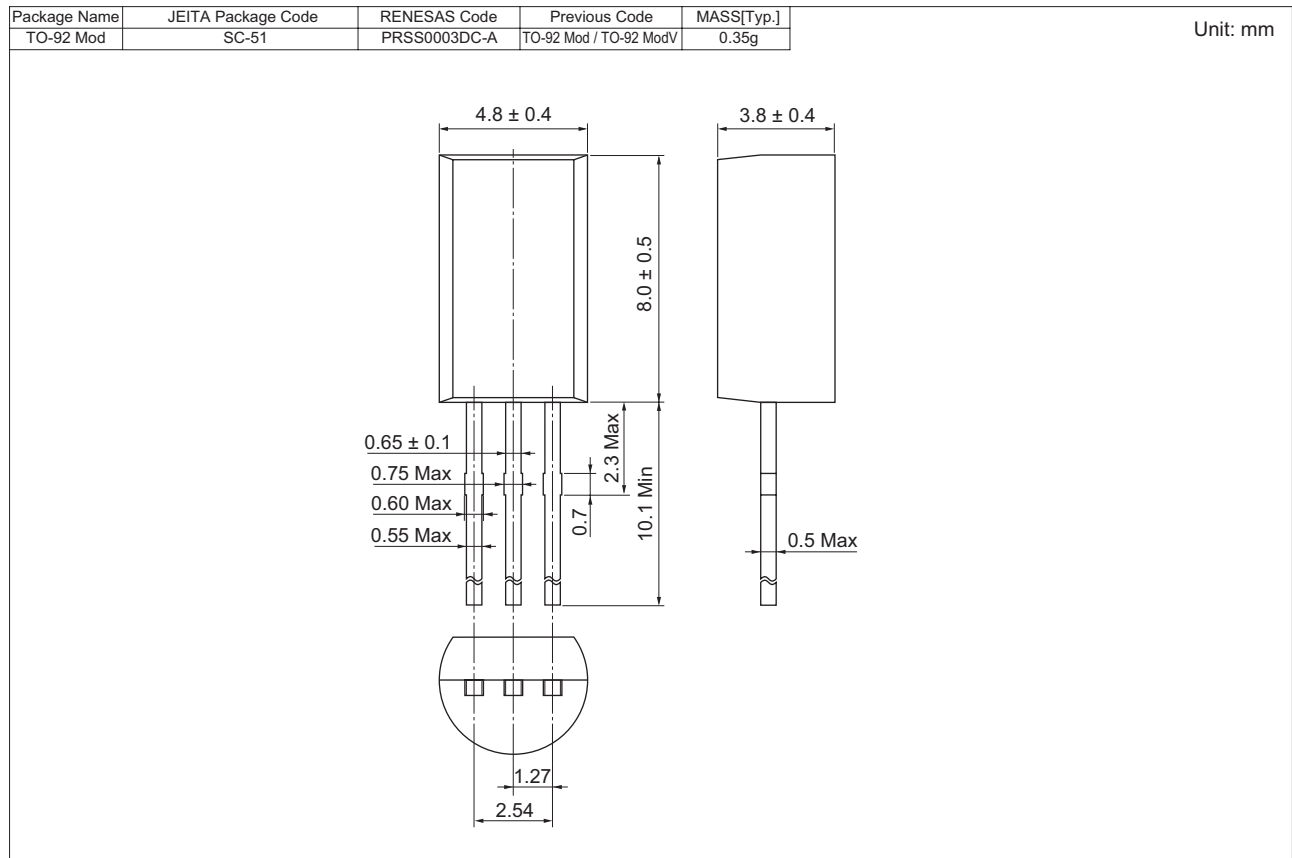
Switching Time Test Circuit



Waveform



Package Dimensions



Since RJK6011DJE is equipped with high voltage FET chip ($V_{DSS} \geq 600$ V), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.

Ordering Information

Part No.	Quantity	Shipping Container
RJK6011DJE-00-Z0	2500 pcs	Hold Box, Radial Taping

Notes:

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510