DCR960G26

Phase Control Thyristor

High Power Semiconductor Devices

Preliminary Information

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR960G28 DCR960G26 DCR960G24	2800 2600 2400	T_{vj} = -40℃ to 125℃, I_{DRM} = I_{RRM} = 50mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

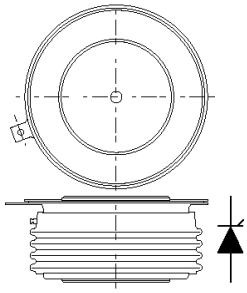
DCR960G26

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	2600V
$I_{T(AV)}$	960A
I_{TSM}	13000A
dV/dt*	1500V/µs
dI/dt	500A/µs

* **Higher dV/dt selections available**



Outline type code: G

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60℃ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	965	A
$I_{T(RMS)}$	RMS value	-	1516	A
I_T	Continuous (direct) on-state current	-	1420	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125℃	13.0	kA
I^2t	I^2t for fusing	V_R = 0	0.845	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0268	℃/W
		Single side cooled	Anode DC	-	0.0527	℃/W
			Cathode DC	-	0.0652	℃/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 11.5kN	Double side	-	0.0072	℃/W
		(with mounting compound)	Single side	-	.0144	℃/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	℃
		Reverse (blocking)		-	125	℃
T_{stg}	Storage temperature range			-55	125	℃
F_m	Clamping force			10	13	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125℃		-	50	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125℃, gate open		-	1500	V/μs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	250	A/μs
		Gate source 30V, 10Ω, t_r < 0.5μs, T_j = 125℃	Non-repetitive	-	500	A/μs
$V_{T(TO)}$	Threshold voltage – Low level	100A to 500A at T_{case} = 125℃		-	0.8	V
	Threshold voltage – High level	500A to 3000A at T_{case} = 125℃		-	0.95	V
r_T	On-state slope resistance – Low level	100A to 500A at T_{case} = 125℃		-	0.7556	mΩ
	On-state slope resistance – High level	500A to 3000A at T_{case} = 125℃		-	0.51	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5μs, T_j = 25℃		TBD	TBD	μs
t_q	Turn-off time	T_j = 125℃, V_R = 200V, dI/dt = 5A/μs, dV_{DR}/dt = 20V/μs linear		150	350	μs
Q_S	Stored charge	I_T = 2000A, T_j = 125℃, dI/dt = 5A/μs,		700	1500	μC
I_L	Latching current	T_j = 25℃, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25℃, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25℃	1.5	V
V_{GD}	Gate non-trigger voltage	At V_{DRM}, T_{case} = 125℃	TBD	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25℃	250	mA
I_{GD}	Gate non-trigger current	V_{DRM} = 5V, T_{case} = 25℃	TBD	mA

CURVES

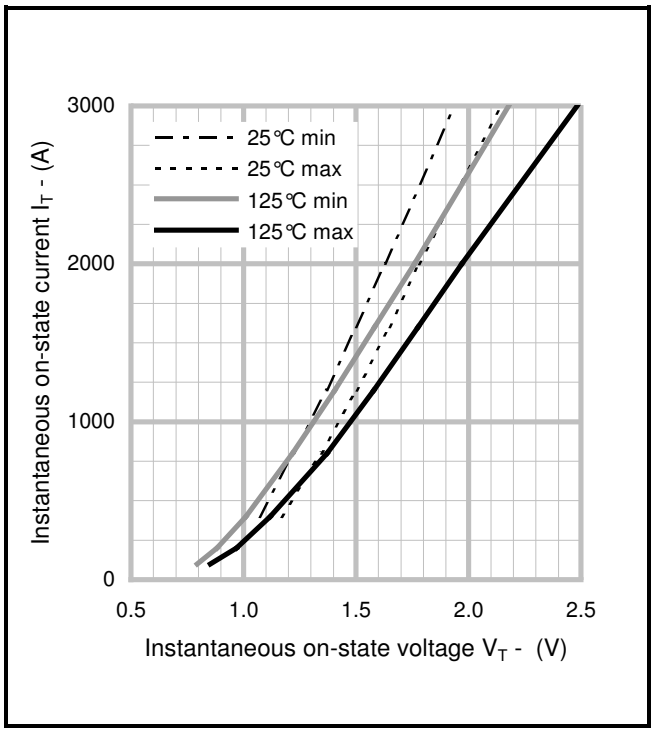


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.404415
B = 0.080354
C = 0.000415
D = 0.003401

these values are valid for T_j = 125℃ for I_T 50A to 3000A

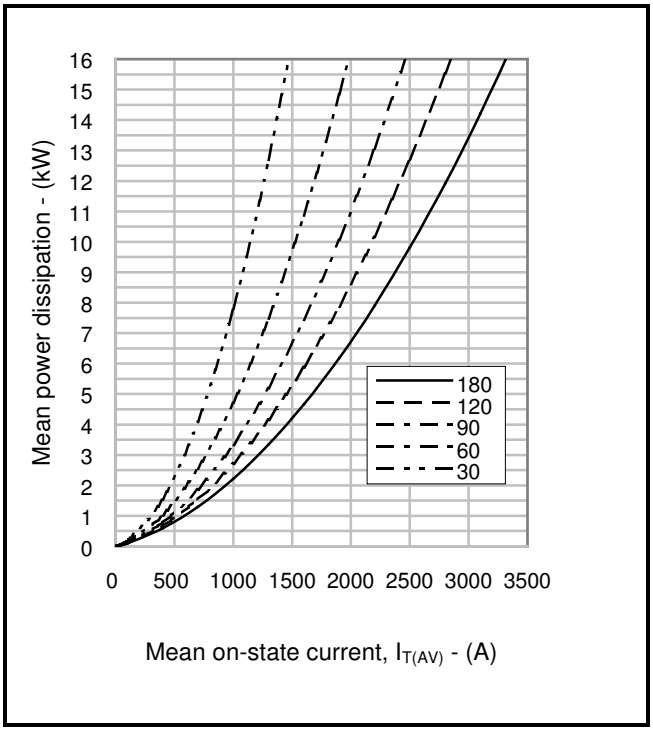


Fig.3 On-state power dissipation – sine wave

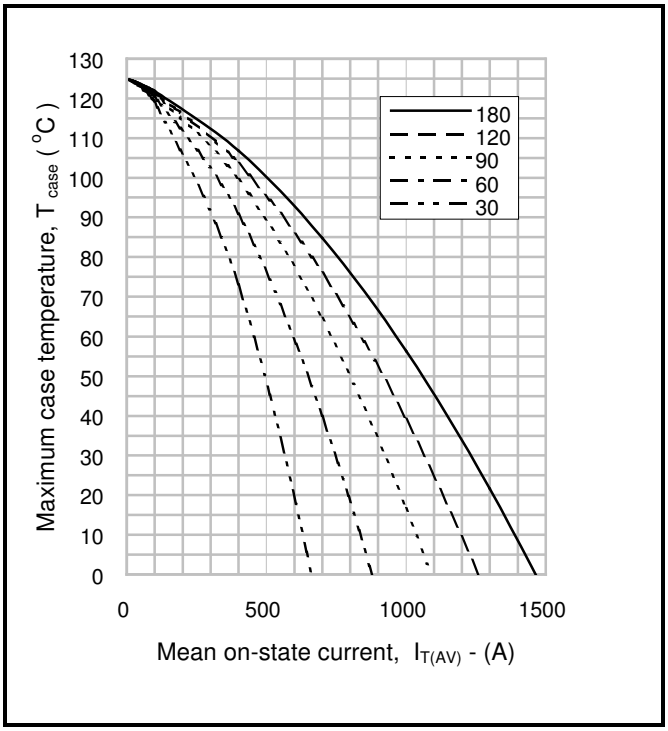


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

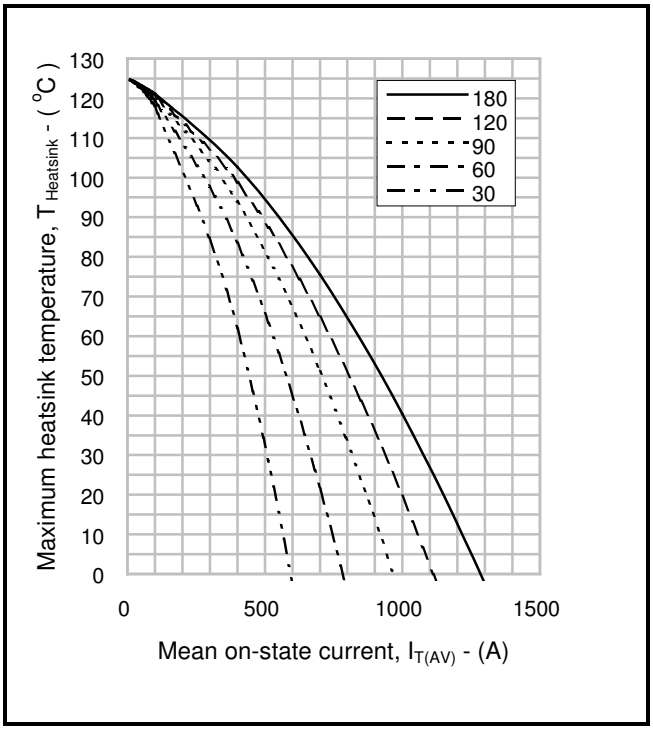


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

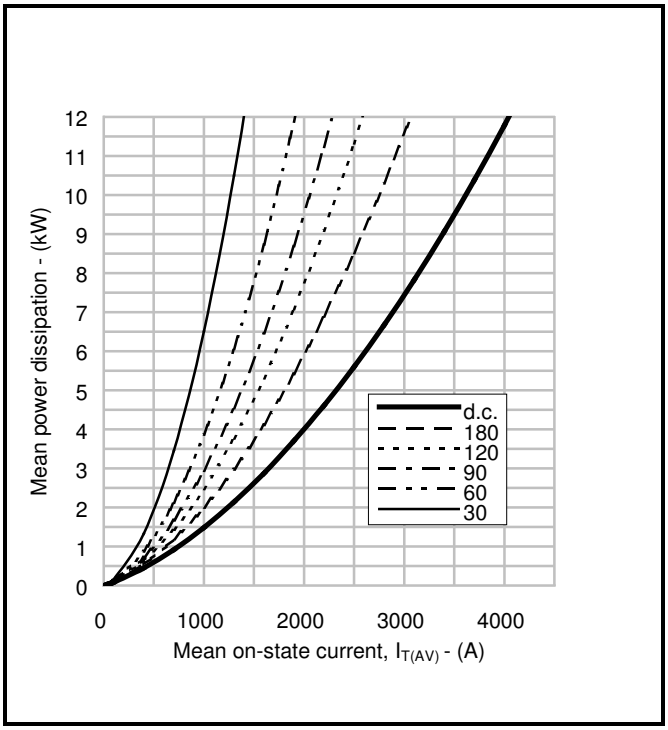


Fig.6 On-state power dissipation – rectangular wave

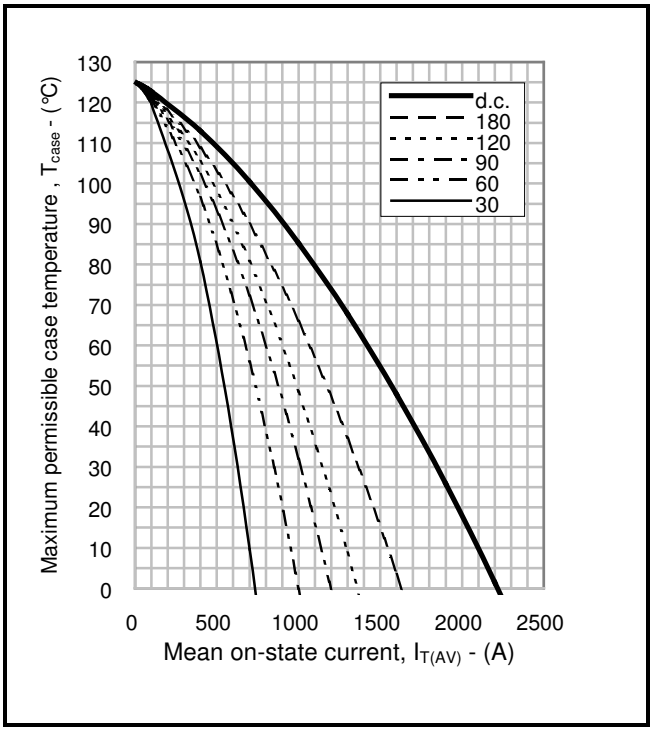


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

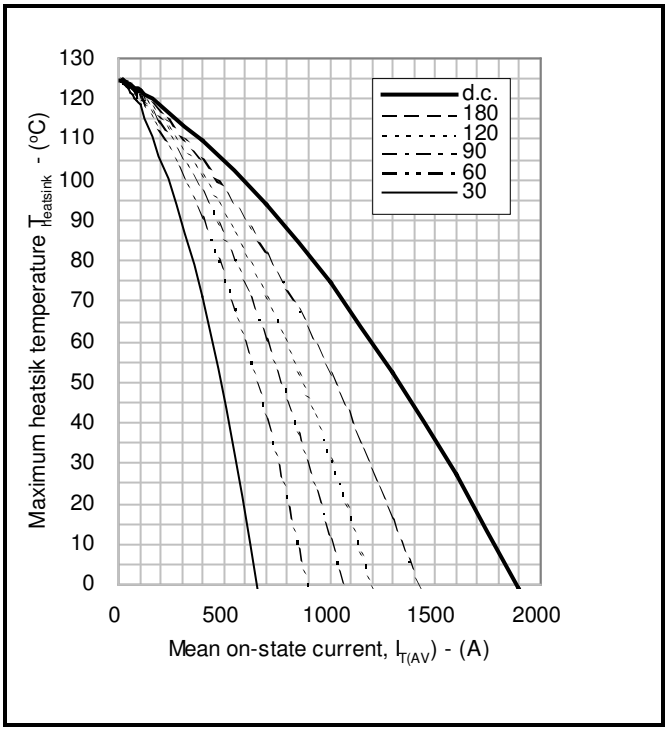
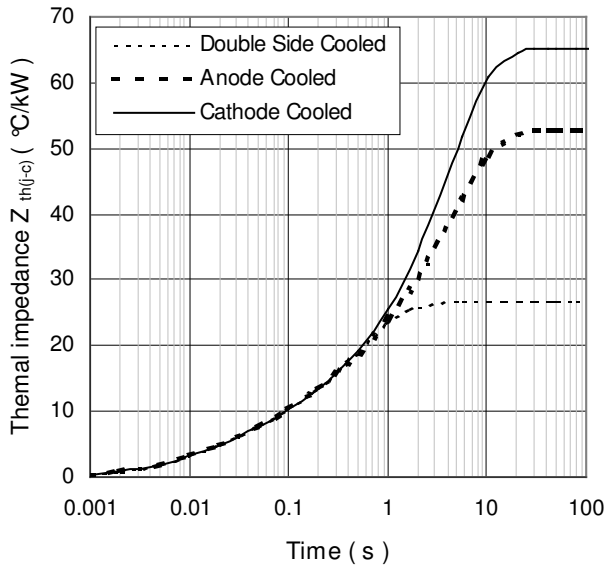


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (°C/kW)	2.2995	5.4226	16.9074	2.1488
	T_i (s)	0.0066401	0.0457025	0.4962482	1.8248
Anode side cooled	R_i (°C/kW)	2.3214	5.2661	10.2686	34.8031
	T_i (s)	0.0066948	0.045528	0.3484209	4.582
Cathode side cooled	R_i (°C/kW)	2.4895	5.9105	7.4256	49.3432
	T_i (s)	0.0070404	0.052895	0.3933903	4.2295

$Z_{th} = \Sigma [R_i \times (1\text{-exp. } (t/t_i))]$ [1]

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ °	sine.	rect.
180	4.15	2.72
120	4.90	4.02
90	5.74	4.79
60	6.53	5.65
30	7.16	6.64
15	7.46	7.18

Anode Side Cooling		
	ΔZ_{th} (z)	
θ °	sine.	rect.
180	4.15	2.72
120	4.89	4.02
90	5.73	4.78
60	6.52	5.65
30	7.15	6.62
15	7.44	7.16

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ °	sine.	rect.
180	4.13	2.71
120	4.87	4.00
90	5.69	4.76
60	6.46	5.60
30	7.07	6.56
15	7.36	7.09

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

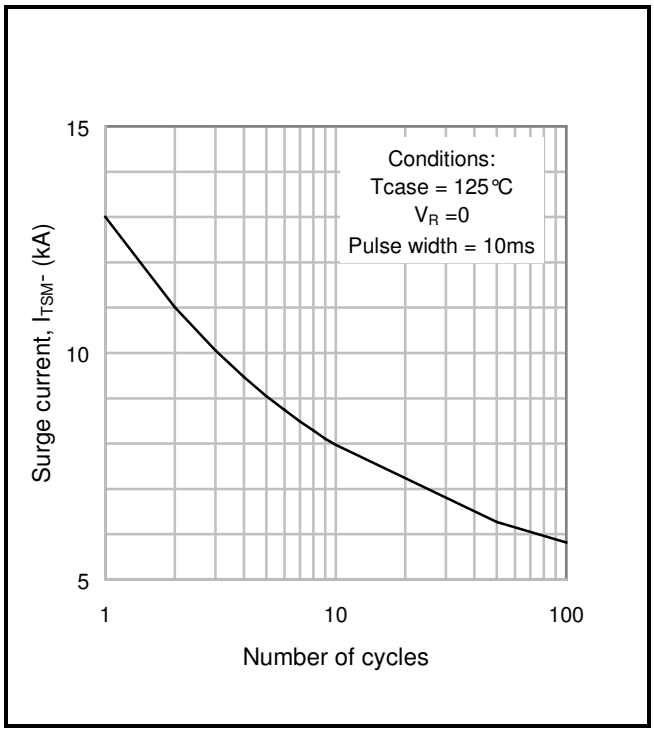


Fig.10 Multi-cycle surge current

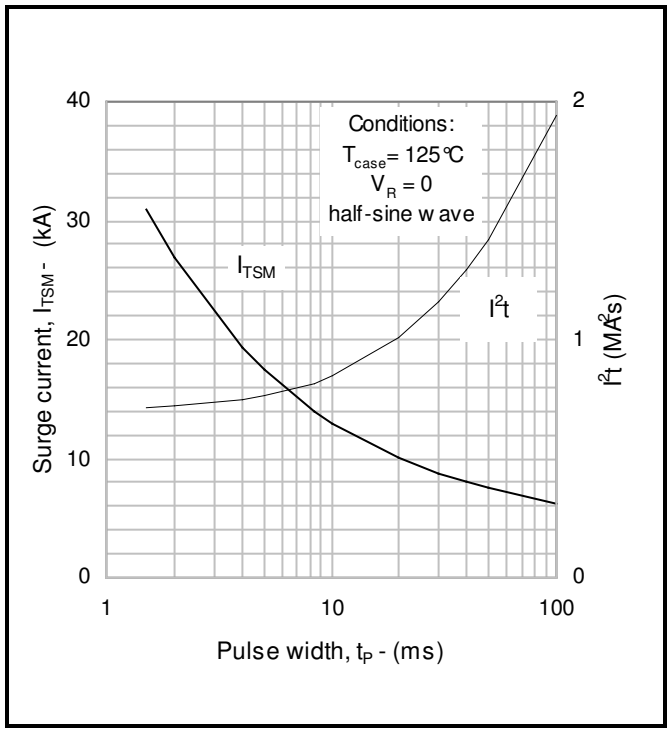


Fig.11 Single-cycle surge current

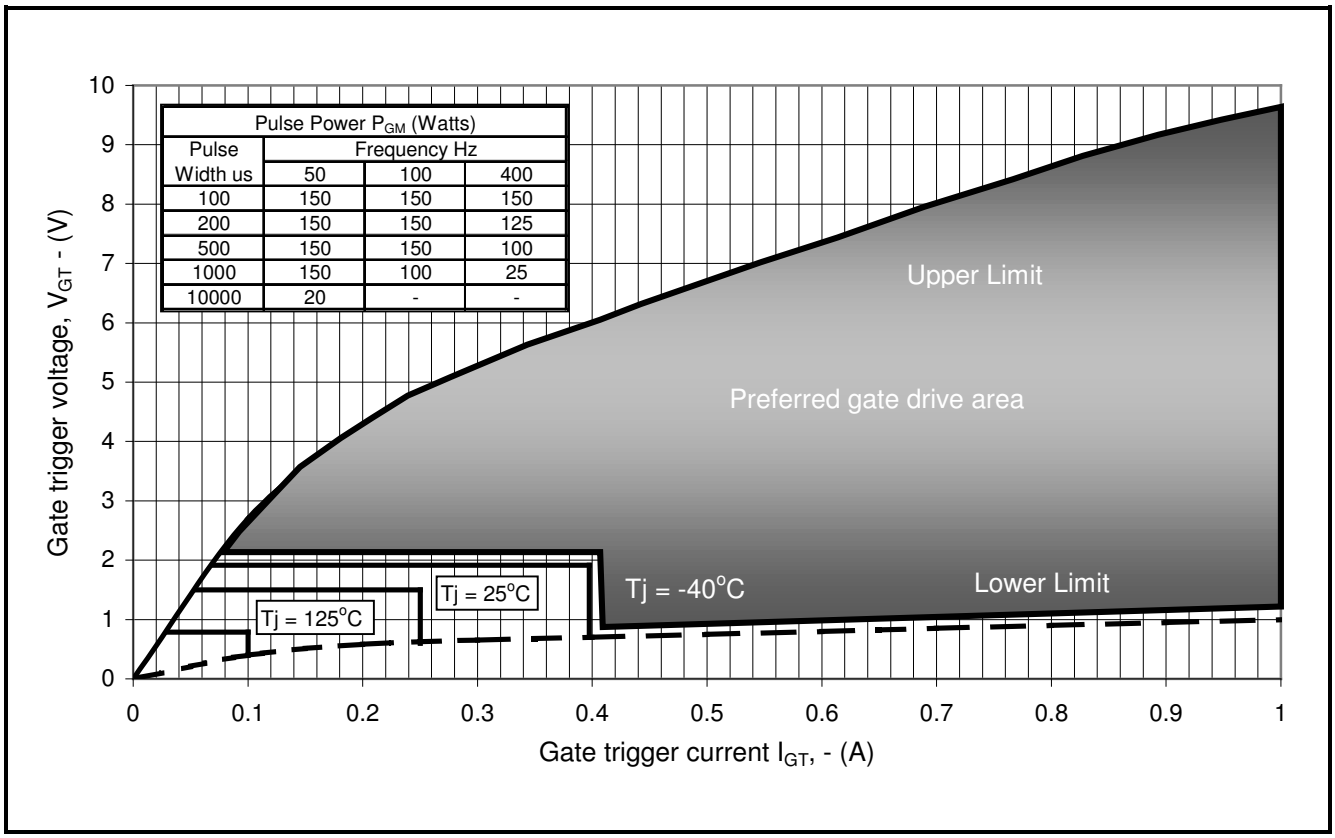


Fig12 Gate Characteristics

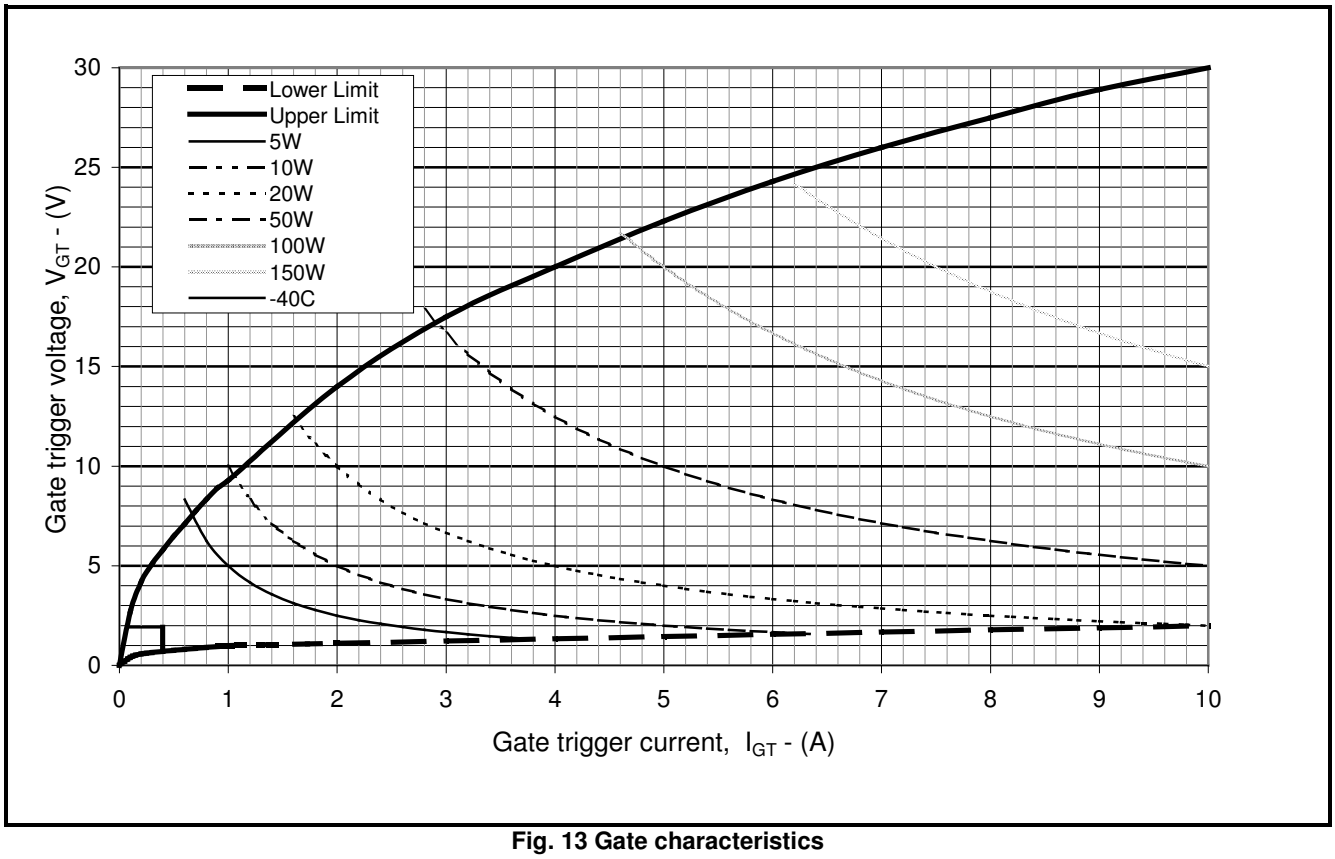
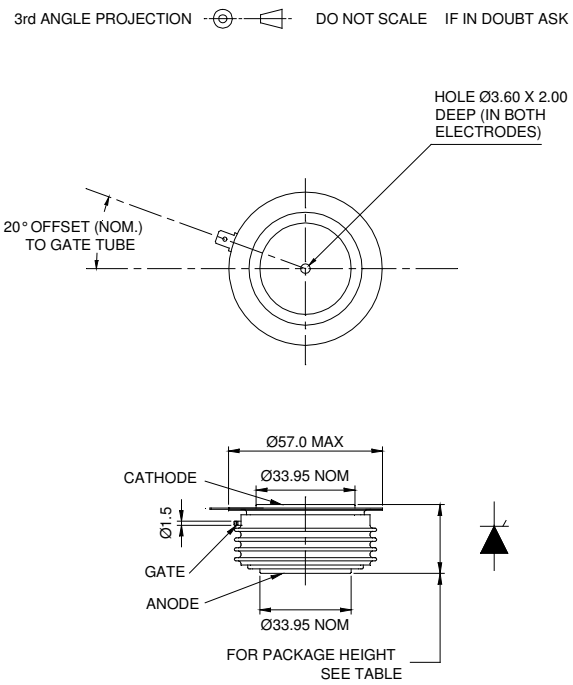


Fig. 13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR803SG18	26.415	25.865
DCR806SG28	26.49	25.94
DCR818SG48	26.84	26.17
DCR820SG65	27.1	26.55
DCR1080G22	26.415	25.865
DCR960G26	**26.49**	**25.94**
DCR780G42	26.72	26.17
DCR690G52	26.84	26.29
DCR590G65	27.1	26.55
DCR470G85	27.46	26.91

Clamping force: 11.5 kN ±10%
Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: G

Fig.14 Package outline