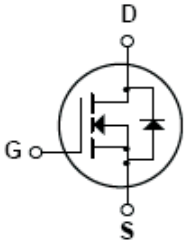
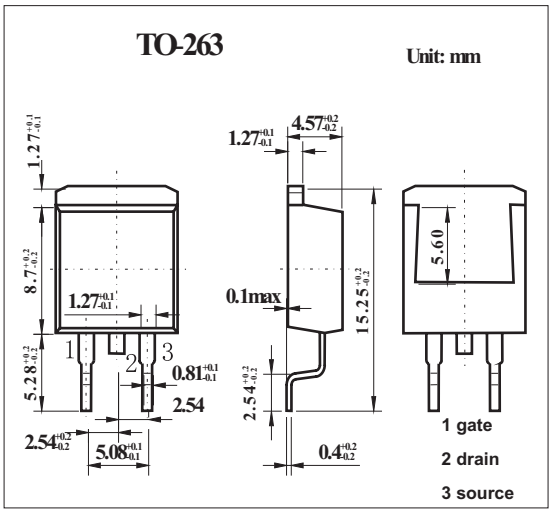
500V N-Channel MOSFET
KQB2N50

Features

- 2.1A, 500 V. $R_{DS(ON)}$ = 5.3Ω @ V_{GS} = 10 V
- Low gate charge (typical 6.0nC)
- Low Crss(typical 4.0pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	500	V
Drain Current Continuous (Tc=25℃)	I_D	2.1	A
Drain Current Continuous (Tc=100℃)		1.33	A
Drain Current Pulsed *1	I_{DM}	8.4	A
Gate-Source Voltage	V_{GSS}	±30	V
Single Pulsed Avalanche Energy*2	E_{AS}	120	mJ
Avalanche Current *1	I_{AR}	2.1	A
Repetitive Avalanche Energy *1	E_{AR}	5.5	mJ
Peak Diode Recovery dv/dt *3	dv/dt	4.5	V/ns
Power dissipation @ Ta=25℃	P_D	3.13	W
Power dissipation @ Tc=25℃	P_D	55	W
Derate above 25℃		0.44	W/℃
Operating and Storage Temperature	T_J, T_{STG}	-55 to150	℃
Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds	T_L	300	℃
Thermal Resistance Junction to Case	$R_{\theta JC}$	2.27	℃/W
Thermal Resistance Junction to Ambient *4	$R_{\theta JA}$	40	℃/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	℃/W

*1 Repetitive Rating:Pulse width limited by maximum junction temperature

*2 l=50mH,I_{AS}=2.1A,V_{DD}=50V,R_G=25Ω,Startion T_J=25℃

*3 I_{SD}≤2.1A,di/dt≤200A/μS,V_{DD}≤B_{VDSS},Startiong T_J=25℃

*4 When mounted on the minimum pad size recommended (PCB Mount)

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 250 μA	500			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		0.48		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			1	μA
		V_{DS} = 400 V, T_C=125℃			10	μA
Gate-Body Leakage Current,Forward	I_{GSSF}	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
Gate-Body Leakage Current,Reverse	I_{GSSR}	V_{GS} =-30 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3.0		5.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.05A		4.2	3.7	Ω
Forward Transconductance	g_{FS}	V_{DS} = 50 V, I_D = 1.05A *		1.45		S
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V,f = 1.0 MHz		180	230	pF
Output Capacitance	C_{oss}			30	40	pF
Reverse Transfer Capacitance	C_{rss}			4	6	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 2.1A,RG=25Ω *		6	20	ns
Turn-On Rise Time	tr			25	60	ns
Turn-Off Delay Time	$t_{d(off)}$			10	30	ns
Turn-Off Fall Time	tf			20	50	ns
Total Gate Charge	Q_g	V_{DS} = 400 V, I_D = 2.1A,V_{GS} = 10 V *		6.0	8.0	nC
Gate-Source Charge	Q_{gs}			1.3		nC
Gate-Drain Charge	Q_{gd}			3.0		nC
Maximum Continuous Drain-Source Diode Forwrad Current	I_S				2.1	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				8.4	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.1 A *			1.4	V
Diode Reverse Recovery Time	trr	V_{GS} = 0 V,dI_F/dt = 100 A/μs,I_S=2.1A		195		ns
Diode Reverse Recovery Current	Qrr			0.69		μC

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%