High Performance, Triple-Output, Auto-Tracking Combo Controller

FEATURES

- Provides Three Accurately Regulated Output Voltages
- Optimized Voltage-Mode PWM Control
- Dual N-Channel MOSFET Synchronous Drivers
- Fast Transient Response
- Adjustable Over-Current Protection Using External MOSFET $R_{DS(ON)}$ - No External Current Sense Resistors Required.
- Programmable Soft Start Function
- 200KHz Free-Running Oscillator
- Robust Output Auto-Tracking Characteristics
- Sink and Source Capabilities with External Circuit

APPLICATIONS

- Advanced PC motherboards
- Information PCs
- Servers and Workstations
- Internet Appliances
- LCD Monitor
- PC Add-On Cards
- DDR Termination

GENERAL DESCRIPTION

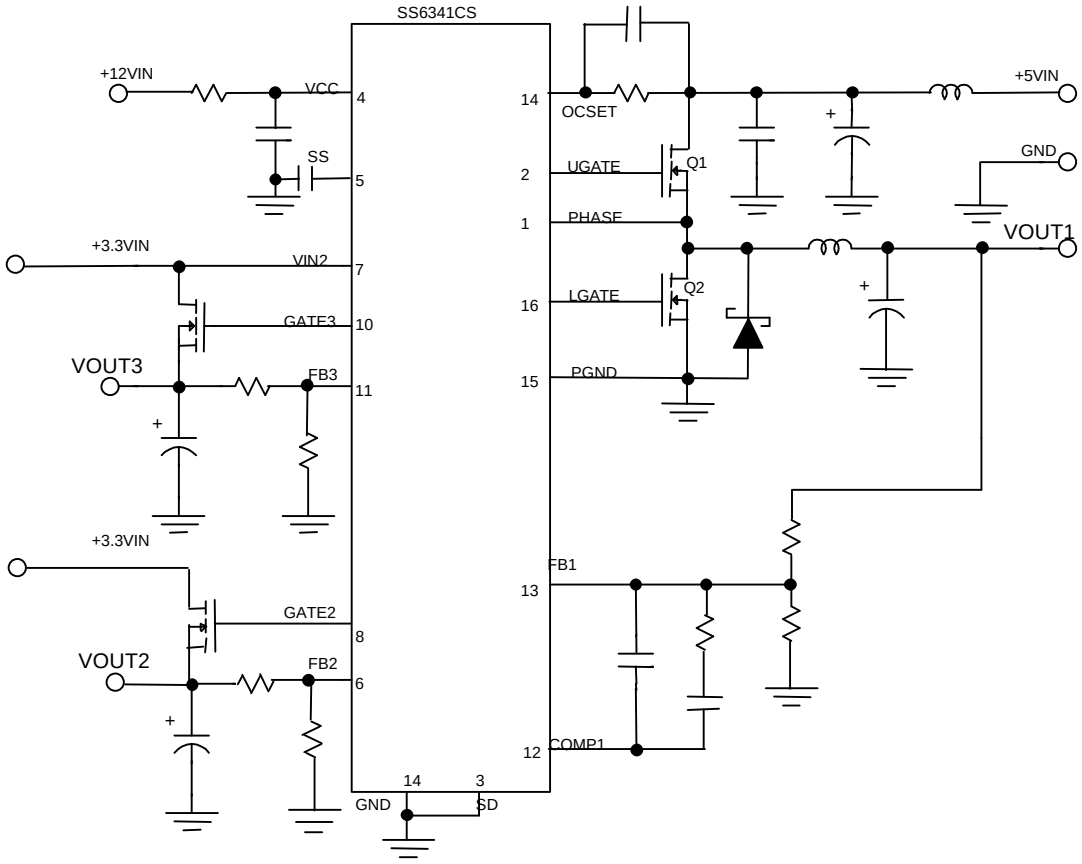
The SS6341 combines a synchronous voltage-mode PWM controller with two linear controllers, including the associated monitoring and protection functions. It is able to power CPUs, GPUs, memories, chipsets and multi-voltage applications. The PWM controller regulates the output voltage using a synchronous rectified step-down converter. The built-in N-Channel MOSFET drivers also help to simplify the design of the step-down converter. The PWM controller features over-current protection using the $R_{DS(ON)}$ of the external MOSFET, improving efficiency and cost, as there is no expensive current sense resistor required.

Two built-in adjustable linear controllers drive external MOSFETs to form two linear regulators that regulate power for multiple system I/Os. The output voltage of both linear regulators can also be adjusted by means of an external resistor divider. Both linear regulators feature current-limiting. For system I/Os requiring current less than 500mA, the SS6340 is recommended as it saves one external MOSFET.

The programmable soft-start design provides a controlled output voltage rise, which limits the current during power-on.

A shutdown function is also provided, for disabling the combo controller.

TYPICAL APPLICATION CIRCUIT



Typical Application with Three Outputs

ORDERING INFORMATION

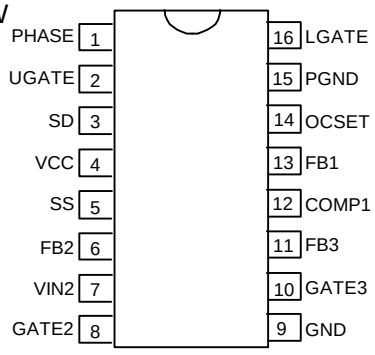
SS6341CXXX

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  S: SMALL OUTLINE

Example: SS6341CSTR
→ in SO-16 Package shipped in Tape & Reel Packing

PIN CONFIGURATION

SO-16
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 15V
UGATE ..... GND - 0.3V to V_{CC} + 0.3V
LGATE ..... GND - 0.3V to V_{CC} + 0.3V
Input Output and I/O Voltage ..... GND - 0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range ..... 0° C to 85°C
Maximum Operating Junction Temperature ..... 100°C
Supply Voltage, VCC ..... 15V±10%

Thermal Information

Thermal Resistance θ_{JA} (°C/W)

SOIC Package ..... 100°C/W
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

TEST CIRCUIT

Refer to the APPLICATION CIRCUIT on page 14.

ELECTRICAL CHARACTERISTICS (V_{cc}=12V, T_J=25°C, Unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC SUPPLY CURRENT						
Supply Current	UGATE, LGATE, GATE2 and GATE3 open	I_{CC}		1.8	5	mA
POWER ON RESET						
Rising VCC Threshold	V_{OCSET}=4.5V	VCC_{THR}	8.6	9.5	10.4	V
Falling VCC Threshold	V_{OCSET}=4.5V	VCC_{THF}	8.2	9.2	10.2	V
Rising VIN2 Under-Voltage Threshold		$VIN2_{THR}$	2.5	2.6	2.7	V
VIN2 Under-Voltage Hysteresis		$VIN2_{HYS}$		130		mV
Rising V_{OCSET1} Threshold		V_{OCSETH}		1.3		V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
OSCILLATOR and REFERENCE						
Free Running Frequency		F	170	200	230	KHz
FB1 Reference Voltage		V_{REF1}	1.287	1.300	1.313	V
FB2 Reference Voltage		V_{REF2}	1.245	1.270	1.295	V
FB3 Reference Voltage		V_{REF3}	1.250	1.275	1.300	V
LINEAR CONTROLLER						
Regulation	$0 < I_{GATE2/3} < 10mA$		-2.5		+2.5	%
Under-Voltage Level	FB2/3 falling	$FB2/3_{UV}$		70	80	%
PWM CONTROLLER ERROR AMPLIFIER						
DC GAIN				76		dB
Gain Bandwidth Product		GBWP		11		MHz
Slew Rate	COMP1=10pF	SR		6		V/µS
PWM CONTROLLER GATE DRIVER						
Upper Drive Source	VCC=12V, V_{UGATE}=11V	R_{UGH}		5.2	6.5	Ω
Upper Drive Sink	VCC=12V, V_{UGATE} =1V	R_{UGL}		3.3	5	Ω
Lower Drive Source	VCC=12V, V_{LGATE}=11V	R_{LGH}		4.1	6	Ω
Lower Drive Sink	VCC=12V, V_{LGATE}=1V	R_{LGL}		3	5	Ω
PROTECTION						
Soft-Start Current		I_{SS}		11		µA
Chip Shutdown Soft Start Threshold					1.0	V

PIN DESCRIPTIONS

Pin 1: PHASE: Over-current detection pin. Connect to the source of the external high-side N-MOSFET. This pin detects the voltage drop across the high-side N-MOSFET $R_{DS(ON)}$ for over-current protection.

Pin 2: UGATE: External high-side N-MOSFET gate drive pin. Connect to the gate of the external high-side N-MOSFET.

Pin 3: SD: To shut down the system, active high or floating. If connecting a resistor to ground, keep the resistor less than 4.7KΩ.

Pin 4: VCC: The chip power supply pin. It also provides the gate bias charge for all the MOSFETs controlled by the IC. Recommended supply voltage is 12V.

Pin 5: SS: Soft-start pin. Connect a capacitor from this pin to ground. This capacitor, along with an internal 10μA (typically) current source, sets the soft-start interval of the converter. Pulling this pin low will shut down the IC.

Pin 6: FB2: Connect this pin to a resistor divider to set the linear regulator output voltage.

Pin 7: VIN2: Connect this pin to a suitable 3.3V source. Additionally, this pin is used to monitor the 3.3V supply. If the voltage drops below 2.6V (typically) following a start-up cycle, the chip shuts down. A new soft-start cycle is initiated upon the return of the 3.3V supply above the under-voltage threshold.

Pin 8: GATE2: Linear Controller output drive pin. This pin can drive either a Darlington NPN transistor or an N-channel MOSFET.

Pin 9: GND: Signal GND for IC. All voltage levels are measured with respect to this pin.

Pin 10: GATE3: Linear Controller output drive pin. This pin can drive either a Darlington NPN transistor or an N-channel MOSFET.

Pin 11: FB3 Negative feedback pin for the linear controller error amplifier. Connect this pin to a resistor divider to set the linear controller output voltage.

Pin 12: COMP1 External compensation pin. Connect to the error amplifier output and PWM comparator. An RC network is connected to FB1 to compensate the voltage control feedback loop of the converter.

Pin 13: FB1 The error amplifier inverting input pin. The FB1 pin and COMP1 pin are used to compensate the voltage-control feedback loop.

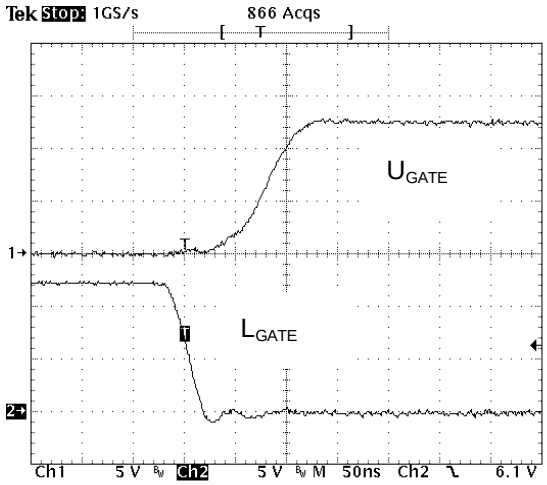
Pin 14: OCSET: Current limit sense pin. Connect a resistor R_{OCSET} from this pin to the drain of the external high-side N-MOSFET. R_{OCSET}, an internal 200μA current source (I_{OCSET}), and the upper N-MOSFET on-resistance ($R_{DS(ON)}$) set the over-current trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

Pin 15: PGND: Driver power GND pin. Connect to a low impedance ground plane close to the lower N-MOSFET source.

Pin 16: LGATE: Lower N-MOSFET gate drive pin.

TYPICAL PERFORMANCE CHARACTERISTICS



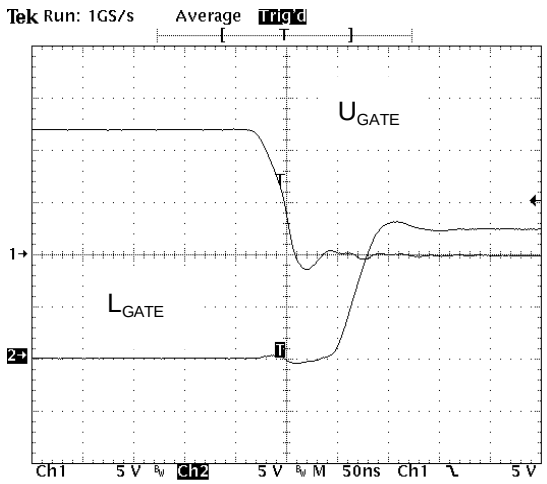


FIG.1 The gate drive waveforms

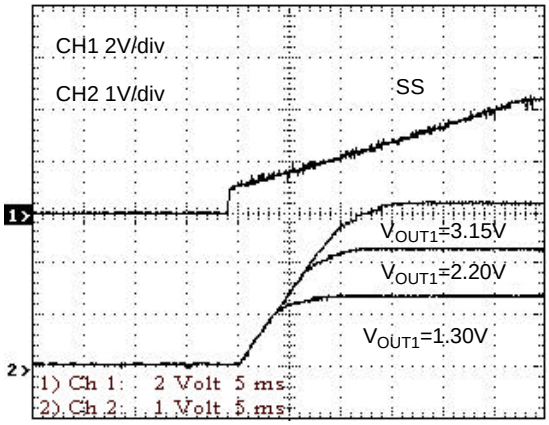


FIG. 2 Soft Start Initiates PWM Output

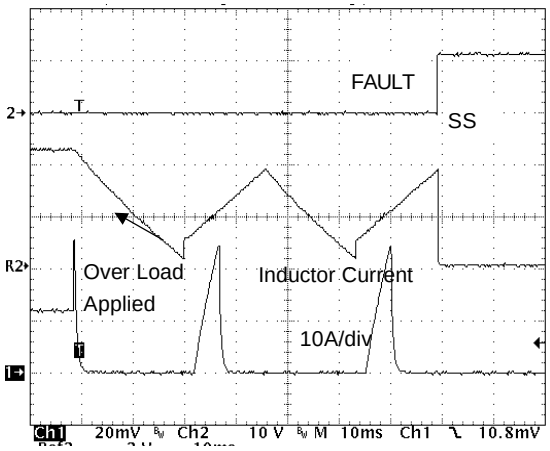


FIG. 3 Over-Current Operation on Inductor

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

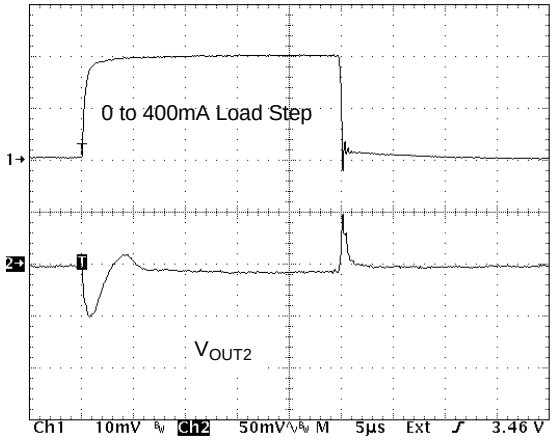


FIG. 4 Transient Response of Linear Regulator

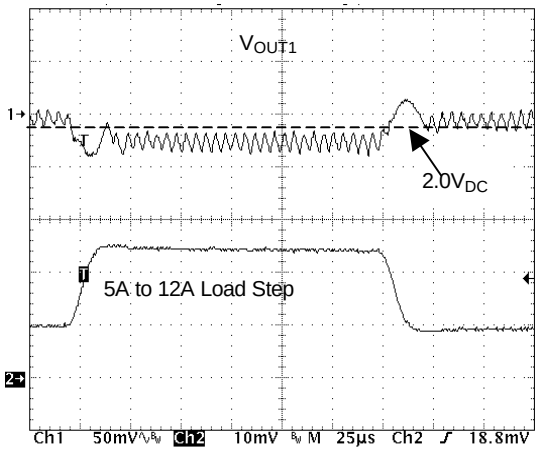


FIG. 5 Transient Response of PWM Output

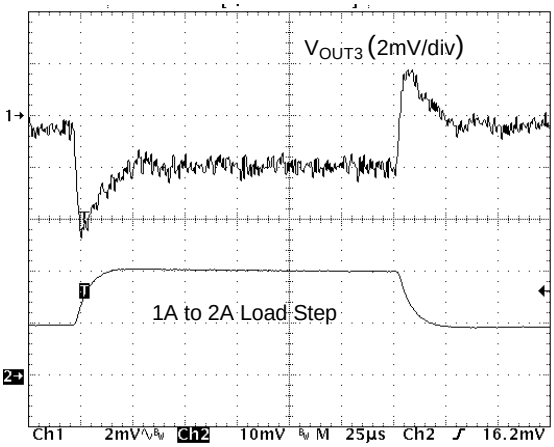


FIG. 6 Transient Response of Linear Controller

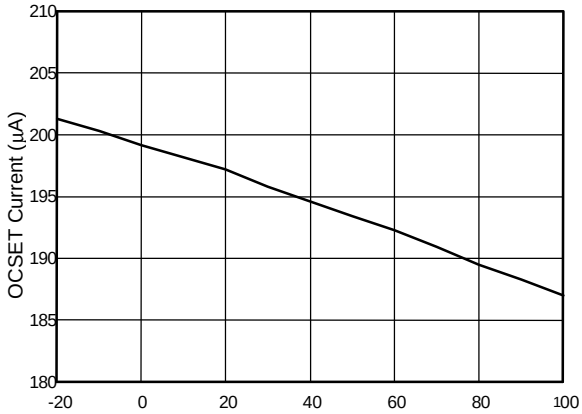


FIG.7 OCSET Current vs.Temperature (°C)

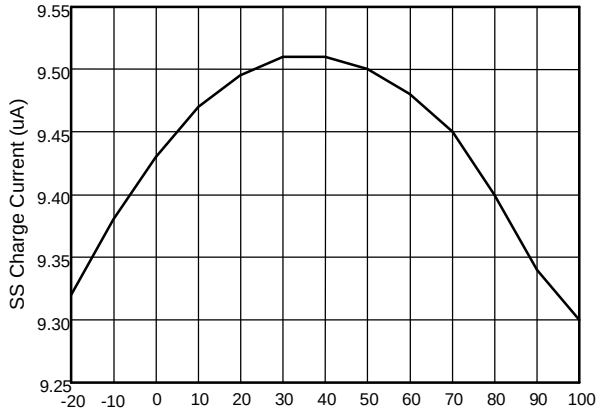


FIG.8 SS Current vs. Temperature (°C)

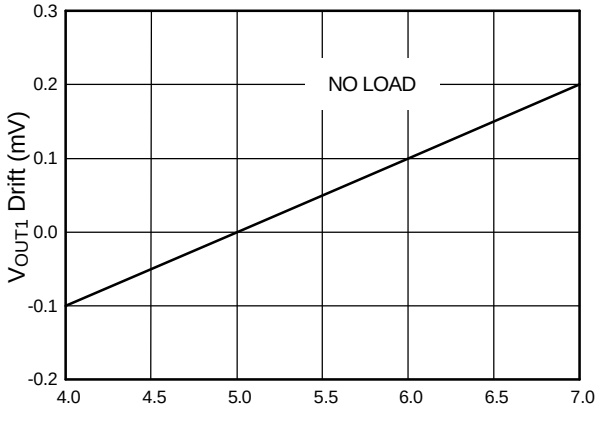
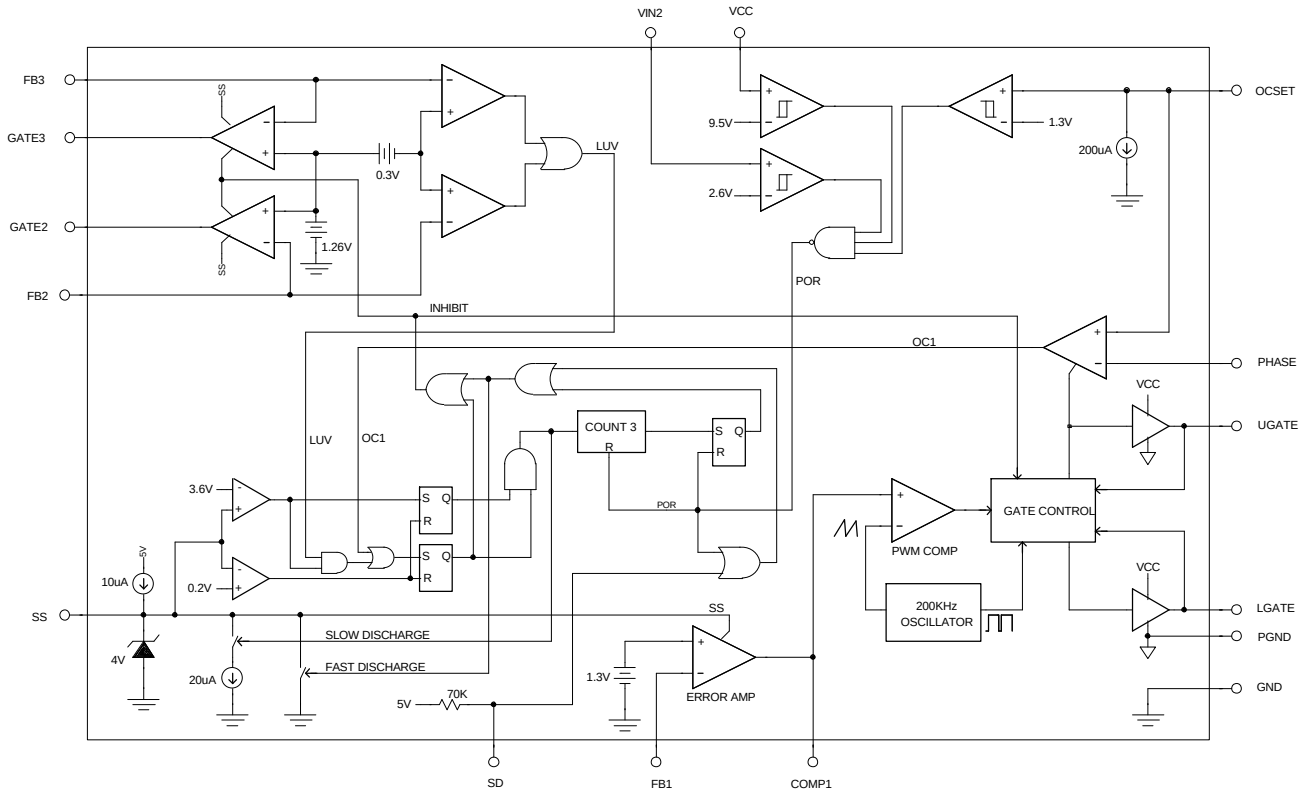


FIG.9 V_{OUT1} Drift vs. VIN (V)

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The SS6341 is designed for applications with multiple voltage demand. This IC has one PWM controller and two linear controllers. The PWM controller is designed to regulate the voltage (V_{OUT1}) by driving 2 MOSFETs (through U_{GATE} and L_{GATE}) in a synchronous rectified buck converter configuration. The regulated voltage level is decided by a resistor divider network.

The Power-On Reset (POR) function continually monitors the +12V input supply voltage at VCC pin, the 5V input voltage at OCSET pin, and the 3.3V input at VIN2 pin. The POR function initiates soft-start operation after all three input supply voltage exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. Initially, the voltage on the SS pin rapidly increases to approximate 1V. Then an internal 10µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. As the SS pin voltage slews from 1V to 4V, the PWM error amplifier reference input (non-inverting terminal) and output (COMP1 pin) are clamped to a level proportional to the SS pin voltage. As the SS pin voltage slews from 1V to 4V, the output clamp generates PHASE pulses of increasing width that charge the output capacitors. Additionally both linear regulators' reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a controlled smooth rise in output voltage.

Fig. 2 shows the soft-start sequence for a typical application. The internal oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse width on the PHASE pin increases. The period of increasing pulse

width continues until the output reaches sufficient voltage to transfer control to the input reference clamp.

Each linear output (V_{OUT2} and V_{OUT3}) initially follows a ramp. When each output reaches sufficient voltage, the input reference clamp slows the rate of output voltage rise.

Over-Current Protection

All outputs are protected against excessive over-current. The PWM controller uses the upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. Both the linear regulator and controller monitor FB2 and FB3 for under-voltage to protect against excessive current.

When the voltage across Q1 (I_D x $R_{DS(ON)}$) exceeds the level (200µA x R_{OCSET}), this signal inhibits all outputs, discharges the soft-start capacitor (C_{ss}) with 10µA current sink, and increments the counter. Css recharges and initiates a soft-start cycle again until the counter increments to 3. This sets the fault latch to disable all outputs. Fig. 3 illustrates the over-current protection for an over load on OUT1.

Should excessive current cause FB2 or FB3 to fall below the linear under-voltage threshold, the LUV signal sets the over-current latch if Css is fully charged. Cycling the bias input power off then on resets the counter and the fault latch.

The over-current function for the PWM controller will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The OC trip point varies with the MOSFET's temperature. To avoid over-current tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $R_{DS(ON)}$ at the highest junction.
2. The minimum I_{OCSET} from the specification table.
3. Ensure $I_{PEAK} > I_{OUT(MAX)}$ + (inductor ripple current) /2.

Shutdown

Compatible with TTL logic levels, holding the SD (pin3) pin low will activate the controller. If connecting a resistor to ground, make sure the resistor is less than 4.7KΩ for normal operation.

Layout Considerations

Any inductance in the switched current path generates a large voltage spike during the switching interval. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component selection and tight layout of critical components using short, wide metal traces minimizes these voltage spikes.

1) A ground plane should be used. Locate the input capacitors (C_{IN}) close to the power switches. Minimize the loop formed by C_{IN}, the upper MOSFET (Q1) and the lower MOSFET (Q2) as much as possible. Connections should be as wide and as short as possible to minimize loop inductance.

2) The connection between Q1, Q2 and output inductor should be as wide and as short as practical, as this connection has fast voltage transitions and can easily induce EMI.

3) The output capacitor (C_{OUT}) should be located as close to the load as possible. Minimizing the transient load magnitude for high slew rate requires low inductance and resistance in the circuit board.

4) The SS6341 is best placed over a quiet ground plane area. The GND pin should be connected to the groundside of the output capacitors. Under no circumstances should GND be returned to a ground inside the C_{IN}, Q1, and Q2 loop. The GND and PGND pins should be shorted right at the IC. This helps to minimize internal ground disturbances in the IC and prevents differences in ground potential from disrupting the internal circuit operation.

5) The wiring traces from the control IC to the MOSFET gate and source should be sized to carry a current of 1A. Locate C_{OUT2} close to the SS6341.

6) The Vcc pin should be decoupled directly to GND by a 1µF ceramic capacitor; trace lengths should be as short as possible.

A multi-layer printed circuit board is recommended. Figure 10 shows the connections of the critical components in the converter. The C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer.

PWM Output Capacitors

The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demand.

The ESR (equivalent series resistance) and ESL (equivalent series inductance) parameters determine the buck capacitor values, rather than actual capacitance. For a given transient load magnitude, the output voltage transient change due to the output capacitor can be found from the following equation:

$$\Delta V_{OUT} = ESR \times \Delta I_{OUT} + ESL \times \frac{\Delta I_{OUT}}{\Delta T}$$

where ΔI_{OUT} is the transient load current step.

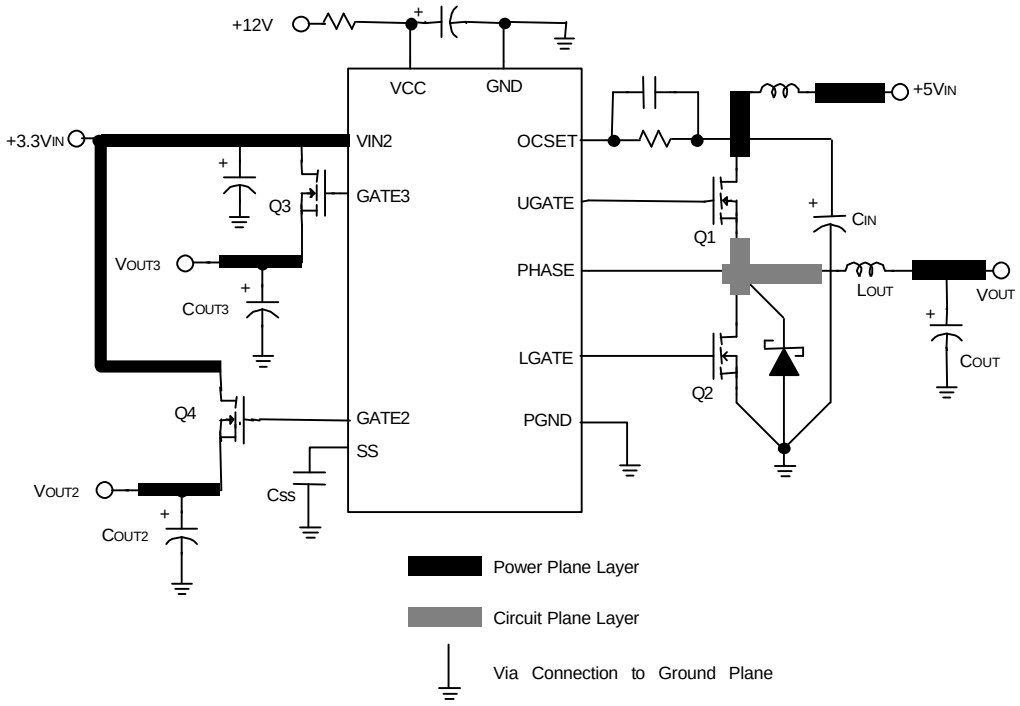


Fig. 10 Printed circuit board power planes and islands

After the initial transient, the ESL dependent term drops off. Because of the strong relationship between output capacitor ESR and output load transient, the output capacitor is usually chosen for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. In most case, multiple electrolytic capacitors of small case size are better than a single large case capacitor.

Output Inductor Selection

The inductor value and type should be chosen based on output slew rate requirement, output ripple requirement and expected peak current, and is primarily controlled by the required current response time. The SS6341 will provide either 0% or 85% duty cycle in response to a load transient. The response time to a transient is different for the application of load and remove of load.

$$t_{RISE} = \frac{L \times \Delta I_{OUT}}{V_{IN} - V_{OUT}}, \quad t_{FALL} = \frac{L \times \Delta I_{OUT}}{V_{OUT}}$$

where ΔI_{OUT} is transient load current step.

In a typical 5V input, 2V output application, a 3μH inductor has a 1A/μS rise time, resulting in a 5μS delay in responding to a 5A load current step. To optimize performance, different combinations of input and output voltage and expected loads may require different inductor values. A smaller value of inductor will improve the transient response at the expense of increased output ripple voltage and inductor core saturation rating.

Peak current in the inductor will be equal to the maximum output load current plus half of inductor ripple current. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f \times L \times V_{IN}}$$

where f = 200KHz oscillator frequency.

The inductor must be able to withstand peak current without saturation, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss

Input Capacitor Selection

Most of the input supply current is supplied by the input bypass capacitor, and the resulting RMS current flow in the input capacitor will heat it up. Use a mix of input bulk capacitors to control the voltage overshoot across the upper MOSFET. The ceramic capacitance for the high frequency decoupling should be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedance. The buck capacitors to supply the RMS current are approximate equal to:

$$I_{RMS} = (1-D) \times \sqrt{D} \times \sqrt{I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{IN} \times D}{f \times L}\right)^2}$$

where $D = \frac{V_{OUT}}{V_{IN}}$

The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage.

PWM MOSFET Selection

In high current PWM application, the MOSFET power dissipation, package type and heatsink are the dominant design factors. The conduction loss is the only component of power dissipation for the lower MOSFET, since it turns on into near zero voltage. The upper MOSFET has conduction loss and switching loss. The gate charge losses are proportional to the switching frequency and are dissipated by the SS6341. However, the gate charge increases the switching interval, t_{SW}, which increase the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

$$P_{UPPER} = I_{OUT}{}^2 \times R_{DS(ON)} \times D + \frac{I_{OUT} \times V_{IN} \times t_{SW} \times f}{2}$$

$$P_{LOWER} = I_{OUT}{}^2 \times R_{DS(ON)} \times (1-D)$$

The equations above do not model the power loss from the reverse recovery of the lower MOSFET's body diode.

The $R_{DS(ON)}$ is different for the two previous equations

even if the same device type is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Logic level MOSFETs should be selected based on on-resistance considerations. $R_{DS(ON)}$ should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. Power dissipation should be calculated based primarily on required efficiency or allowable thermal dissipation.

A Schottky diode is used as a clamp to prevent the parasitic MOSFET body diode from conducting during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode's rated reverse breakdown voltage must be greater than twice the maximum input voltage.

Linear Controller MOSFET Selection

The power dissipated in a linear regulator is :

$$P_{LINEAR} = I_{OUT} \times (V_{IN2} - V_{OUT})$$

Select a package and heatsink that maintains junction temperature below the maximum rating while operating at the highest expected ambient temperature.

Linear Output Capacitor

The output capacitors for the linear controller provide dynamic load current. The linear controller uses dominant pole compensation integrated in the error amplifier and is insensitive to output capacitor selection. C_{OUT2} and C_{OUT3} should be selected for transient load regulation.

Notes

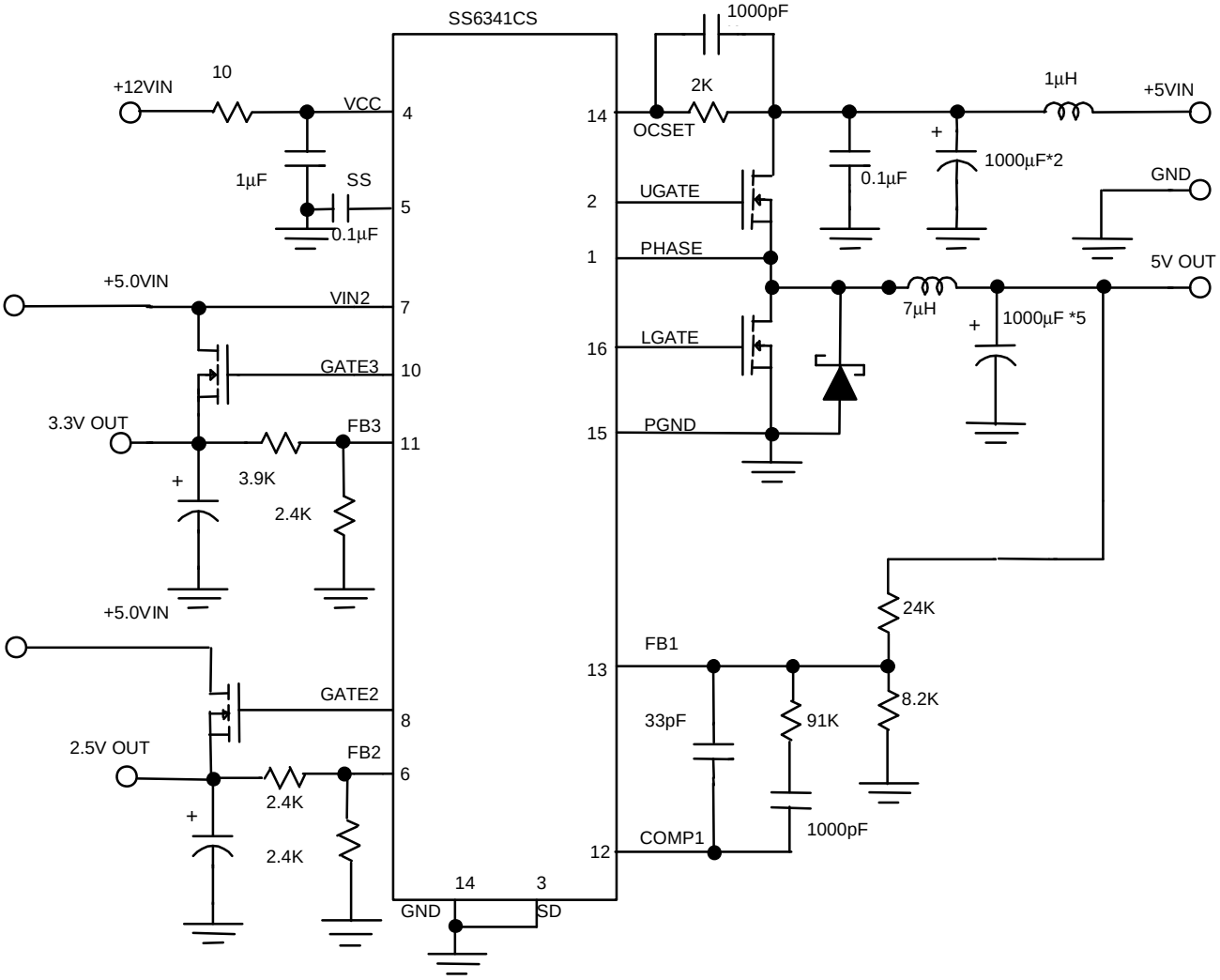
V_{OUT1} - The PWM output

V_{OUT2} - The output of the linear controller managed by FB2 and GATE2

V_{OUT3} - The output of the linear controller managed by FB3 and GATE3

These refer to the **TYPICAL APPLICATION CIRCUITS** on pages 3 and 14.

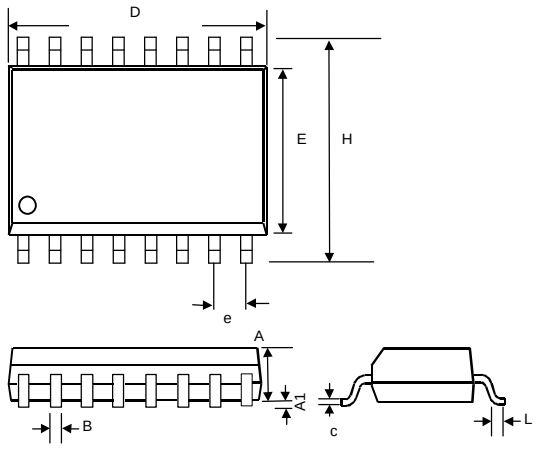
APPLICATION CIRCUIT



Typical Application Circuit for Multiple Outputs

PACKAGE DIMENSIONS

- **16 LEAD PLASTIC SO (300 mil) (unit: mm)**



SYMBOL	MIN	MAX
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27(TYP)	
H	10.00	10.65
L	0.40	1.27