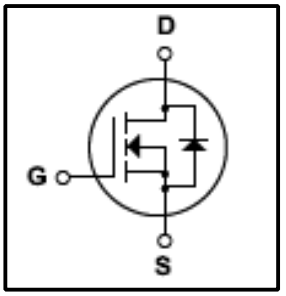
## *Silicon N-Channel MOSFET*




## Features

■2A,600V, $R_{DS(on)}$(Max 5Ω)@$V_{GS}$=10V

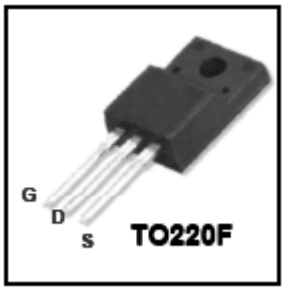
■ Ultra-low Gate Charge(Typical 9.0nC)

■ Fast Switching Capability

■ 100%Avalanche Tested

■ Isolation Voltage ( $V_{ISO}$ = 4000V AC )

■ Maximum Junction Temperature Range(150℃)




## General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, VDMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for high efficiency switch mode power supply.

## Absolute Maximum Ratings

| Symbol | Parameter | | Value | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain Source Voltage | | 600 | V |
| $I_D$ | Continuous Drain Current(@Tc=25℃) | | 2.0* | A |
| | Continuous Drain Current(@Tc=100℃) | | 1.5* | A |
| $I_{DM}$ | Drain Current Pulsed | (Note1) | 9.5* | A |
| $V_{GS}$ | Gate to Source Voltage | | ±30 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 140 | mJ |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 2.8 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 4.5 | V/ns |
| $P_D$ | Total Power Dissipation(@Tc=25℃) | | 23 | W |
| | Derating Factor above 25℃ | | 0.18 | W/℃ |
| $T_J$, $T_{stg}$ | Junction and Storage Temperature | | -55~150 | ℃ |
| $T_L$ | Channel Temperature | | 300 | ℃ |

*Drain current limited by junction temperature

## Thermal Characteristics

| Symbol | Parameter | Value | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | - | - | 5.5 | ℃/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | - | - | 62.5 | ℃/W |

## Electrical Characteristics (Tc = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Type | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | VGS = ±30 V, VDS = 0 V | - | - | ±100 | nA |
| Gate−source breakdown voltage | | $V_{(BR)GSS}$ | IG = ±10 μA, VDS = 0 V | ±30 | - | - | V |
| Drain cut−off current | | $I_{DSS}$ | VDS = 600 V, VGS = 0 V | - | - | 10 | μA |
| | | | VDS = 480 V, Tc = 125℃ | - | - | 100 | μA |
| Drain−source breakdown voltage | | $V_{(BR)DSS}$ | ID = 250 μA, VGS = 0 V | 600 | - | - | V |
| Gate threshold voltage | | $V_{GS(th)}$ | VDS = 10 V, ID =250 μA | 2 | - | 4 | V |
| Drain−source ON resistance | | $R_{DS(ON)}$ | VGS = 10 V, ID =0.8A | - | 4.3 | 5 | Ω |
| Forward Transconductance | | gfs | VDS = 50 V, ID =0.8A | - | 2.0 | - | S |
| Input capacitance | | $C_{iss}$ | VDS = 25 V, | - | 270 | 350 | pF |
| Reverse transfer capacitance | | $C_{rss}$ | VGS = 0 V, | - | 6 | 8 | |
| Output capacitance | | $C_{oss}$ | f = 1 MHz | - | 40 | 50 | |
| Switching time | Rise time | tr | VDD =300 V, | - | 10 | 30 | ns |
| | Turn−on time | ton | ID = 2.0 A | - | 25 | 60 | |
| | Fall time | tf | RG=25 Ω | - | 20 | 50 | |
| | Turn−off time | toff | (Note4,5) | - | 25 | 60 | |
| Total gate charge (gate−source plus gate−drain) | | Qg | VDD = 320 V, | - | 9.0 | 11 | nC |
| Gate−source charge | | Qgs | VGS = 10 V, | - | 1.6 | - | |
| Gate−drain (“miller”) Charge | | Qgd | ID = 6.5 A (Note4,5) | - | 4.3 | - | |

## Source−Drain Ratings and Characteristics (Ta = 25°C)

| Characteristics | Symbol | Test Condition | Min | Type | Max | Unit |
|---|---|---|---|---|---|---|
| Continuous drain reverse current | $I_{DR}$ | - | - | - | 2.0 | A |
| Pulse drain reverse current | $I_{DRP}$ | - | - | - | 9.5 | A |
| Forward voltage (diode) | $V_{DSF}$ | IDR = 2 A, VGS = 0 V | - | - | 1.4 | V |
| Reverse recovery time | trr | IDR = 2.0A, VGS = 0 V, | - | 180 | - | ns |
| Reverse recovery charge | Qrr | dIDR / dt = 100 A / μs | - | 0.72 | - | μC |

Note 1.Repeativity rating :pulse width limited by junction temperature
2.L=18.5mH,$I_{AS}$=2.0A,$V_{DD}$=50V,$R_G$=0Ω,Starting $T_J$=25℃
3.$I_{SD}$≤2.0A,di/dt≤200A/us, $V_{DD}$<$BV_{DSS}$,STARTING TJ=25℃
4.Pulse Test: Pulse Width≤300us,Duty Cycle≤2%
5.Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

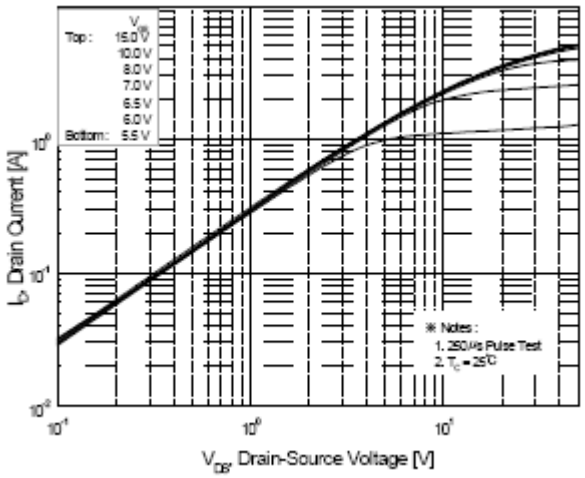



**Fig. 1 On-State Characteristics**

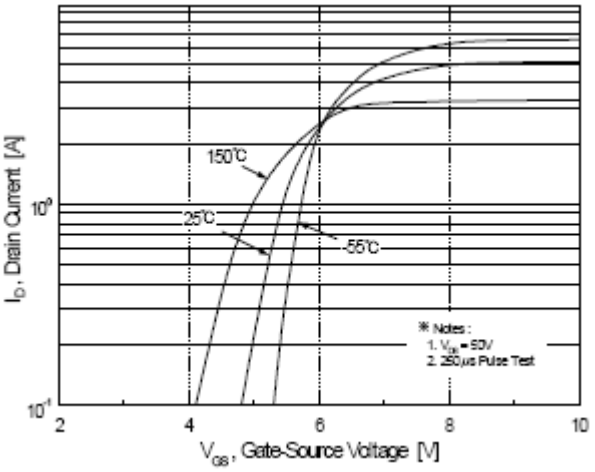



**Fig.2 Transfer Current Characteristics**

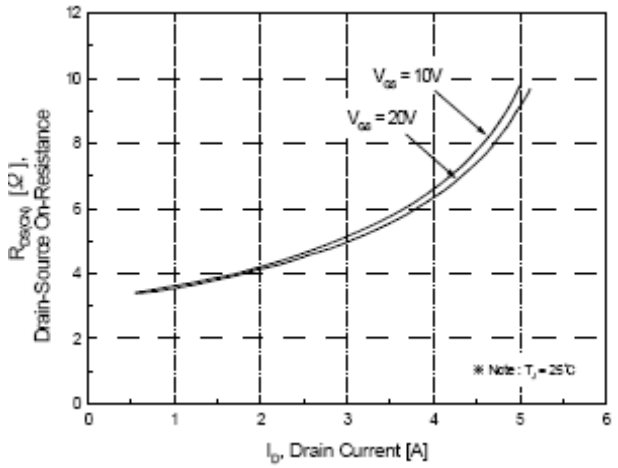



**Fig.3 On-Resistance Variation vs Drain Current**

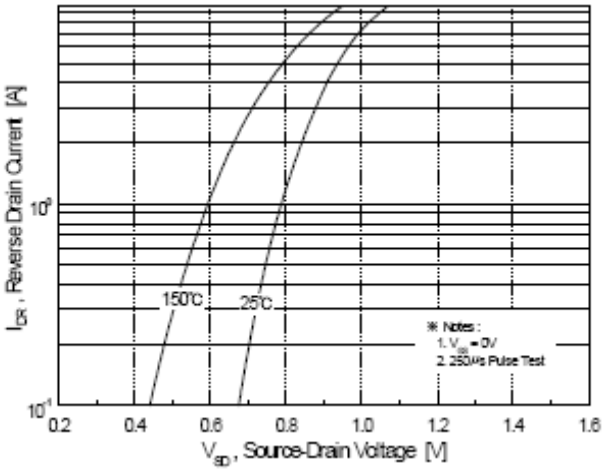



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

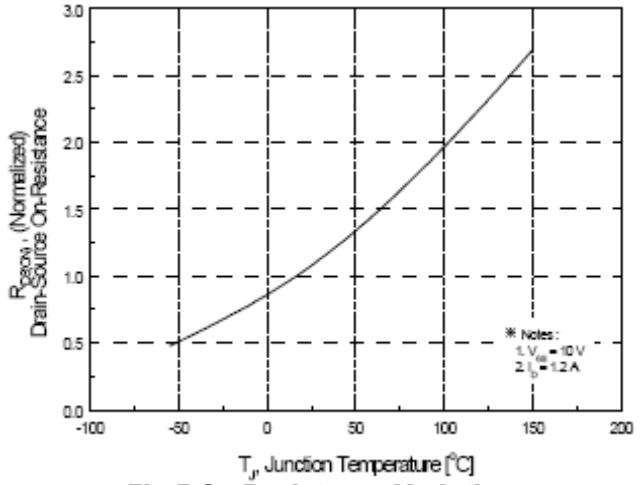



**Fig.5 On-Resistance Variation vs Junction Temperature**

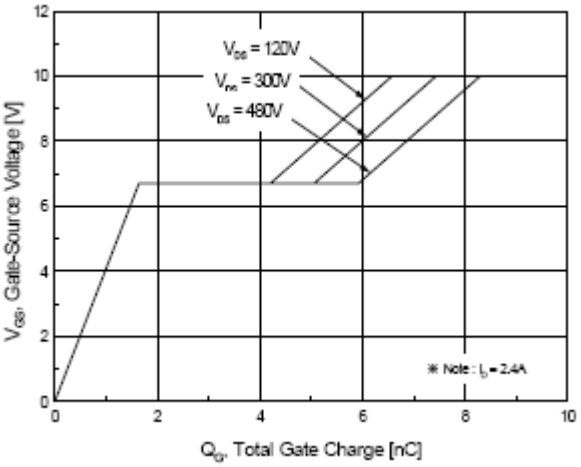



**Fig.6 Gate Charge Characteristics**

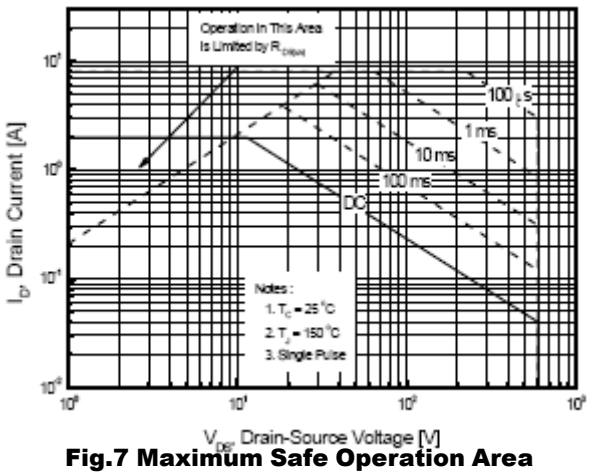



**Fig.7 Maximum Safe Operation Area**

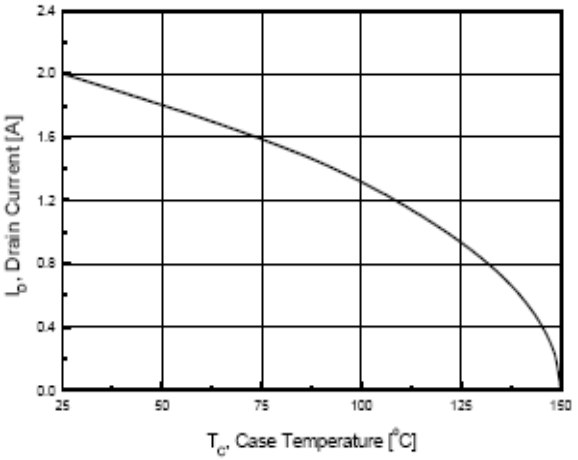



**Fig.8 Maximum Drain Current vs Case Temperature**

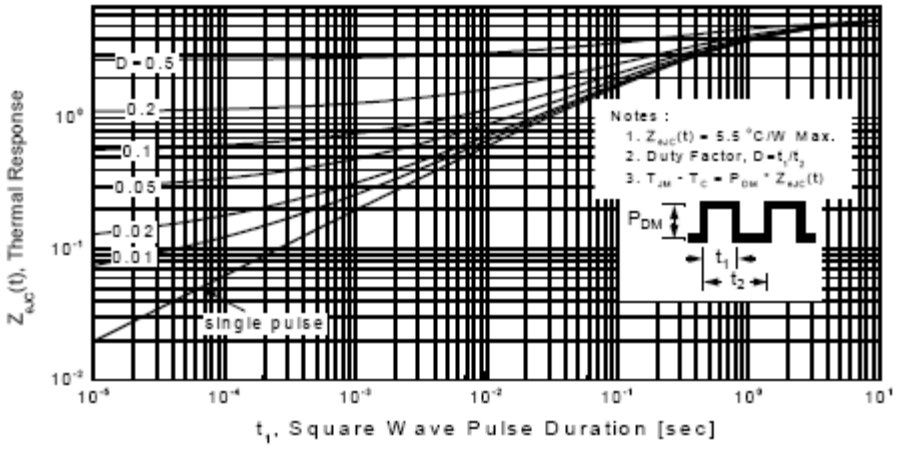



**Fig.9 Transient Thermal Response Curve**

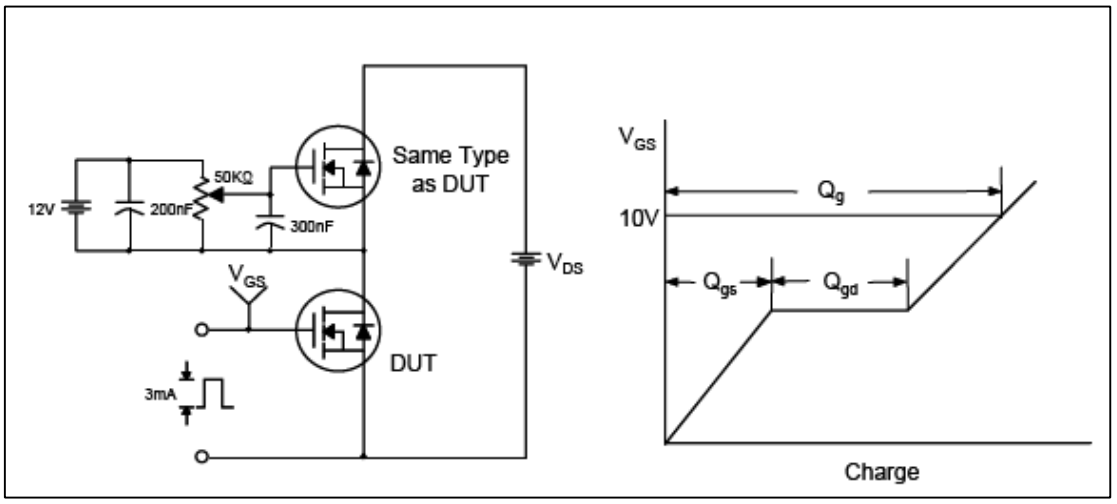



**Fig.10 Gate Test Circuit & Waveform**

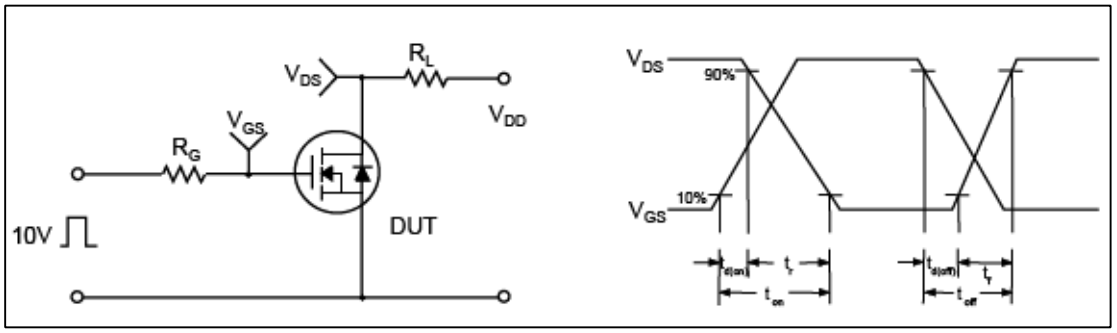



**Fig.11 Resistive Switching Test Circuit & Waveform**

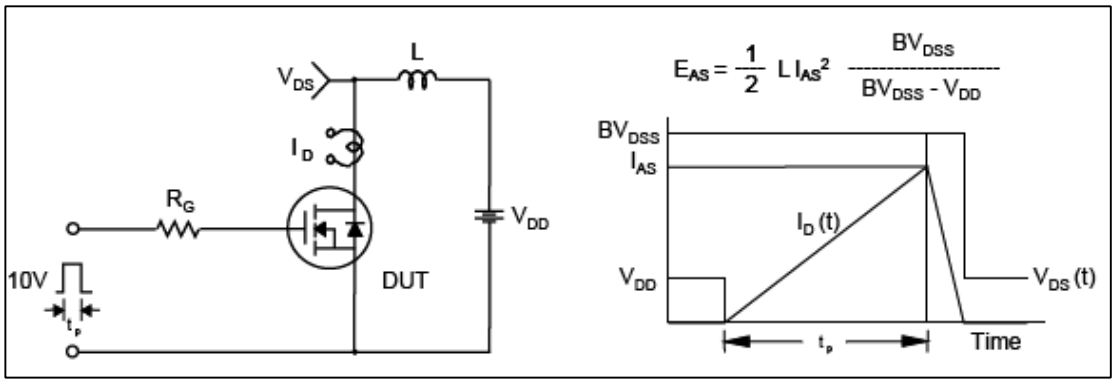



**Fig.12 Unclamped Inductive Switching Test Circuit & Waveform**

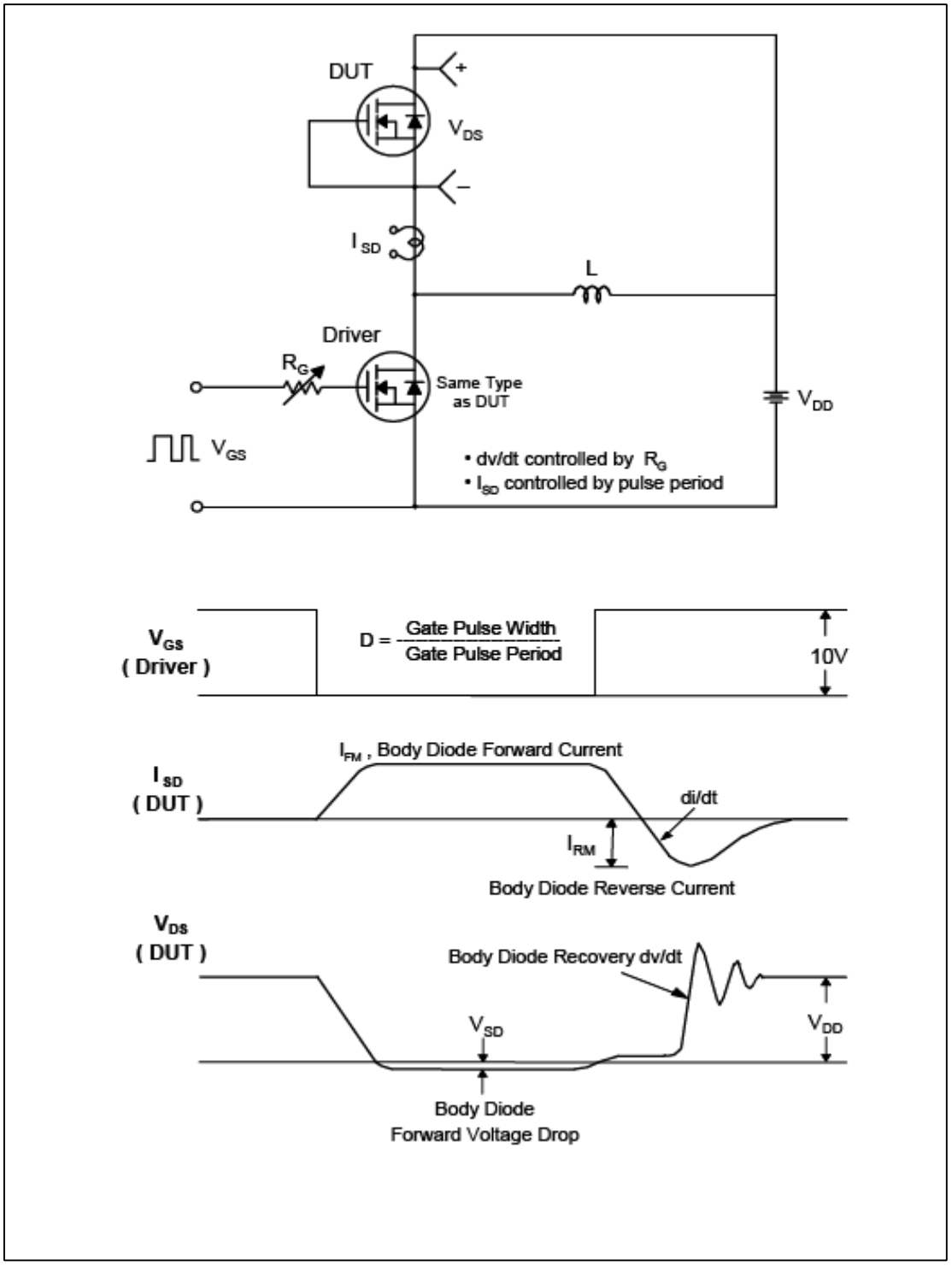



**Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform**

## TO-220F Package Dimension