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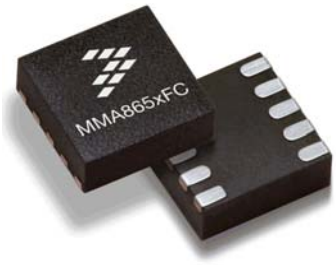
RoHS

Xtrinsic MMA8653FC 3-Axis, 10-bit Digital Accelerometer

MMA8653FC

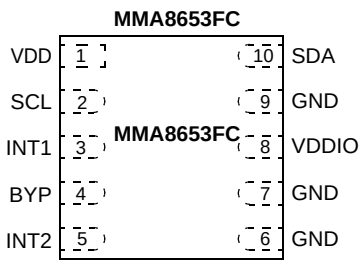
The MMA8653FC is an intelligent, low-power, three-axis, capacitive micromachined accelerometer with 10 bits of resolution. This accelerometer is packed with embedded functions with flexible user programmable options, configurable to two interrupt pins. Embedded interrupt functions enable overall power savings, by relieving the host processor from continuously polling data. There is access to either low-pass or high-pass filtered data, which minimizes the data analysis required for jolt detection and faster transitions. The device can be configured to generate inertial wake-up interrupt signals from any combination of the configurable embedded functions, enabling the MMA8653FC to monitor inertial events and to remain in a low-power mode during periods of inactivity. The MMA8653FC is available in a small 10-pin DFN package (2 mm x 2 mm x 1 mm).

Top and Bottom View



10-PIN DFN
2 mm x 2 mm x 1 mm
CASE 2162

Top View



Pin Connections

Features

- 1.95V to 3.6V supply voltage
- 1.62V to 3.6V digital interface voltage
- ±2g, ±4g, and ±8g dynamically selectable full-scale ranges
- Output Data Rates (ODR) from 1.56 Hz to 800 Hz
- 10-bit digital output
- I^2C digital output interface with programmable interrupts
- One embedded channel of configurable motion detection (Freefall)
- Orientation (Portrait/Landscape) detection with default hysteresis
- Automatic ODR change triggered by the Auto-Wake / Sleep state change
- Self-Test

Typical Applications

- eCompass applications tilt compensation
- Static orientation detection (Portrait/Landscape, Up/Down, Left/Right, Back/Front position identification)
- Notebook, eReader, and Laptop Tumble and Freefall Detection
- Real-time orientation detection (virtual reality and gaming 3D user position feedback)
- Real-time activity analysis (pedometer step counting, freefall drop detection for HDD, dead-reckoning GPS backup)
- Motion detection for portable product power saving (Auto-SLEEP and Auto-WAKE for cell phone, PDA, GPS, gaming)
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)
- User interface (menu scrolling by orientation change)

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
MMA8653FCR1	-40°C to +85°C	DFN-10	Tape and Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

freescale Xtrinsic

Feature comparison of the MMA8653FC devices

Feature List	MMA8652FC	MMA8653FC
Digital Resolution (Bits)	12	10
Digital Sensitivity in 2g mode (Counts/g)	1024	256
Low-Power Mode	Yes	Yes
Auto-WAKE	Yes	Yes
Auto-SLEEP	Yes	Yes
32-Level FIFO	Yes	No
Low-Pass Filter	Yes	Yes
High-Pass Filter	Yes	No
Transient Detection with High-Pass Filter	Yes	No
Orientation Detection Portrait to Landscape = 30°, Landscape to Portrait = 60°, and Fixed 45° Threshold	Yes	Yes
Programmable Orientation Detection	Yes	No
Data-Ready Interrupt	Yes	Yes
Single-Tap Interrupt	Yes	No
Double-Tap Interrupt	Yes	No
Directional Tap Interrupt	Yes	No
Freefall/Motion Interrupt	Yes	Yes
Transient Interrupt with Direction	Yes	No

Contents

1 Block Diagram and Pin Descriptions

1.1 Block diagram

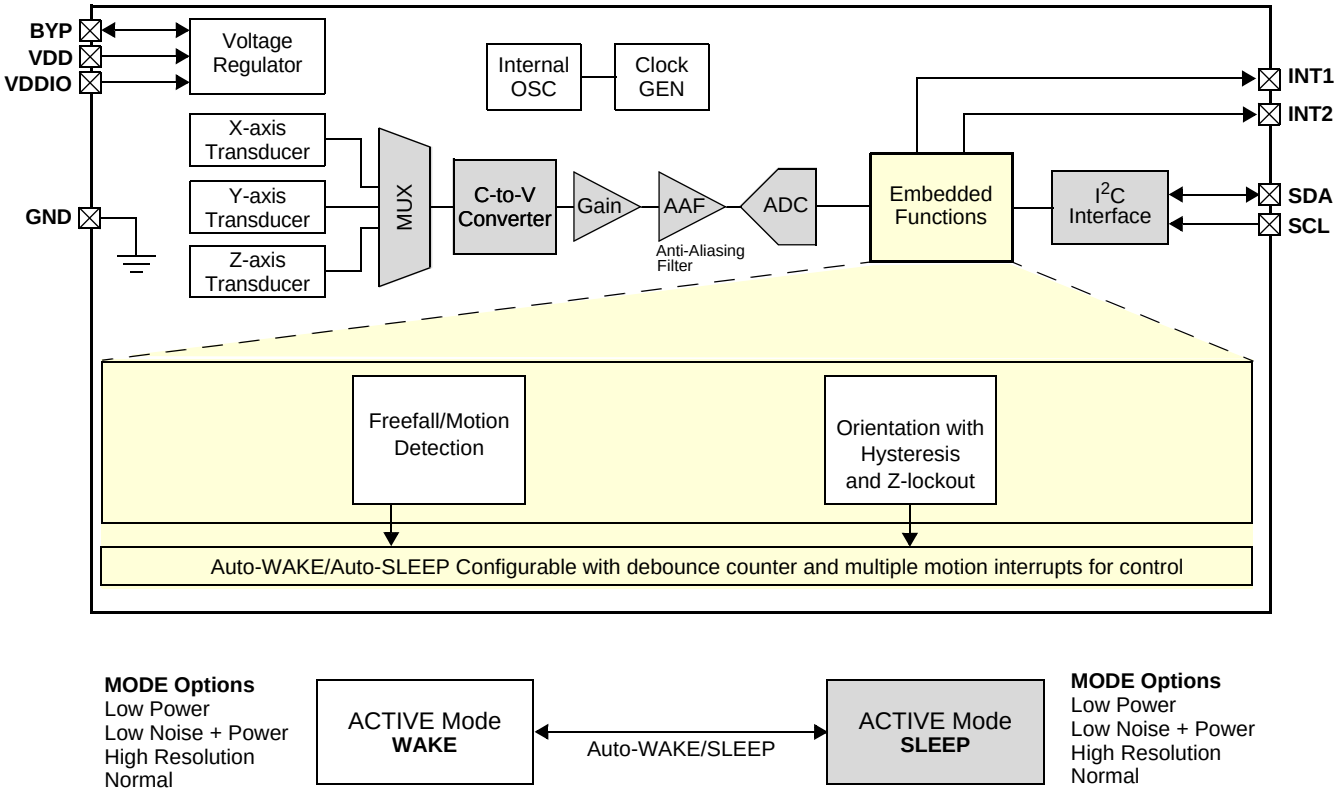


Figure 1. MMA8653 block diagram

1.2 Pin descriptions

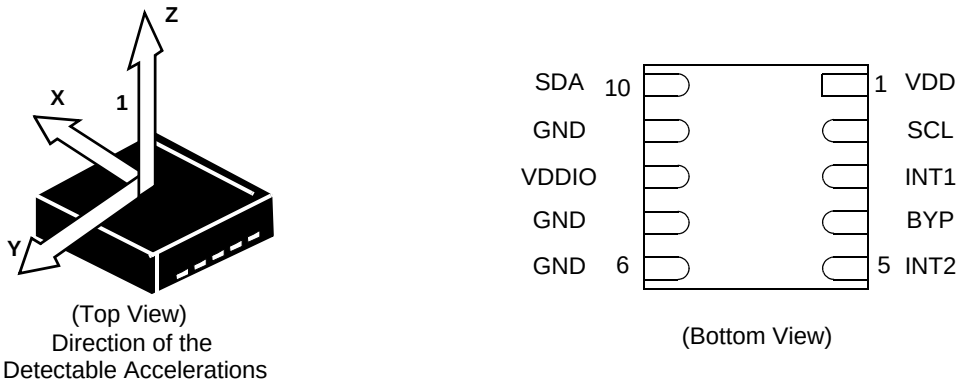


Figure 2. Direction of the detectable accelerations

1.3 Orientation definitions

Figure 3 shows the device configuration in the 6 different orientation modes. There are several registers to configure the orientation detection and are described in detail in the register setting section.

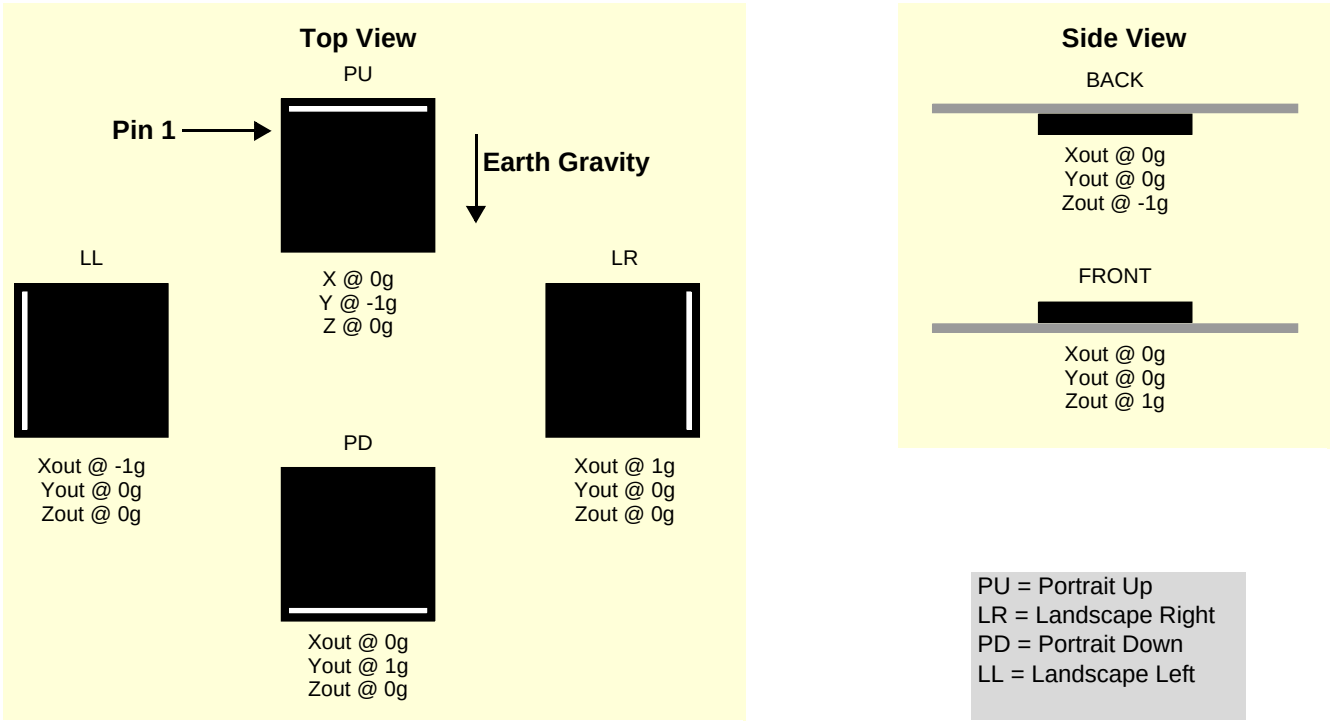
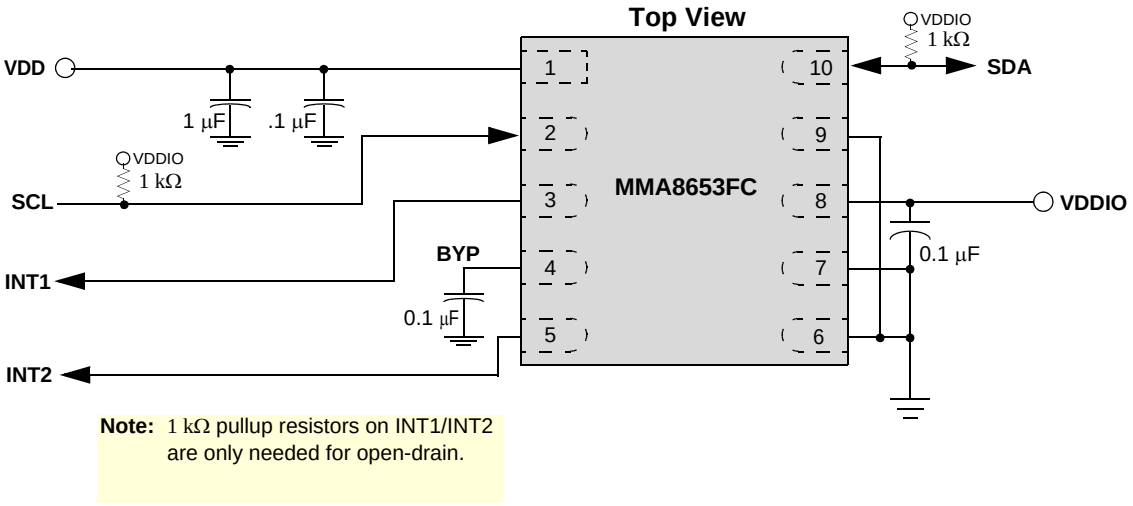


Figure 3. Landscape/Portrait orientation

1.4 Recommended application diagram



Note: 1 kΩ pullup resistors on INT1/INT2 are only needed for open-drain.

Figure 4. Application diagram

Table 1. Pin descriptions

Pin #	Pin Name	Description	Notes
1	VDD	Power supply	Device power is supplied through the VDD line. Power supply decoupling capacitors should be placed as near as possible to the pins 1 and 8 of the device.
2	SCL	I^2C Serial Clock	7-bit I^2C device address is 0x1D. The control signals SCL and SDA are not tolerant of voltages more than VDDIO + 0.3V. If VDDIO is removed, then the control signals SCL and SDA will clamp any logic signals with their internal ESD protection diodes. The SDA and SCL I^2C connections are open drain, and therefore usually require a pullup resistor.
3	INT1	Interrupt 1	The interrupt source and pin settings are user-programmable through the I^2C interface.
4	BYP	Internal regulator output capacitor connection	
5	INT2	Interrupt 2	See INT1.
6	GND	Ground	
7	GND	Ground	
8	VDDIO	Digital Interface Power supply	
9	GND	Ground	
10	SDA	I^2C Serial Data	See SCL.

2 Mechanical and Electrical Specifications

2.1 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Maximum ratings

Rating	Symbol	Value	Unit
Maximum acceleration (all axes, 100 μs)	g_{max}	10,000	g
Supply voltage	VDD	-0.3 to + 3.6	V
Input voltage on any control pin (SCL, SDA)	Vin	-0.3 to VDDIO + 0.3	V
Drop Test	D_{drop}	1.8	m
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latch-up Current at T = 85°C	—	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage of the part or cause the part to otherwise fail.

This part is ESD-sensitive. Improper handling can cause permanent damage to the part.

2.2 Mechanical characteristics

Table 4. Mechanical characteristics at VDD = 2.5V, VDDIO = 1.8V, T = 25°C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Measurement Range	FS[1:0] set to 00 2g Mode	FS		±2		g
	FS[1:0] set to 01 4g Mode			±4		
	FS[1:0] set to 10 8g Mode			±8		
Sensitivity	FS[1:0] set to 00 2g Mode	So		256		counts/g
	FS[1:0] set to 01 4g Mode			128		
	FS[1:0] set to 10 8g Mode			64		
Sensitivity Accuracy		Soa		±2.64		%
Sensitivity Change vs. Temperature	FS[1:0] set to 00 2g Mode	TCSo		±0.04		%/°C
	FS[1:0] set to 01 4g Mode					
	FS[1:0] set to 10 8g Mode					
Zero-g Level Offset Accuracy[1]	FS[1:0] 2g, 4g, 8g	TyOff		±40		mg
Zero-g Level Offset Accuracy Post-Board Mount[2]	FS[1:0] 2g, 4g, 8g	TyOffPBM		±60		mg
Zero-g Level Change vs. Temperature	-40°C to 85°C	TCOff		±0.3		mg/°C
Self-Test Output Change[3] X Y Z	FS[1:0] set to 0 4g Mode	Vst	 50 50 50			LSB
ODR Accuracy 2 MHz Clock			-20		+20	%
Output Data Bandwidth		BW	ODR/3		ODR/2	Hz
Output Noise	Normal Mode ODR = 400 Hz	Noise		216		µg/√Hz
Operating Temperature Range		Top	-40		+85	°C
Package weight				TBD		g

1. Before board mount.
2. Post-board mount offset specifications are based on an 8-layer PCB, relative to 25°C.
3. Self-Test is one direction only.

2.3 Electrical characteristics

Table 5. Electrical characteristics at VDD = 2.5V, VDDIO = 1.8V, T = 25°C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD[1]	1.95	2.5	3.6	V
Interface Supply Voltage		VDDIO[1]	1.62	1.8	3.6	V
Low Power Mode	ODR = 1.56 Hz	I_{dd}LP		6		µA
	ODR = 12.5 Hz			6		
	ODR = 50 Hz			14		
	ODR = 100 Hz			24		
	ODR = 200 Hz			44		
	ODR = 400 Hz			85		
	ODR = 800 Hz			165		
Normal Mode	ODR = 1.56 Hz	I_{dd}		24		µA
	ODR = 12.5 Hz			24		
	ODR = 50 Hz			24		
	ODR = 100 Hz			44		
	ODR = 200 Hz			85		
	ODR = 400 Hz			165		
	ODR = 800 Hz			165		
Current during Boot Sequence, 0.5 mSec max duration using recommended Bypass Cap	VDD = 2.5V	Idd Boot			1	mA
Value of Capacitor on BYP Pin	-40°C to 85°C	Cap	75	100	470	nF
STANDBY Mode Current at 25°C	VDD = 2.5V, VDDIO = 1.8V STANDBY Mode	I_{dd}Stby		1.8	5	µA
STANDBY Mode Current over temperature range	VDD = 2.5V, VDDIO = 1.8V STANDBY Mode	I_{dd}Stby		TBD	TBD	µA
Digital High Level Input Voltage SCL, SDA		VIH	0.75*VDDIO			V
Digital Low Level Input Voltage SCL, SDA		VIL			0.3*VDDIO	V
High Level Output Voltage INT1, INT2	I_O = 500 µA	VOH	0.9*VDDIO			V
Low Level Output Voltage INT1, INT2	I_O = 500 µA	VOL			0.1*VDDIO	V
Low Level Output Voltage SDA	I_O = 500 µA	VOLS			0.1*VDDIO	V
Output Source Current	Voltage high level VOUT = 0.75 x VDD, VDD = 2.5V	I_{source}	3			mA
Output Sink Current	Voltage high level VOUT = 0.25 x VDD, VDD = 2.5V	I_{sink}	3			mA
Power-on Ramp Time		Tpu	0.001		1000	ms
Time from VDDIO on and VDD > Vmin until I^2C is ready for operation	Cbyp = 100 nF	BT		350	500	µs
Turn-on time (STANDBY to first sample available)		Ton			2/ODR + 1[2]	ms
Turn-on time (Power down to first sample available)		Ton			2/ODR + 2[2]	ms

1. There is no requirement for power supply sequencing. The VDDIO input voltage can be higher than the VDD input voltage.

2. Note that the first sample is typically not very precise; only the second or third or fourth sample (depending on ODR/MODS settings) has full precision.

2.4 I^2C interface characteristics

Table 6. I^2C slave timing values(1)

Parameter	Symbol	I^2C Fast Mode		Unit
		Min	Max	
SCL Clock Frequency	f_{SCL}	0	400	kHz
Bus Free Time between STOP and START condition	t_{BUF}	1.3		µs
(Repeated) START Hold Time	$t_{HD;STA}$	0.6		µs
(Repeated) START Setup Time	$t_{SU;STA}$	0.6		µs
STOP Condition Setup Time	$t_{SU;STO}$	0.6		µs
SDA Data Hold Time	$t_{HD;DAT}$	0.05	0.9(2)	µs
SDA Valid Time(3)	$t_{VD;DAT}$		0.9(2)	µs
SDA Valid Acknowledge Time(4)	$t_{VD;ACK}$		0.9(2)	µs
SDA Setup Time	$t_{SU;DAT}$	100		ns
SCL Clock Low Time	t_{LOW}	1.3		µs
SCL Clock High Time	t_{HIGH}	0.6		µs
SDA and SCL Rise Time	t_r	20 + 0.1 C_b(5)	300	ns
SDA and SCL Fall Time	t_f	20 + 0.1 C_b(5)	300	ns
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	ns

1. All values referred to VIH (min) and VIL (max) levels.
2. This device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. $t_{VD;DAT}$ = time for Data signal from SCL LOW to SDA output.
4. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. C_b = total capacitance of one bus line in pF.

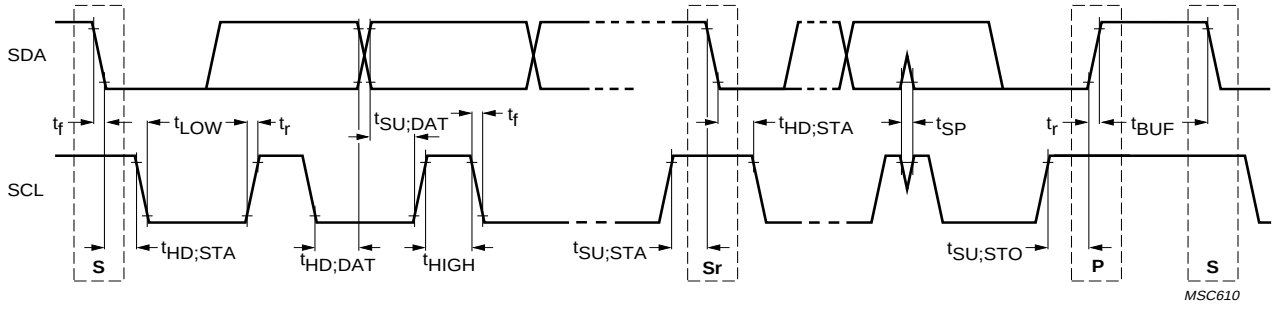


Figure 5. I^2C slave timing

3 Terminology

3.1 Sensitivity

The sensitivity is represented in counts/g.

- In 2g mode, sensitivity = 256 counts/g.
- In 4g mode, sensitivity = 128 counts/g.
- In 8g mode, sensitivity = 64 counts/g.

3.2 Zero-g offset

Zero-g Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if the sensor is stationary. A sensor stationary on a horizontal surface will measure 0g in X-axis and 0g in Y-axis, whereas the Z-axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT Registers 0x00, data expressed as a 2's complement number). A deviation from ideal value in this case is called Zero-g offset.

Offset is to some extent a result of stress on the MEMS sensor, and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress.

3.3 Self-Test

Self-Test can be used to verify the transducer and signal chain functionality without the need to apply external mechanical stimulus.

When Self-Test is activated:

- An electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case, the sensor outputs will exhibit a change in their DC levels which, are related to the selected full scale through the device sensitivity.
- The device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

4 Modes of Operation

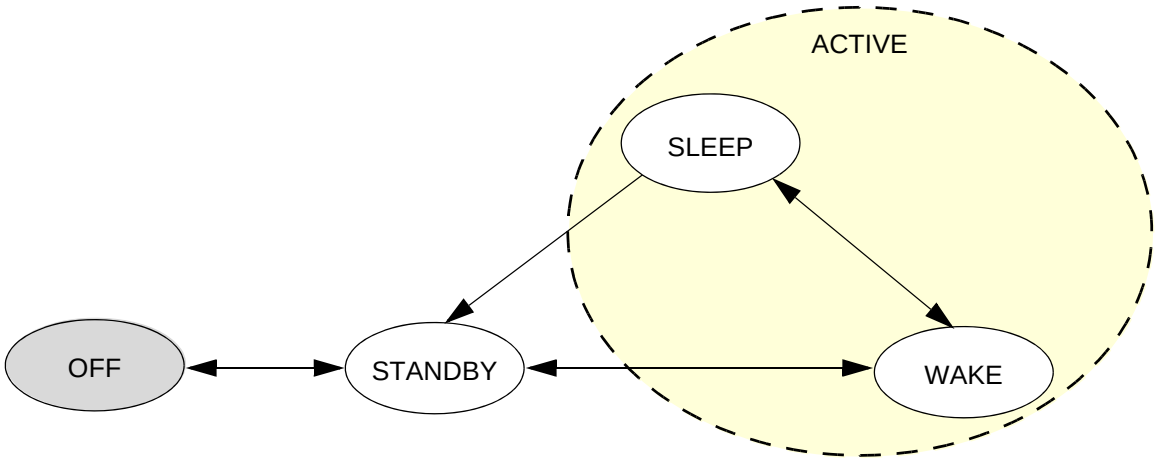


Figure 6. Operating modes for MMA8653FC

Table 7. Operating modes

Mode	I^2C Bus State	VDD	VDDIO	Description
OFF	Powered Down	<1.8V	VDDIO Can be > VDD	• The device is powered off. • All analog and digital blocks are shutdown. • I^2C bus inhibited.
STANDBY	I^2C communication with MMA8653FC is possible	ON	VDDIO = High VDD = High ACTIVE bit is cleared	• Only digital blocks are enabled. • Analog subsystem is disabled. • Internal clocks disabled.
ACTIVE (WAKE/SLEEP)	I^2C communication with MMA8653FC is possible	ON	VDDIO = High VDD = High ACTIVE bit is set	All blocks are enabled (digital, analog).

Some registers are reset when transitioning from STANDBY to ACTIVE. These registers are all noted in the device memory map register table.

The SLEEP and WAKE modes are ACTIVE modes. For more information about how to use the SLEEP and WAKE modes and how to transition between these modes, see Section 5, “Functionality”.

5 Functionality

The MMA8653FC is a low-power, digital output 3-axis linear accelerometer with a I^2C interface, and has embedded logic that is used to detect events and notify an external microprocessor over interrupt lines.

- 8-bit or 10-bit data
- Four different oversampling options that allow for the optimum resolution vs. current consumption trade-off to be made for a given application
- Low power and auto-WAKE/SLEEP modes for reducing current consumption
- Freefall/Motion detection (1 channel)
- Single default angle for portrait landscape detection algorithm, for addressing screen orientation
- Two independent interrupt output pins that are programmable among 4 interrupt sources (Data Ready, Freefall/Motion, Orientation, Auto-WAKE)

All functionality is available in 2g, 4g or 8g dynamic measurement ranges. There are many configuration settings for enabling all of the different functions. Separate application notes are available to help configure the device for each embedded functionality.

5.1 Device calibration

The device is factory calibrated for sensitivity and Zero-g offset for each axis. The trim values are stored in Non-Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the circuitry. In normal use, further calibration in the end application is not necessary. However, the MMA8653FC allows you to adjust the offset for each axis after power-up, by changing the default offset values. The user offset adjustments are stored in 3 volatile 8-bit registers (OFF_X, OFF_Y, OFF_Z).

5.2 8-bit or 10-bit data

The measured acceleration data is stored in the following registers as 2's complement 10-bit numbers:

- OUT_X_MSB, OUT_X_LSB
- OUT_Y_MSB, OUT_Y_LSB
- OUT_Z_MSB, OUT_Z_LSB

The most significant 8-bits of each axis are stored in OUT_X (Y, Z)_MSB, so applications needing only 8-bit results can use these 3 registers (and ignore the OUT_X/Y/Z_LSB registers). To do this (use only 8-bit results), the F_READ bit in CTRL_REG1 must be set. When the F_READ bit is cleared, the fast read mode is disabled.

- **When the full-scale is set to 2g**, the measurement range is -2g to +1.996g, and each count corresponds to (1/256)g (3.8mg) at 10-bit resolution.
- **When the full-scale is set to 4g**, the measurement range is -4g to +3.992g, and each count corresponds to (1/128)g
- (7.8mg) at 10-bit resolution.
- **When the full-scale is set to 8g**, the measurement range is -8g to +7.984g, and each count corresponds to (1/64)g (15.6 mg) at 10-bit resolution.
- **If only the 8-bit results are used**, then the resolution is reduced by a factor of 16.

For more information about the data manipulation between data formats and modes, see application note AN4083, *Data Manipulation and Basic Settings for Xtrinsic MMA865xFC Accelerometers*. There is a device driver available that can be used with the Sensor Toolbox demo board (LFSTBEB865xFC) with this application note.

Table 8. Accelerometer 10-bit output data

10-bit Data	Range ±2g (3.9 mg)	Range ±4g (7.8 mg)	Range ±8g (15.6 mg)
01 1111 1111	1.996g	+3.992g	+7.984g
01 1111 1110	1.992g	+3.984g	+7.968g
…	…	…	…
00 0000 0001	0.003g	+0.007g	+0.015g
00 0000 0000	0.000g	0.000g	0.000g
11 1111 1111	-0.003g	-0.007g	-0.015g
…	…	…	…
10 0000 0001	-1.961g	-3.992g	-7.984g
10 0000 0000	-2.000g	-4.000g	-8.000g

Table 8. Accelerometer 10-bit output data (Continued)

8-bit Data	Range ±2g (15.6 mg)	Range ±4g (31.25 mg)	Range ±8g (62.5 mg)
0111 1111	1.984g	+3.968g	+7.937g
0111 1110	1.968g	+3.937g	+7.875g
…	…	…	…
0000 0001	+0.015g	+0.031g	+0.062g
0000 0000	0.000g	0.000g	0.000g
1111 1111	-0.015g	-0.031g	-0.062g
…	…	…	…
1000 0001	-1.984g	-3.968g	-7.937g
1000 0000	-2.000g	-4.000g	-8.000g

Table 9. Accelerometer 8-bit output data

8-bit Data	Range ±2g (15.6 mg)	Range ±4g (31.25 mg)	Range ±8g (62.5 mg)
0111 1111	1.9844g	+3.9688g	+7.9375g
0111 1110	1.9688g	+3.9375g	+7.8750g
…	…	…	…
0000 0001	+0.0156g	+0.0313g	+0.0625g
0000 0000	0.000g	0.0000g	0.0000g
1111 1111	-0.0156g	-0.0313g	-0.0625g
…	…	…	…
1000 0001	-1.9844g	-3.9688g	-7.9375g
1000 0000	-2.0000g	-4.0000g	-8.0000g

5.3 Low power modes vs. high resolution modes

The MMA8653FC can be optimized for lower power modes or for higher resolution of the output data. One of the oversampling schemes of the data can activated when MODS = 10 in Register 0x2B, which will improve the resolution of the output data only. The highest resolution is achieved at 1.56 Hz.

There is a trade-off between low power and high resolution. Low power can be achieved when the oversampling rate is reduced. When MODS = 11, the lowest power is achieved. The lowest power is achieved when the sample rate is set to 1.56 Hz.

5.4 Auto-WAKE/SLEEP mode

The MMA8653FC can be configured to transition between sample rates (with their respective current consumption) based on four of the interrupt functions of the device. The advantage of using the Auto-WAKE/SLEEP is that the system can automatically transition to a higher sample rate (higher current consumption) when needed, but spends the majority of the time in the SLEEP mode (lower current) when the device does not require higher sampling rates.

- **Auto-WAKE** refers to the device being triggered by one of the interrupt functions to transition to a higher sample rate. This may also interrupt the processor to transition from a SLEEP mode to a higher power mode.
- **SLEEP mode** occurs after the accelerometer has not detected an interrupt for longer than the user-definable timeout period. The device will transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode, to save on current during this period of inactivity.

The interrupts that can WAKE the device from SLEEP are the following: Orientation detection, and Freefall/Motion detection. The interrupts that can keep the device from falling asleep are the same interrupts that can wake the device.

5.5 Freefall detection

MMA8653FC has a flexible interrupt architecture for detecting either a Freefall or a Motion.

- Freefall can be enabled where the set threshold *must be less than* the configured threshold.
- Motion can be enabled where the set threshold *must be greater than* the configured threshold.

The motion configuration has the option of enabling or disabling a high-pass filter to eliminate tilt data (static offset); the freefall configuration does not use the high-pass filter.

MMA8653FC has an interrupt architecture for detecting a Freefall.

- Freefall can be enabled where the set threshold *must be less than* the configured threshold.

The freefall configuration does not use a high-pass filter.

5.5.1 Freefall detection

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is *below a user-specified threshold for a user-definable amount of time*. The usable threshold ranges are normally between ±100 mg and ±500 mg.

5.6 Orientation detection

The MMA8653FC incorporates an advanced algorithm for orientation detection (ability to detect all 6 orientations), with one default trip point setting. The transition from portrait to landscape is at a fixed 45° threshold angle and at a fixed ±15° hysteresis angle. This allows for smooth transition from portrait to landscape at approximately 30°, and then from landscape to portrait at approximately 60°.

The MMA8653FC orientation detection algorithm confirms the reliability of the function with a configurable Z-lockout angle. Based on the known functionality of linear accelerometers, it is not possible to rotate the device about the Z-axis, to detect change in acceleration at slow angular speeds. The angle at which the device no longer detects the orientation change is referred to as the “Z-lockout angle”. The device operates at a fixed 29° angle from the flat position, with an accuracy of ± 2°.

- Figure 7 shows the definition of the orientations (PU, PD, LL, LR, BACK, FRONT).
- Figure 8 shows the definitions of the trip angles, going from landscape to portrait and then from portrait to landscape.

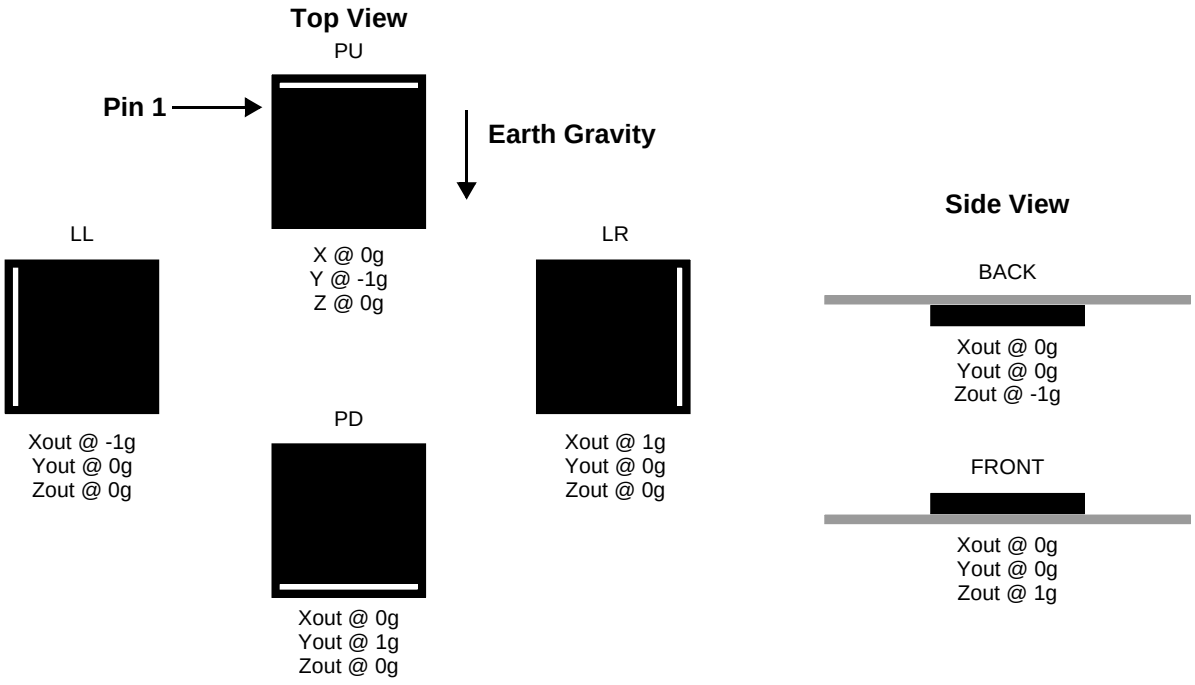


Figure 7. Landscape/Portrait orientation

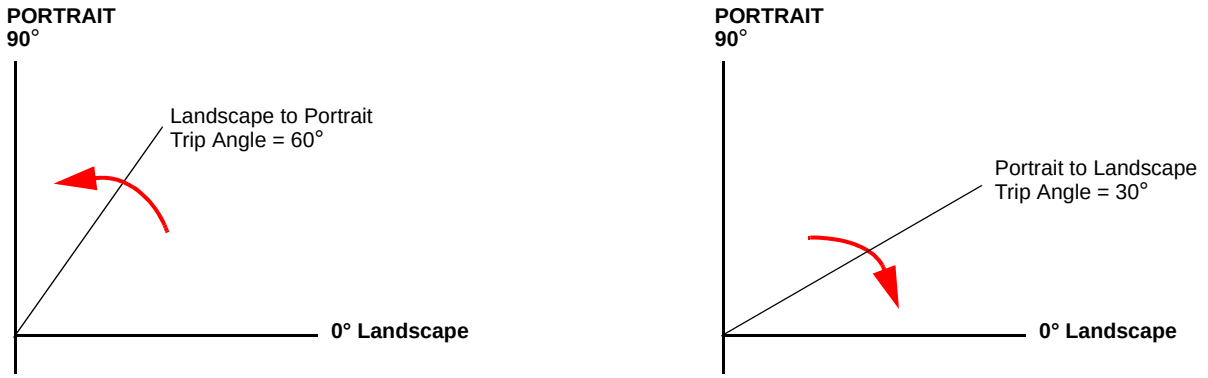


Figure 8. Landscape to Portrait transition

Figure 9 shows the Z-angle lockout region.

.

When lifting the device upright from the flat position, the device will be active for orientation detection as low as 29° from 0° flat. This is the only setting available.

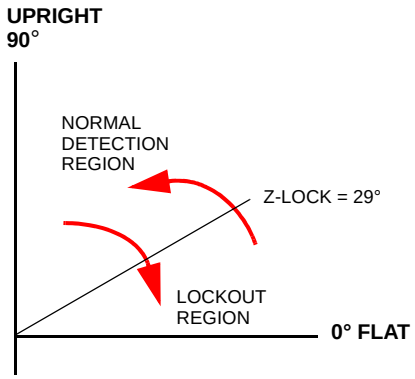


Figure 9. Z-Tilt angle lockout transition

5.7 Interrupt register configurations

There are 4 configurable interrupts in the MMA8653FC: Data Ready, Motion/Freefall, Orientation, and Auto-SLEEP events.

These 4 interrupt sources can be routed to one of two interrupt pins.

The interrupt source must be enabled and configured.

If the event flag is asserted because the event condition is detected, then the corresponding interrupt pin (INT1 or INT2) will assert.

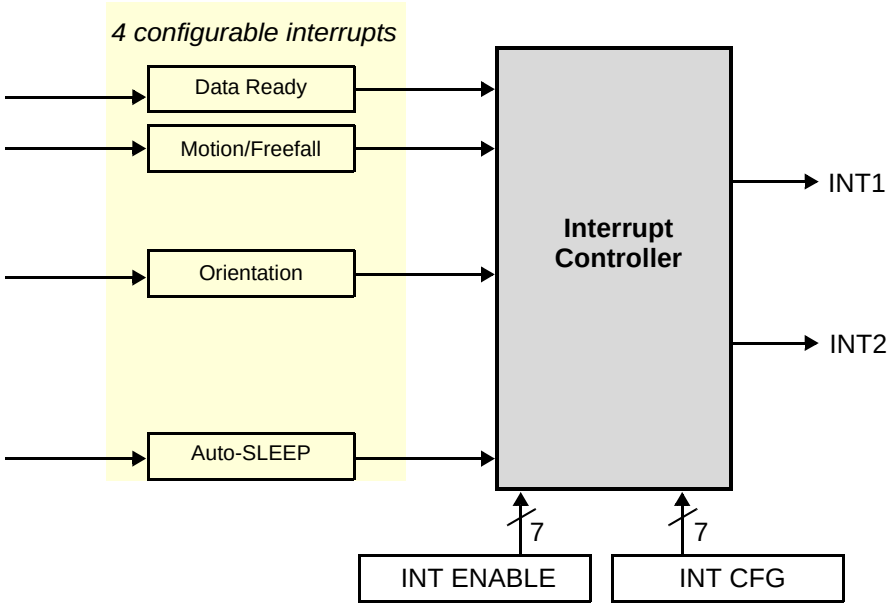


Figure 10. System interrupt generation

- The MMA8653FC features an interrupt signal that indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.
- The MMA8653FC may also be configured to generate *other interrupt signals* accordingly, to the programmable embedded functions of the device for Motion, Freefall, and Orientation.

5.8 Serial I²C interface

Acceleration data may be accessed through an I²C interface, thus making the device particularly suitable for direct interfacing to a microcontroller. The acceleration data and configuration registers embedded inside the MMA8653FC are accessed through the I²C serial interface (Table 10, “Serial Interface pins").

- To enable the I²C interface, VDDIO line must be tied high (i.e., to the interface supply voltage). If VDD is not present and VDDIO is present, then the MMA8653FC is in OFF mode—and communications on the I²C interface are ignored.
- The I²C interface may be used for communications between other I²C devices; the MMA8653FC does not affect the I²C bus.

Table 10. Serial Interface pins

Pin Name	Pin Description	Notes
SCL	I²C Serial Clock	**There are two signals associated with the I²C bus; the Serial Clock Line (SCL) and the Serial Data line (SDA).** • SDA is a bidirectional line used for sending and receiving the data to/from the interface. • External pullup resistors connected to VDDIO are expected for SDA and SCL. When the bus is free, both SCL and SDA lines are high.
SDA	I²C Serial Data	

The I²C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I²C standards (Table 6, “I2C slave timing values").

I²C operation:

1. The transaction on the bus is started through a start condition (START) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After START has been transmitted by the Master, the bus is considered busy.
2. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the 8th bit tells whether the Master is *receiving data from the slave* or is *transmitting data to the slave*.
3. After a start condition and when an address is sent, each device in the system compares the first 7 bits with its address. If the device’s address matches the sent address, then the device considers itself addressed by the Master.
4. The 9th clock pulse following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low, so that it remains stable low during the high period of the acknowledge clock period.
5. A Master may also issue a repeated START during a data transfer. The MMA8653FC expects repeated STARTs to be used to randomly read from specific registers.
6. A low-to-high transition on the SDA line *while the SCL line is high* is defined as a stop condition (STOP). A data transfer is always terminated by a STOP.

The MMA8653FC's standard slave address is 0011101 or 0x01D. The slave addresses are factory programmed; alternate addresses are available upon request.

Table 11. I²C Device address sequence

Command	[6:0] Device address	[6:0] Device address	R/W	8-bit final value
Read	0011101	0x1D	1	0x3B
Write	0011101	0x1D	0	0x3A

5.8.1 Single byte read

1. The transmission of an 8-bit command begins on the falling edge of SCL. After the 8 clock cycles are used to send the command, note that *the data returned* is sent with the MSB first after the data is received. Figure 11 "Single Byte Read timing (I²C)" shows the timing diagram for the accelerometer 8-bit I²C read operation.
2. The Master (or MCU) transmits a start condition (ST) to the MMA8653FC [slave address (0x1D), with the R/W bit set to “0” for a write], and the MMA8653FC sends an acknowledgement.

3. Next the Master (or MCU) transmits the address of the register to read, and the MMA8653FC sends an acknowledgement.
4. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8653FC (0x1D), with the R/W bit set to “1” for a read from the previously selected register.
5. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

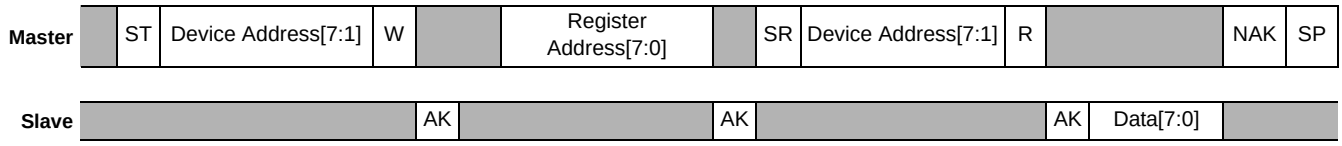


Figure 11. Single Byte Read timing (I^2C)

For the following subsections, use the following legend.

Legend

ST: Start Condition	SP: Stop Condition	NAK: No Acknowledge	W: Write = 0
SR: Repeated Start Condition	AK: Acknowledge	R: Read = 1	

5.8.2 Multiple byte read

(See Table 11, “I^2C Device address sequence" for next auto-increment address.)

1. When performing a multi-byte read or “burst read”, the MMA8653FC automatically increments the received register address commands after a read command is received.
2. After following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8653FC acknowledgment (AK) is received,
3. Until a no acknowledge (NAK) occurs from the Master,
4. Followed by a stop condition (SP), which signals the end of transmission.

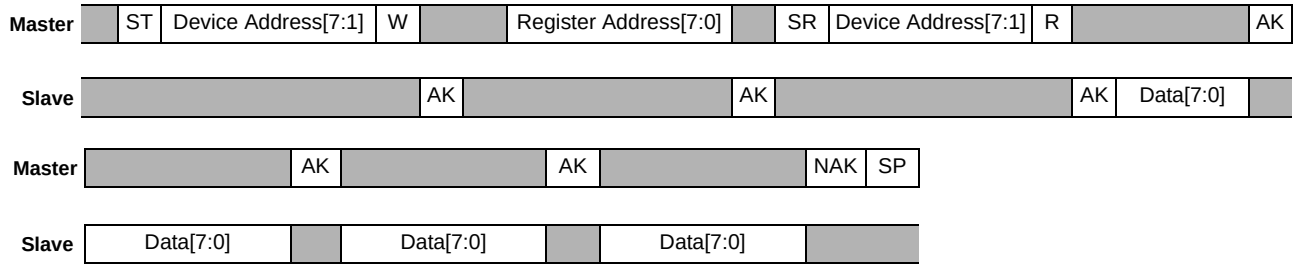


Figure 12. Multiple Byte Read timing (I^2C)

5.8.3 Single byte write

1. To start a write command, the Master transmits a start condition (ST) to the MMA8653FC, slave address ($1D) with the R/W bit set to “0” for a write,
2. The MMA8653FC sends an acknowledgement.
3. Next the Master (MCU) transmits the address of the register to write to, and the MMA8653FC sends an acknowledgement.
4. Then the Master (or MCU) transmits the 8-bit data to write to the designated register, and the MMA8653FC sends an acknowledgement that it has received the data. Because this transmission is complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA8653FC is now stored in the appropriate register.

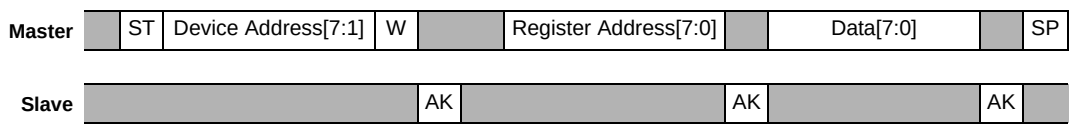


Figure 13. Single Byte Write timing (I^2C)

5.8.4 Multiple byte write

(See Table 11, "I^2C Device address sequence" for next auto-increment address.)

1. After a write command is received, the MMA8653FC *automatically increments* the received register address commands.
2. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA8653FC acknowledgment (ACK) is received.

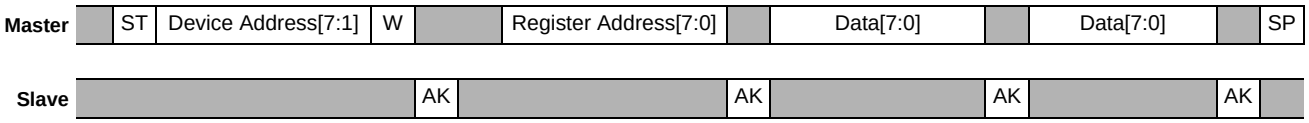


Figure 14. Multiple Byte Write timing (I^2C)

6 Register Descriptions

6.1 Register address map

Table 12. MMA8653FC Register Address Map

Field	Type	Register Address	Auto-Increment Address		Default	Hex Value	Comment
			F_READ = 0	F_READ = 1			
STATUS[1][2]	R	0x00	0x01		00000000	0x00	Real time status
OUT_X_MSB[1]	R	0x01	0x02	0x03	Output	—	[7:0] are 8 MSBs of 10-bit sample.
OUT_X_LSB[1]	R	0x02	0x03	0x00	Output	—	[7:6] are 2 LSBs of 10-bit real-time sample
OUT_Y_MSB[1]	R	0x03	0x04	0x05	Output	—	[7:0] are 8 MSBs of 10-bit real-time sample
OUT_Y_LSB[1]	R	0x04	0x05	0x00	Output	—	[7:6] are 2 LSBs of 10-bit real-time sample
OUT_Z_MSB[1]	R	0x05	0x06	0x00	Output	—	[7:0] are 8 MSBs of 10-bit real-time sample
OUT_Z_LSB[1]	R	0x06	0x00		Output	—	[7:6] are 2 LSBs of 10-bit real-time sample
Reserved	R	0x07–0x0A	—		00000000	0x00	Reserved. Read return 0x00.
SYSMOD	R	0x0B	0x0C		00000000	0x00	Current System Mode
INT_SOURCE[1][2]	R	0x0C	0x0D		00000000	0x00	Interrupt status
WHO_AM_I[3]	R	0x0D	0x0E		01001010	0x5A	Device ID (0x5A)
XYZ_DATA_CFG[3][4]	R/W	0x0E	0x0F		00000000	0x00	Dynamic Range Settings
Reserved	R	0x0F	—		00000000	0x00	Reserved. Read return 0x00.
PL_STATUS[1][2]	R	0x10	0x11		00000000	0x00	Landscape/Portrait orientation status
PL_CFG[3][4]	R/W	0x11	0x12		10000000	0x80	Landscape/Portrait configuration.
PL_COUNT[3][4]	R/W	0x12	0x13		00000000	0x00	Landscape/Portrait debounce counter
PL_BF_ZCOMP[3]	R	0x13	0x14		01000100	0x44	Back/Front, Z-Lock Trip threshold
PL_THS_REG[3]	R	0x14	0x15		10000100	0x84	Portrait to Landscape Trip angle
FF_MT_CFG[3][4]	R/W	0x15	0x16		00000000	0x00	Freefall/Motion functional block configuration
FF_MT_SRC[1][2]	R	0x16	0x17		00000000	0x00	Freefall/Motion event source register
FF_MT_THS[3][4]	R/W	0x17	0x18		00000000	0x00	Freefall/Motion threshold register
FF_MT_COUNT[3][4]	R/W	0x18	0x19		00000000	0x00	Freefall/Motion debounce counter
Reserved	R	0x19–0x28	—		00000000	0x00	Reserved. Read return 0x00.
ASLP_COUNT[3][4]	R/W	0x29	0x2A		00000000	0x00	Counter setting for Auto-SLEEP/WAKE
CTRL_REG1[3][4]	R/W	0x2A	0x2B		00000000	0x00	Data Rates, ACTIVE Mode.
CTRL_REG2[3][4]	R/W	0x2B	0x2C		00000000	0x00	Sleep Enable, OS Modes, RST, ST
CTRL_REG3[3][4]	R/W	0x2C	0x2D		00000000	0x00	Wake from Sleep, IPOL, PP_OD
CTRL_REG4[3][4]	R/W	0x2D	0x2E		00000000	0x00	Interrupt enable register
CTRL_REG5[3][4]	R/W	0x2E	0x2F		00000000	0x00	Interrupt pin (INT1/INT2) map
OFF_X[3][4]	R/W	0x2F	0x30		00000000	0x00	X-axis offset adjust
OFF_Y[3][4]	R/W	0x30	0x31		00000000	0x00	Y-axis offset adjust
OFF_Z[3][4]	R/W	0x31	0x0D		00000000	0x00	Z-axis offset adjust

1. The register data is only valid in ACTIVE mode.
2. Register contents are reset when transition from STANDBY to ACTIVE mode occurs.
3. Register contents are preserved when transition from ACTIVE to STANDBY mode occurs.
4. Modification of this register's content can only occur when device is in STANDBY mode, except CTRL_REG1 ACTIVE bit and CTRL_REG2 RST bit.

Note: Auto-increment addresses that are not a simple increment are highlighted in **bold**.
The auto-increment addressing is only enabled when device registers are read using I^2C *burst read mode*.
The *internally stored* auto-increment address is cleared whenever an I^2C STOP condition is detected.

6.2 Register bit map

Reg	Field	Definition	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	STATUS	Data Status	R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
01	OUT_X_MSB	10-bit X Data	R	XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2
02	OUT_X_LSB	10-bit X Data	R	XD1	XD0	0	0	0	0	0	0
03	OUT_Y_MSB	10-bit Y Data	R	YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2
04	OUT_Y_LSB	10-bit Y Data	R	YD1	YD0	0	0	0	0	0	0
05	OUT_Z_MSB	10-bit Z Data	R	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2
06	OUT_Z_LSB	10-bit Z Data	R	ZD1	ZD0	0	0	0	0	0	0
07–0A	Reserved	—	R	0	0	0	0	0	0	0	0
0B	SYSMOD	System Mode	R	0	0	0	0	0	0	SYSMOD1	SYSMOD0
0C	INT_SOURCE	Interrupt Status	R	SRC_ASLP	0	0	SRC_LNDPRT	0	SRC_FF_MT	0	SRC_DRDY
0D	WHO_AM_I	ID Register	R	0	1	0	1	1	0	1	0
0E	XYZ_DATA_CFG	Data Config	R/W	0	0	0	0	0	0	FS1	FS0
0F	Reserved	—	R	—	—	—	—	—	—	—	—
10	PL_STATUS	Portrait Landscape Status	R	NEWLP	LO	0	0	0	LAPO[1]	LAPO[0]	BAFRO
11	PL_CFG	Portrait Landscape Configuration	R/W	DBCNTM	PL_EN	0	0	0	0	0	0
12	PL_COUNT	Portrait Landscape Debounce	R/W	DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE[2]	DBNCE[1]	DBNCE[0]
13	PL_BF_ZCOMP	Portrait Landscape Back/Front Z Comp	R	0	1	0	0	0	1	0	0
14	PL_THS_REG	Portrait Landscape Threshold	R	1	0	0	0	0	1	0	0
15	FF_MT_CFG	Freefall/Motion Config	R/W	ELE	OAE	ZEFE	YEFE	XEFE	0	0	0
16	FF_MT_SRC	Freefall/Motion Status	R	EA	0	ZHE	ZHP	YHE	YHP	XHE	XHP
17	FF_MT_THS	Freefall/Motion Threshold	R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
18	FF_MT_COUNT	Freefall/Motion Debounce	R/W	D7	D6	D5	D4	D3	D2	D1	D0
19–28	Reserved	—	R	—	—	—	—	—	—	—	—
29	ASLP_Count	Counter setting for Auto-SLEEP/WAKE	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2A	CTRL_REG1	Control Reg1	R/W	ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	0	F_READ	ACTIVE
2B	CTRL_REG2	Control Reg2	R/W	ST	RST	—	SMODS1	SMODS0	SLPE	MODS1	MODS0
2C	CTRL_REG3	Control Reg3	R/W	—	—	WAKE_LNDPRT	—	WAKE_FF_MT	0	IPOL	PP_OD
2D	CTRL_REG4	Control Reg4	R/W	INT_EN_ASLP	—	—	INT_EN_LNDPRT	—	INT_EN_FF_MT	0	INT_EN_DRDY
2E	CTRL_REG5	Control Reg5	R/W	INT_CFG_ASLP	—	—	INT_CFG_LNDPRT	—	INT_CFG_FF_MT	0	INT_CFG_DRDY
2F	OFF_X	X 8-bit offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30	OFF_Y	Y 8-bit offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31	OFF_Z	Z 8-bit offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0

Note: Bits showing "—" can read as either 0 or 1, and these bits have no definition.

6.3 Data registers

The following are the data registers for the MMA8653FC. For more information about data manipulation of the MMA8653FC, see application note, AN4083.

6.3.1 0x00: STATUS, Data Status Register

This register contains the X, Y, Z data overwrite and data ready flags.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Figure 15. 0x00: STATUS, Data Status Register (Read Only)

Table 13. STATUS register bits

Field	Description
ZYXOW	**X, Y, Z-axis Data Overwrite**. Default value: 0 ZYXOW is set whenever a new acceleration data is produced before completing the retrieval of the previous set. This event occurs when the content of at least one acceleration data register (i.e., OUT_X, OUT_Y, OUT_Z) has been overwritten. ZYXOW is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the channels are read. 0: No data overwrite has occurred 1: Previous X, Y, or Z data was overwritten by new X, Y, or Z data before it was read
ZOW	**Z-axis Data Overwrite**. Default value: 0 ZOW is set whenever a new acceleration sample related to the Z-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. ZOW is cleared anytime OUT_Z_MSB register is read. 0: No data overwrite has occurred 1: Previous Z-axis data was overwritten by new Z-axis data before it was read
YOW	**Y-axis Data Overwrite**. Default value: 0 YOW is set whenever a new acceleration sample related to the Y-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. YOW is cleared anytime OUT_Y_MSB register is read. 0: No data overwrite has occurred 1: Previous Y-axis data was overwritten by new Y-axis data before it was read
XOW	**X-axis Data Overwrite**. Default value: 0 XOW is set whenever a new acceleration sample related to the X-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. XOW is cleared any time OUT_X_MSB register is read. 0: No data overwrite has occurred 1: Previous X-axis data was overwritten by new X-axis data before it was read
ZYXDR	**X, Y, Z-axis new Data Ready**. Default value: 0 ZYXDR signals that a new sample for any of the enabled channels is available. ZYXDR is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the channels are read. 0: No new set of data ready 1: A new set of data is ready
ZDR	**Z-axis new Data Available**. Default value: 0 ZDR is set whenever a new acceleration sample related to the Z-axis is generated. ZDR is cleared any time OUT_Z_MSB register is read. 0: No new Z-axis data is ready 1: A new Z-axis data is ready
YDR	**Y-axis new Data Available**. Default value: 0 YDR is set whenever a new acceleration sample related to the Y-axis is generated. YDR is cleared any time OUT_Y_MSB register is read. 0: No new Y-axis data ready 1: A new Y-axis data is ready
XDR	**X-axis new Data Available**. Default value: 0 XDR is set whenever a new acceleration sample related to the X-axis is generated. XDR is cleared any time OUT_X_MSB register is read. 0: No new X-axis data ready 1: A new X-axis data is ready

6.3.2 0x01: OUT_X_MSB, Accelerometer X-axis data register

6.3.3 0x02: OUT_X_LSB, Accelerometer X-axis data register

6.3.4 0x03: OUT_Y_MSB, Accelerometer Y-axis data register

6.3.5 0x04: OUT_Y_LSB, Accelerometer Y-axis data register

6.3.6 0x05: OUT_Z_MSB, Accelerometer Z-axis data register

6.3.7 0x06: OUT_Z_LSB, Accelerometer Z-axis data register

These registers contain the X-axis, Y-axis, and Z-axis10-bit output sample data expressed as 2's complement numbers.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2

Figure 16. 0x01: OUT_X_MSB, X_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD1	XD0	0	0	0	0	0	0

Figure 17. 0x02: OUT_X_LSB, X_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2

Figure 18. 0x03: OUT_Y_MSB, Y_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD1	YD0	0	0	0	0	0	0

Figure 19. 0x04: OUT_Y_LSB, Y_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2

Figure 20. 0x05: OUT_Z_MSB, Z_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD1	ZD0	0	0	0	0	0	0

Figure 21. 0x06: OUT_Z_LSB, Z_LSB Register (Read Only)

OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x01 to 0x06 to reduce reading the status followed by 10-bit axis data to 7 bytes. If the F_READ bit is set (0x2A bit 1), auto increment will skip over LSB registers. This will shorten the data acquisition from 7 bytes to 4 bytes. The LSB registers can only be read immediately following the read access of the corresponding MSB register. A random read access to the LSB registers is not possible. Reading the MSB register and then the LSB register in sequence ensures that both bytes (LSB and MSB) belong to the same data sample, even if a new data sample arrives between reading the MSB and the LSB byte.

6.4 System registers

6.4.1 0x0B: SYSMOD, System Mode Register

The System mode register indicates the current device operating mode. Applications using the Auto-SLEEP/WAKE mechanism should use this register to synchronize the application with the device operating mode transitions.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SYSMOD1	SYSMOD0

Figure 22. 0x0B: SYSMOD, System Mode Register (Read Only)

Table 14. SYSMOD register

Field	Description
SYSMOD[1:0]	**System Mode**. Default value: 00. 00: STANDBY mode 01: WAKE mode 10: SLEEP mode

6.4.2 0x0C: INT_SOURCE, System Interrupt Status Register

In the interrupt source register the status of the various embedded features can be determined. The bits that are set (logic '1') indicate which function has asserted an interrupt and conversely the bits that are cleared (logic '0') indicate which function has not asserted or has de-asserted an interrupt. **The bits are set by a low to high transition and are cleared by reading the appropriate interrupt source register.**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRC_ASLP	0	0	SRC_LNDPRT	0	SRC_FF_MT	0	SRC_DRDY

Figure 23. 0x0C: INT_SOURCE, System Interrupt Status Register (Read Only)

Table 15. INT_SOURCE register

Field	Description
SRC_ASLP	**Auto-SLEEP/WAKE interrupt status bit**. Default value: 0. • Logic '1' indicates that an interrupt event that can cause a WAKE to SLEEP or SLEEP to WAKE system mode transition has occurred. • Logic '0' indicates that no WAKE to SLEEP or SLEEP to WAKE system mode transition interrupt event has occurred. **WAKE to SLEEP** transition occurs when no interrupt occurs for a time period that exceeds the user specified limit (ASLP_COUNT). This causes the system to transition to a user specified low ODR setting. **SLEEP to WAKE** transition occurs when the user specified interrupt event has woken the system; thus causing the system to transition to a user specified high ODR setting. • Reading the SYSMOD register clears the SRC_ASLP bit.
SRC_LNDPRT	**Portrait/Landscape Orientation interrupt status bit**. Default value: 0. Logic '1' indicates that an interrupt was generated due to a change in the device orientation status. Logic '0' indicates that no change in orientation status was detected. • This bit is asserted whenever **"**NEWLP**"** bit in the PL_STATUS is asserted and the interrupt has been enabled. • This bit is cleared by reading the PL_STATUS register.
SRC_FF_MT	**Freefall/Motion interrupt status bit**. Default value: 0. Logic '1' indicates that the Freefall/Motion function interrupt is active. Logic '0' indicates that no Freefall or Motion event was detected. • This bit is asserted whenever "EA" bit in the FF_MT_SRC register is asserted and the FF_MT interrupt has been enabled. • This bit is cleared by reading the FF_MT_SRC register.
SRC_DRDY	**Data Ready Interrupt bit status**. Default value: 0. Logic '1' indicates that the X, Y, Z data ready interrupt is active indicating the presence of new data and/or data overrun. Otherwise if it is a logic '0' the X, Y, Z interrupt is not active. • This bit is asserted when the ZYXOW and/or ZYXDR is set and the interrupt has been enabled. • This bit is cleared by reading the X, Y, and Z data. It is not cleared by simply reading the Status Register (0x00).

6.4.3 0x0D: WHO_AM_I, Device ID Register

The device identification register identifies the part. The default value is 0x5A. This value is factory programmed. Consult the factory for custom alternate values.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	1	0	1	0

Figure 24. 0x0D: WHO_AM_I, Device ID Register (Read Only)

6.4.4 0x0E: XYZ_DATA_CFG Register

The XYZ_DATA_CFG register sets the dynamic range.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	FS1	FS0

Figure 25. 0x0E: XYZ_DATA_CFG Register (Read/Write)

Table 16. XYZ_DATA_CFG register

Field	Description
FS[1:0]	**Output buffer data format full scale**. Default value: 00 (2g).

The default full scale value range is 2g.

Table 17. Full Scale Range

FS1	FS0	Full Scale Range
0	0	2g
0	1	4g
1	0	8g
1	1	Reserved

6.5 Portrait/Landscape embedded function registers

For more details on the meaning of the different user configurable settings and for example code refer to Freescale application note AN4078.

6.5.1 0x10: PL_STATUS, Portrait/Landscape Status Register

This status register can be read to get updated information on any change in orientation by reading Bit 7, or on the specifics of the orientation by reading the other bits. For further understanding of Portrait Up, Portrait Down, Landscape Left, Landscape Right, Back and Front orientations please refer to Figure 3 "Landscape/Portrait orientation". The interrupt is cleared when reading the PL_STATUS register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NEWLP	LO	0	0	0	LAPO[1]	LAPO[0]	BAFRO

Figure 26. 0x10: PL_STATUS, Portrait/Landscape Status Register (Read Only)

Table 18. PL_STATUS register

Field	Description
NEWLP	**Portrait/Landscape status change flag**. Default value: 0. 0: No change 1: BAFRO and/or LAPO and/or Z-Tilt lockout value has changed
LO	**Z-Tilt Angle Lockout**. Default value: 0. 0: Lockout condition has not been detected 1: Z-Tilt lockout trip angle has been exceeded. Lockout has been detected.
LAPO[1:0](1)	**Landscape/Portrait orientation**. Default value: 00 00: Portrait Up: Equipment standing vertically in the normal orientation 01: Portrait Down: Equipment standing vertically in the inverted orientation 10: Landscape Right: Equipment is in landscape mode to the right 11: Landscape Left: Equipment is in landscape mode to the left
BAFRO	**Back or Front orientation**. Default value: 0 0: Front: Equipment is in the front facing orientation 1: Back: Equipment is in the back facing orientation

1. *The default power up state is BAFRO = 0, LAPO = 0, and LO = 0.*

- NEWLP is set to 1 after the first orientation detection after a STANDBY to ACTIVE transition, and whenever a change in LO, BAFRO, or LAPO occurs.
- NEWLP bit is cleared anytime PL_STATUS register is read.
- The Orientation mechanism state change is limited to a maximum 1.25g.
- LAPO BAFRO and LO continue to change when NEWLP is set.
- The current position is locked if the absolute value of the acceleration experienced on any of the three axes is greater than 1.25g.

6.5.2 0x11: PL_CFG, Portrait/Landscape Configuration Register

This register enables the Portrait/Landscape function and sets the behavior of the debounce counter.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	PL_EN	0	0	0	0	0	0

Figure 27. 0x11: PL_CFG, Portrait/Landscape Configuration Register (Read/Write)

Table 19. PL_CFG register

Field	Description
DBCNTM	**Debounce counter mode selection**. Default value: 1 0: Decrements debounce whenever condition of interest is no longer valid 1: Clears counter whenever condition of interest is no longer valid.
PL_EN	**Portrait/Landscape Detection Enable**. Default value: 0 0: Portrait/Landscape Detection is Disabled 1: Portrait/Landscape Detection is Enabled

6.5.3 0x12: PL_COUNT, Portrait/Landscape Debounce Counter Register

This register sets the debounce count for the orientation state transition. The minimum debounce latency is determined by the data rate set by the product of the selected system ODR and PL_COUNT registers. Any transition from WAKE to SLEEP or vice versa resets the internal Landscape/Portrait debounce counter.

NOTE

The debounce counter weighting (time step) changes based on the ODR and the Oversampling mode. Table 21, “PL_COUNT Relationship with the ODR" explains the time step value for all sample rates and all Oversampling modes.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE[2]	DBNCE[1]	DBNCE[0]

Figure 28. 0x12: PL_COUNT, Portrait/Landscape Debounce Counter Register (Read/Write)

Table 20. PL_COUNT register

Field	Description
DBCNE[7:0]	**Debounce Count value**. Default value: 0000_0000.

Table 21. PL_COUNT Relationship with the ODR

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

6.5.4 0x13: PL_BF_ZCOMP, Back/Front and Z Compensation Register

The Z-Lock angle compensation bits allow the user to operate the device at the default, the Z-lockout angle is fixed to 30° upon power up. The Back to Front trip angle is fixed to ±75°.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	1	0	0

Figure 29. 0x13: PL_BF_ZCOMP, Back/Front and Z Compensation Register (Read Only)

Table 22. PL_BF_ZCOMP register

Field	Description
0100 0100	

6.5.5 0x14: PL_THS_REG, Portrait/Landscape Threshold and Hysteresis Register

This register represents the Portrait to Landscape trip threshold register used to set the trip angle for transitioning from Portrait to Landscape and Landscape to Portrait. This register includes a value for the hysteresis.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	0	0	1	0	0

Figure 30. 0x14: PL_THS_REG, Portrait/Landscape Threshold and Hysteresis Register (Read Only)

:

Table 23. PL_THS_REG register

Field	Description
1000 0100	

6.6 Motion and Freefall embedded function registers

The freefall/motion function can be configured in either Freefall or Motion Detection mode via the **OAE** configuration bit (0x15: FF_MTG_CFG, bit 6). The freefall/motion detection block can be disabled by setting all three bits ZEFE, YEFE, and XEFE to zero.

Depending on the register bits **ELE** (0x15: FF_MTG_CFG, bit 7) and **OAE** (0x15: FF_MTG_CFG, bit 6), each of the freefall and motion detection block can operate in four different modes:

6.6.1 Motion and freefall mode

6.6.1.1 Mode 1: Freefall Detection with ELE = 0, OAE = 0

In this mode, the **EA** bit (0x16: FF_MTG_SRC, bit 7) indicates a freefall event after the debounce counter is complete. The ZEFE, YEFE, and XEFE control bits determine which axes are considered for the freefall detection. Once the EA bit is set, and DBCNTM = 0, the EA bit can get cleared only after the delay specified by FF_MT_COUNT. This is because the counter is in decrement mode. If DBCNTM = 1, the EA bit is cleared as soon as the freefall condition disappears, and will not be set again before the delay specified by FF_MT_COUNT has passed. Reading the FF_MT_SRC register does not clear the EA bit. The event flags (0x16) ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e. high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set.

6.6.1.2 Mode 2: Freefall Detection with ELE = 1, OAE = 0

In this mode, the **EA** event bit indicates a freefall event after the debounce counter. Once the debounce counter reaches the time value for the set threshold, the EA bit is set, and remains set until the FF_MT_SRC register is read. When the FF_MT_SRC register is read, the EA bit and the debounce counter are cleared and a new event can only be generated after the delay specified by FF_MT_CNT. The ZEFE, YEFE, and XEFE control bits determine which axes are considered for the freefall detection. While EA = 0, the event flags ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e., high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set. The event flags ZHE, ZHP, YHE, YHP, XHE, and XHP are latched when the EA event bit is set.

The event flags ZHE, ZHP, YHE, YHP, XHE, and XHP will start changing only after the FF_MT_SRC register has been read.

6.6.1.3 Mode 3: Motion Detection with ELE = 0, OAE = 1

In this mode, the **EA** bit indicates a motion event after the debounce counter time is reached. The ZEFE, YEFE, and XEFE control bits determine which axes are taken into consideration for motion detection. Once the **EA** bit is set, and DBCNTM = 0, the EA bit can get cleared only after the delay specified by FF_MT_COUNT. If DBCNTM = 1, the **EA** bit is cleared as soon as the motion high g condition disappears.

The event flags ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e., high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set. Reading the FF_MT_SRC does not clear any flags, nor is the debounce counter reset.

6.6.1.4 Mode 4: Motion Detection with ELE = 1, OAE = 1

In this mode, the EA bit indicates a motion event after debouncing. The ZEFE, YEFE, and XEFE control bits determine which axes are taken into consideration for motion detection. Once the debounce counter reaches the threshold, the EA bit is set, and remains set until the FF_MT_SRC register is read. When the FF_MT_SRC register is read, all register bits are cleared and the debounce counter are cleared and a new event can only be generated after the delay specified by FF_MT_CNT.

While the bit EA is zero, the event flags ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e., high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set. When the EA bit is set, these bits keep their current value until the FF_MT_SRC register is read.

6.6.2 0x15: FF_MT_CFG, Freefall/Motion Configuration Register

This is the Freefall/Motion configuration register for setting up the conditions of the freefall or motion function.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ELE	OAE	ZEFE	YEFE	XEFE	0	0	0

Figure 31. 0x15: FF_MT_CFG, Freefall/Motion Configuration Register (Read/Write)

Table 24. FF_MT_CFG register

Field	Description
ELE	**Event Latch Enable**: Event flags are latched into FF_MT_SRC register. Reading of the FF_MT_SRC register clears the event flag EA and all FF_MT_SRC bits. Default value: 0. ELE denotes whether the enabled event flag will to be latched in the FF_MT_SRC register or the event flag status in the FF_MT_SRC will indicate the real-time status of the event. If ELE bit is set to a logic '1', then the event flags are frozen when the EA bit gets set, and are cleared by reading the FF_MT_SRC source register. 0: Event flag latch disabled 1: Event flag latch enabled
OAE	**Motion detect / Freefall detect flag selection**. Default value: 0. (Freefall Flag) OAE bit allows the selection between Motion (logical OR combination) and Freefall (logical AND combination) detection. 0: Freefall flag (Logical AND combination) 1: Motion flag (Logical OR combination)
ZEFE	**Event flag enable on Z**. Default value: 0. **ZEFE** enables the detection of a motion or freefall event when the measured acceleration data on X, Y, Z channel is beyond the threshold set in FF_MT_THS register. If the ELE bit is set to logic '1' in the FF_MT_CFG register new event flags are blocked from updating the FF_MT_SRC register. 0: Event detection disabled 1: Raise event flag on measured acceleration value beyond preset threshold
YEFE	**Event flag enable on Y event**. Default value: 0. **YEFE** enables the detection of a motion or freefall event when the measured acceleration data on X, Y, Z channel is beyond the threshold set in FF_MT_THS register. If the ELE bit is set to logic '1' in the FF_MT_CFG register new event flags are blocked from updating the FF_MT_SRC register. 0: Event detection disabled 1: Raise event flag on measured acceleration value beyond preset threshold
XEFE	**Event flag enable on X event**. Default value: 0. **XEFE** enables the detection of a motion or freefall event when the measured acceleration data on X, Y, Z channel is beyond the threshold set in FF_MT_THS register. If the ELE bit is set to logic '1' in the FF_MT_CFG register new event flags are blocked from updating the FF_MT_SRC register. 0: Event detection disabled 1: Raise event flag on measured acceleration value beyond preset threshold

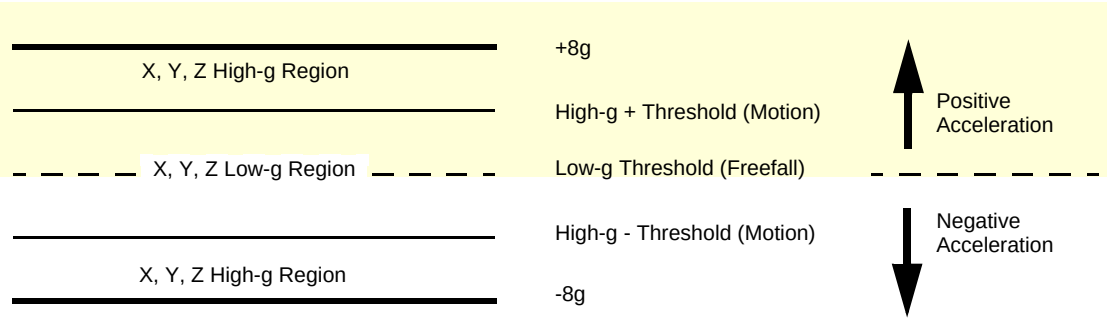


Figure 32. FF_MT_CFG high and low g Level

6.6.3 0x16: FF_MT_SRC, Freefall/Motion Source Status Register

This register keeps track of the acceleration event which is triggering (or has triggered, in case of ELE bit in FF_MT_CFG register being set to 1) the event flag. In particular EA is set to a logic ‘1’ when the logical combination of acceleration events flags specified in FF_MT_CFG register is true. This bit is used in combination with the values in INT_EN_FF_MT and INT_CFG_FF_MT register bits to generate the freefall/motion interrupts.

An X,Y, or Z motion is true when the acceleration value of the X or Y or Z channel is higher than the preset threshold value defined in the FF_MT_THS register.

Conversely an X, Y, and Z low event is true when the acceleration value of the X and Y and Z channel is lower than the preset threshold value defined in the FF_MT_THS register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EA	0	ZHE	ZHP	YHE	YHP	XHE	XHP

Figure 33. 0x16: FF_MT_SRC, Freefall and Motion Source Status Register (Read Only)

Table 25. FF_MT_SRC register

Field	Description
EA	**Event Active Flag**. Default value: 0. 0: No event flag has been asserted 1: One or more event flag has been asserted. See the description of the OAE bit to determine the effect of the 3-axis event flags on the EA bit.
ZHE	**Z Motion Flag**. Default value: 0. 0: No Z Motion event detected 1: Z Motion has been detected This bit reads always zero if the ZEFE control bit is set to zero
ZHP	**Z Motion Polarity Flag**. Default value: 0. 0: Z event was Positive g, 1: Z event was Negative g This bit read always zero if the ZEFE control bit is set to zero
YHE	**Y Motion Flag**. Default value: 0. 0: No Y Motion event detected 1: Y Motion has been detected This bit read always zero if the YEFE control bit is set to zero
YHP	**Y Motion Polarity Flag**. Default value: 0 0: Y event detected was Positive g 1: Y event was Negative g This bit reads always zero if the YEFE control bit is set to zero
XHE	**X Motion Flag**. Default value: 0 0: No X Motion event detected 1: X Motion has been detected This bit reads always zero if the XEFE control bit is set to zero
XHP	**X Motion Polarity Flag**. Default value: 0 0: X event was Positive g 1: X event was Negative g This bit reads always zero if the XEFE control bit is set to zero

6.6.4 0x17: FF_MT_THS, Freefall and Motion Threshold Register

FF_MT_THS is the threshold register used to detect freefall motion events.

- The unsigned 7-bit FF_MT_THS threshold register holds the threshold for the freefall detection **where the magnitude of the X and Y and Z acceleration values is lower than the threshold value**.
- Conversely, the FF_MT_THS also holds the threshold for the motion detection **where the magnitude of the X or Y or Z acceleration value is higher than the threshold value**.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Figure 34. 0x17: FF_MT_THS, Freefall and Motion Threshold Register (Read/Write)

Table 26. FF_MT_THS Bit Descriptions

Field	Description
DBCNTM	**Debounce counter mode selection**. Default value: 0. 0: increments or decrements debounce, 1: increments or clears counter.
THS[7:1]	**Freefall /Motion Threshold**: Default value: 000_0000.

The threshold resolution is 0.063g/LSB and the threshold register has a range of 0 to 127 counts. The maximum range is to 8g. Note that even when the full scale value is set to 2g or 4g the motion detects up to 8g.

DBCNTM bit configures the way in which the debounce counter is reset when the inertial event of interest is momentarily not true.

- **When DBCNTM bit is '1'**, the debounce counter is cleared to 0 whenever the inertial event of interest is no longer true as shown in Figure 36 "DBCNTM bit function", (b).
- **While the DBCNTM bit is set to logic '0'**, the debounce counter is decremented by 1 whenever the inertial event of interest is no longer true (Figure 36 "DBCNTM bit function", (c)) until the debounce counter reaches 0 or the inertial event of interest becomes active.

Decrementing the debounce counter acts as a median enabling the system to filter out irregular spurious events which might impede the detection of inertial events.

6.6.5 0x18: FF_MT_COUNT, Debounce Register

This register sets the number of debounce sample counts for the event trigger.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 35. 0x18 FF_MT_COUNT, Debounce Register (Read/Write)

Table 27. FF_MT_COUNT register

Field	Description
D[7:0]	**Count value**. Default value: 0000_0000

This register sets the minimum number of debounce sample counts of continuously matching the detection condition user selected for the freefall, motion event.

When the internal debounce counter reaches the FF_MT_COUNT value a Freefall/Motion event flag is set. The debounce counter will never increase beyond the FF_MT_COUNT value. Time step used for the debounce sample count depends on the ODR chosen and the Oversampling mode as shown in Table 28, “FF_MT_COUNT Relationship with the ODR".

Table 28. FF_MT_COUNT Relationship with the ODR

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

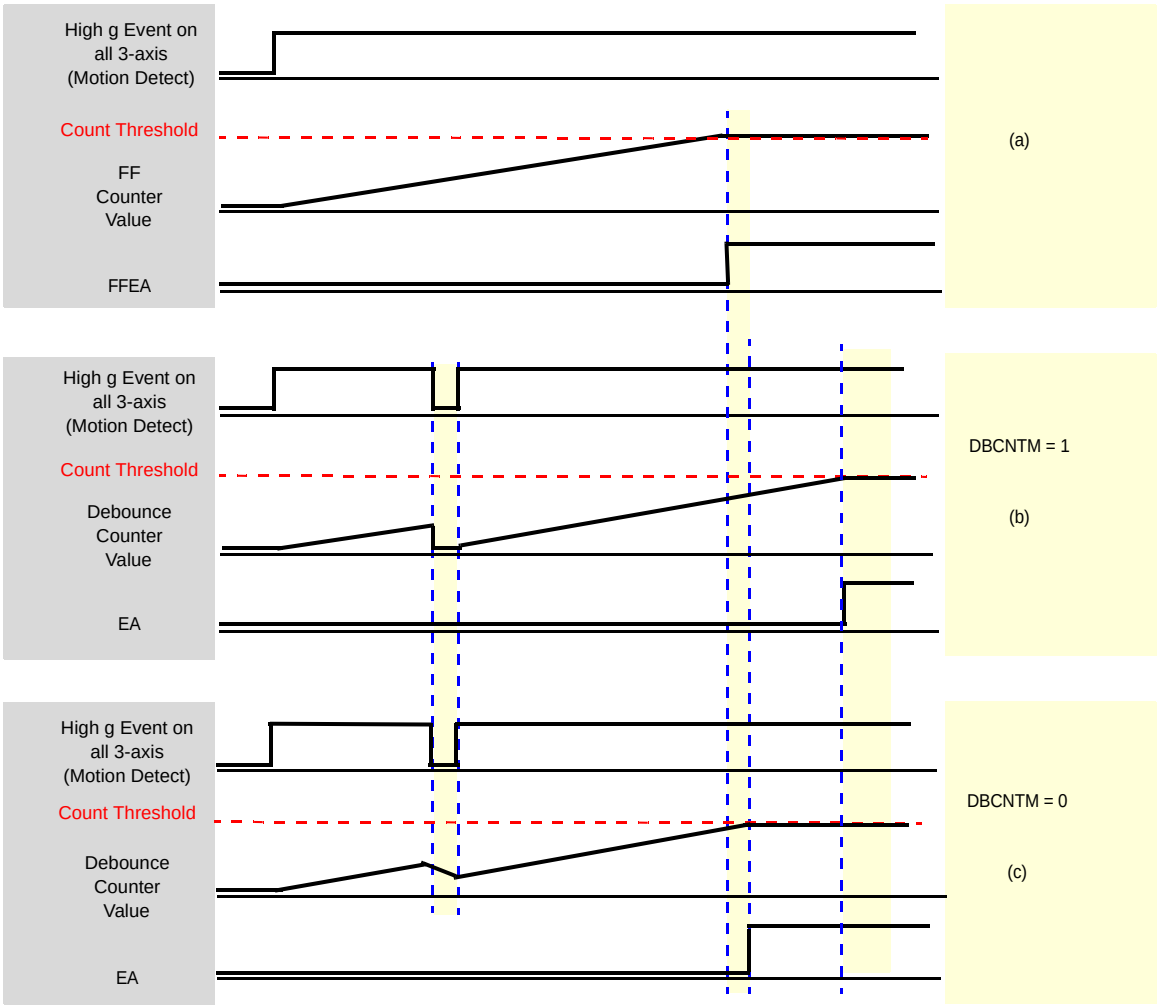


Figure 36. DBCNTM bit function

6.7 Auto-WAKE/SLEEP Detection

6.7.1 0x29: ASLP_COUNT, Auto-WAKE/SLEEP Detection Register (Read/Write)

The ASLP_COUNT register sets the minimum time period of inactivity required to change the current ODR value, from the value specified in the **DR[2:0]** register to **ASLP_RATE** register value, provided that the **SLPE** bit is set to a logic '1' in the **CTRL_REG2** register. See Table 30, "ASLP_COUNT Relationship with ODR" for functional blocks that may be monitored for inactivity in order to trigger the "return to SLEEP" event.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 37. 0x29: ASLP_COUNT Auto-WAKE/SLEEP Detection Register (Read/Write)

Table 29. ASLP_COUNT register

Field	Description
D[7:0]	**Duration value**. Default value: 0000_0000.

D7-D0 defines the minimum duration time to change current ODR value from **DR** to **ASLP_RATE**. Time step and maximum value depend on the ODR chosen as shown in Table 30, "ASLP_COUNT Relationship with ODR".

Table 30. ASLP_COUNT Relationship with ODR

Output Data Rate (ODR)	Duration	ODR Time Step	ASLP_COUNT Step
800 Hz	0 to 81s	1.25 ms	320 ms
400 Hz	0 to 81s	2.5 ms	320 ms
200 Hz	0 to 81s	5 ms	320 ms
100 Hz	0 to 81s	10 ms	320 ms
50 Hz	0 to 81s	20 ms	320 ms
12.5 Hz	0 to 81s	80 ms	320 ms
6.25 Hz	0 to 81s	160 ms	320 ms
1.56 Hz	0 to 162s	640 ms	640 ms

Table 31. SLEEP/WAKE Mode Gates and Triggers

Interrupt Source	Event restarts timer and delays Return to SLEEP	Event will WAKE from SLEEP
SRC_LNDPRT	Yes	Yes
SRC_FF_MT	Yes	Yes
SRC_ASLP	No	No
SRC_DRDY	No	No

In order to wake the device, the desired functions must be enabled in CTRL_REG4 and set to WAKE from SLEEP in CTRL_REG3. All enabled functions will still function in SLEEP mode at the SLEEP ODR. Only the functions that have been selected for WAKE from SLEEP will **WAKE** the device.

MMA8653FC has 2 functions that can be used to keep the sensor from falling asleep namely, Orientation, and Motion/Freefall. One or more of these functions can be enabled. To WAKE the device, 2 functions are provided : Orientation, and the Motion/Freefall. The Auto-WAKE/SLEEP interrupt does not affect the WAKE/SLEEP, nor does the data ready interrupt.

If the Auto-SLEEP bit is disabled, then the device can only toggle between STANDBY and WAKE mode. If Auto-SLEEP interrupt is enabled, transitioning from ACTIVE mode to Auto-SLEEP mode and vice versa generates an interrupt.

6.8 Control registers

NOTE

Except for STANDBY mode selection, the device must be in STANDBY mode to change any of the fields within CTRL_REG1 (0x2A).

6.8.1 0x2A: CTRL_REG1, System Control 1 Register

This register configures the Auto-WAKE sample frequency, data rate selection, and enables the fast read mode and STANDBY/ACTIVE selection.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	0	F_READ	ACTIVE

Figure 38. 0x2A: CTRL_REG1, System Control 1 Register (Read/Write)

Table 32. CTRL_REG1 register

Field	Description
ASLP_RATE[1:0]	**Configures the Auto-WAKE sample frequency when the device is in SLEEP Mode**. Default value: 00. See Table 33, “SLEEP Mode Rates".
DR[2:0]	**Data rate selection**. Default value: 000. See Table 34, “System Output Data Rate Selection ".
F_READ	**Fast Read mode**: Data format limited to single Byte Default value: 0. 0: Normal mode 1: Fast Read mode
ACTIVE	**STANDBY/ACTIVE selection**. Default value: 00. 0: STANDBY mode 1: ACTIVE mode

Table 33. SLEEP Mode Rates

ASLP_RATE1	ASLP_RATE0	Frequency (Hz)	Notes
0	0	50	When the device is in Auto-SLEEP mode, the system ODR and the data rate for all the system functional blocks are overridden by the data rate set by the ASLP_RATE field.
0	1	12.5	
1	0	6.25	
1	1	1.56	

DR[2:0] bits select the Output Data Rate (ODR) for acceleration samples in WAKE mode. The default value is **000 for a data rate of 800 Hz.**

Table 34. System Output Data Rate Selection

DR2	DR1	DR0	ODR	Period	Notes
0	0	0	800 Hz	1.25 ms	default (STANDBY mode)
0	0	1	400 Hz	2.5 ms	
0	1	0	200 Hz	5 ms	
0	1	1	100 Hz	10 ms	
1	0	0	50 Hz	20 ms	
1	0	1	12.5 Hz	80 ms	
1	1	0	6.25 Hz	160 ms	
1	1	1	1.56 Hz	640 ms	

ACTIVE bit selects between STANDBY mode and ACTIVE mode.

Table 35. Full Scale Selection

Active	Mode
0	STANDBY (default)
1	ACTIVE

F_Read bit selects between normal and Fast Read mode. When selected, the address auto-increment will skip over the LSB data bytes.

6.8.2 0x2B: CTRL_REG2, System Control 2 Register

This register is used enable Self-Test, Software Reset, and Auto-Sleep. In addition, it enables you to configure the SLEEP and WAKE mode power scheme selection.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ST	RST	—	SMODS1	SMODS0	SLPE	MODS1	MODS0

Figure 39. 0x2B: CTRL_REG2, System Control 2 Register (Read/Write)

Table 36. CTRL_REG2 register

Field	Description
ST	**Self-Test Enable**. Default value: 0. ST bit activates the self-test function. When ST is set, X, Y, and Z outputs will shift. RST bit is used to activate the software reset. The reset mechanism can be enabled in STANDBY and ACTIVE mode. 0: Self-Test disabled 1: Self-Test enabled
RST	**Software Reset.** Default value: 0. 0: Device reset disabled 1: Device reset enabled.
SMODS[1:0]	**SLEEP mode power scheme selection**. Default value: 00. See Table 37, “MODS Oversampling Modes" and Table 38, “MODS Oversampling Modes Current Consumption and Averaging Values at each ODR"
SLPE	**Auto-SLEEP enable**. Default value: 0. 0: Auto-SLEEP is not enabled; 1: Auto-SLEEP is enabled.
MODS[1:0]	**WAKE mode power scheme selection.** Default value: 00. See Table 37, “MODS Oversampling Modes" and Table 38, “MODS Oversampling Modes Current Consumption and Averaging Values at each ODR"

When the reset bit is enabled, all registers are rest and are loaded with default values. Writing ‘1’ to the RST bit immediately resets the device, no matter whether it is in ACTIVE/WAKE, ACTIVE/SLEEP, or STANDBY mode.

The I^2C communication system is reset to avoid accidental corrupted data access.

At the end of the boot process the RST bit is de-asserted to 0. Reading this bit will return a value of zero.

The **(S)MODS[1:0]** bits select which Oversampling mode is to be used shown in Table 37, “MODS Oversampling Modes". The Oversampling modes are available in both WAKE Mode MOD[1:0] and also in the SLEEP Mode SMOD[1:0].

Table 37. MODS Oversampling Modes

(S)MODS1	(S)MODS0	Power Mode
0	0	Normal
0	1	Low Noise Low Power
1	0	High Resolution
1	1	Low Power

Table 38. MODS Oversampling Modes Current Consumption and Averaging Values at each ODR

ODR	Mode							
	Normal (00)		Low Noise Low Power (01)		High Resolution (10)		Low Power (11)	
	Current μA	OS Ratio	Current μA	OS Ratio	Current μA	OS Ratio	Current μA	OS Ratio
1.56 Hz	TBD	128	TBD	32	TBD	1024	TBD	16
6.25 Hz	TBD	32	TBD	8	TBD	256	TBD	4
12.5 Hz	TBD	16	TBD	4	TBD	128	TBD	2
50 Hz	TBD	4	TBD	4	TBD	32	TBD	2

Table 38. MODS Oversampling Modes Current Consumption and Averaging Values at each ODR (Continued)

ODR	Mode							
	Normal (00)		Low Noise Low Power (01)		High Resolution (10)		Low Power (11)	
	Current μA	OS Ratio	Current μA	OS Ratio	Current μA	OS Ratio	Current μA	OS Ratio
100 Hz	TBD	4	TBD	4	TBD	16	TBD	2
200 Hz	TBD	4	TBD	4	TBD	8	TBD	2
400 Hz	TBD	4	TBD	4	TBD	4	TBD	2
800 Hz	TBD	2	TBD	2	TBD	2	TBD	2

Note: TBD current values will be added later.

6.8.3 0x2C: CTRL_REG3, System Control 3 Register

This register is used to control the Auto-WAKE/SLEEP function by setting the orientation or Freefall/Motion as an interrupt to wake up. This register also configures the interrupt pins INT1 and INT2.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	WAKE_LNDPRT	—	WAKE_FF_MT	0	IPOL	PP_OD

Figure 40. 0x2C CTRL_REG3, System Control 3 Register (Read/Write)

Table 39. CTRL_REG3 register

Field	Description
WAKE_LNDPRT	0: Orientation function is bypassed in SLEEP mode. Default value: 0. 1: Orientation function interrupt can wake up system
WAKE_FF_MT	0: Freefall/Motion function is bypassed in SLEEP mode. Default value: 0. 1: Freefall/Motion function interrupt can wake up
IPOL	**Interrupt polarity ACTIVE high, or ACTIVE low**. Default value: 0. IPOL bit selects the polarity of the interrupt signal. When IPOL is '0' (default value) any interrupt event will signaled with a logical 0. 0: ACTIVE low 1: ACTIVE high
PP_OD	**Push-Pull/Open Drain selection on interrupt pad**. Default value: 0. PP_OD bit configures the interrupt pin to Push-Pull or in Open Drain mode. The default value is 0 which corresponds to Push-Pull mode. The Open Drain configuration can be used for connecting multiple interrupt signals on the same interrupt line. 0: Push-Pull 1: Open Drain

6.8.4 0x2D: CTRL_REG4, Interrupt Enable Register (Read/Write)

This register enables the following interrupts: Auto-WAKE/SLEEP, Orientation detection, Freefall/Motion, and Data Ready.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EN_ASLP	—	—	INT_EN_LNDP	—	INT_EN_FF_MT	0	INT_EN_DRDY

Figure 41. 0x2D: CTRL_REG4, Interrupt Enable Register (Read/Write)

Table 40. CTRL_REG4 register

Field	Description	
INT_EN_ASLP	**Auto-SLEEP/WAKE Interrupt Enable**	0 interrupt is disabled (default) 1 interrupt is enabled **Note:** The corresponding functional block interrupt enable bit enables the functional block to route its event detection flags to the system's interrupt controller. The interrupt controller routes the enabled functional block interrupt to the INT1 or INT2 pin.
INT_EN_LNDPRT	**Orientation (Landscape/Portrait) Interrupt Enable**	
INT_EN_FF_MT	**Freefall/Motion Interrupt Enable**	
INT_EN_DRDY	**Data Ready Interrupt Enable**	

6.8.5 0x2E: CTRL_REG5, Interrupt Configuration Register (Read/Write)

This register maps the desired interrupts to INT2 or INT1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_CFG_ASL	—	—	INT_CFG_LNDP	—	INT_CFG_FF_M	0	INT_CFG_DRD

Figure 42. 0x2E: CTRL_REG5, Interrupt Configuration Register

Table 41. CTRL_REG5 register

Field	Description	
INT_CFG_ASLP	**Auto-SLEEP/WAKE INT1/INT2 Configuration**	0 Interrupt is routed to INT2 pin (default) 1 Interrupt is routed to INT1 pin
INT_CFG_LNDPRT	**Orientation INT1/INT2 Configuration**	
INT_CFG_FF_MT	**Freefall/motion INT1/INT2 Configuration**	
INT_CFG_DRDY	**Data Ready INT1/INT2 Configuration**	

The system's interrupt controller shown in Figure 10 "System interrupt generation" uses the corresponding bit field in the CTRL_REG5 register to determine the routing table for the INT1 and INT2 interrupt pins. If the bit value is logic '0' the functional block's interrupt is routed to INT2, and if the bit value is logic '1' then the interrupt is routed to INT1. One or more functions can assert an interrupt pin; therefore a host application responding to an interrupt should read the INT_SOURCE (0x0C) register to determine the appropriate sources of the interrupt.

6.9 Data calibration registers

The 2's complement offset correction registers values are used to realign the Zero-g position of the X, Y, and Z-axis after the device is mounted on a board. The resolution of the offset registers is 1.96 mg/LSB. The 2's complement 8-bit value would result in an offset compensation range ±250 mg for each axis. 0x2F: OFF_X, Offset Correction X Register.

Bit 7	Bit 6S	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 43. 0x2F: OFF_X, Correction X Register (Read/Write)

Table 42. OFF_X register

Field	Description
D[7:0]	**X-axis offset value**. Default value: 0000_0000.

6.9.1 0x30: OFF_Y, Offset Correction Y Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 44. 0x30: OFF_Y, Offset Correction Y Register (Read/Write)

Table 43. OFF_Y register

Field	Description
D[7:0]	**Y-axis offset value**. Default value: 0000_0000.

6.9.2 0x31: OFF_Z, Offset Correction Z Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 45. 0x31: OFF_Z, Offset Correction Z Register (Read/Write)

Table 44. OFF_Z register

Field	Description
D[7:0]	**Z-axis offset value**. Default value: 0000_0000.

7 Mounting Guidelines

Surface mount printed circuit board (PCB) layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the PCB and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. These guidelines are for soldering and mounting the Dual Flat No-Lead (DFN) package inertial sensors to PCBs. The purpose is to minimize the stress on the package after board mounting. The MMA865xFC digital output accelerometers use the DFN package platform. This section describes suggested methods of soldering these devices to the PCB for consumer applications.

7.1 Overview of soldering considerations

Information provided here is based on experiments executed on DFN devices. They do not represent exact conditions present at a customer site. Therefore, this information should be used as guidance only and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

7.2 Halogen content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

7.3 PCB mounting/soldering recommendations

1. The PCB land should be designed as Non Solder Mask Defined (NSMD) as shown in Figure 46 "Package mounting measurements".
2. No additional via pattern underneath package.
3. PCB land pad is 0.6 mm x 0.225 mm as shown in Figure 46 "Package mounting measurements".
4. Solder mask opening = PCB land pad edge + 0.125 mm larger all around = 0.725 mm x 1.950 mm
5. Stencil opening = PCB land pad -0.05 mm smaller all around = 0.55 mm x 0.175 mm.
6. Stencil thickness is 100 or 125 um.
7. Do not place any components or vias at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
8. Signal traces connected to pads are as symmetric as possible. Put dummy traces on NC pads, to have same length of exposed trace for all pads.
9. Use a standard pick and place process and equipment. Do not use a hand soldering process.
10. Use caution when putting an assembled PCB into an enclosure, noting where the screw-down holes are and if any press-fitting is involved. It is important that the assembled PCB remain flat after assembly, to ensure optimal electronic operation of the device.
11. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.
12. No copper traces on top layer of PCB under the package. This will cause planarity issues with board mount. Freescale DFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

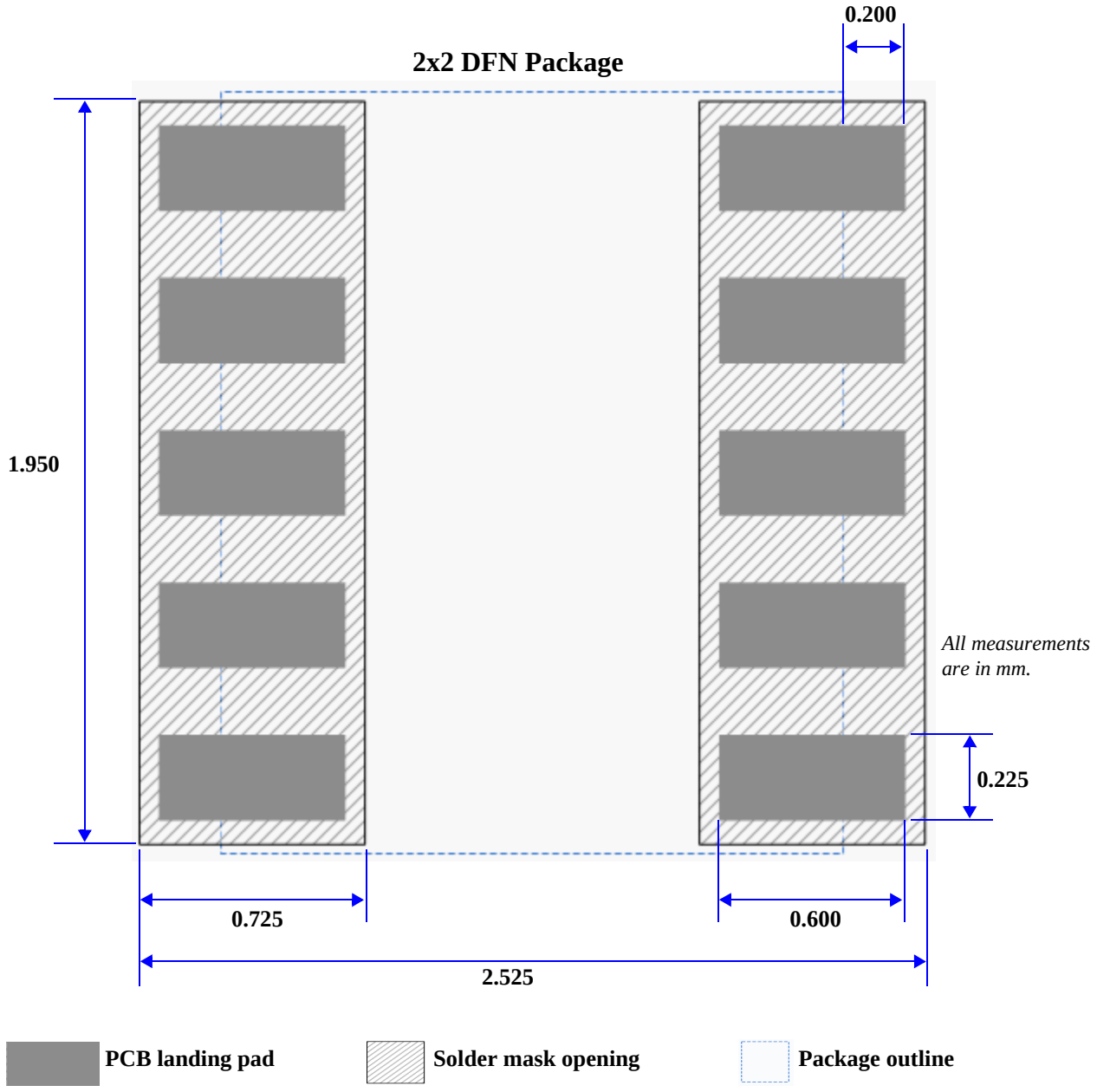


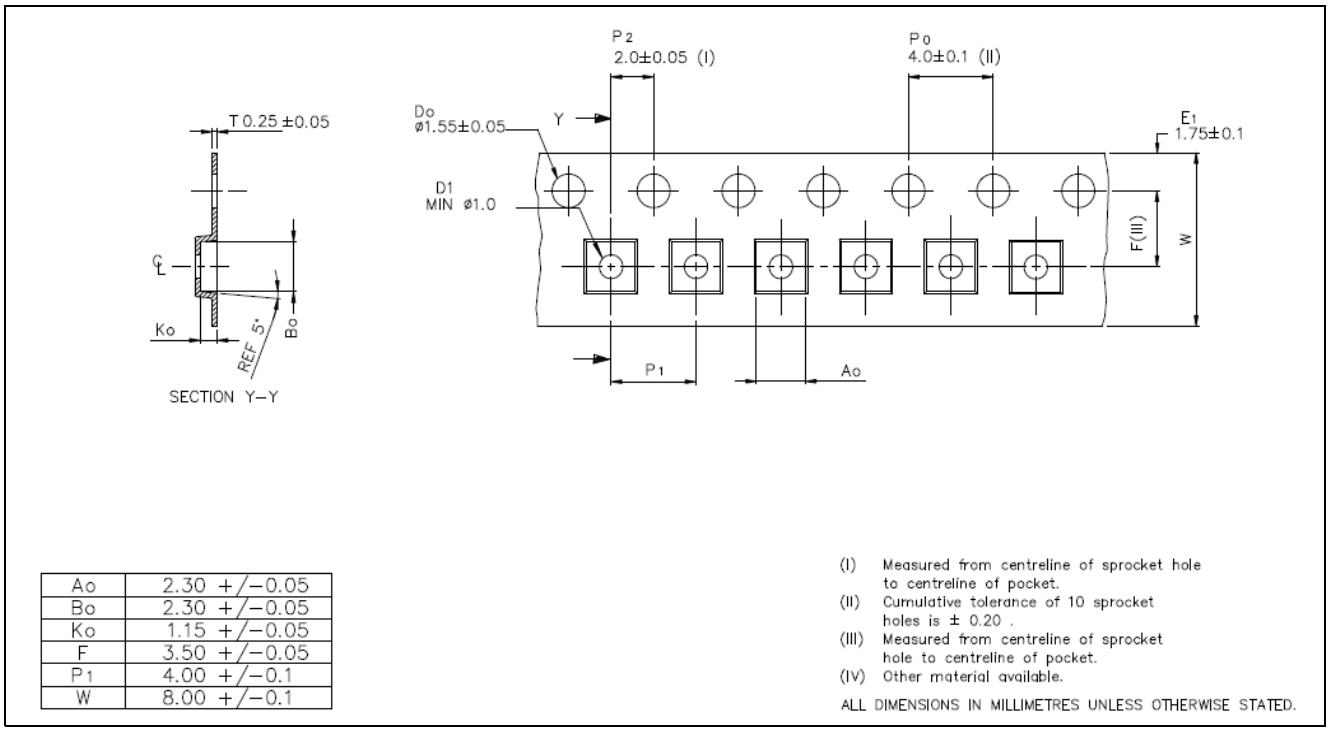
Figure 46. Package mounting measurements

Table 45. Board mounting guidelines

Description	Value (mm)
Landing Pad Width	0.225
Landing Pad Length	0.600
Solder Mask Pattern Width	0.725
Solder Mask Pattern Length	1.950
Landing Pad Extended Length	0.200
I/O Pads Extended Length	2.525

8 Tape and Reel

8.1 Tape dimensions



Ao	2.30 +/−0.05
Bo	2.30 +/−0.05
Ko	1.15 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 47. Carrier tape

8.2 Device orientation

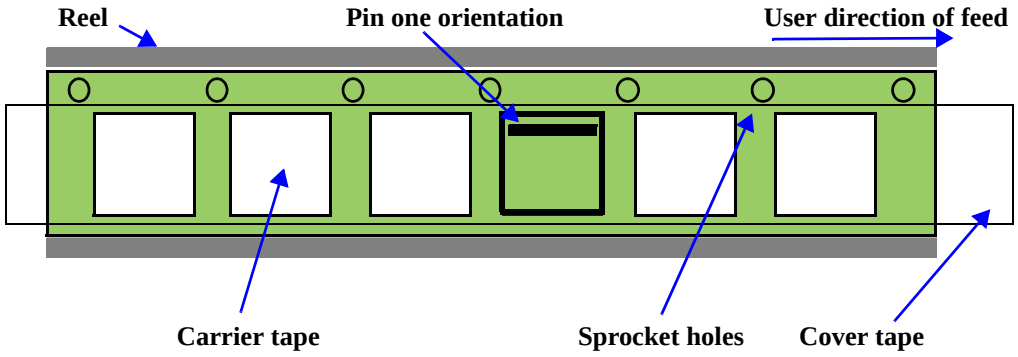


Figure 48. Device orientation on carrier tape

9 Package Dimensions

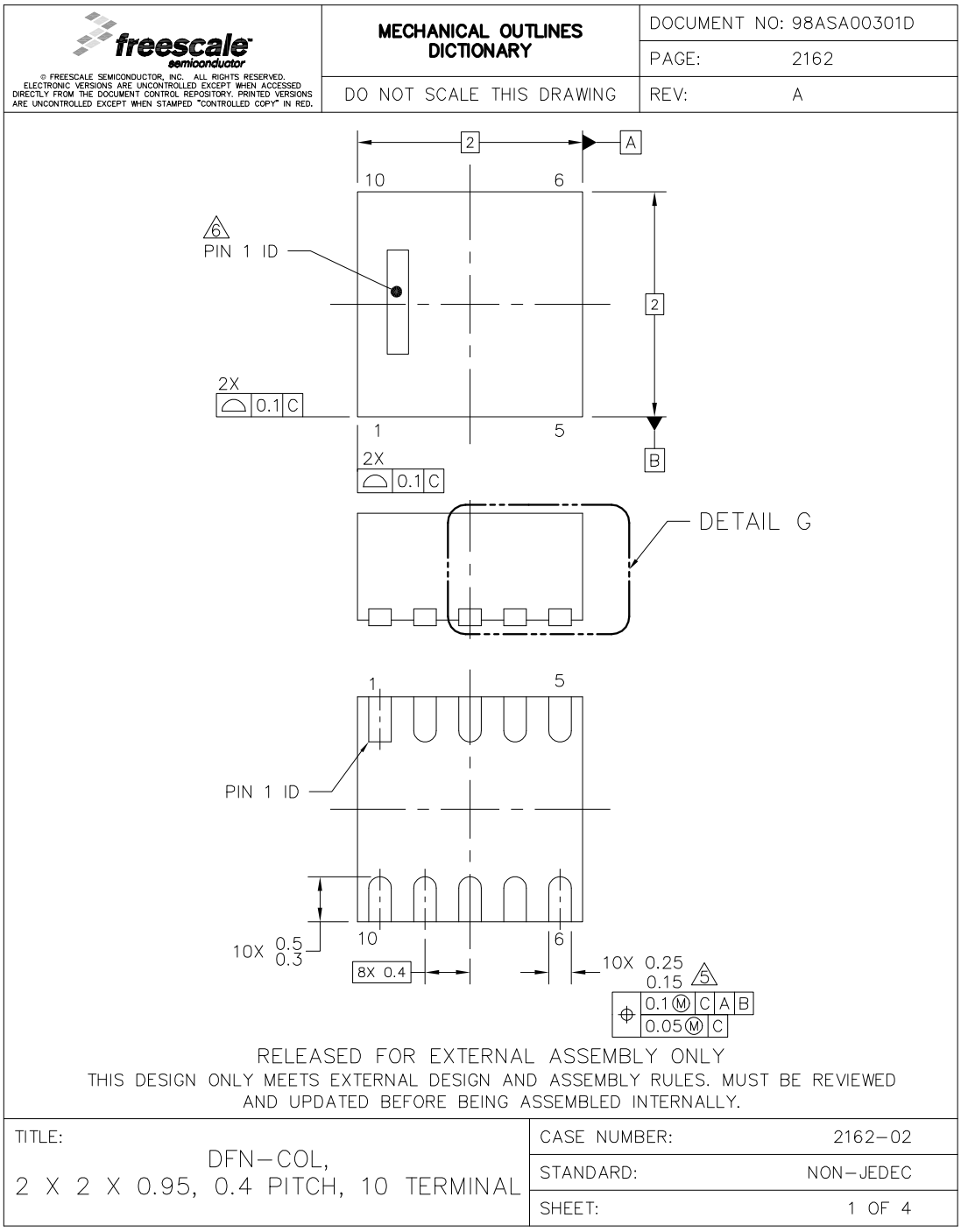


Figure 49. CASE 2162-02, ISSUE O, 10-Lead DFN—page 1

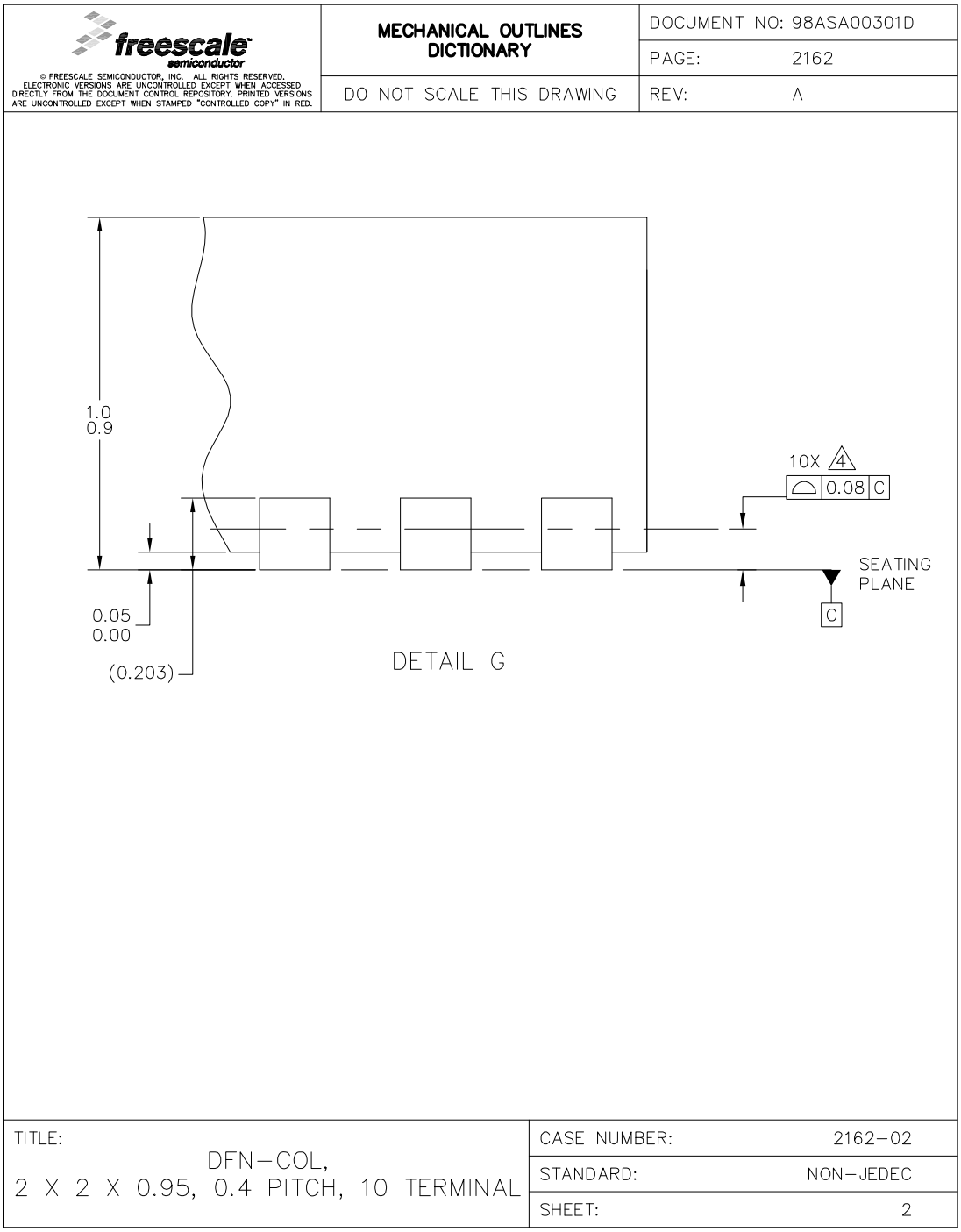


Figure 50. CASE 2162-02, ISSUE O, 10-Lead DFN—page 2

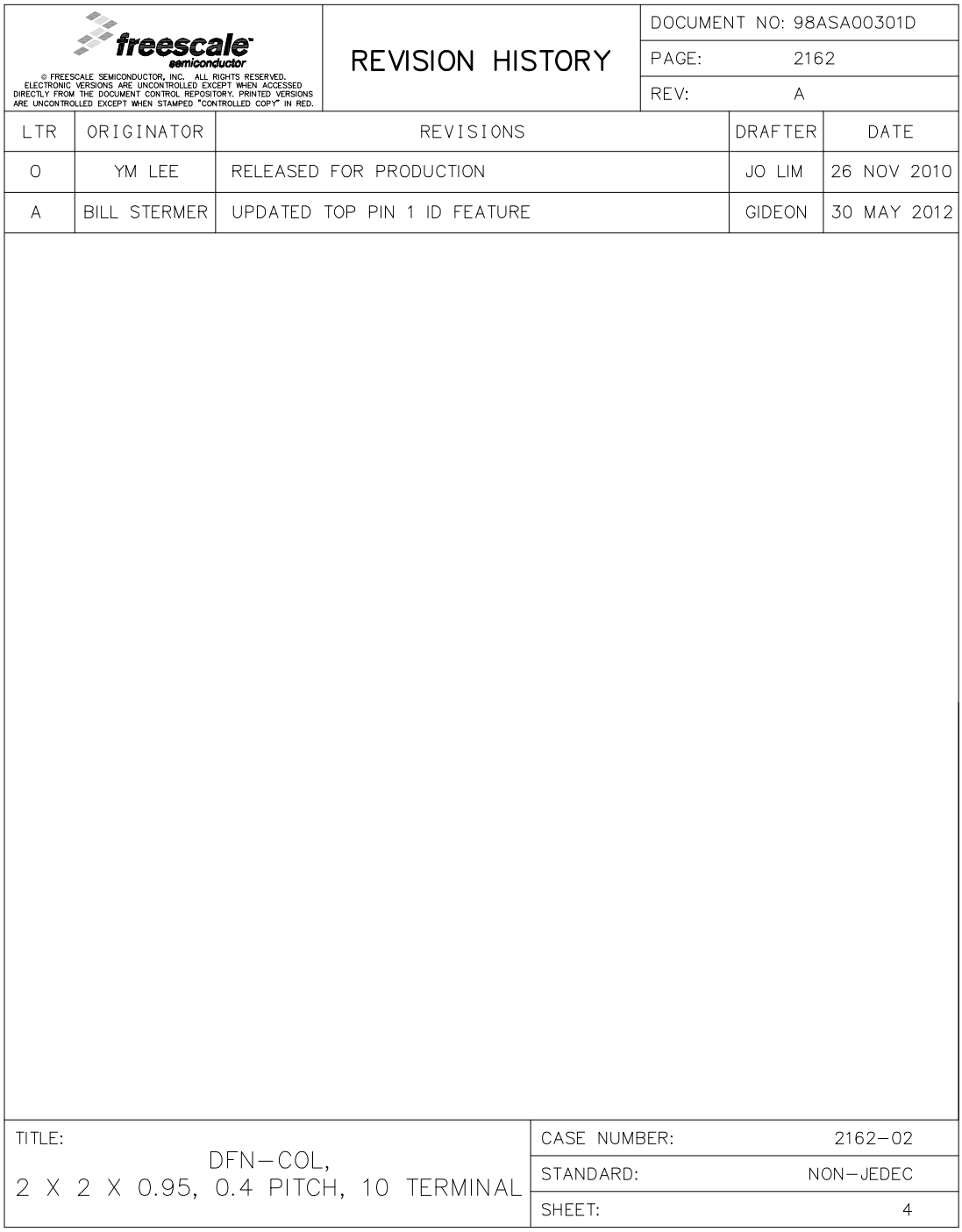
freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00301D
		PAGE: 2162
	DO NOT SCALE THIS DRAWING	REV: A

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS NON JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO ALL TERMINALS.
5. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURE BETWEEN 0.15 AND 0.25 FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHALL NOT BE MEASURED IN THE RADIUS AREA.
6. PIN 1 ID ON TOP WILL BE LASER MARKED.

TITLE: DFN–COL, 2 X 2 X 0.95, 0.4 PITCH, 10 TERMINAL	CASE NUMBER: 2162–02
	STANDARD: NON–JEDEC
	SHEET: 3

Figure 51. CASE 2162-02, ISSUE O, 10-Lead DFN—page 3



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REVISION HISTORY

DOCUMENT NO: 98ASA00301D
PAGE: 2162
REV: A

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	YM LEE	RELEASED FOR PRODUCTION	JO LIM	26 NOV 2010
A	BILL STERMER	UPDATED TOP PIN 1 ID FEATURE	GIDEON	30 MAY 2012

TITLE: DFN–COL, 2 X 2 X 0.95, 0.4 PITCH, 10 TERMINAL	CASE NUMBER: 2162–02
	STANDARD: NON–JEDEC
	SHEET: 4

Figure 52. CASE 2162-02, ISSUE O, 10-Lead DFN—page 4

10 Revision History

Table 46. Revision history MMA8653FC

Revision number	Revision date	Description of changes
0	08/2012	• Initial release

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Document Number: MMA8653FC
Rev. 0
08/2012

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