

17-27GHz High Power Amplifier

GaAs Monolithic Microwave IC

preliminary

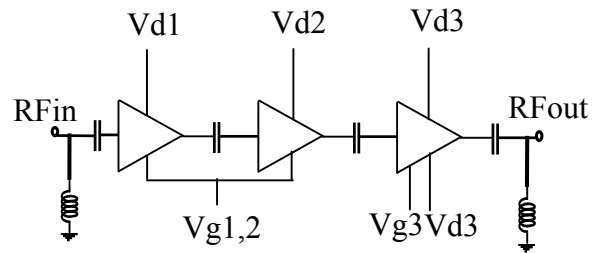
Description

The CHA5056 is three-stage monolithic high power amplifier.

The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

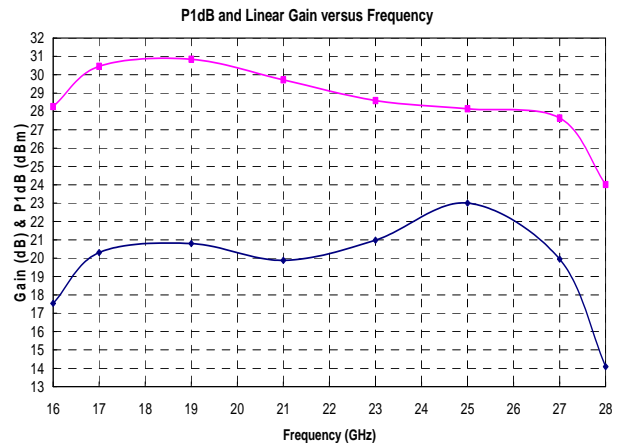
The circuit is manufactured with a power PHEMT process, 0.15µm gate length, via holes through the substrate.

It is supplied in chip form.



Main Features

- Broadband performance 17-27GHz
- 21dB Linear Gain
- ESD protected
- 29dBm Output Power @ 1dB compression
- DC power consumption @ 1dB compression: 940mA@4.5V
- Chip size: 3.15 x 2.2 x 0.1mm



Typical On Wafer Measurement

Main Characteristics

Tamb. = 25°C, Vd = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		27	GHz
G	Small signal gain		21		dB
P1dB	Output power @ 1dB gain compression		29		dBm
Id1dB	Drain current @ 1dB gain compression		940		mA

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb. = 25°C; Vd = 4,5V and Id = 890mA, CW biasing mode. These values are representative of on wafer measurements.

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		27	GHz
G	Small signal gain		21		dB
P1dB	Pulsed output power at 1dB compression (1)		29		dBm
S11	Input return loss		2.0:1		
S22	Ouput return loss		2.2:1		
OIP3	Output IP3		39		dBm
Vd 1,2,3	DC Drain Voltage		4.5		V
Vg 1-2,3	DC Gate Voltage		-1.7		V
Id	Small Signal Bias current (2)		890		mA
Id1dB	Bias current at 1dB compression		940		mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

(2) This parameter is fixed by gate voltage Vg.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage	+5	V
Id	Maximum Small Signal Bias current	1100	mA
Vg	Gate bias voltage	-4 to +0.8	V
Pin	Maximum input power overdrive	+13.0	dBm
Tch	Maximum channel temperature	+175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

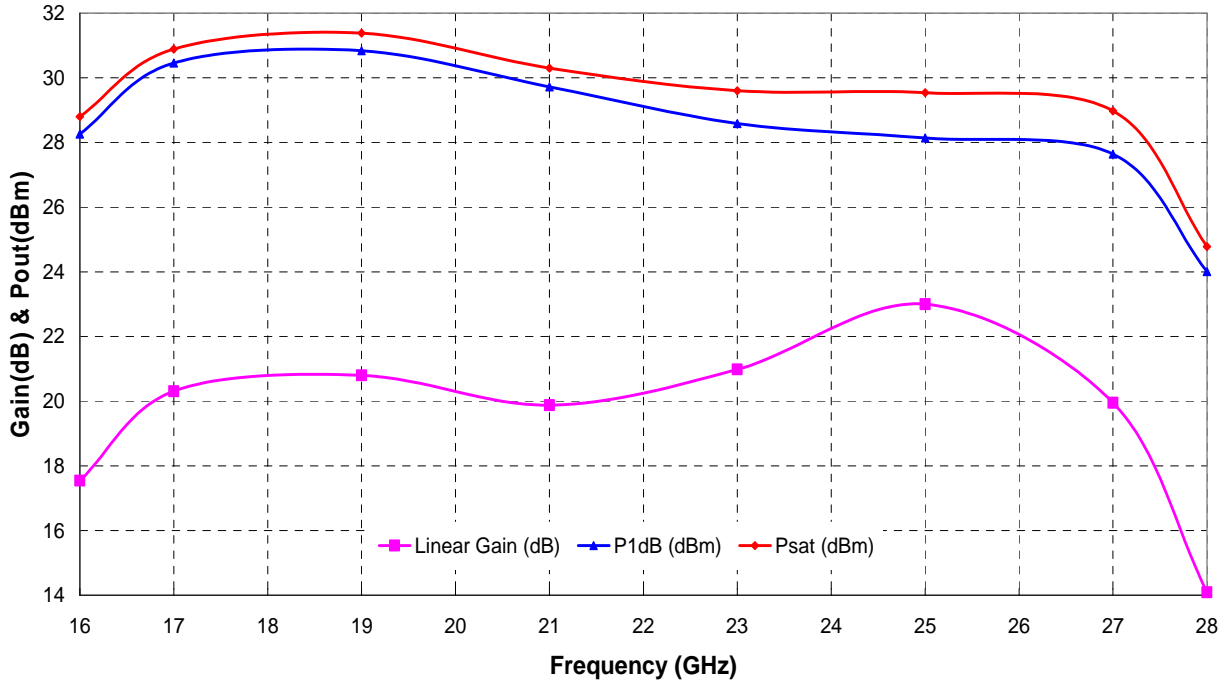
(1) Operation of this device above anyone of these parameters may cause permanent damage.

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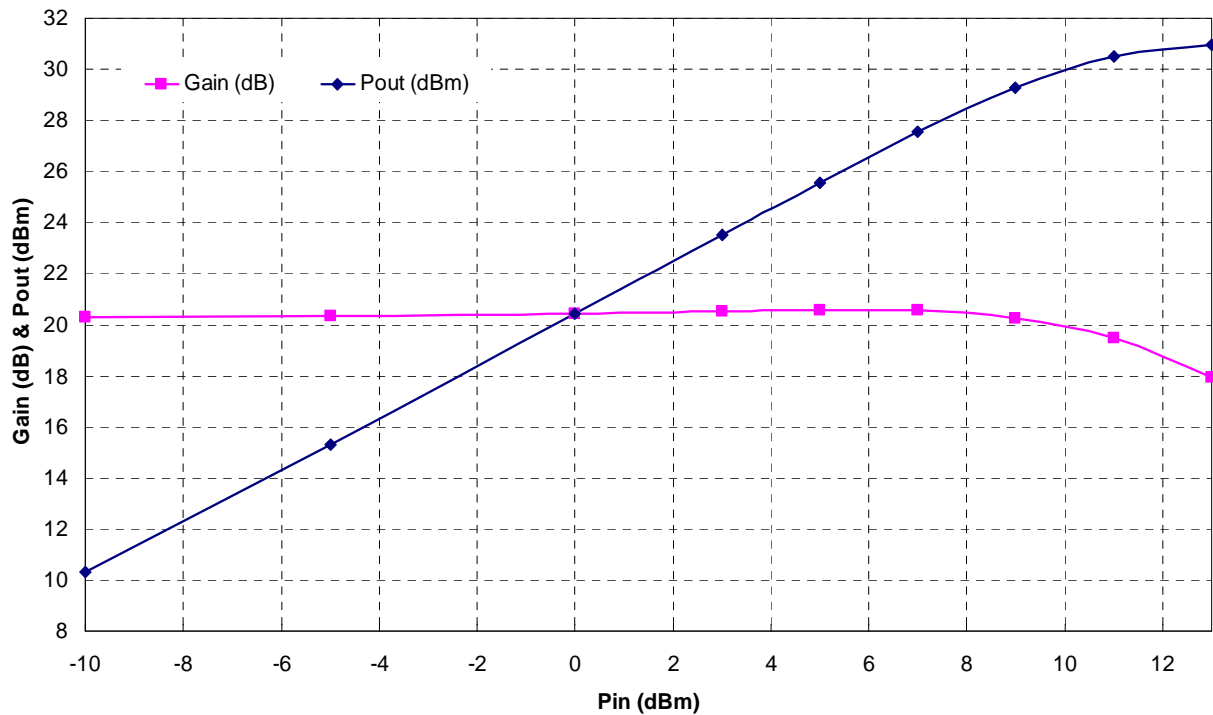
Typical Measured Performance

Pulsed On wafer measurement (without bonding wires at the RF ports)
 Tamb = +25°C, Vd = +4.5V, Small Signal Id = 890mA

Linear Gain & P1dB & Psat versus Frequency

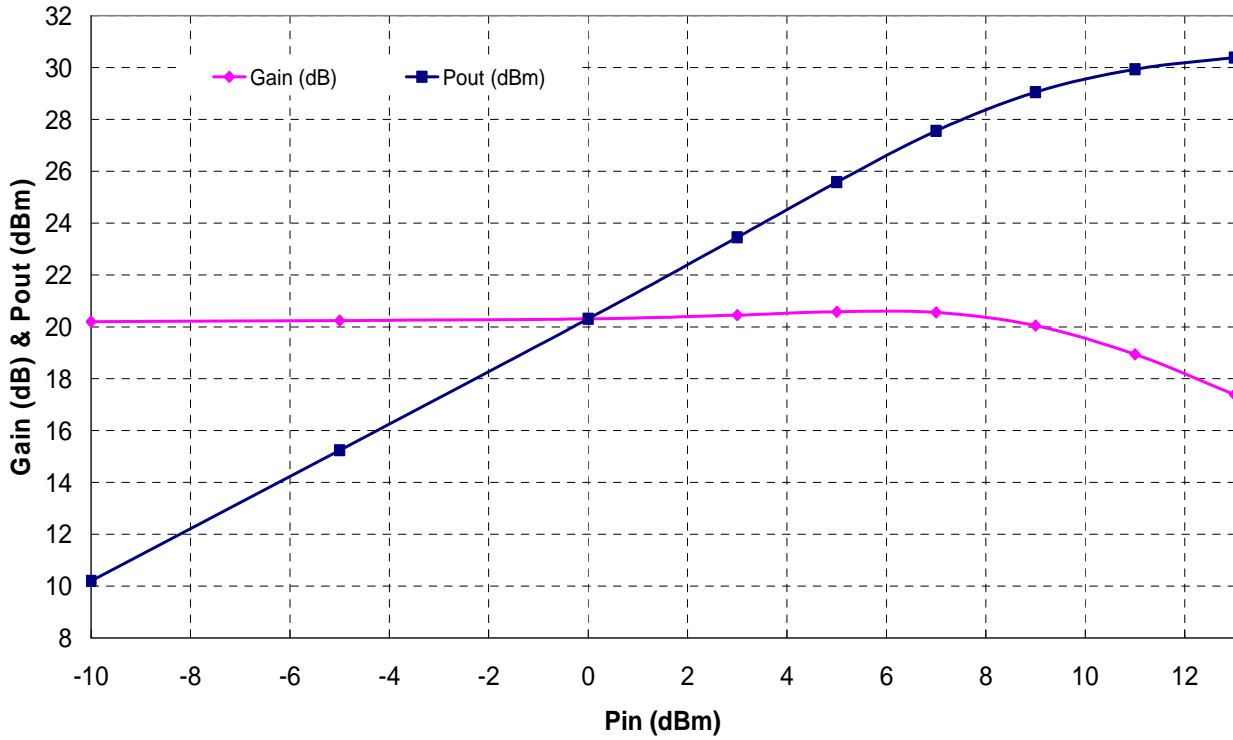


Gain & Pout versus Pin @ Freq=17GHz

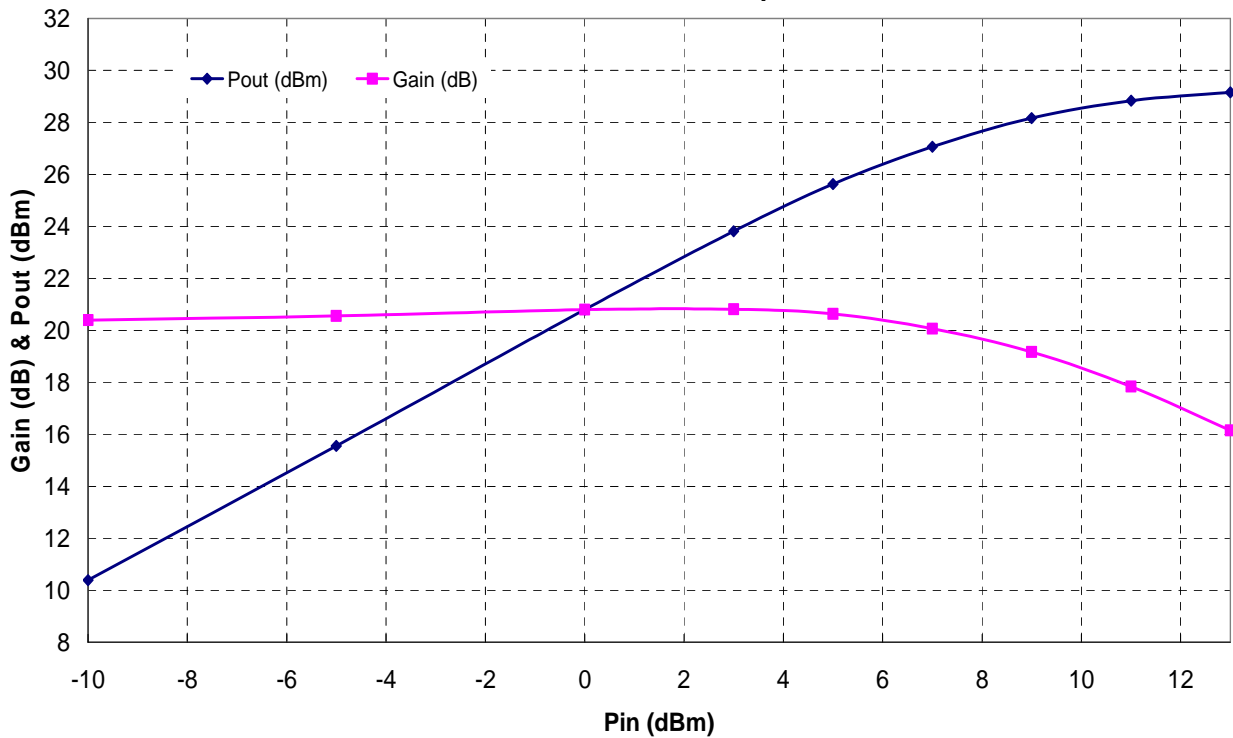


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Gain & Pout versus Pin @Freq=21GHz



Gain & Pout versus Pin @Freq=27GHz



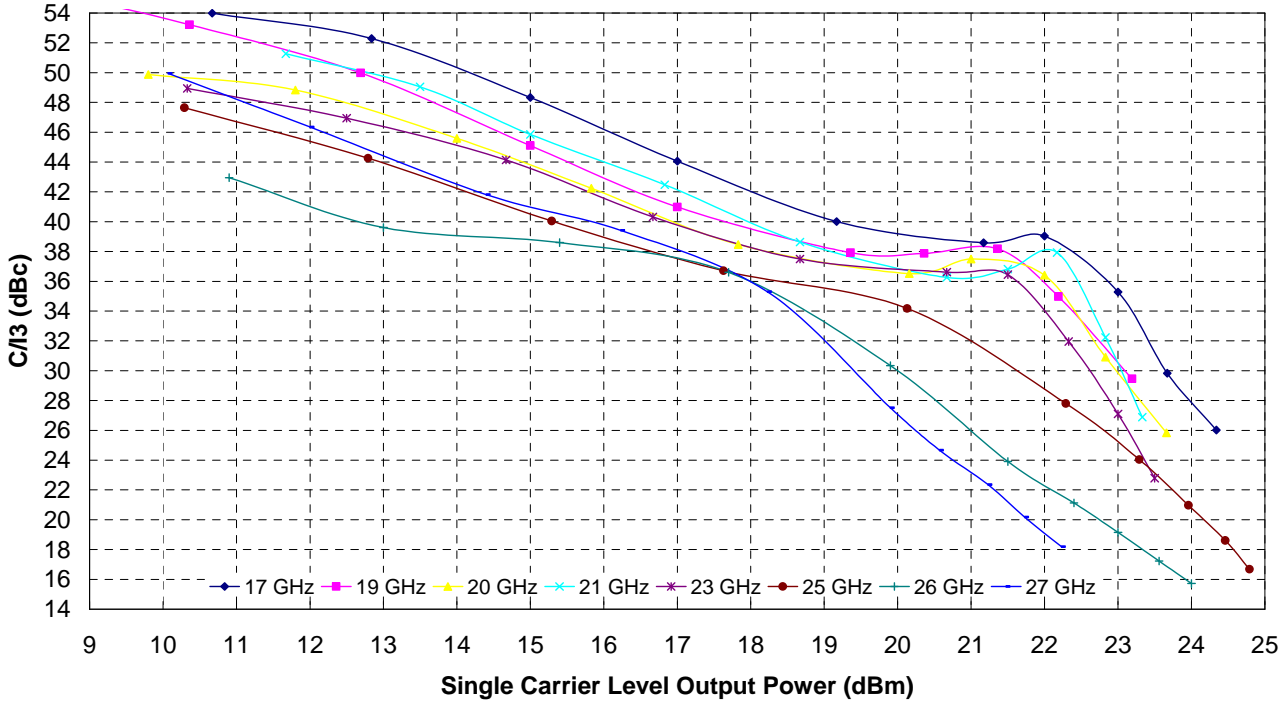
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Typical Measured Performance

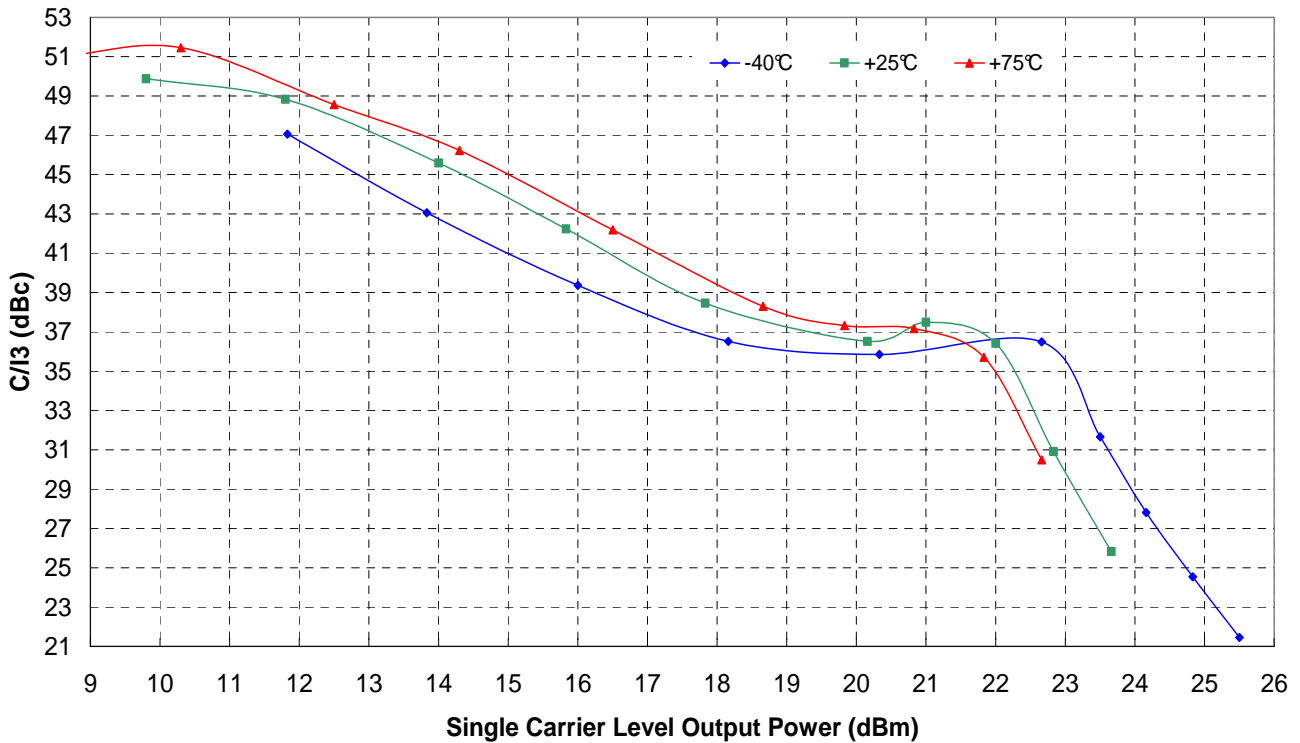
On JIG measurement:

Tamb = +25°C, Vd = +4.5V, Id = 890mA

C/I3 versus Single Carrier Level Output Power at 25°C

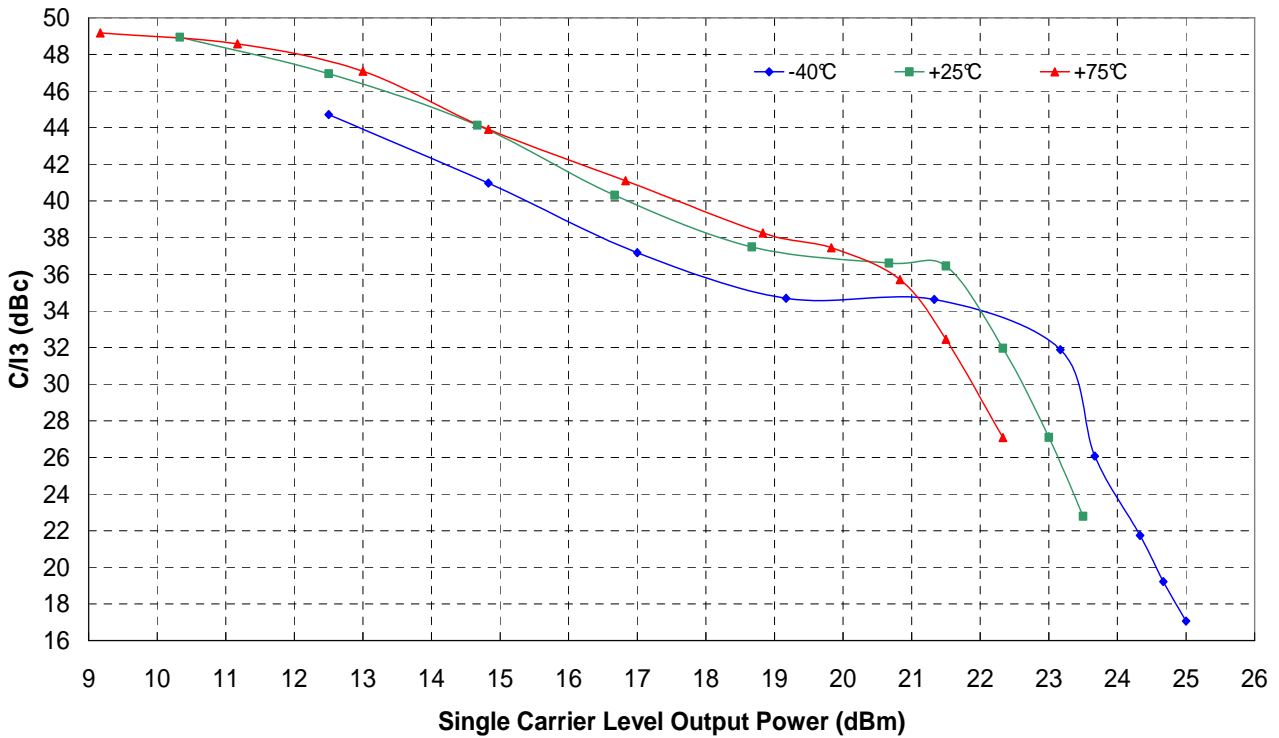


C/I3 versus Temperature at 20GHz

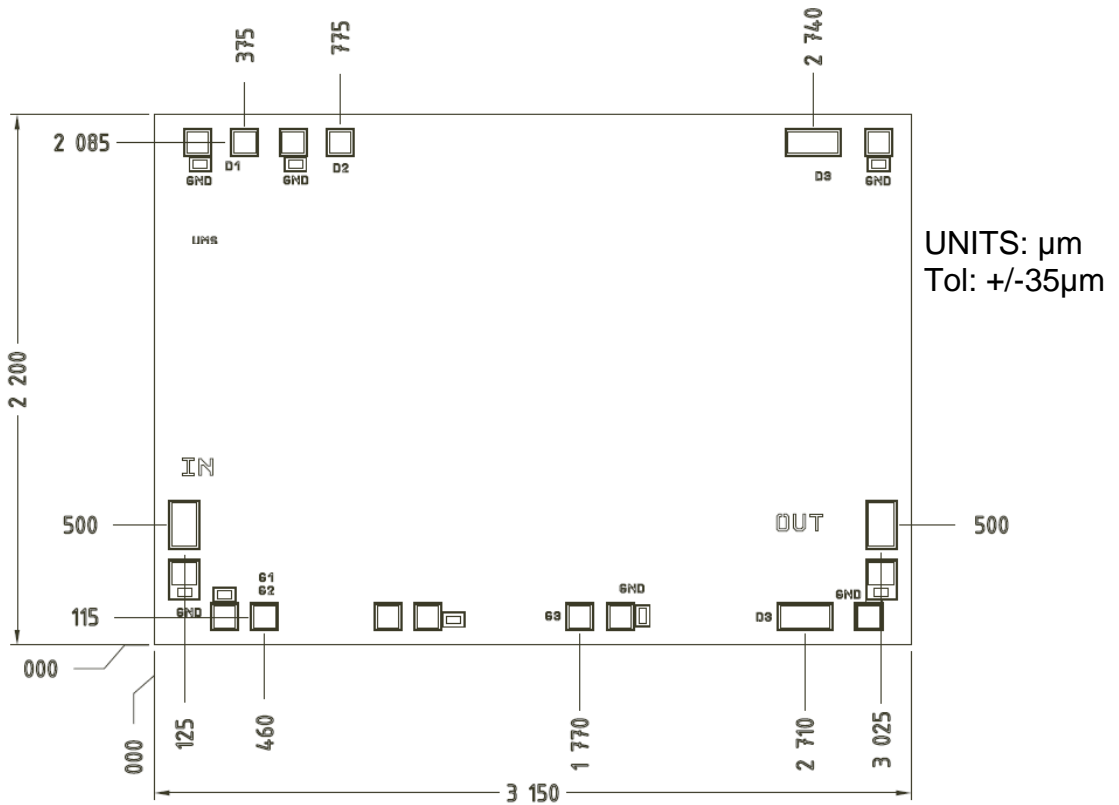


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C/I3 versus Temperature at 23GHz



Chip Assembly and Mechanical Data



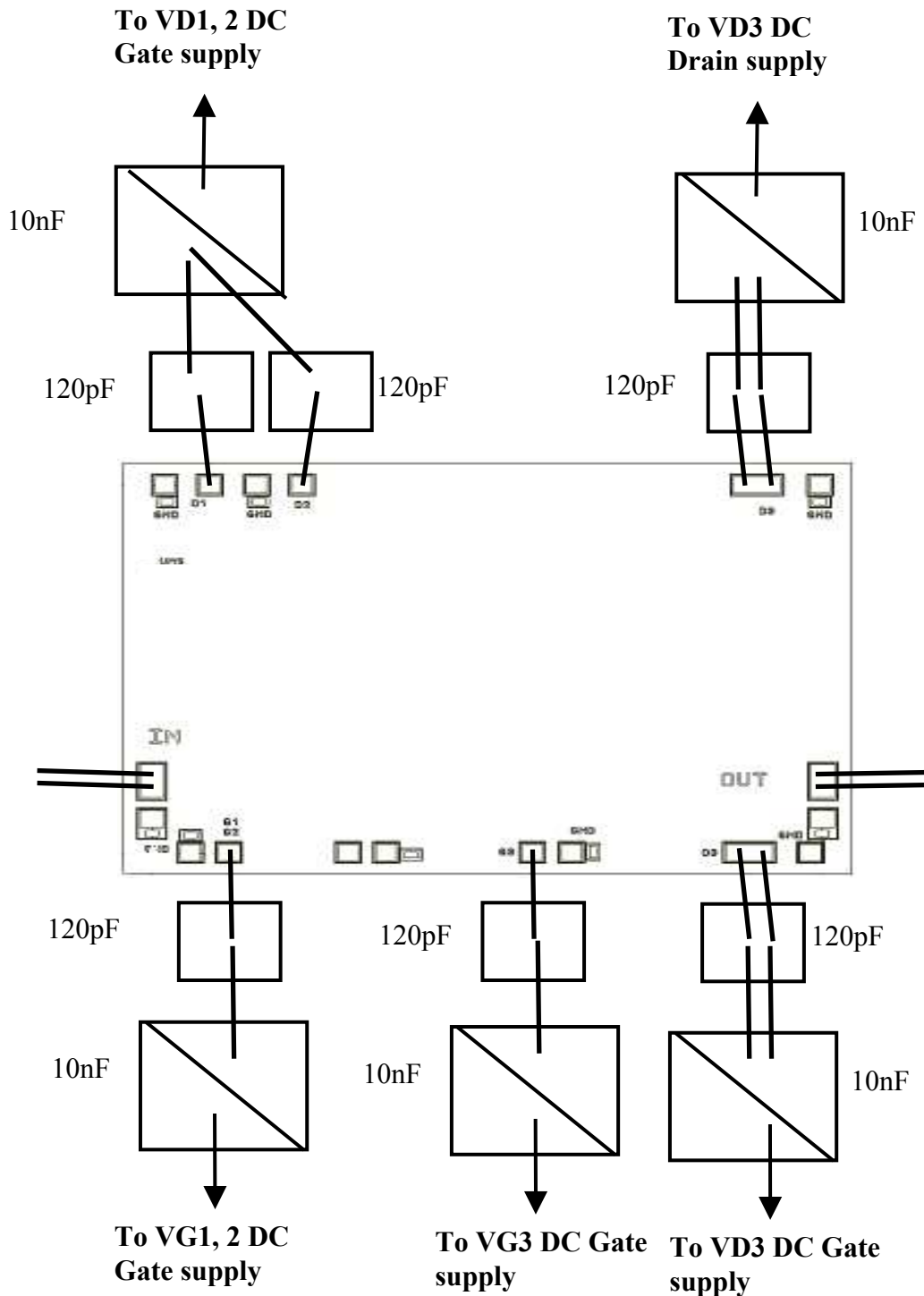
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Note: Supply feed might be capacitively bypassed.

25 μ m diameter gold wire is to be preferred.

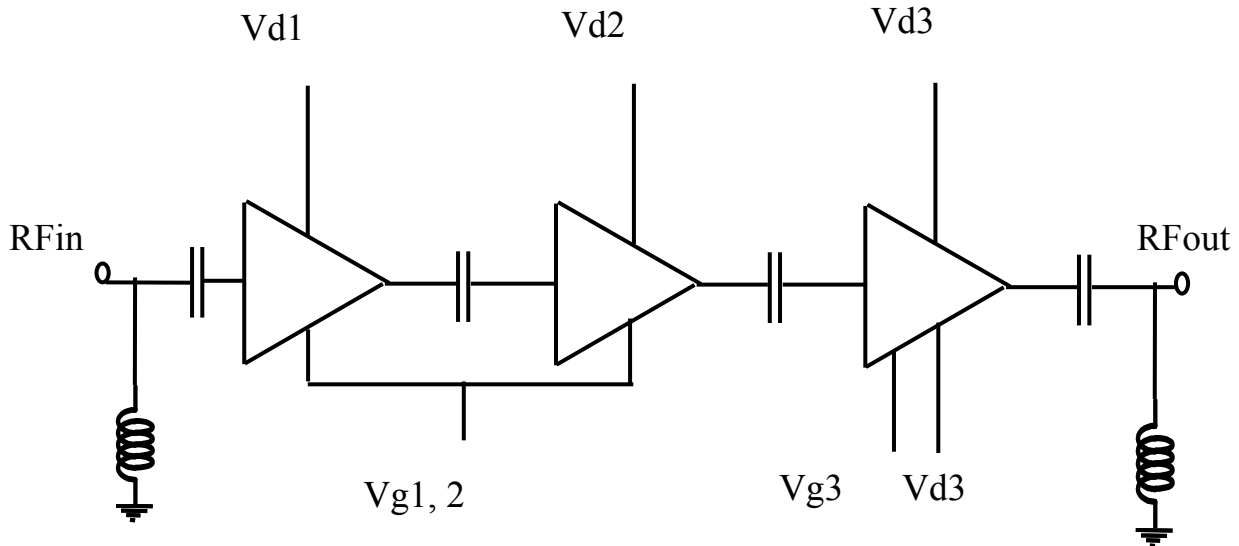
DC Pads Size: 114/114 μ m, RF Pads Size: 129/204 μ m, Chip thickness: 100 μ m.

RF wire bonding length: 700 μ m max



Note*preliminary*

Due to ESD protection RFin and RFout are DC grounded, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections are also implemented on gate accesses.

Ordering Information

Chip form:

CHA5056-98F/00

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