DATA SHEET

PCF2104x
LCD controller/driver

Product specification
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Philips
Semiconductors

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CONTENTS

1 FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5×7 character format plus cursor; 5×8 for kana (Japanese syllabary) and user-defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I^2C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.
- I^2C-bus address: 011101 SA0.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2104x integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device.

The PCF2104x is optimized for chip-on-glass applications. The 'x' in 'PCF2104x' represents a specific letter code for a character set in the character generator ROM (CGROM).

Two standard character sets are currently available, specified by the letters 'C' and 'L' (see Figs 5 and 6). Other character sets are available on request.

The PCF2104x is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5×8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104x interfaces to most microcontrollers via a 4 or 8-bit bus, or via the 2-wire I^2C-bus.

3.1 Packages

- PCF2104xU/2; chip with bumps in tray
- PCF2104xU/7; chip with bumps on tape.

For further details see Chapter 18.

3.2 Available types

- PCF2104CU/x: character set 'C' in CGROM
- PCF2104LU/x: character set 'L' in CGROM
- PCF2104NU/x: character set 'N' in CGROM.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2104CU/2	–	chip with bumps in tray	–
PCF2104CU/7	–	chip with bumps on tape	–
PCF2104LU/2	–	chip with bumps in tray	–
PCF2104LU/7	–	chip with bumps on tape	–
PCF2104NU/2	–	chip with bumps in tray	–
PCF2104NU/7	–	chip with bumps on tape	–

5 BLOCK DIAGRAM

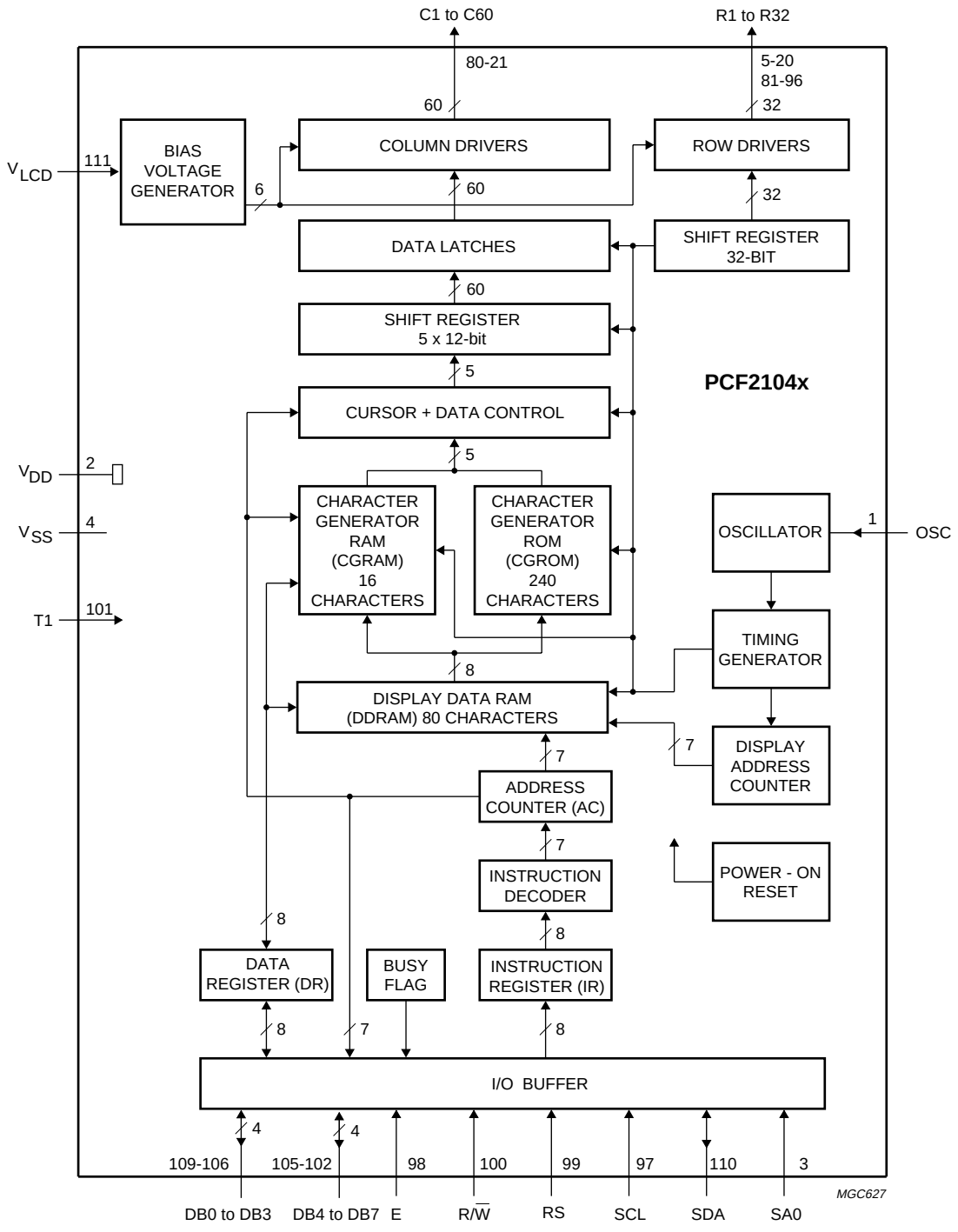


Fig.1 Block diagram.

6 PINNING

SYMBOL	FFC PAD	TYPE	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	P	logic supply voltage
SA0	3	I	I^2C-bus address pin input
V_{SS}	4	P	ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I^2C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test pad input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I^2C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

7 PIN FUNCTIONS

7.1 RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

7.2 R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

7.3 E: data bus clock (parallel control)

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.

7.4 DB0 to DB7: data bus (parallel control)

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2104x. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I^2C-bus control is used.

7.5 C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

7.6 R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

7.7 V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display.

7.8 OSC: oscillator

When the on-chip oscillator is used, this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

7.9 SCL: serial clock line

Input for the I^2C-bus clock signal.

7.10 SDA: serial data line

Input/output for the I^2C-bus data line.

7.11 SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2104xs on the same I^2C-bus.

7.12 T1: test pad

Must be connected to V_{SS}. Not user accessible.

8 FUNCTIONAL DESCRIPTION (see Fig.1)

8.1 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The optimum levels depend on the multiplex rate and are selected automatically when the number of lines in the display is defined.

The optimum value of V_{OP} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. The relationships are given in Table 1.

Using a 5-level bias scheme for 1 : 16 MUX rate allows $V_{OP} < 5$ V for most LCD liquids. The effect on the display contrast is negligible.

Table 1 Optimum values for V_{OP}

MUX RATE	NUMBER OF BIAS LEVELS	V_{OP}/V_{th}	DISCRIMINATION V_{on}/V_{off}
1 : 16	5	3.67	1.277
1 : 32	6	5.19	1.196

8.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. Pin OSC must be connected to V_{DD}.

8.3 External clock

If an external clock is to be used, it must be input at pin OSC. The resulting display frame frequency is given by $f_{frame} = {}^{1}\!/_{2304} f_{osc}$. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

8.4 Power-on reset

The Power-on reset block initializes the chip after power-on or power failure.

8.5 Registers

The PCF2104x has two 8-bit registers, an instruction register (IR) and a data register (DR). The register select signal (RS) determines which register will be accessed.

The instruction register stores instruction codes such as display clear and cursor shift, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to, but not read from, by the system controller.

The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM (corresponding to the address in the Address Counter) is written to the data register prior to being read by the ‘Read data’ instruction.

8.6 Busy Flag

The Busy Flag indicates the free/busy status of the PCF2104x. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The Busy Flag is output at pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the Busy Flag is at logic 0 or waiting for the required number of clock cycles.

8.7 Address Counter (AC)

The Address Counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'Set CGRAM address' and 'Set DDRAM address'. After a read/write operation the Address Counter is automatically incremented or decremented by 1. The Address Counter contents are output to the bus (DB0 to DB6) when RS = logic 0 and R/$\overline{W}$ = logic 1.

8.8 Display data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data, represented by 8-bit character codes. DDRAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown in Fig.2. With no display shift, the characters represented by the codes in the first 12 or 24 RAM locations, starting at address 00 in line 1, are displayed. Subsequent lines display data starting at addresses 20, 40, or 60 Hex. Figures 3 and 4 show the DDRAM-to-display mapping scheme when the display is shifted.

The address range for a 1-line display is 00 to 4F; for a 2-line display from 00 to 27 (line 1) and 40 to 67 (line 2); for a 4-line display from 00 to 13, 20 to 33, 40 to 53 and 60 to 73 for lines 1, 2, 3 and 4 respectively. For 2 and 4-line displays the end address of one line and the start address of the next line are not consecutive. When the display is shifted each line wraps around independently of the others (see Figs 3 and 4).

When data is written to the DDRAM wrap-around occurs from 4F to 00 in 1-line mode and from 27 to 40 and 67 to 00 in 2-line mode; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line mode.

8.9 Character generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5 $\times$ 8 dot format from 8-bit character codes. Figures 5 and 6 show the character sets currently available.

8.10 Character generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the character generator RAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.5). Figure 8 shows the addressing principle for the CGRAM.

8.11 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Fig.9) at the DDRAM address contained in the Address Counter. When the Address Counter contains the CGRAM address the cursor will be inhibited.

8.12 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.13 LCD row and column drivers

The PCF2104x contains 32 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 10 and 11 show typical waveforms.

In the 1-line mode (1 : 16) the row outputs are driven in pairs: R1/R17, R2/R18 for example. This allows the output pairs to be connected in parallel, thereby providing greater drive capability.

Unused outputs should be left unconnected.

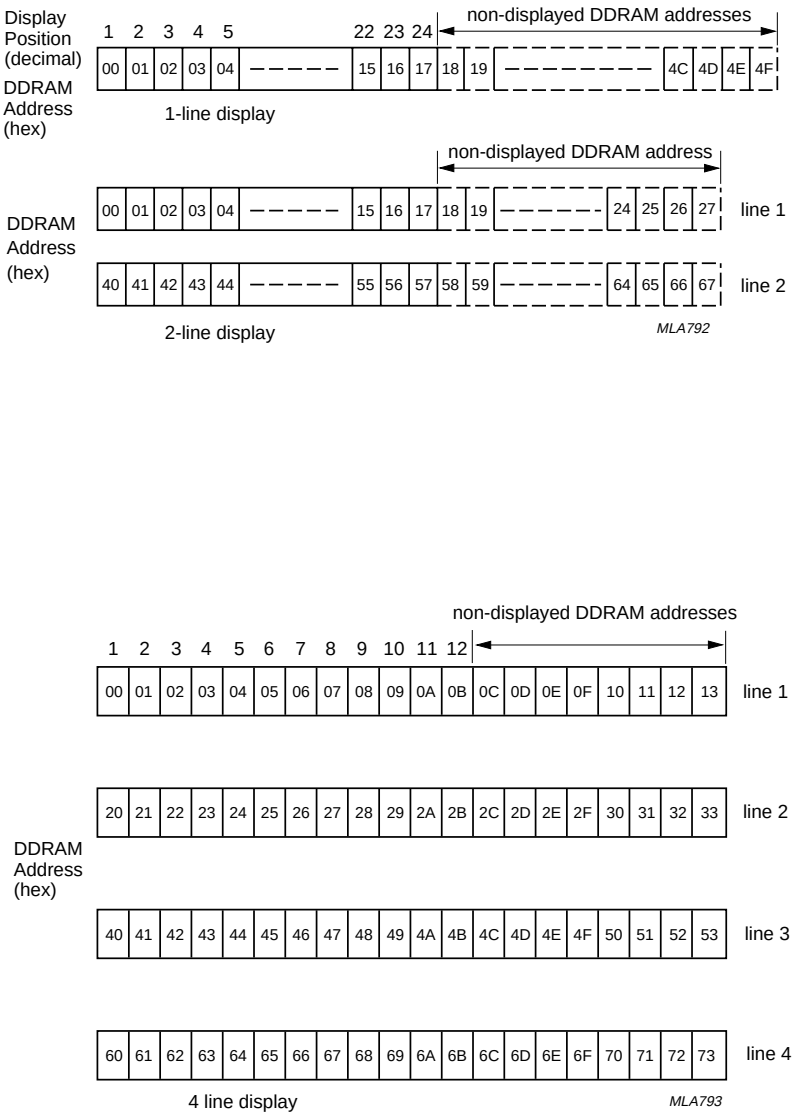


Fig.2 DDRAM-to-display mapping; no shift (PCF2104x).

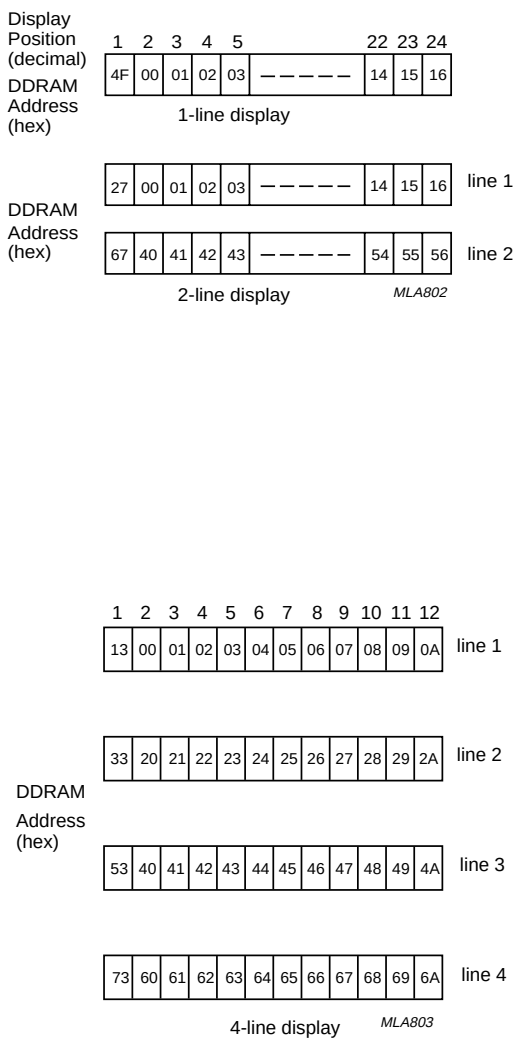


Fig.3 DDRAM-to-display mapping; right shift (PCF2104x).

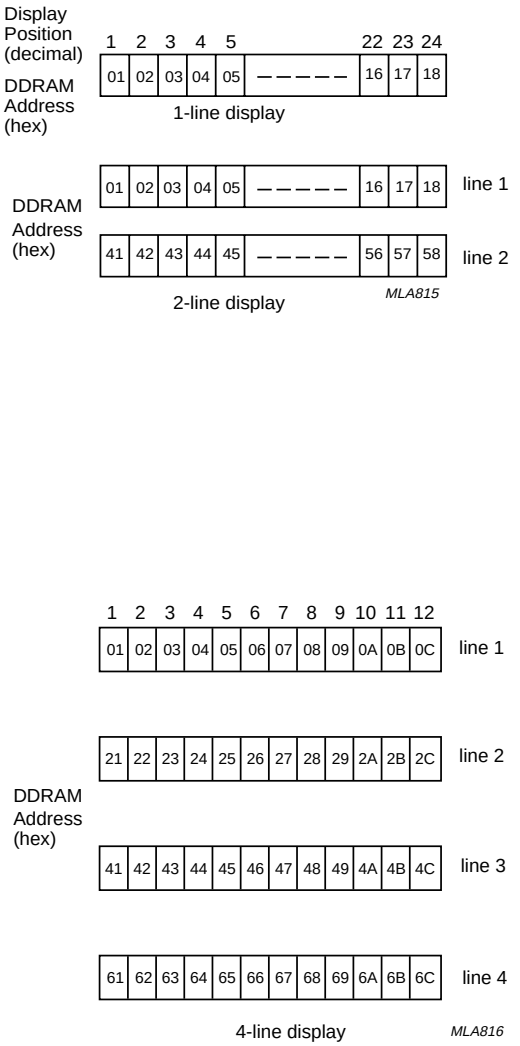


Fig.4 DDRAM-to-display mapping; left shift (PCF2104x).

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MLB895

Fig.5 Character set ‘C’ in CGROM; **PCF2104C**.

lower 6 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

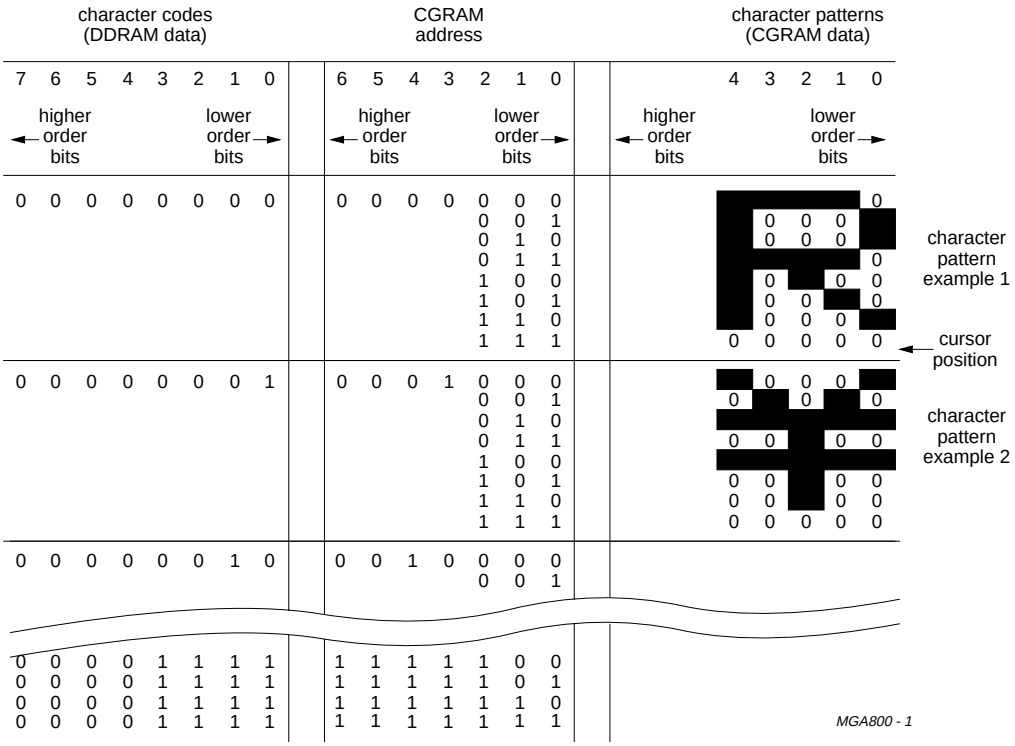
MGC629

Fig.6 Character set ‘L’ in CGROM; **PCF2104L**.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGM134

Fig.7 Character set ‘N’ in CGROM; **PCF2104N**.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

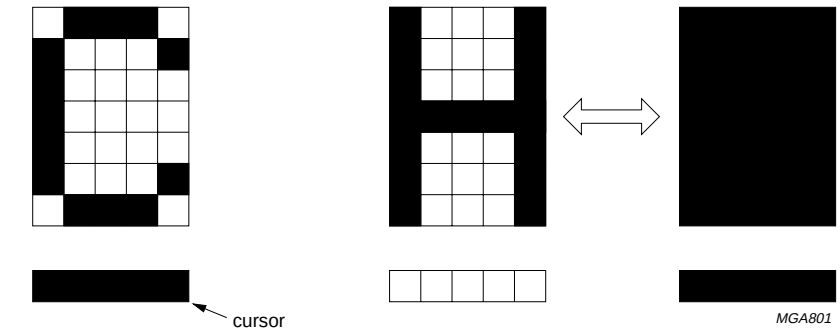
CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4; bit 4 being at the left end, as shown in the figure.

CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read Busy Flag and address' instruction.

Fig.8 Relationship between CGRAM addresses, data and display patterns.



5 x 7 dot character font

alternating display

cursor display example

blink display example

Fig.9 Cursor and blink display examples.

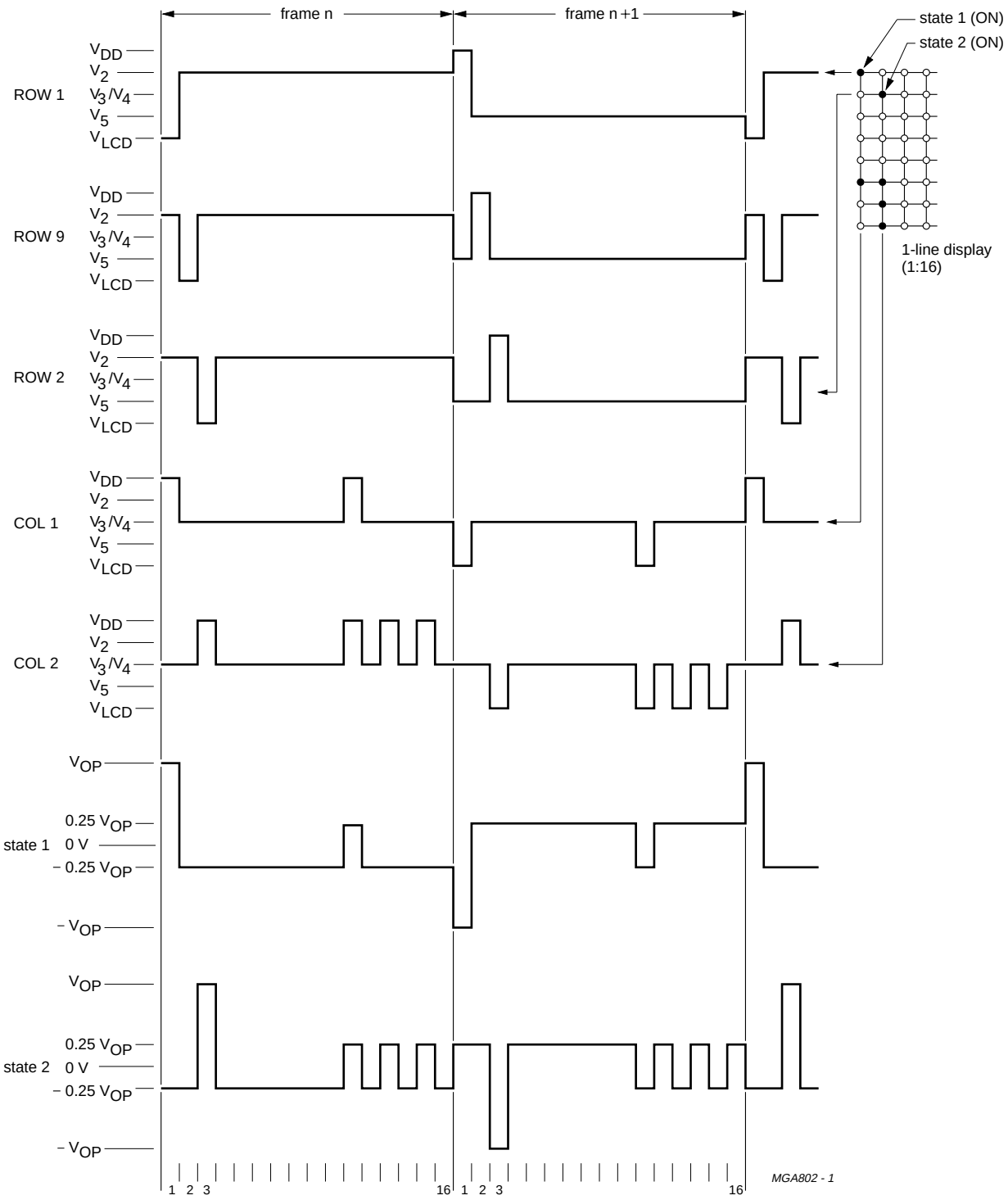


Fig.10 Typical LCD waveforms; 1-line mode.

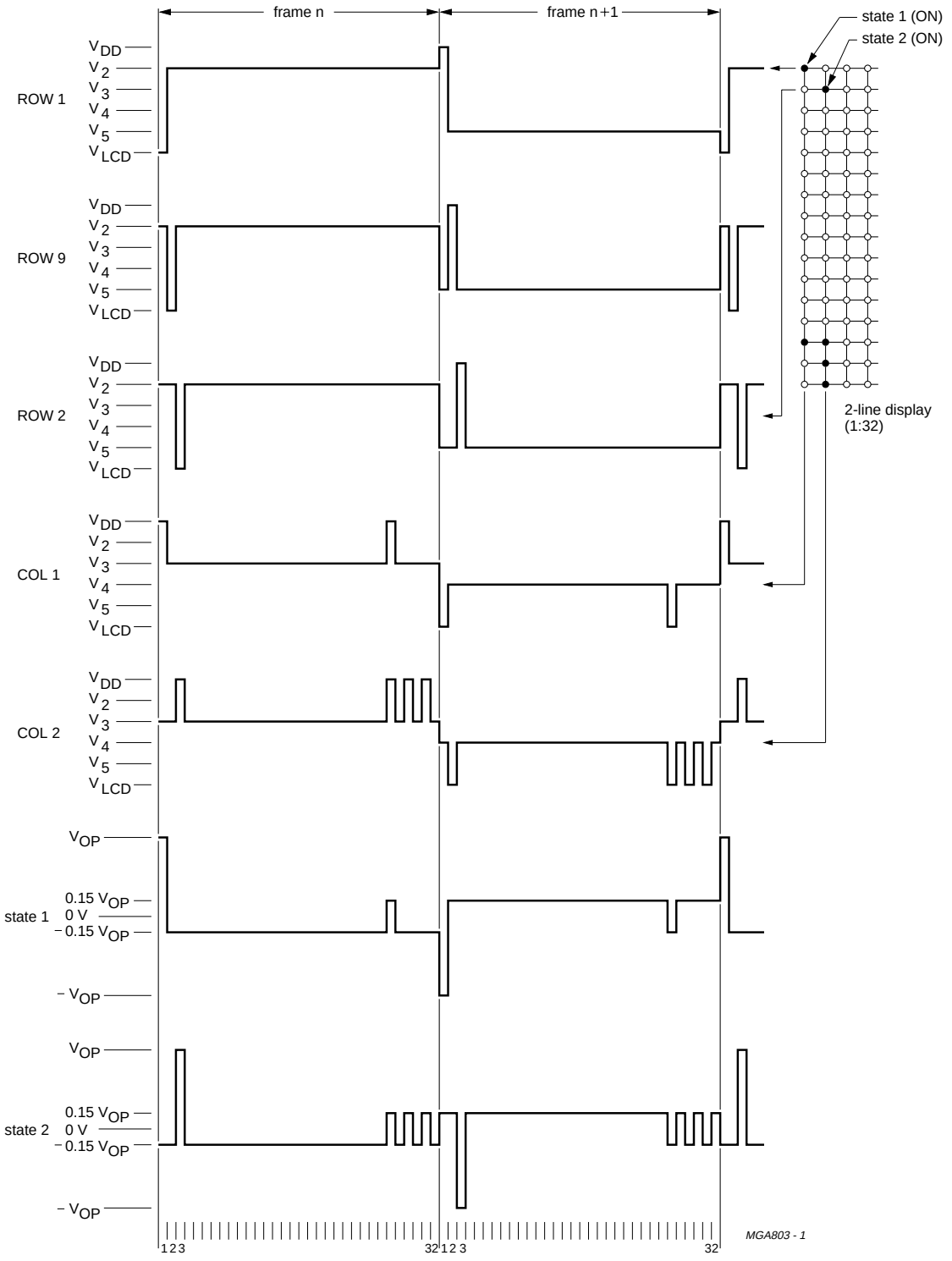


Fig.11 Typical LCD waveforms; 2-line mode.

8.14 Programming of MUX 1 : 16 displays with PCF2104x

The PCF2104x can be used in the following ways:

- 1-line mode to drive a 2-line display
- 2 × 12 characters with MUX rate 1 : 16, resulting in better contrast. The internal data flow of the chip is optimized for this purpose.

Using the 'Function set' instruction, M and N are set to 0, 0 (respectively). Figures 12, 13 and 14 show the DDRAM addresses of the display characters. The second row of each table corresponds to either the right half of a 1-line display or to the second line of a 2-line display. Wrap around of data during display shift or when writing data is non-standard.

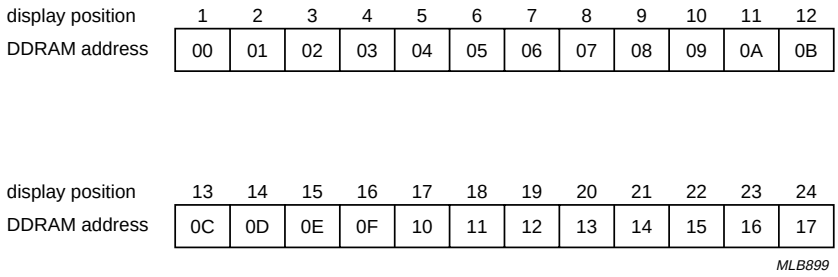


Fig.12 DDRAM-to-display mapping; no shift (PCF2104x).

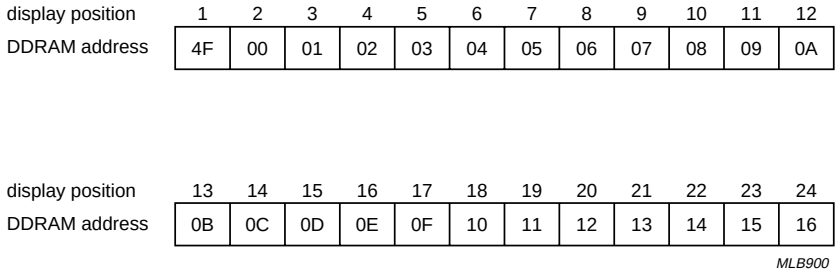


Fig.13 DDRAM-to-display mapping; right shift (PCF2104x).

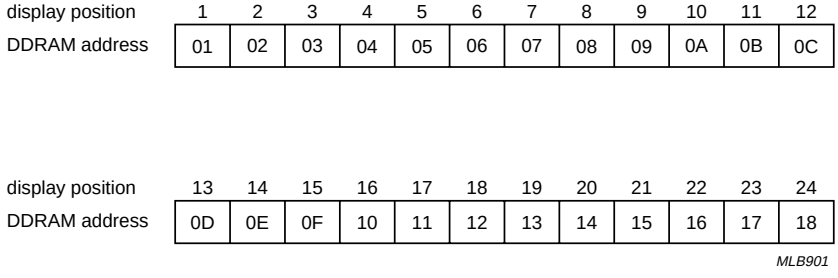


Fig.14 DDRAM-to-display mapping; left shift (PCF2104x).

8.15 Programming of MUX 1 : 32 displays with PCF2104x

To drive a 2-line by 24 characters MUX 1 : 32 display, use instruction ‘Function set’ to set M, N to 0, 1 (respectively).

To drive a 4-line by 12 characters MUX 1:32 display, use instruction ‘Function set’ to set M, N to 1, 1 (respectively).

8.16 Reset function

The PCF2104 automatically initializes (resets) when power is turned on. The state after reset is given in Table 2.

Table 2 State after reset

STEP	DESCRIPTION
1	Display clear.
2	Function set: DL = 1: 8-bit interface M, N = 0 1-line display G = 0: not used
3	Display on/off control: D = 0: display off C = 0: cursor off; B = 0: blink off;
4	Entry mode set: I/D = 1: +1 (increment) G = 0: not used
5	Default address pointer to DDRAM. The Busy Flag (BF) indicates the busy state (BF = logic 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software. See Tables 10 and 11.
6	I^2C-bus interface reset.

9 INSTRUCTIONS

Only two PCF2104x registers, the instruction register (IR) and the data register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interfacing to peripheral control ICs.
The PCF2104x operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2104x functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, thus enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the Busy Flag/address read instruction will be executed.

Because the Busy Flag is set to logic 1 while an instruction is being executed, it is advisable to ensure that the flag it is at logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the Busy Flag is HIGH will not be executed.

Table 3 Instructions (note 1)

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES(2)
NOP	0	0	0	0	0	0	0	0	0	0	No operation.	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in Address Counter.	165
Return home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in Address Counter Also returns shifted display to original position DDRAM contents remain unchanged.	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	3
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DDRAM contents.	3
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data length (DL), number of display lines (N, M) and voltage generator control (G).	3
Set CGRAM address	0	0	0	1	A_{CG}						Sets CGRAM address.	3
Set DDRAM address	0	0	1	A_{DD}							Sets DDRAM address.	3
Read busy flag and address	0	1	BF	A_C							Reads Busy Flag (BF) indicating internal operation is being performed and reads Address Counter contents.	0
Read data	1	1	read data								Reads data from CGRAM or DDRAM.	3
Write data	1	0	write data								Writes data to CGRAM or DDRAM.	3

Notes

1. In the I^2C-bus mode the DL bit is don't care. 8-bit mode is assumed.
   In the I^2C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}} = 6.67\ \mu s$; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

Table 4 Command bit identities

BIT	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
N (M = 0)	2 line × 12 characters; MUX 1 : 16	2 lines × 24 characters; MUX 1 : 32
N (M = 1)	reserved	4 lines × 12 characters; MUX 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

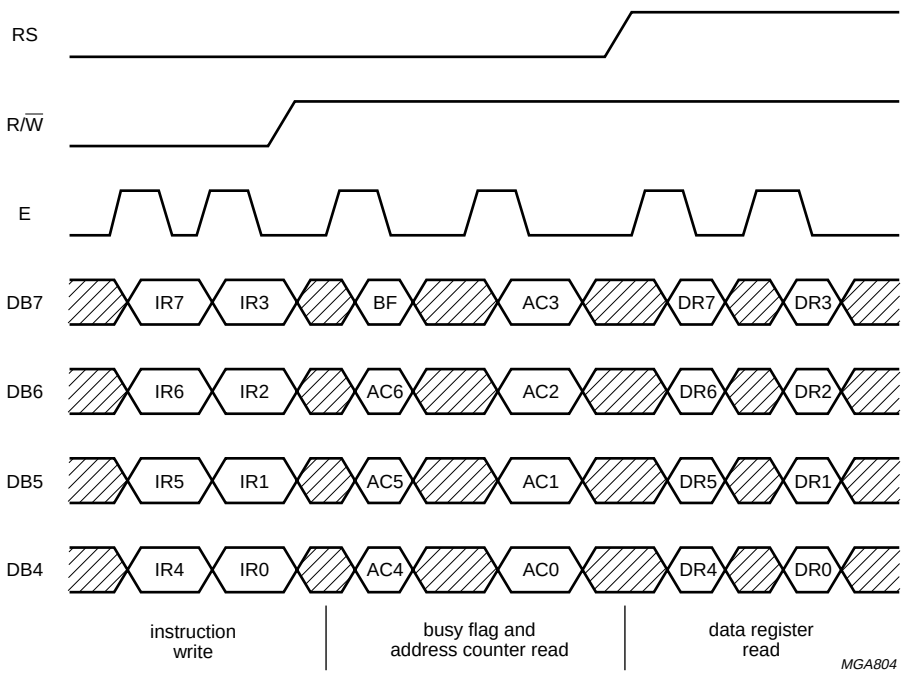
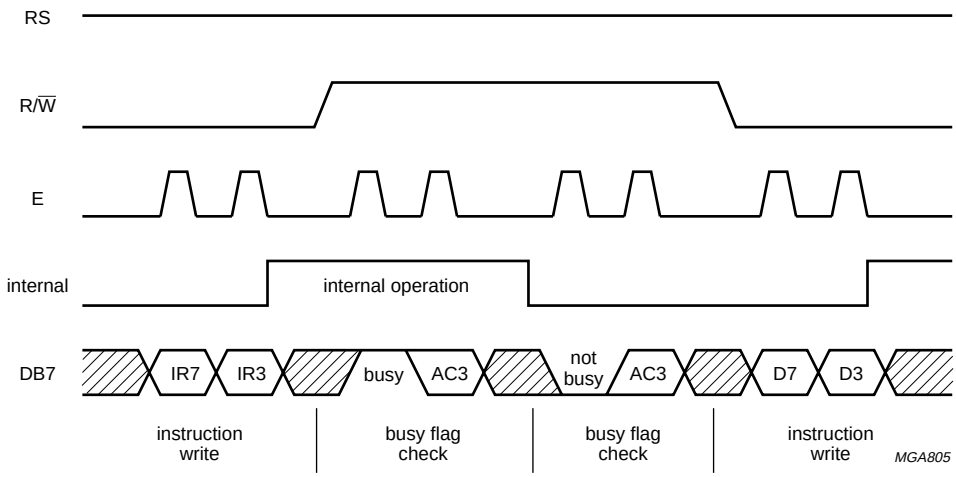


Fig.15 4-bit transfer example.



IR7, IR3: instruction 7th bit, 3rd bit.
AC3: Address Counter 3rd bit.

Fig.16 An example of 4-bit data transfer timing sequence.

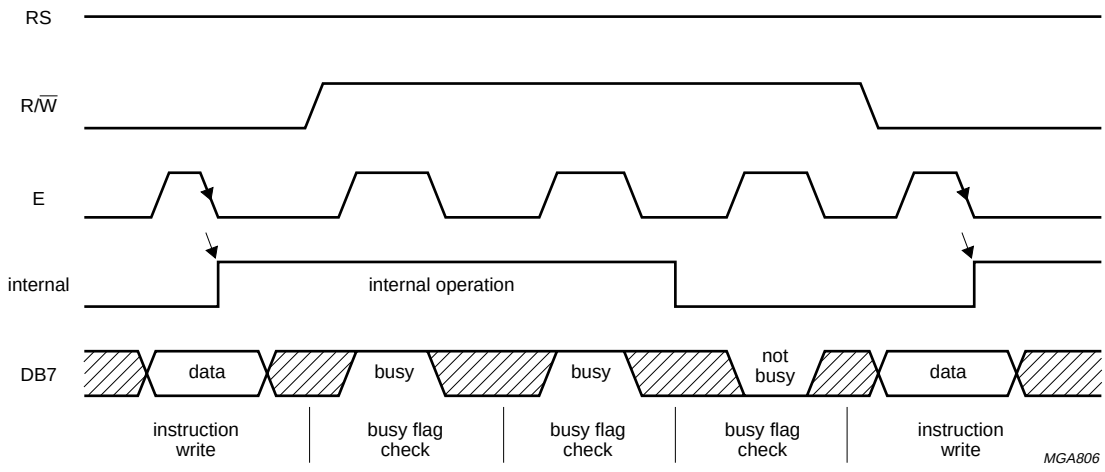


Fig.17 Example of Busy Flag check timing sequence.

9.1 Clear display

'Clear display' writes space code 20 (hexadecimal) into all DDRAM addresses (the character pattern for character code 20 must be a blank pattern), sets the DDRAM Address Counter to logic 0 and returns the display to its original position if it was shifted. Consequently, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed) and sets the entry mode to I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction 'Clear display' requires extra execution time. This may be allowed for by checking the Busy Flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM Address Counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 I/D

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written to or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

9.3.2 S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Consequently, it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = logic 0 the display does not shift.

9.4 Display on/off control

9.4.1 D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to logic 1.

9.4.2 C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.9).

9.4.3 B

The character indicated by the cursor blinks when B = logic 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (see Fig.9). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}. The cursor and the blink can be set to display simultaneously.

9.5 Cursor/display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position of the line (40 or 20 decimal). When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

9.6 Function set

9.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = logic 1 or in two nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus(1).

Function set from I^2C-bus interface: DL bit can not bet set to logic 0 from the I^2C-bus interface. If bit DL has been set to logic 0 via the parallel bus, programming via the I^2C-bus interface is complicated.

9.6.2 N, M

Sets number of display lines.

(1) In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first function set instruction after power-on G and H are set to 1. A second function set must then be sent (2 nibbles) to set G and H to their required values.

9.7 Set CGRAM address

'Set CGRAM address' sets bits 0 to 5 of the CGRAM address (A_{CG} in Table 3) into the Address Counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read busy flag and address' instruction.

9.8 Set DDRAM address

Set DDRAM address sets the DDRAM address (A_{DD} in Table 3) into the Address Counter (binary A[6] to A[0). Data can then be written to or read from the DDRAM.

Table 5 Hexadecimal address ranges

ADDRESS	FUNCTION
00 to 4F	1-line by 24
00 to 0B and 0C to 4F	2-line by 12
00 to 27 and 40 to 67	2-line by 24
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-line by 12

9.9 Read busy flag and address

'Read busy flag and address' reads the Busy Flag (BF). When BF = logic 1 it indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0, so BF should be checked before sending another instruction.

At the same time, the value of the Address Counter expressed in binary A[6] to A[0] is read out. The Address Counter is used by both CGRAM and DDRAM and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

Writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written to is determined by the previous specification of CGRAM or DDRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D0 to D4 of CGRAM data are valid, bits D5 to D7 are 'don't care'.

9.11 Read data from CGRAM or DDRAM

Reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'Set address' instruction determines whether the CGRAM or DDRAM is to be read.

The 'Read data' instruction gates the content of the data register (DR) to the bus while E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions that update the data register (DR) are:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'Write data, 'Cursor/display shift', 'Clear display', 'Return home') will not modify the data register content.

10 INTERFACE TO MICROCONTROLLER (PARALLEL INTERFACE)

The PCF2104x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In the 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB0 to DB7. Three further control lines E, RS, and R/$\overline{W}$ are required.

In the 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB4 to DB7 in 8-bit mode) are sent in the first cycle and the lower order bits (DB0 to DB3 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the Busy Flag check. 4-bit operation is selected by instruction. See Figs 15, 16 and 17 for examples of bus protocol.

In the 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

11 INTERFACE TO MICROCONTROLLER (I²C-BUS INTERFACE)

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

11.3 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

11.4 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

11.5 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

11.6 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2104x READ and WRITE cycles is illustrated in Figs 22, 23 and 24.

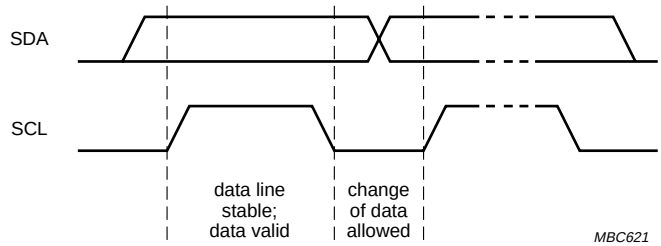


Fig.18 Bit transfer.

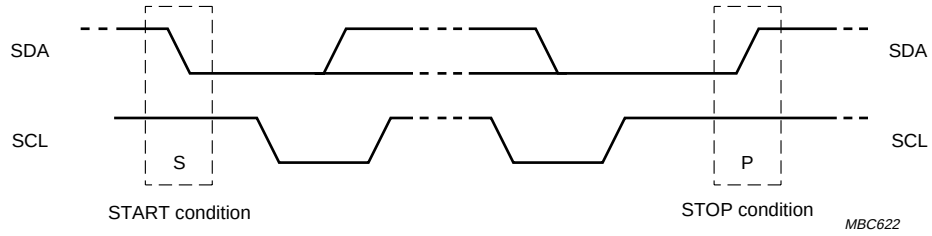


Fig.19 Definition of START and STOP conditions.

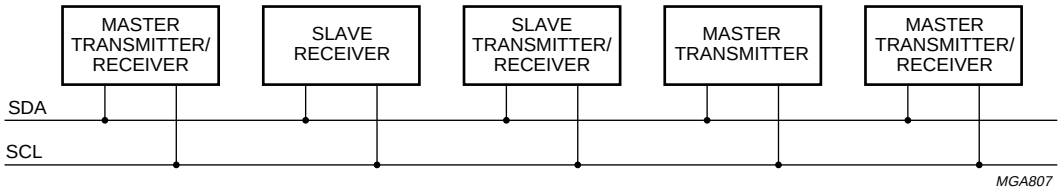


Fig.20 System configuration.

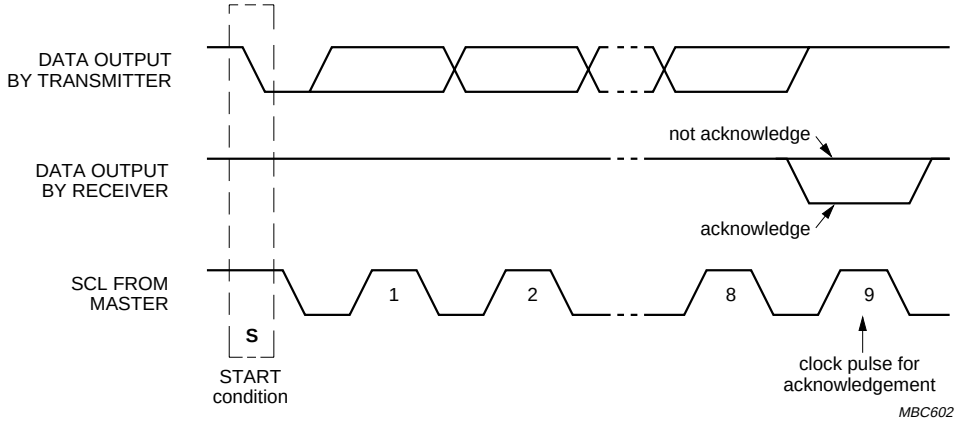


Fig.21 Acknowledgement on the I^2C-bus.

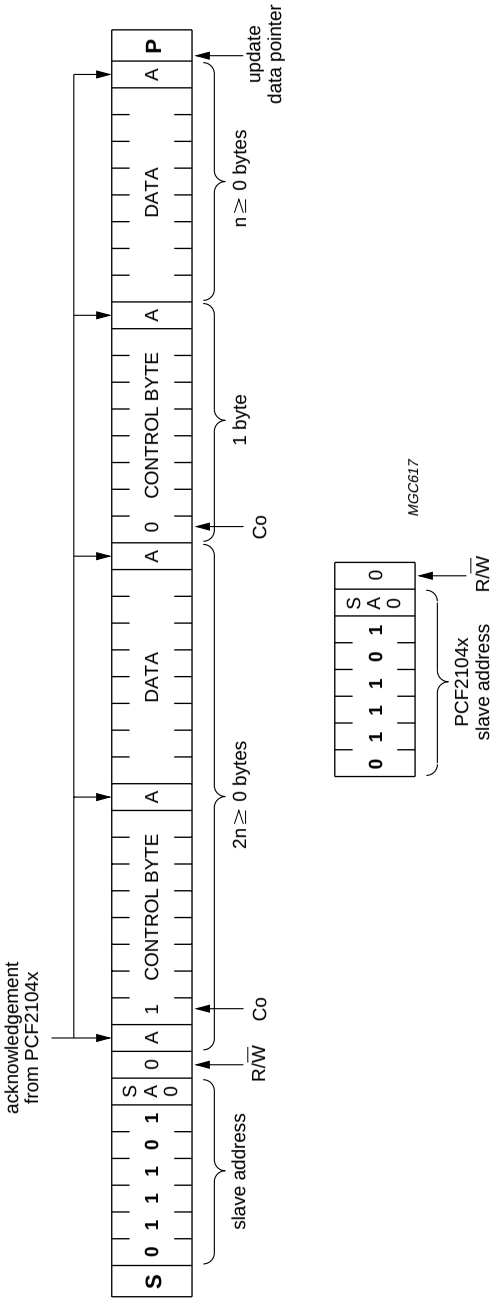


Fig.22 Master transmits to slave receiver; WRITE mode.

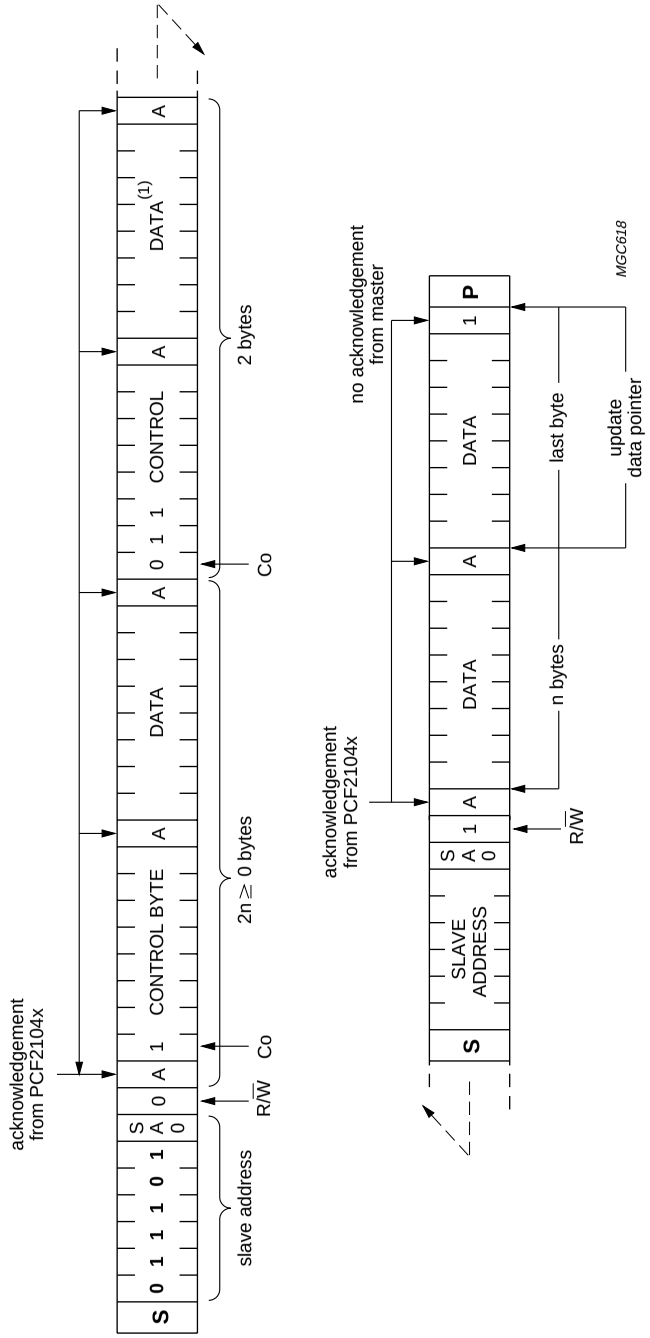


Fig.23 Master reads after setting word address; write word address, set RS/$\overline{RW}$; READ data.

(1) Last data byte is a dummy byte (may be omitted).

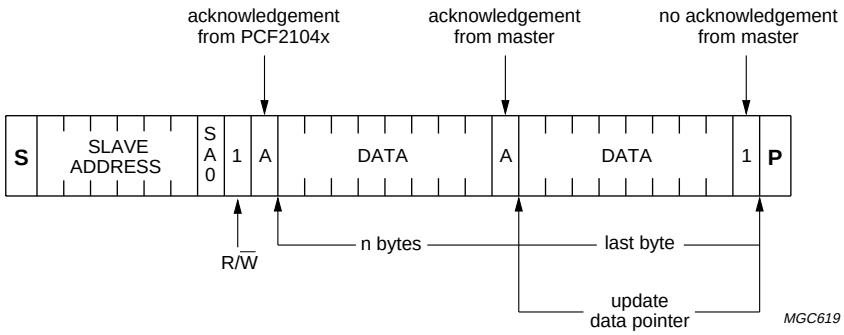


Fig.24 Master reads slave immediately after first byte; READ mode (RS previously defined).

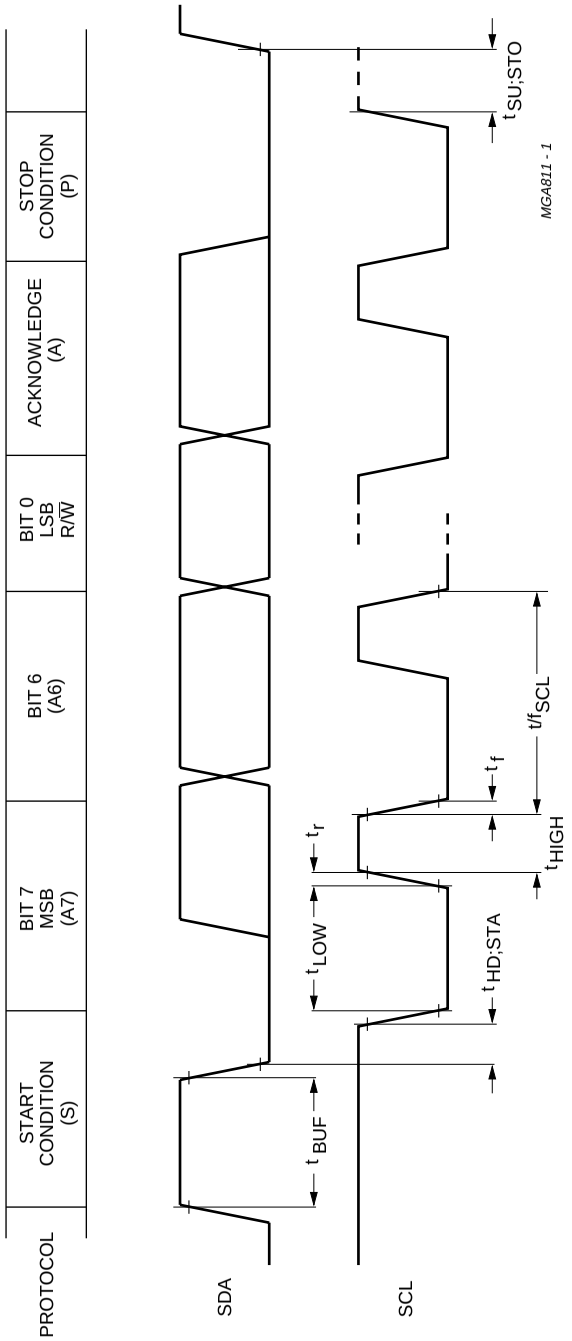


Fig.25 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} – 11	V_{DD}	V
V_I	input voltage OSC, RS, R/$\overline{W}$, E and DB0 to DB7	V_{SS} – 0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	–50	+50	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

14 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} – 3.5 to V_{DD} – 9 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} – 9	–	V_{DD} – 3.5	V
I_{DD}	supply current external V_{LCD}	note 1	–	–	–	
I_{DD1}	supply current 1		–	200	500	µA
I_{DD2}	supply current 2	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	200	300	µA
I_{DD3}	supply current 3	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	150	200	µA
I_{LCD}	V_{LCD} input current	notes 1 and 6	–	50	100	µA
V_{POR}	Power-on reset voltage level	note 2	–	1.3	1.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic						
V_{IL1}	LOW level input voltage pins E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		V_{SS}	–	$0.3V_{DD}$	V
V_{IH1}	HIGH level input voltage pins E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(osc)}$	LOW level input voltage pin OSC		V_{SS}	–	$V_{DD} - 1.5$	V
$V_{IH(osc)}$	HIGH level input voltage pin OSC		$V_{DD} - 0.1$	–	V_{DD}	V
I_{pu}	pull-up current at pins DB0 to DB7, RS and R/$\overline{W}$	$V_I = V_{SS}$	0.04	0.15	1.00	µA
$I_{OL(DB)}$	LOW level output current pins DB0 to DB7	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	–	–	mA
$I_{OH(DB)}$	HIGH level output current pins DB0 to DB7	V_{OH} = 4 V; V_{DD} = 5 V	–1.0	–	–	mA
I_{L1}	leakage current pins OSC, E, RS, R/$\overline{W}$, DB0 to DB7 and SA0	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
I²C-bus						
SDA, SCL						
V_{IL2}	LOW level input voltage	note 3	V_{SS}	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage	note 3	$0.7V_{DD}$	–	V_{DD}	V
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
C_i	input capacitance	note 4	–	–	7	pF
$I_{OL(SDA)}$	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance pins R1 to R32	note 5	–	1.5	3	kΩ
R_{COL}	column output resistance pins C1 to C60	note 5	–	3	6	kΩ
V_{tol1}	bias voltage tolerance pins R1 to R32 and C1 to C60	note 6	–	±20	±130	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; $V_0 = V_{DD}$; bus inactive; internal or external clock with duty cycle 50% (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R32 and C1 to C60) with load current I_{load} = 150 µA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time.
6. LCD outputs open-circuit.

15 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	note 1	40	65	100	Hz
f_{osc}	external clock frequency		90	150	225	kHz
Bus timing characteristics: Parallel Interface; notes 1 and 2						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2104X)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AH}	address hold time		25	–	–	ns
t_{DSW}	data set-up time		60	–	–	ns
t_{HD}	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2104X TO MICROCONTROLLER)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AH}	address hold time		25	–	–	ns
t_{DHD}	data delay time		–	–	150	ns
t_{HD}	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4	–	–	µs

Notes

1. V_{DD} = 5.0 V.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

16 TIMING DIAGRAMS

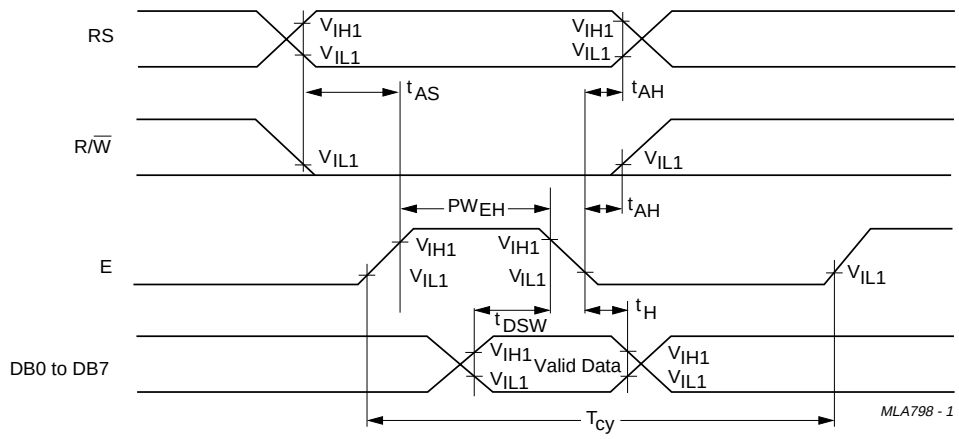


Fig.26 Parallel bus write operation sequence; writing data from microcontroller to PCF2104x.

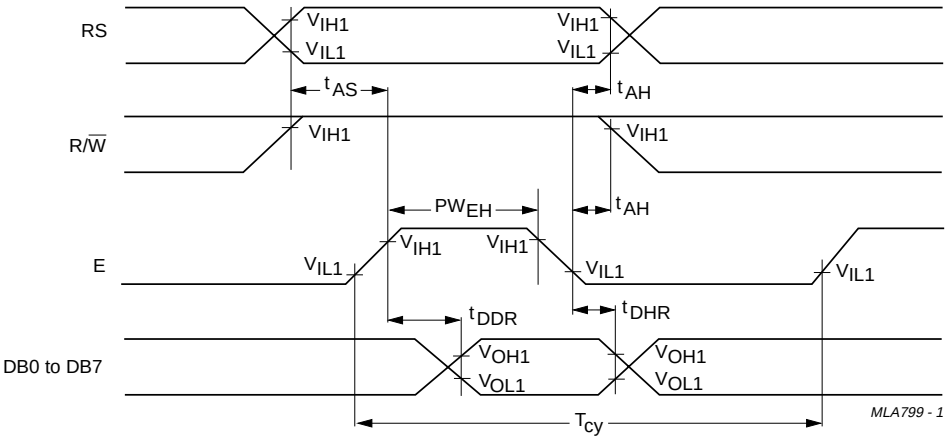


Fig.27 Parallel bus read operation sequence; reading data from PCF2104x to microcontroller.

17 APPLICATION INFORMATION

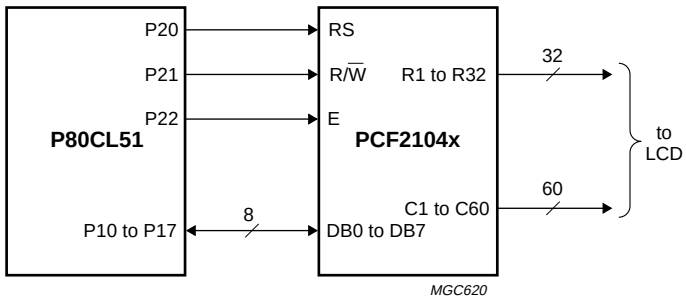


Fig.28 Direct connection to 8-bit microcontroller; 8-bit bus.

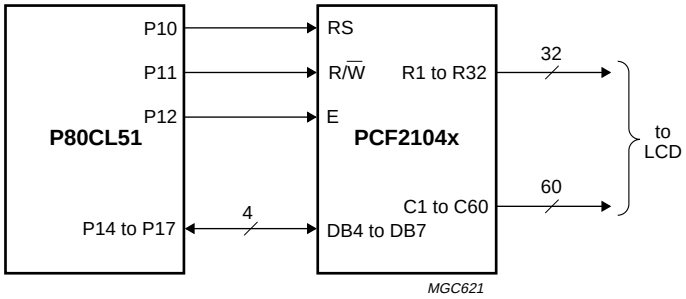


Fig.29 Direct connection to 8-bit microcontroller; 4-bit bus.

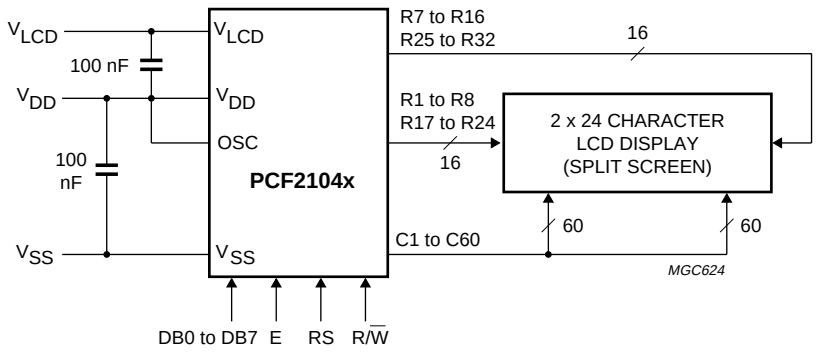


Fig.30 Typical application using parallel interface.

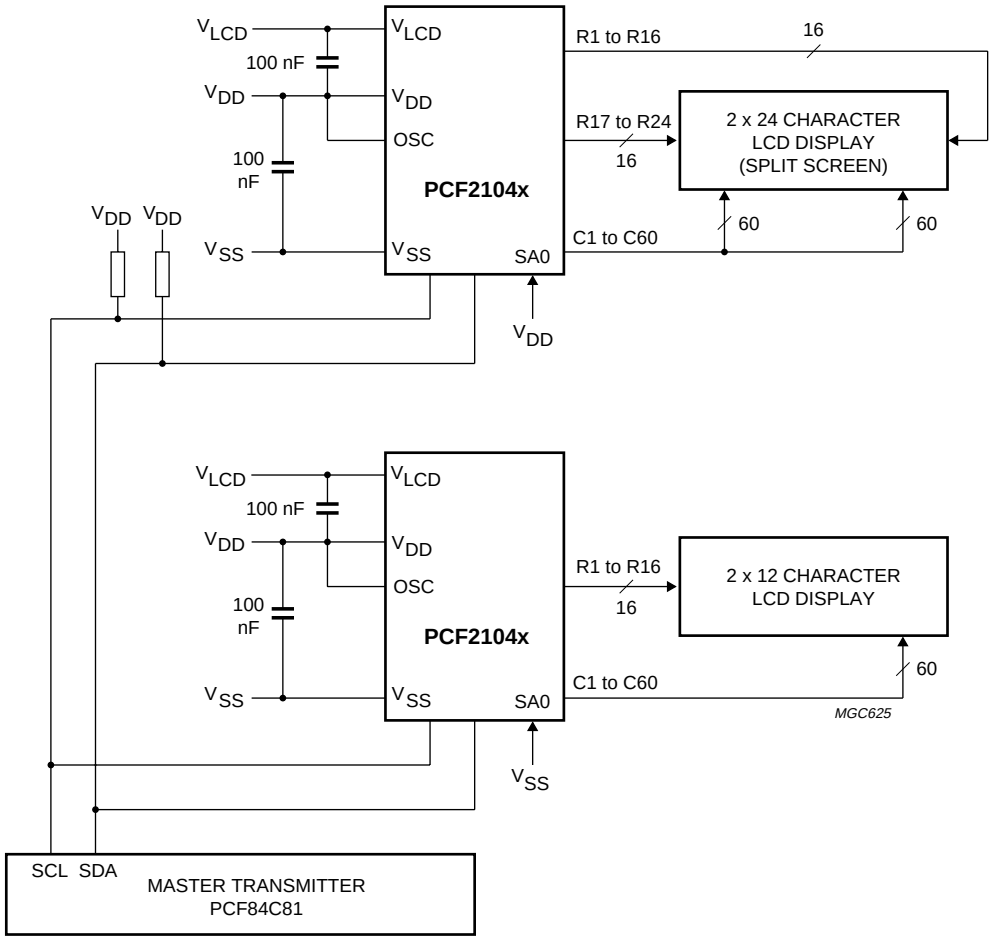


Fig.31 Application using I²C-bus interface.

17.1 8-bit operation, 2 × 12 display using internal reset

Table 7 shows an example of a 1-line display in 8-bit operation. The PCF2104x functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes the display position only and DDRAM contents remain unchanged. Display data entered first can be displayed when the 'Return home' instruction is performed.

17.2 4-bit operation, 2 × 12 display using internal reset

The program must set functions prior to 4-bit operation. Table 6 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2104x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 6 step 3).

Thus, DB4 to DB7 of the function set are written twice.

17.3 8-bit operation, 2 × 24 display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 8). It should be noted that both lines of the display are always shifted together, data does not shift from one line to the other.

17.4 I^2C operation, 2 × 12 display

A control byte is required with most instructions (see Table 9).

17.5 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2104x must be initialized by instruction. Tables 10 and 11 show how this may be performed for 8-bit and 4-bit operation.

Table 6 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2104x is initialized by the internal reset circuit).		Initialized. No display appears.
2	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0		Sets to 4-bit operation. In this instance operation is handled as 8-bits by initialization and only this instruction completes with one write.
3	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0 RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0		Sets to 4-bit operation, selects 2 $\times$ 12 display. 4-bit operation starts from this point and resetting is needed.
4	Display on/off control: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0 RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 1; DB5 = 1; DB4 = 0		Turns on display and cursor. Entire display is blank after initialization.
5	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0 RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 1; DB4 = 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
6	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1 RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 1; DB4 = 0	**P**_	Writes ‘P’. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.

Table 7 8-bit operation, 1-line display example; using internal reset (character set ‘A’)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2104x is initialized by the internal reset function).		Initialized. No display appears.
2	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0		Sets to 8-bit operation, selects 2 × 12 display.
3	Display mode on/off control: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**P**_	Writes ‘P’. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 1; DB4 = 1; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0	**PH**_	Writes ‘H’.
7		| | |	
8	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1	**PHILIPS**_	Writes ‘S’.
9	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 1	**PHILIPS**_	Sets mode for display shift at the time of write.
10	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**HILIPS** _	Writes space.
11	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**ILIPS M**_	Writes ‘M’.
12		| | |	

STEP	INSTRUCTION	DISPLAY	OPERATION
13	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 1	**MICROKO_**	Writes ‘O’.
14	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**MICROKO**	Shifts only the cursor position to the left.
15	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**MICROKO**	Shifts only the cursor position to the left.
16	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1	**ICROCO**	Writes ‘C’ correction. The display moves to the left.
17	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 0	**MICROCO**	Shifts the display and cursor to the right.
18	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 1; DB1 = 0; DB0 = 0	**MICROCO_**	Shifts only the cursor to the right.
19	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**ICROCOM_**	Writes ‘M’.
20			
21	Return home: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 0	**PHILIPS M**	Returns both display and cursor to the original position (address 0).

Table 8 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2104x is initialized by the internal reset function).		Initialized. No display appears.
2	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0		Sets to 8-bit operation, selects 2 × 24 display
3	Display on/off control: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**P**_	Writes ‘P’. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6		|	
7	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1	**PHILIPS**_	Writes ‘S’.
8	Set DDRAM address: RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**PHILIPS** _	Sets DDRAM address to position the cursor at the head of the 2nd line.
9	Write data to CGRAM/ DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**PHILIPS** **M**_	Writes ‘M’.
10		|	
11	Write data to CGRAM/ DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 1	**PHILIPS** **MICROCO**_	Writes ‘O’.
12	Write data to CGRAM/ DDRAM: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 1	**PHILIPS** **MICROCO**_	Sets mode for display shift at the time of write.

STEP	INSTRUCTION	DISPLAY	OPERATION
13	Write data to CGRAM/ DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**HILIPS** **ICROCOM_**	Writes ‘M’. Display is shifted to the left. The first and second lines shift together.
14			
15	Return home: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 0	**PHILIPS** **MICROCOM**	Returns both display and cursor to the original position (address 0).

Table 9 Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
1	I²C-bus start		Initialized. No display appears.
2	Slave address for write: SA6 = 0; SA5 = 1; SA4 = 1; SA3 = 1; SA2 = 0; SA1 = 1; SA0 = 0; R/$\overline{W}$ = 0; Ack = 1		During the acknowledge cycle SDA will be pulled-down by the PCF2104x.
3	Send a control byte for function set: Co = 0; RS = 0; R/$\overline{W}$ = 0; Ack = 1		Control byte sets RS and R/$\overline{W}$ for following data bytes.
4	Function set: DB7 = 0; DB6 = 0; DB5 = 1; DB4 = X; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 1		Selects 1-line display; SCL pulse during acknowledge cycle starts execution of instruction.
5	Display on/off control: DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 0; Ack = 1	_	Turns on display and cursor. Entire display shows character Hex 20 (blank in ASCII-like character sets).
6	Entry mode set: DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 0; Ack = 1	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM. Display is not shifted.
7	I²C-bus start	_	For writing data to DDRAM, RS must be set to 1. Therefore a control byte is needed.
8	Slave address for write: SA6 = 0; SA5 = 1; SA4 = 1; SA3 = 1; SA2 = 0; SA1 = 1; SA0 = 0; R/$\overline{W}$ = 0; Ack = 1	_	
9	Send a control byte for write data: Co = 0; RS = 1; R/$\overline{W}$ = 0; Ack = 1	_	
10	Write data to DDRAM: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 1	**P**_	Writes ‘P’. The DDRAM has been selected at power-up. The cursor is incremented by 1 and shifted to the right.
11	Write data to DDRAM: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 1	**PH**_	Writes ‘H’.
12 to 15		| | | |	
16	Write data to DDRAM: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1; Ack = 1	**PHILIPS**_	Writes ‘S’.

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
17	(optional I²C-bus stop) I²C-bus start + slave address for write (as step 8)	**PHILIPS_**	
18	Control byte: Co = 1; RS = 0; R/$\overline{W}$ = 0; Ack = 1	**PHILIPS_**	
19	Return home: DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 0; Ack = 1	**PHILIPS**	Sets DDRAM address 0 in Address Counter. (Also returns shifted display to original position. DDRAM contents unchanged). This instruction does not update the Data Register (DR).
20	Control byte for read: Co = 0; RS = 1; R/$\overline{W}$ = 1; Ack = 1	**PHILIPS**	DDRAM content will be read from following instructions. The R/$\overline{W}$ has to be set to 1 while still in I²C-bus write mode.
21	I²C-bus start	**PHILIPS**	
22	Slave address for read: SA6 = 0; SA5 = 1; SA4 = 1; SA3 = 1; SA2 = 0; SA1 = 1; SA0 = 0; R/$\overline{W}$ = 1; Ack = 1	**PHILIPS**	During the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out. In the previous instruction neither a ‘Set address’ nor a ‘Read data’ has been performed. Therefore the content of the DR was unknown.
23	Read data: 8 × SCL + master acknowledge; note 2: DB7 = X; DB6 = X; DB5 = X; DB4 = X; DB3 = X; DB2 = X; DB1 = X; DB0 = X; Ack = 1	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA. MSB is DB7. During master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface.
24	Read data: 8 × SCL + master acknowledge; note 2: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 0	**PHILIPS**	8 × SCL; code of letter ‘H’ is read first. During master acknowledge code of ‘I’ is loaded into the I²C-bus interface.
25	Read data: 8 × SCL + no master acknowledge; note 2: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 1; Ack = 1	**PHILIPS**	No master acknowledge; After the content of the I²C-bus interface register is shifted out no internal action is performed. No new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted.
26	I²C stop	**PHILIPS**	

Notes

1. X = don’t care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 10 Initialization by instruction, 8-bit interface (note 1)

STEP	DESCRIPTION
Power-on or unknown state	
|	
Wait 2 ms after V_{DD} rises above V_{POR}	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = X; DB2 = X; DB1 = X; DB0 = X	BF cannot be checked before this instruction. ‘Function set’ (interface is 8-bits long).
|	
Wait 2 ms	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = X; DB2 = X; DB1 = X; DB0 = X	BF cannot be checked before this instruction.‘Function set’ (interface is 8-bits long).
|	
Wait more than 40 µs	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = X; DB2 = X; DB1 = X; DB0 = X	BF cannot be checked before this instruction. ‘Function set’ (interface is 8-bits long).
| |	BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = N; DB2 = M; DB1 = X; DB0 = 0	‘Function set’ (interface is 8-bits long). Specify the number of display lines.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0	‘Display off’.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 1	‘Clear display’.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = I/D; DB0 = S	‘Entry mode set’.
|	
Initialization ends	

Note

1. X = don’t care.

Table 11 Initialization by instruction, 4-bit interface. Not applicable for I^2C-bus operation

STEP	DESCRIPTION
Power-on or unknown state	
|	
Wait 2 ms after V_{DD} rises above V_{POR}	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1	BF cannot be checked before this instruction. ‘Function set’ (interface is 8-bits long).
|	
Wait 2 ms	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1	BF cannot be checked before this instruction. ‘Function set’ (interface is 8-bits long).
|	
Wait 40 μs	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1	BF cannot be checked before this instruction. ‘Function set’ (interface is 8-bits long).
| |	BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0	‘Function set’ (set interface to 4-bits long). Interface is 8-bits long.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0	‘Function set’ (interface is 4-bits long).
RS = 0; R/$\overline{W}$ = 0; DB7 = N; DB6 = M; DB5 = 0; DB4 = 0	Specify number of display lines and voltage generator characteristic.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0	‘Display off’.
RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 0; DB5 = 0; DB4 = 0	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0	‘Clear display’.
RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 0; DB5 = 0; DB4 = 0	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0	‘Entry mode set’.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = I/D; DB4 = S	
|	
Initialization ends	

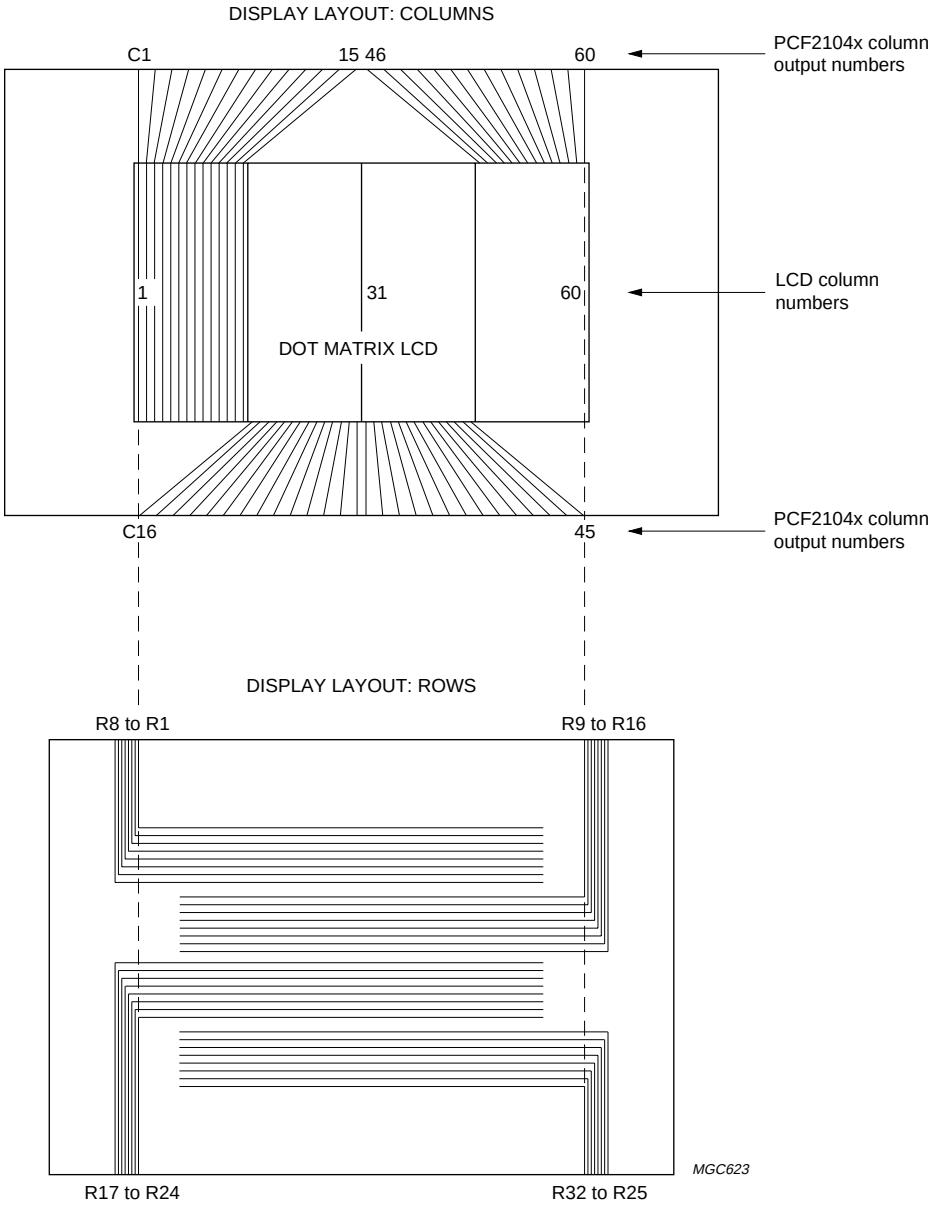


Fig.32 Example of 4 × 12 display layout (PCF2104x).

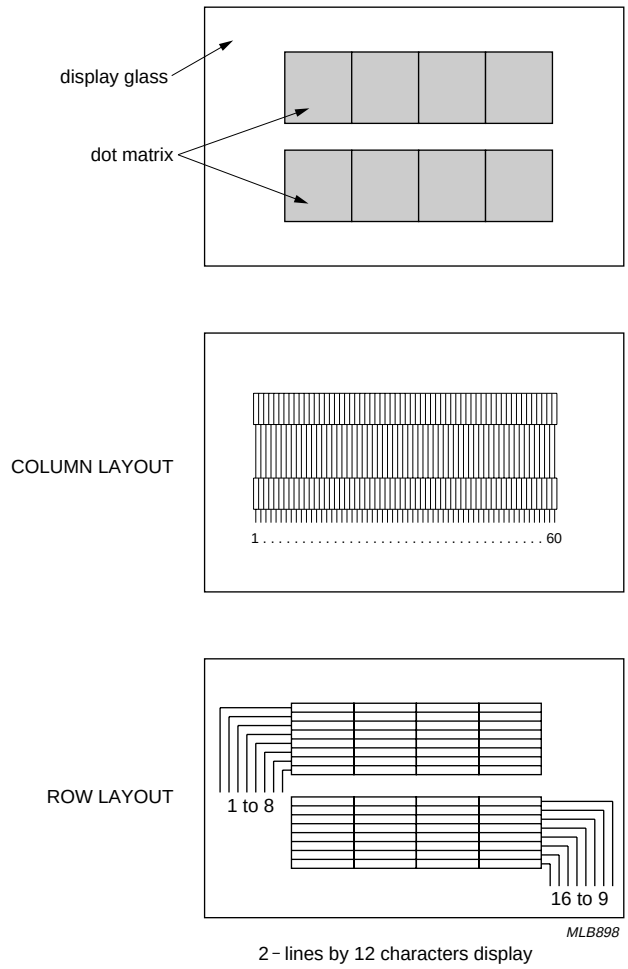


Fig.33 Display example (PCF2104x); 2 lines by 12 characters.

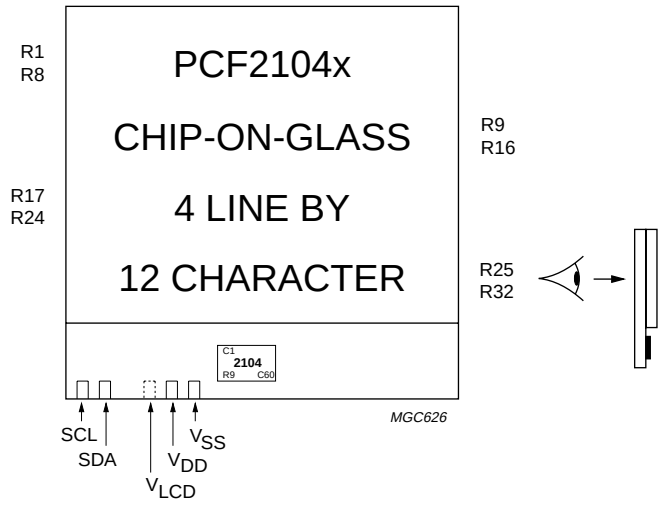
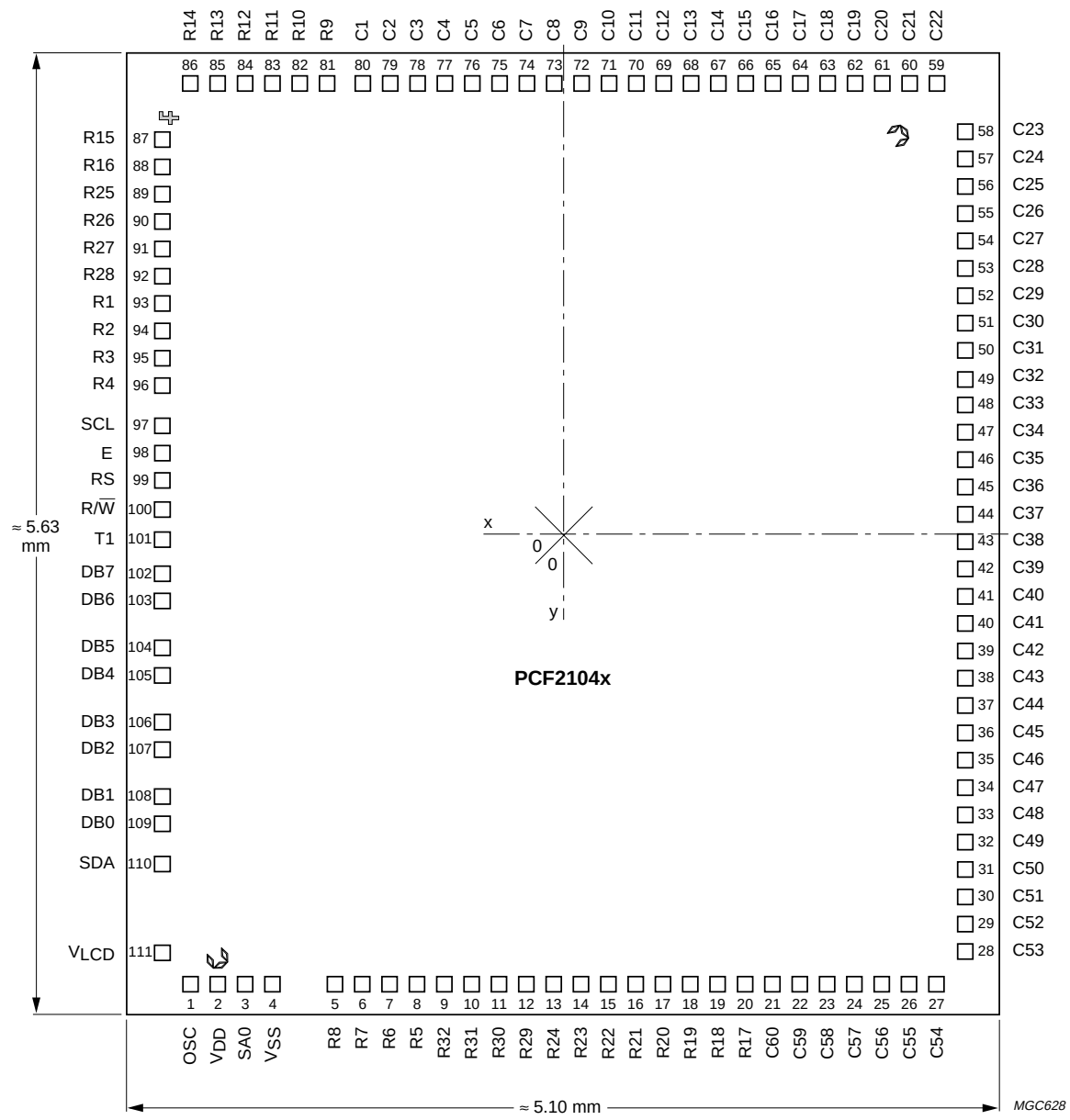


Fig.34 Chip-on-glass application.

18 BONDING PAD LOCATIONS



Chip dimensions: approximately 5.10 × 5.63 mm.
Gold bump dimensions: approximately 89 × 89 × 25 µm.

Fig.35 Bonding pad locations.

Table 12 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to centre of chip, see Fig.35

SYMBOL	PAD	x	y
OSC	1	−2184.5	−2637
V_{DD}	2	−2024.5	−2637
SA0	3	−1864.5	−2637
V_{SS}	4	−1704.5	−2637
R8	5	−1339	−2637
R7	6	−1179	−2637
R6	7	−1019	−2637
R5	8	−859	−2637
R32	9	−699	−2637
R31	10	−539	−2637
R30	11	−379	−2637
R29	12	−219	−2637
R24	13	−59	−2637
R23	14	101	−2637
R22	15	261	−2637
R21	16	421	−2637
R20	17	581	−2637
R19	18	741	−2637
R18	19	901	−2637
R17	20	1061	−2637
C60	21	1221	−2637
C59	22	1381	−2637
C58	23	1541	−2637
C57	24	1701	−2637
C56	25	1861	−2637
C55	26	2021	−2637
C54	27	2181	−2637
C53	28	2350	−2445
C52	29	2350	−2285
C51	30	2350	−2125
C50	31	2350	−1965
C49	32	2350	−1805
C48	33	2350	−1645
C47	34	2350	−1485
C46	35	2350	−1325
C45	36	2350	−1165
C44	37	2350	−1005
C43	38	2350	−845

SYMBOL	PAD	x	y
C42	39	2350	−685
C41	40	2350	−525
C40	41	2350	−365
C39	42	2350	−205
C38	43	2350	−45
C37	44	2350	115
C36	45	2350	275
C35	46	2350	435
C34	47	2350	595
C33	48	2350	755
C32	49	2350	915
C31	50	2350	1075
C30	51	2350	1235
C29	52	2350	1395
C28	53	2350	1555
C27	54	2350	1715
C26	55	2350	1875
C25	56	2350	2035
C24	57	2350	2195
C23	58	2350	2355
C22	59	2185	2637.5
C21	60	2025	2637.5
C20	61	1865	2637.5
C19	62	1705	2637.5
C18	63	1545	2637.5
C17	64	1385	2637.5
C16	65	1225	2637.5
C15	66	1065	2637.5
C14	67	905	2637.5
C13	68	745	2637.5
C12	69	585	2637.5
C11	70	425	2637.5
C10	71	265	2637.5
C9	72	105	2637.5
C8	73	−55	2637.5
C7	74	−215	2637.5
C6	75	−375	2637.5
C5	76	−535	2637.5

SYMBOL	PAD	x	y
C4	77	–695	2637.5
C3	78	–855	2637.5
C2	79	–1015	2637.5
C1	80	–1175	2637.5
R9	81	–1385	2637.5
R10	82	–1545	2637.5
R11	83	–1705	2637.5
R12	84	–1865	2637.5
R13	85	–2025	2637.5
R14	86	–2185	2637.5
R15	87	–2349	2308
R16	88	–2349	2148
R25	89	–2349	1988
R26	90	–2349	1828
R27	91	–2349	1668
R28	92	–2349	1508
R1	93	–2349	1348
R2	94	–2349	1188
R3	95	–2349	1028
R4	96	–2349	868
SCL	97	–2349	632
E	98	–2349	472
RS	99	–2349	312
R/$\overline{W}$	100	–2349	142
T1	101	–2349	–34
DB7	102	–2349	–233
DB6	103	–2349	–393
DB5	104	–2349	–668
DB4	105	–2349	–828
DB3	106	–2349	–1103
DB2	107	–2349	–1263
DB1	108	–2349	–1538
DB0	109	–2349	–1698
SDA	110	–2349	–1933
V_{LCD}	111	–2349	–2453
RECPAT ‘F’		–2327.5	2427.5
RECPAT ‘C’		–2027.5	–2512.5
RECPAT ‘C’		1982.5	2297.5

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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