HARRIS SEMICONDUCTOR

HS-546RH
HS-547RH

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

June 1993

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Gamma Dose ..... 2×10^4 RAD(Si)
- No Latch-Up
- No Channel Interaction During Overvoltage
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switch
- Analog Signal Range ..... ±15V
- Access Time 1.0µs

Applications

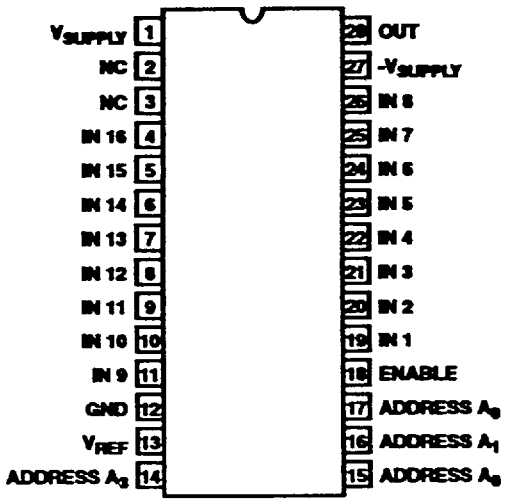
- Data Acquisition Systems
- Control Systems
- Telemetry

Description

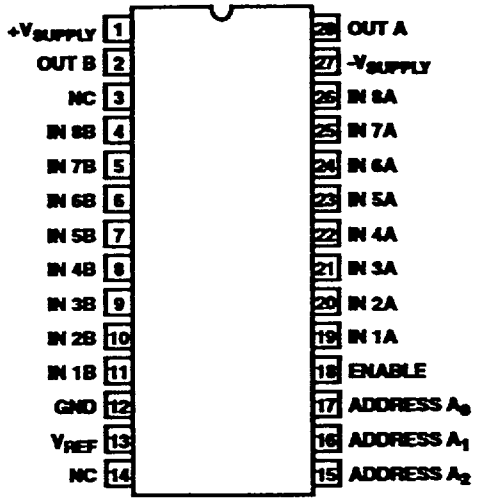
The HS-546RH and HS-547RH are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels with ±15V supplies and digital inputs will sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur: each input presents 1KΩ of resistance under this condition. These features make the HS-546RH and HS-547RH ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HS-546 is a 16 channel device and the HS-547 is an 8 channel differential version. If input overvoltage protection is not needed, the HS-506 and HS-507 multiplexers are recommended.

Pinouts

HS1-546RH
TOP VIEW



HS1-547RH
TOP VIEW

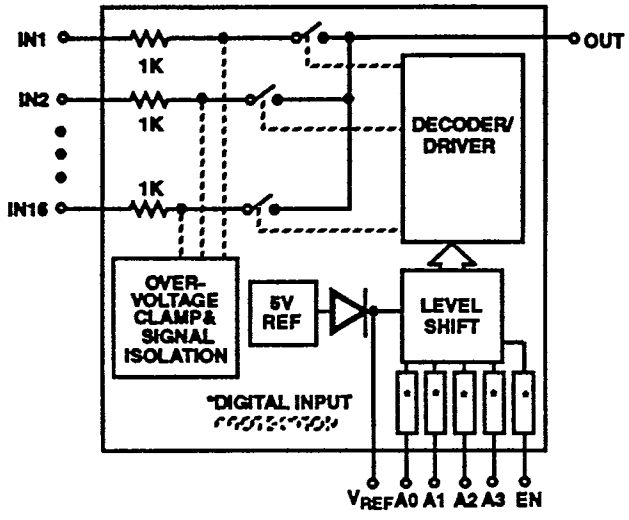


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

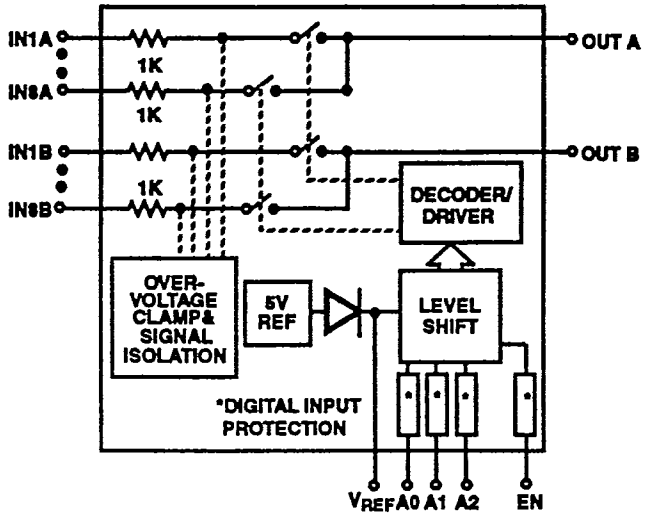
File Number 3544

Functional Diagrams

HS-546RH



HS-547RH



HS-546RH TRUTH TABLE

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HS-547RH TRUTH TABLE

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Specifications HS-546RH, HS-547RH

Absolute Maximum Ratings

Supply Voltage Between Pins 1 and 27 ..... +44V
$+V_{SUPPLY}$ to Ground ..... +22V
$-V_{SUPPLY}$ to Ground ..... -25V
Analog Input Overvoltage:
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Digital Input Overvoltage:
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 200mA, whichever occurs first
Continuous Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Maximum 40mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +275°C

Junction Temperature ..... +175°C
Thermal Resistance, Junction-to-Case (θ_{JC})
Ceramic DIP Package ..... 18°C/W
Thermal Resistance, Junction-to-Ambient (θ_{JA})
Ceramic DIP Package ..... 50°C/W
Power Dissipation (at +75°C)
Ceramic DIP Package 2.0W
Power Dissipation Derating Factor (above +75°C)
Ceramic DIP Package ..... 20.0mW/°C
ESD Classification ..... <2000V

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... V_{SUPPLY}

Logic Low Level (V_{AL}) ..... 0 to 0.8V
Logic High Level (V_{AH}) ..... +4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially GND All Unused Inputs		1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}			1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
Leakage Current into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = -10V		1	+25°C	-10	+10	nA
				2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = +10V		1	+25°C	-10	+10	nA
				2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V		1	+25°C	-10	+10	nA
			HS-546	2, 3	+125°C, -55°C	-300	+300	nA
			HS-547	2, 3	+125°C, -55°C	-200	+200	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V		1	+25°C	-10	+10	nA
			HS-546	2, 3	+125°C, -55°C	-300	+300	nA
			HS-547	2, 3	+125°C, -55°C	-200	+200	nA
Leakage Current From an "ON" Driver into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V All Unused Inputs = -10V		1	+25°C	-10	+10	nA
			HS-546	2, 3	+125°C, -55°C	-300	+300	nA
			HS-547	2, 3	+125°C, -55°C	-200	+200	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All Unused Inputs = +10V		1	+25°C	-10	+10	nA
			HS-546	2, 3	+125°C, -55°C	-300	+300	nA
			HS-547	2, 3	+125°C, -55°C	-200	+200	nA
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "ON" Switch	$-I_{D(OFF)}$ Over Voltage	V_S = 33V, V_D = 0V, E_N = 0.8V V_S Applied at ≤25% Duty Cycle		1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	µA
		V_S = -33V, V_D = 0V, E_N = 0.8V V_S Applied at ≤25% Duty Cycle		1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	µA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 4.0V		1, 2, 3	+25°C, +125°C, -55°C	-	2.0	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 4.0V		1, 2, 3	+25°C, +125°C, -55°C	-1.0	-	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V		1, 2, 3	+25°C,+ 125°C, -55°C	-	2.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V		1, 2, 3	+25°C,+125°C, -55°C	-1.0	-	mA

Specifications HS-546RH, HS-547RH

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	$+R_{DS1}$	V_S = +10V, I_D = -100µA	1	+25°C	-	1500	Ω
			2, 3	+125°C, -55°C	-	1800	Ω
	$-R_{DS1}$	V_S = -10V, I_D = +100µA	1	+25°C	-	1500	Ω
			2, 3	+125°C, -55°C	-	1800	Ω
Logic Level Voltage	V_{AL1}	Notes 1, 2	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH1}	Notes 1, 2	1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
	V_{AL2}	Note 3	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH2}	Note 3	1, 2, 3	+25°C, +125°C, -55°C	6.0	-	V
Difference in Switch "ON" Resistance Between Channels	$+\Delta R_{DS1}$	$\frac{(+R_{DS1}MAX) - (+R_{DS1}MIN) \times 100}{+R_{DS1}AVE}$	1	+25°C	-	7	%
	$-\Delta R_{DS1}$	$\frac{(-R_{DS1}MAX) - (-R_{DS1}MIN) \times 100}{-R_{DS1}AVE}$	1	+25°C	-	7	%

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, (Pin 13) = OPEN, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 1kΩ, CL = 12.5pF	9	+25°C	25	-	ns
			10, 11	+125°C, -55°C	5	-	ns
Propogation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10kΩ, CL = 14pF	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 1kΩ, CL = 12.5pF	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	1000	ns
	$t_{OFF(EN)}$	R_L = 1kΩ, CL = 12.5pF	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, (Pin 13) = OPEN, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V f = 1MHz		4	+25°C	-	12	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V f = 1MHz	HS-546	4	+25°C	-	85	pF
			HS-547	4	+25°C	-	50	pF
Capacitance: Input Switcht	C_{IS}	V+ = V- = 0V f = 1MHz		4	+25°C	-	15	pF
Charge Transfer Error	V_{CTE}	V_S = GND V_{GEN} = 0V to 5V		4	+25°C	-	10	mV
Off Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1KΩ, C_L = 15pF, VS = 7 V_{RMS} f = 100kHz		4,5	+25°C	-50	-	dB

Specifications HS-546RH, HS-547RH

TABLE 4. POST 20k RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at $+V_{SUPPLY}$ = +15V. $-V_{SUPPLY}$ = -15V. V_{EN} = 4.5V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially GND All Unused Inputs		1	+25°C	-1.0	1.0	µA
	I_{IL}			1	+25°C	-1.0	1.0	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.5V All Unused Inputs = –10V		1	+25°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.5V All Unused Inputs = +10V		1	+25°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.5V All Unused Inputs = -10V	HS-546	1	+25°C	-300	+300	nA
			HS-547	1	+25°C	-200	+200	
	$-I_{D(OFF)}$	V_D = –10V, V_{EN} = 0.5V All Unused Inputs = +10V	HS546	1	+25°C	-300	+300	nA
			HS-547	1	+25°C	-200	+200	
Leakage Current From an "ON" Driver into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V All Unused Inputs = -10V	HS-546	1	+25°C	-300	+300	nA
			HS-547	1	+25°C	-200	+200	
	$-I_{D(ON)}$	V_S = V_D = –10V All Unused Inputs = +10V	HS-546	1	+25°C	-300	+300	nA
			HS-547	1	+25°C	-200	+200	
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "ON" Switch	$-I_{D(OFF)}$ Over Voltage	V_S = 33V, V_D = 0V, E_N = 0.5V V_S Applied at ≤25% Duty Cycle		1	+25°C	-5.0	+5.0	µA
		V_S = -33V, V_D = 0V, E_N = 0.5V V_S Applied at ≤25% Duty Cycle		1	+25°C	-5.0	+5.0	µA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 4.5V		1	+25°C		2.0	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 4.5V		1	+25°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V		1	+25°C	-	2.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V		1	+25°C	-1.0	-	mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = +10V, I_D = -100µA		1	+25°C	-	1800	Ω
	$-R_{DS1}$	V_S = -10V, I_D = +100µA		1	+25°C	-	1800	Ω
Logic Level Voltage	V_{AL1}	Notes 1,2		1	+25°c	-	0.5	V
	V_{AH1}	Notes 1,2		1	+25°c	4.5	-	V
	V_{AL2}	Note 3		1	+25°c	-	0.5	V
	V_{AH2}	Note 3		1	+25°c	6.5		V
Difference in Switch "ON" Resistance Between Channels	$+\Delta R_{DS1}$	$\frac{(+R_{DS1}MAX) - (+R_{DS1}MIN) \times 100}{+R_{DS1}AVE}$		1	+25°C	-	7	%
	$-\Delta R_{DS1}$	$\frac{(-R_{DS1}MAX) - (-R_{DS1}MIN) \times 100}{-R_{DS1}AVE}$		1	+25°C	-	7	%

Specifications HS-546RH, HS-547RH

TABLE 4A. POST 20k RAD AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 1kΩ, CL = 12.5pF	9	+25°C	5	-	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10kΩ, CL = 14pF	9	+25°C	-	1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 1kΩ, CL = 12.5pF	9	+25°C	-	1000	ns
	$t_{OFF(EN)}$	R_L = 1kΩ, CL = 12.5pF	9	+25°C	-	1000	ns

NOTES:

1. Used for forcing conditions for all DC tests, unless otherwise specified.
2. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply recommended.
3. V_{REF} = +10V
4. The parameters listed in this table are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
5. Worst case isolation occurs on channel 8B due to proximity of the output pins.

TABLE 5. DC POST BURN-IN DELTA ELECTRICAL SPECIFICATIONS

Device tested Per Table 1.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address,or Enable Pins	I_{AH} I_{AL}	Same as Table 1	1	+25°C	-100	+100	nA
Leakage Current into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	Same as Table 1	1	+25°C	-10	+10	nA
	$-I_{S(OFF)}$	Same as Table 1	1	+25°C	-10	+10	nA
Leakage Current into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	Same as Table 1	1	+25°C	-10	+10	nA
	$-I_{D(OFF)}$	Same as Table 1	1	+25°C	-10	+10	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	$+I_{D(ON)}$	Same as Table 1	1	+25°C	-10	+10	nA
	$-I_{D(ON)}$	Same as Table 1	1	+25°C	-10	+10	nA
Switch On Resistance	+10V $R_{(DS)}$	Same as Table 1	1	+25°C	-150	+150	Ω
	-10V $R_{(DS)}$	Same as Table 1	1	+25°C	-150	+150	Ω
Positive Supply Current	$I_{(+)}$	Same as Table 1	1	+25°C	-200	+200	µA
Negative Supply Current	$I_{(-)}$	Same as Table 1	1	+25°C	-100	+100	µA
Positive Standby Supply Current	$+I_{SBY}$	Same as Table 1	1	+25°C	-200	+200	µA
Negative Standby Supply Current	$-I_{SBY}$	Same as Table 1	1	+25°C	-100	+100	µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1, 7
Group D		Samples/5005	1, 7
Group E, Subgroup 2		Samples/5005	1, 7

Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 72 Hour, +125°C method 1015 Condition A

Room Temperature Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D

Electrical Tests Subgroups 1, 7, 9 (T2)

Burn-In Delta Calculation (T0 - T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

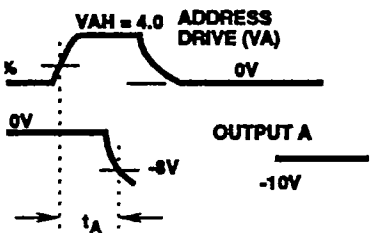
Data Package Generation (Note 3)

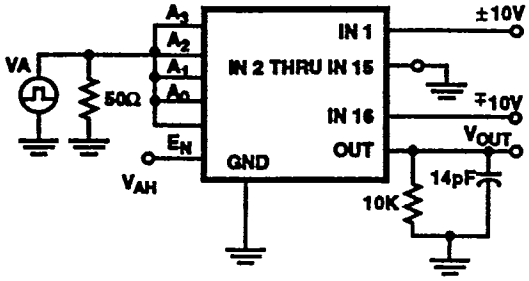
NOTES:

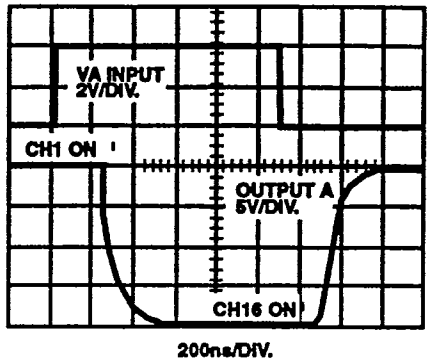
1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) – 55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Switching Waveforms

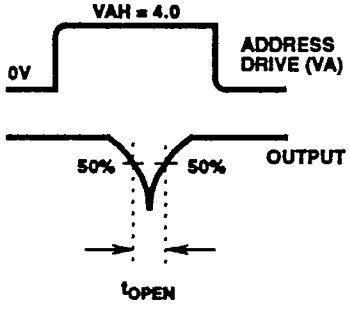
ACCESS TIME

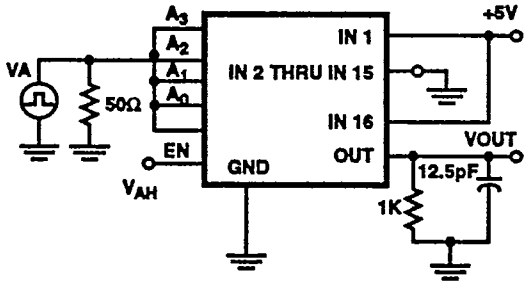


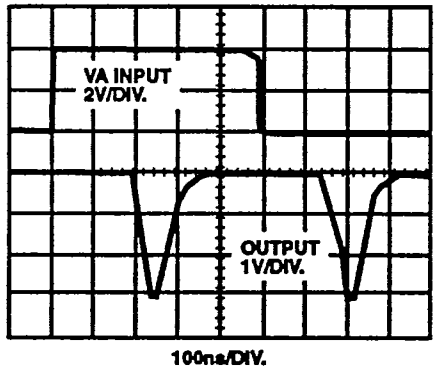




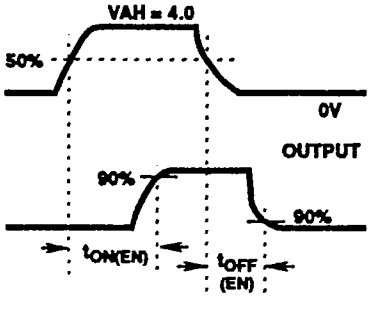
BREAK-BEFORE-MAKE DELAY (t_{OPEN})

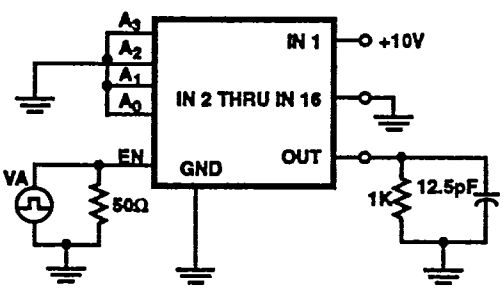


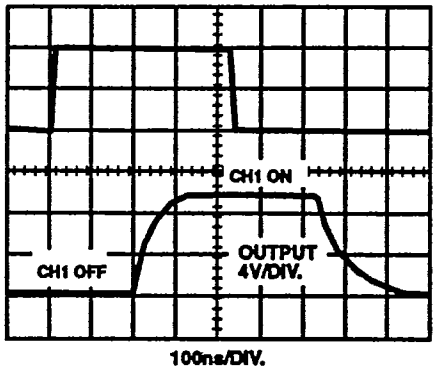




ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

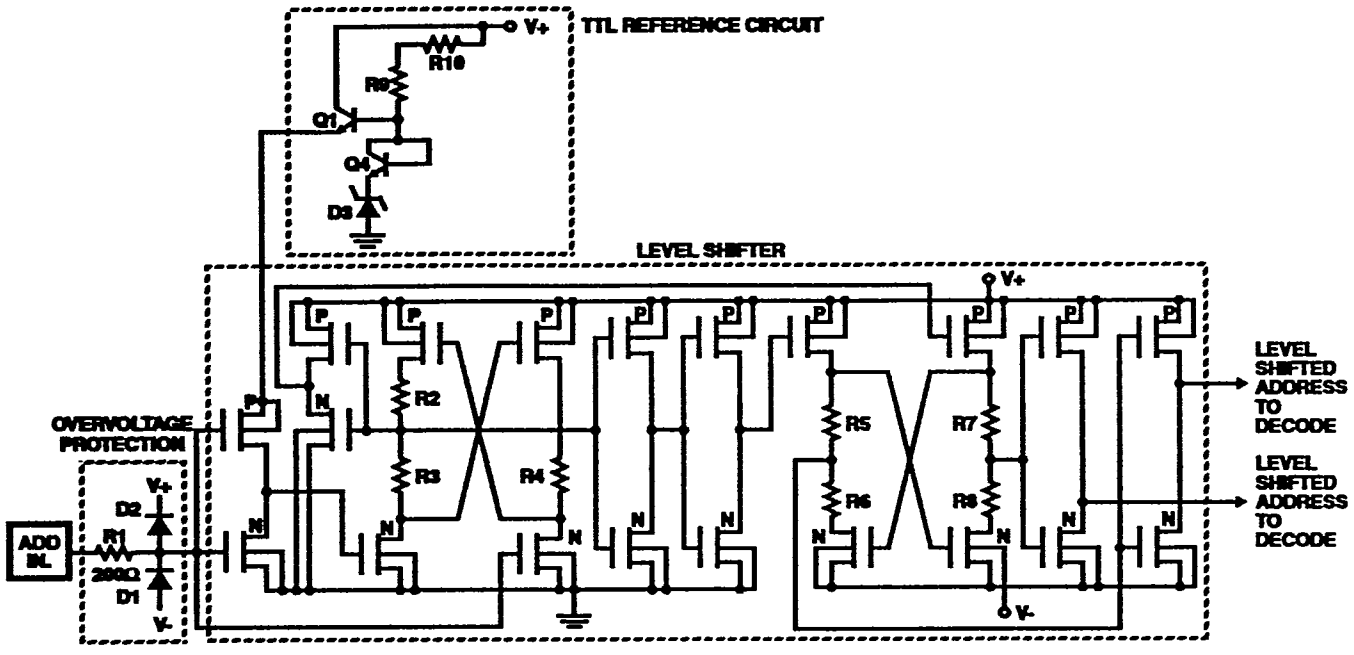




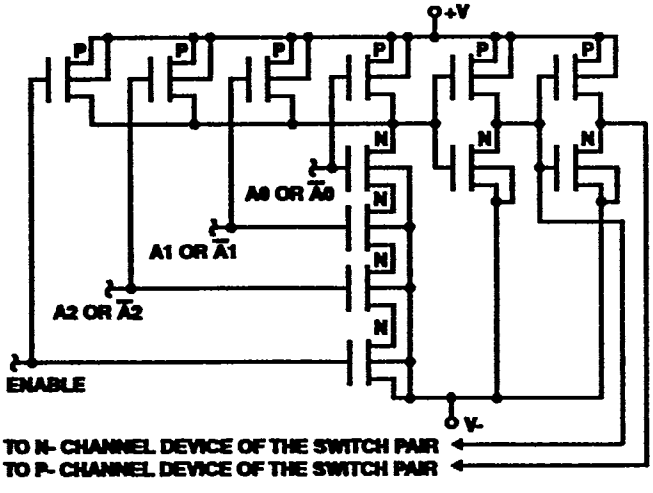


Schematic Diagrams

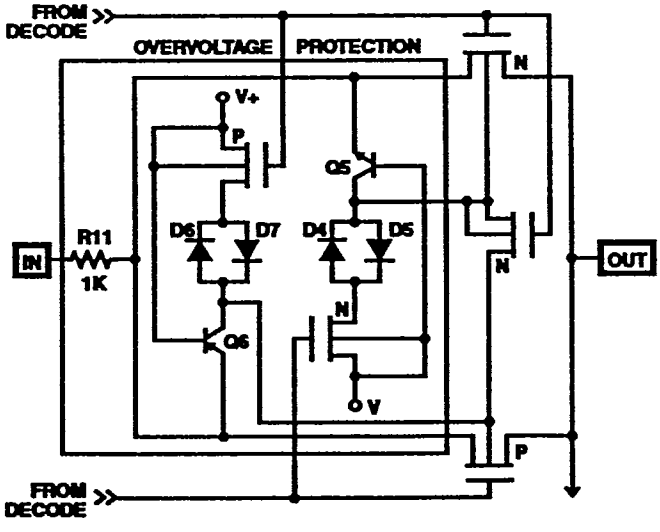
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



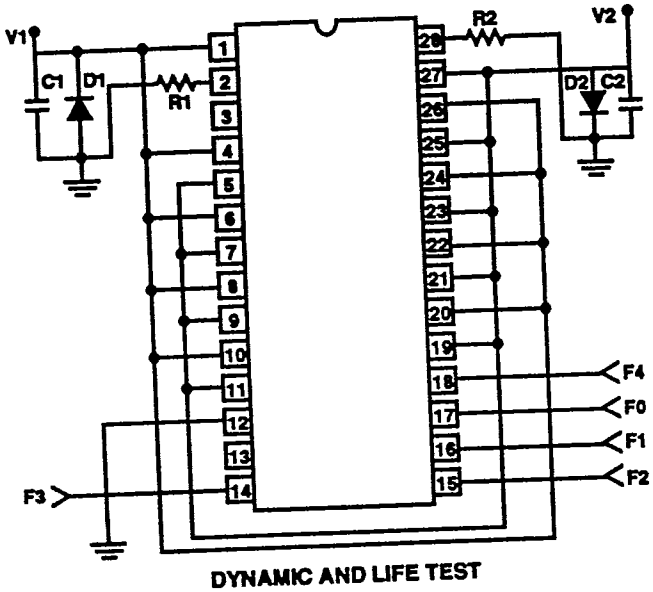
ADDRESS DECODER



MULTIPLEX SWITCH

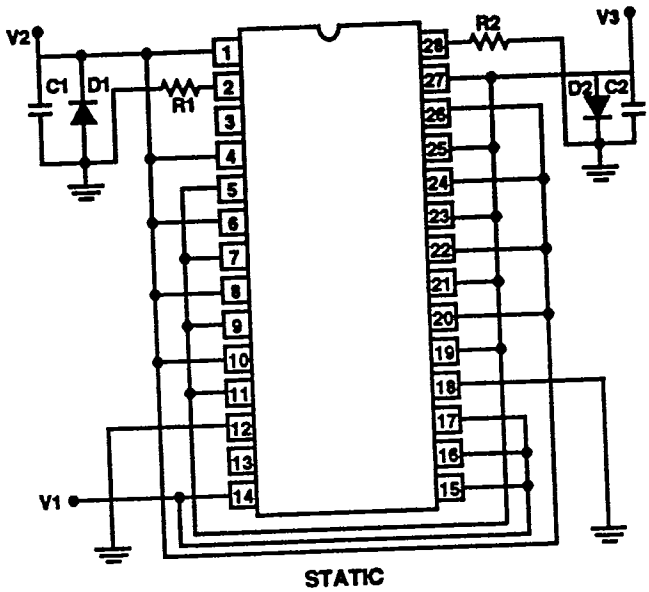


Burn-In/Life Test Circuits



DYNAMIC AND LIFE TEST

V1 = +15.5 volts minimum, +16 volts maximum
V2 = -15.5 volts maximum, -16 volts minimum
R1, R2 = 10K ohms, ± 5%, 1/4 or 1/2 Watt (per socket)
C1, C2 = 0.01µF minimum (per socket) or 0.1µF minimum (per row)
D1, D2 = 1N4002 or equivalent (per board)
F0 = 100KHz, 10%; F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2
40-60% duty cycle; V_{IL} = 0.08 volts max;
V_{IH} = 4.0 volts minimum

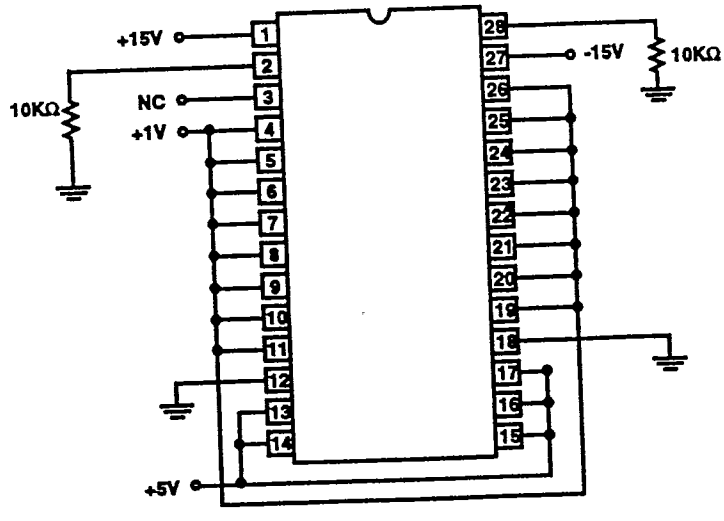


STATIC

V1 = +5 volts minimum, +6 volts maximum
V2 = +15 volts minimum, +16 volts maximum
V3 = -15 volts maximum, -16 volts minimum
R1, R2 = 10K ohms, ±5%, 1/4 or 1/2 Watt (per socket)
C1, C2 =0.01µF minimum (per socket) or 0.1µF minimum (per row)
D1, D2 = 1N4002 or equivalent (per board)

NOTES:
1. The Above Test Circuits are Utilized for All Package Types
2. The Dynamic Test Circuit is Utilized for All Life Testing

Irradiation Circuit



NOTE: All irradiation testing is performed in the 28 pin DIP package

HS-546RH, HS-547RH

Metallization Topology

DIE DIMENSIONS:
83.9 x 159 x 19 mils

METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

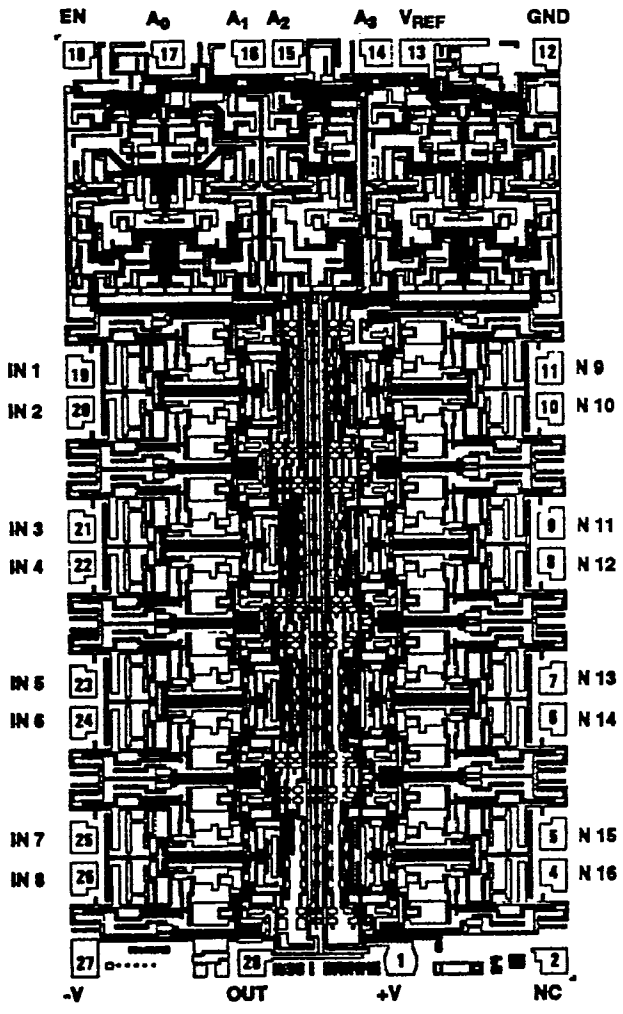
WORST CASE CURRENT DENSITY:
1.4×10^5 A/cm^2

TRANSISTOR COUNT:
HS-546 485
HS-547 485

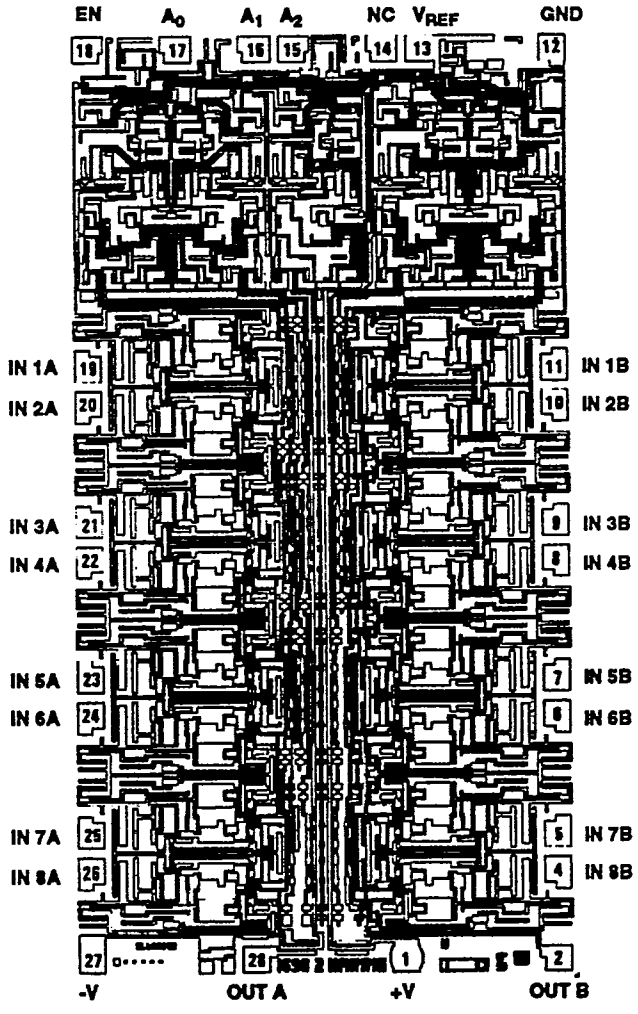
PROCESS: CMOS-DI

Metallization Mask Layout

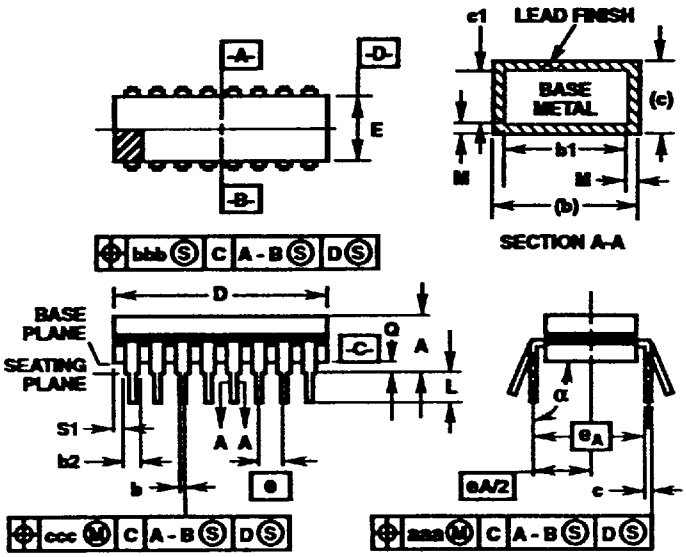
HS-546RH



HS-547RH



Packaging



F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch
11. Lead Finish: Type A.
12. Material: Compliant to MIL-M-38510

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