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FAN1084

4.5A Adjustable/Fixed Low Dropout Linear Regulator

Features

- Fast transient response
- Low dropout voltage at up to 4.5A
- Load regulation: 0.5% typical
- On-chip thermal limiting
- Standard TO-220 and TO-263 center cut packages

Applications

- Desktop PCs, RISC and embedded processors' supply
- GTL, SSTL logic Reference bus supply
- Low voltage V_{CC} logic supply
- Battery-powered circuitry
- Post regulator for switching supply
- Cable and ADSL modems' DSP core supply
- Set Top Boxes and Web Boxes modules' supply

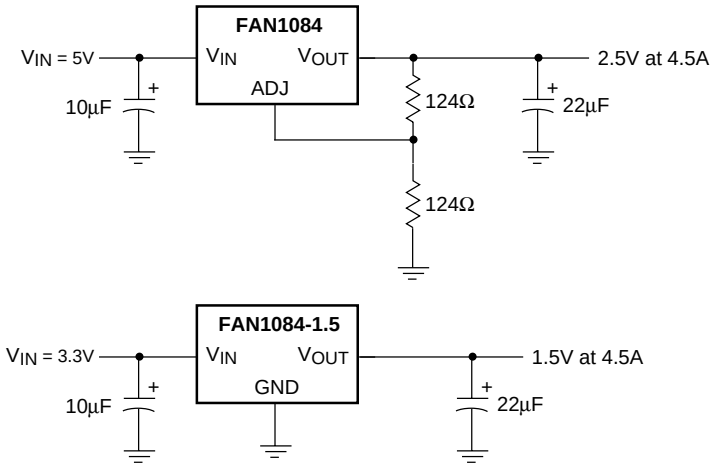
Description

The FAN1084 and FAN1084-1.5 are low dropout three-terminal regulators with 4.5A output current capability. These devices have been optimized for low voltage applications including V_{TT} bus termination, where transient response and minimum input voltage are critical. The FAN1084 is ideal for low voltage microprocessor applications requiring a regulated output from 1.5V to 3.6A with an input supply of 5V or less. The FAN1084-1.5 offers fixed 1.5V with 4.5A current capabilities for GTL+ bus V_{TT} termination.

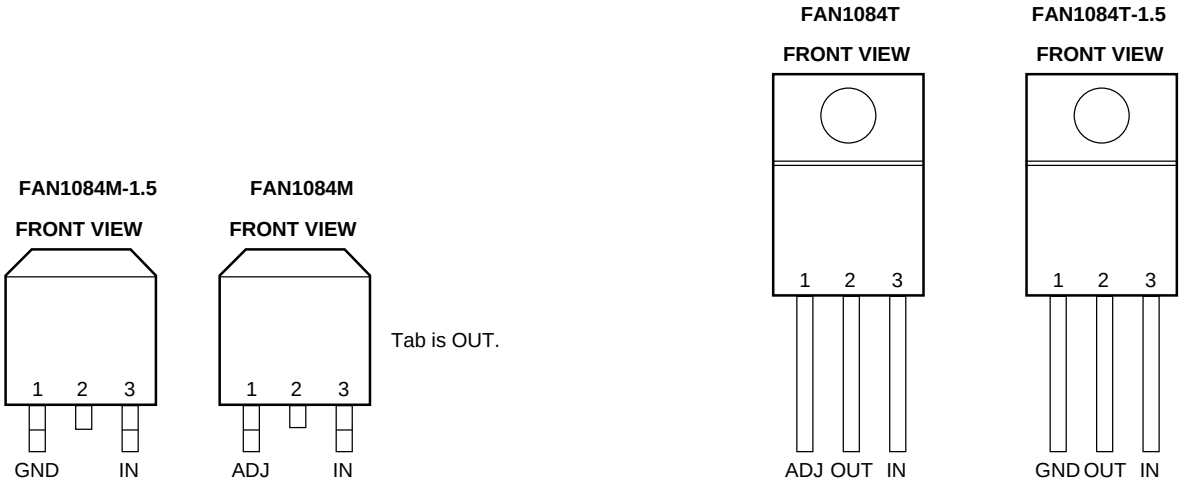
On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

The FAN1084 series regulators are available in the industry-standard TO-220 and TO-263 center cut power packages.

Block Diagram



Pin Assignments



3-Lead Plastic TO-263
Θ_{JC}=10°C/W*

3-Lead Plastic TO-220
Θ_{JC}=3°C/W*

*With package soldered to 0.5 square inch copper area over backside ground plane or internal power plane, Θ_{JA} can vary from 30°C/W to more than 40°C/W. Other mounting techniques may provide better power dissipation than 30°C/W.

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	–65	150	°C
Lead Temperature (Soldering, 10 seconds)		300	°C

Preliminary Information

Electrical Characteristics

Operating Conditions: $4.75 \le V_{IN} < 5.25V$, $T_j = 25°C$ unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max	Units
Reference Voltage[3]	Adj connected to ground, I_{OUT} = 10mA	1.23	1.250	1.27	V
Output Voltage[5]	I_{OUT} = 10mA	1.475	1.5	1.525	V
Line Regulation[1, 2]	I_{OUT} = 10mA		0.5	2	%
Load Regulation[1, 2]	10mA ≤ I_{OUT} ≤ 4.5A		0.5	2.5	%
Dropout Voltage	ΔV_{REF} = 2%, I_{OUT} = 4.5A			1.5	V
Current Limit	($V_{IN} - V_{OUT}$) = 2V		5.5		A
Adjust Pin Current[3]			35	100	µA
Mimimum Load Current[4]	1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 5.75V		10		mA
Quiescent Current[4]	V_{IN} = 5V		4		mA
Thermal Resistance, Junction to Case	TO-220		3		°C/W
	TO-263		10		°C/W
Thermal Shutdown[4]			150		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation. Power dissipation is determined by input/output differential and the output currrent. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. FAN1084 only.
4. Guaranteed by design.
5. FAN1084-1.5 only.

Typical Performance Characteristics

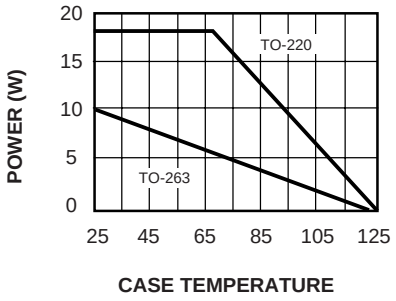


Figure 1. Maximum Power Dissipation

Preliminary Information

Applications Information

General

The FAN1084 and FAN1084-1.5 are three-terminal regulators optimized for GTL+ V_{TT} termination and logic applications. These devices are short-circuit protected, and offer thermal shutdown to turn off the regulator when the junction temperature exceeds about 150°C. The FAN1084 series provides low dropout voltage and fast transient response. Frequency compensation uses capacitors with low ESR while still maintaining stability. This is critical in addressing the needs of low voltage high speed microprocessor buses like GTL+.

Stability

The FAN1084 series requires an output capacitor as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100µF aluminum electrolytic on the output to ensure stability. The frequency compensation of these devices optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <1Ω. It is also recommended to use bypass capacitors such as a 22µF tantalum or a 100µF aluminum on the adjust pin of the FAN1084 for low ripple and fast transient response. When these bypassing capacitors are not used at the adjust pin, smaller values of output capacitors provide equally good results.

Protection Diodes

In normal operation, the FAN1084 series does not require any protection diodes. For the FAN1084, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under short-circuit conditions.

A protection diode between the input and output pins is usually not needed. An internal diode between the input and the output pins on the FAN1084 series can handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input can generate those levels of current; a diode from output to input is then recommended, as shown in Figure 2. Usually, normal power supply cycling or system “hot plugging and unplugging” will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the ouput, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

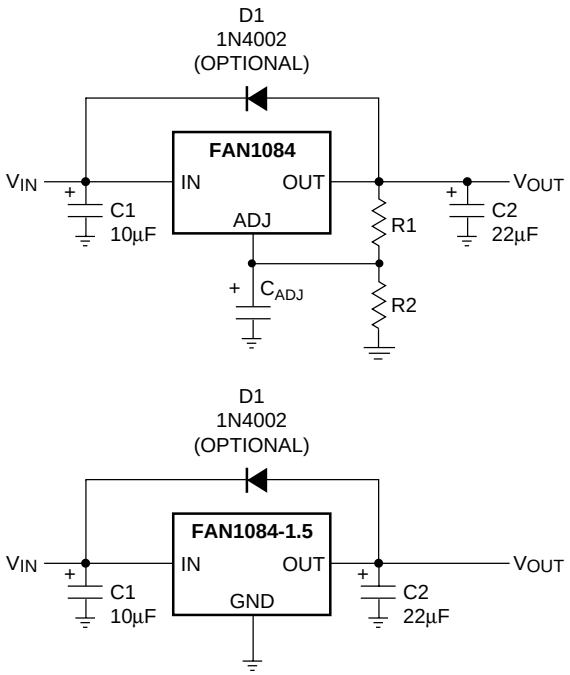


Figure 2. Optional Protection

Ripple Rejection

In applications that require improved ripple rejection, a bypass capacitor from the adjust pin of the FAN1084 to ground reduces the output ripple by the ratio of V_{OUT}/1.25V. The impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1 (typically in the range of 100Ω to 120Ω) in the feedback divider network in Figure 2. Therefore, the value of the required adjust pin capacitor is a function of the input ripple frequency. For example, if R1 equals 100Ω and the ripple frequency equals 120Hz, the adjust pin
capacitor should be 22µF. At 10kHz, only 0.22µF is needed.

Output Voltage

The FAN1084 regulator develops a 1.25V reference voltage between the ouput pin and the adjust pin (see Figure 3). Placing a resistor R1 between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. Normally, this current is the specified minimum load current of 10mA.

The current out of the adjust pin adds to the current from R1. Its output voltage contribution is small and only needs consideration when a very precise output voltage setting is required.

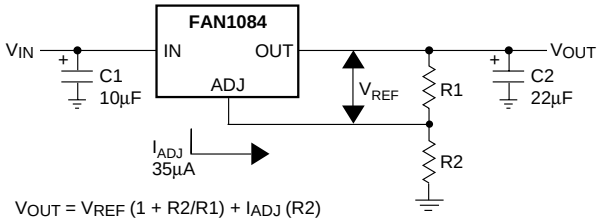


Figure 3. Basic Regulation Circuit

Load Regulation

It is not possible to provide true remote load sensing because the FAN1084 series are three-terminal devices. Load regulation is limited by the resistance of the wire connecting the regulator to the load. Load regulation per the data sheet specification is measured at the bottom of the package.

For fixed voltage devices, negative side sensing is a true Kelvin connection with the ground pin of the device returned to the negative side of the load. This is illustrated in Figure 4.

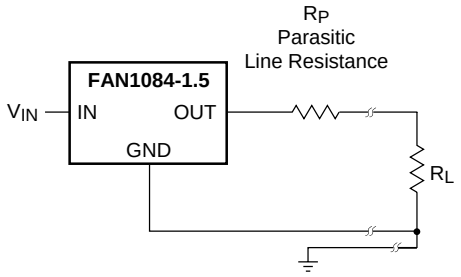


Figure 4. Connection for Best Load Regulation

For adjustable voltage devices, negative side sensing is a true Kelvin connection with the bottom of the output divider returned to the negative side of the load. The best load regulation is obtained when the top of the resistor divider R1 connects directly to the regulator output and not to the load. Figure 5 illustrates this point.

If R1 connects to the load, then the effective resistance between the regulator and the load would be:

R_P X (1 + R2/R1), R_P = Parasitic Line Resistance

The connection shown in Figure 5 does not multiply R_P by the divider ration. As an example, R_P is about four milliohms per foot with 16-gauge wire. This translates to 4mV per foot at 1A load current. At higher load currents, this drop represents a significant percentage of the overall regulation. It is important to keep the positive lead between the regulator and the load as short as possible and to use large wire or PC board traces.

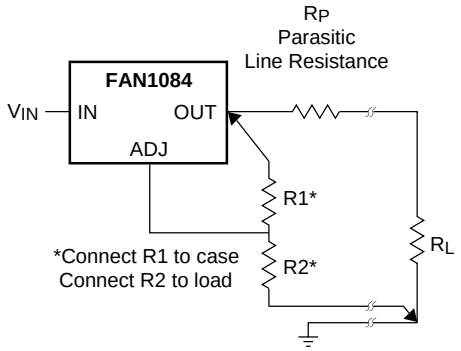


Figure 5. Connection for Best load Regulation

Thermal Conditions

The FAN1084 series protect themselves under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heatsink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The electrical characteristics section provides a separate thermal resistance and maximum junction temperature for both the control circuitry and the power transistor. Calculate the maximum junction temperature for both sections to ensure that both thermal limits are met.

For example, look at using an FAN1084T to generate 4.5A @ 1.5V from a 3.3V source (3.2V to 3.6V).

Assumptions

- V_{IN} = 3.6V worst case
- V_{OUT} = 1.475V worst case
- I_{OUT} = 4.5A continuous
- T_A = 60°C
- $\theta_{Case\text{-}to\text{-}Ambient}$ = 5°C/W (assuming both a heatsink and a thermally conductive material)

The power dissipation in this application is:
$P_D = (V_{IN} - V_{OUT}) * (I_{OUT}) = (3.6 - 1.475) * (4.5) = 9.6W$

From the specification table:
$T_J = T_A + (P_D) * (\theta_{Case\text{-}to\text{-}Ambient} + \theta_{JC})$
$= 60 + (9.6) * (5 + 3) = 137°C$

The junction temperature is below the maximum thermal limit.

Preliminary Information

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Use of a thermally conductive material at the case-to-heat sink interface is recommended. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance. The cases of the FAN1084 series are directly connected to the output of the device.

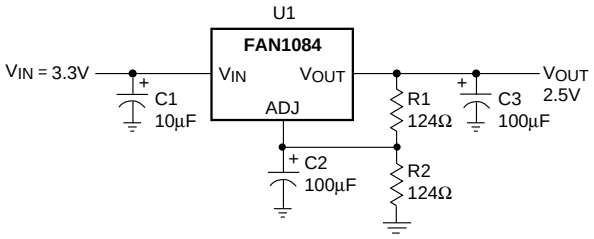


Figure 6. Application Circuit

Table 1. Bill of Materials for Application Circuit for the FAN1084

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2, C3	2	Xicon	L10V100	100µF, 10V Aluminum
R1, R2	2	Generic		124Ω, 1%
U1	1	Fairchild	FAN1084T	4.5A Regulator

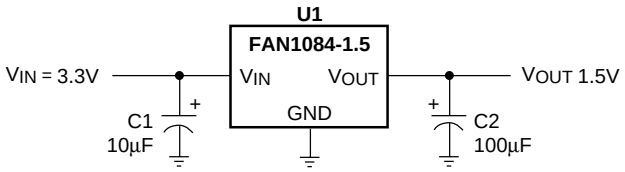


Figure 7. Application Circuit (FAN1084-1.5)

Table 2. Bill of Materials for Application Circuit for the FAN1084-1.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	FAN1084T-1.5	4.5A Regulator

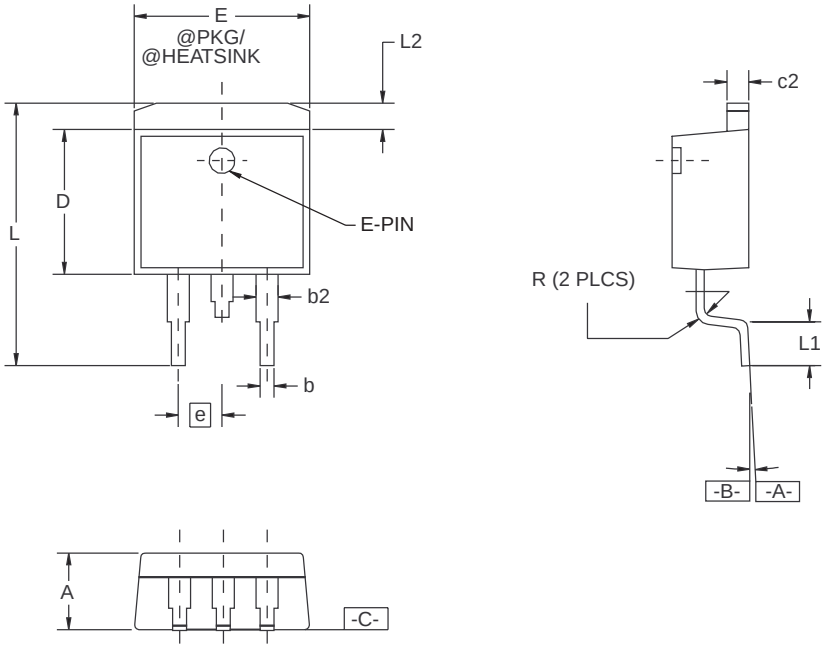
Mechanical Dimensions

3-Lead TO-263 Center Cut Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.48	
α	0°	8°	0°	8°	

Notes:

1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length ismeasured with ref. to Datum -A- with lead surface (at inner R).
4. Dimension exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.

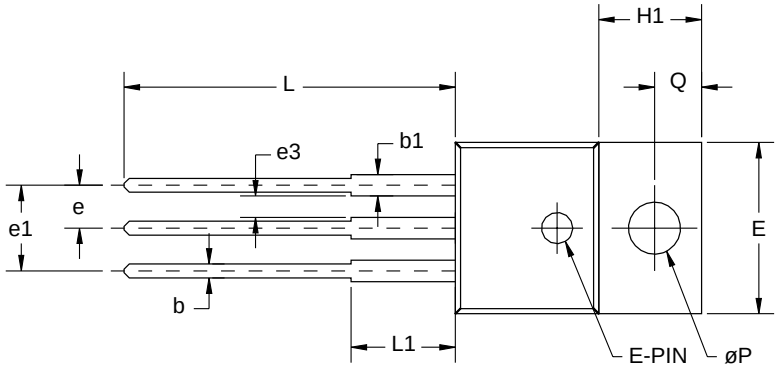


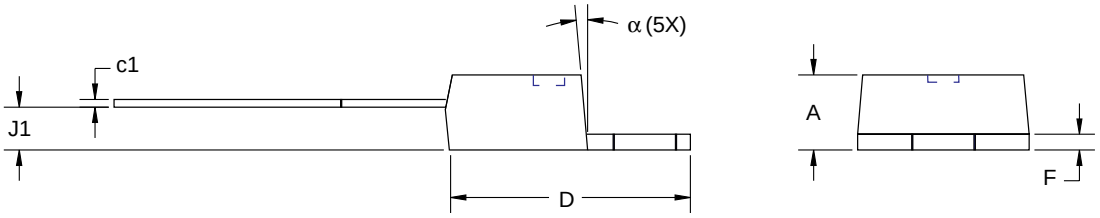
Mechanical Dimensions (continued)

3-Lead TO-220 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.140	.190	3.56	4.83	
b	.015	.040	.38	1.02	
b1	.045	.070	1.14	1.78	
c1	.014	.022	.36	.56	
øP	.139	.161	3.53	4.09	
D	.560	.650	14.22	16.51	
E	.380	.420	9.65	10.67	
e	.090	.110	2.29	2.79	
e1	.190	.210	4.83	5.33	
e3	.045	—	1.14	—	
F	.020	.055	.51	1.40	
H1	.230	.270	5.94	6.87	
J1	.060	.115	2.04	2.92	
L	.500	.580	12.70	14.73	
L1	.250 BSC		6.35 BSC		
Q	1.00	1.35	2.54	3.43	
α	3°	7°	3°	7°	

Notes:
1. Dimension c1 apply for lead finish.





Ordering Information

Product Number	Package
FAN1084MC	TO-263
FAN1084T	TO-220
FAN1084MC-1.5	TO-263
FAN1084T-1.5	TO-220

Preliminary Information

FAN1086

1.5A Adjustable/Fixed Low Dropout Linear Regulator

Target Specification

Features

- Low dropout voltage
- Load regulation: 0.05% typical
- Trimmed current limit
- On-chip thermal limiting
- Standard SOT-223 and TO-263 packages
- Three-terminal adjustable or fixed 2.5V, 2.85V, 3.3V, 5V

Applications

- Active SCSI terminators
- High efficiency linear regulators
- Post regulators for switching supplies
- Battery chargers
- 5V to 3.3V linear regulators
- Motherboard clock supplies

Description

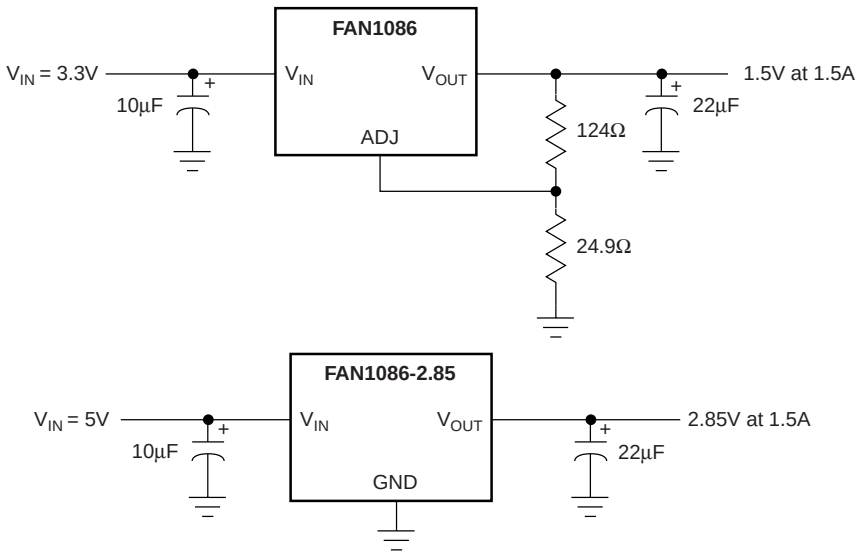
The FAN1086 and FAN1086-2.5, -2.85, -3.3 and -5 are low dropout three-terminal regulators with 1.5A output current capability. These devices have been optimized for low voltage where transient response and minimum input voltage are critical. The 2.85V version is designed specifically to be used in Active Terminators for SCSI bus.

Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperatures that would create excessive junction temperatures.

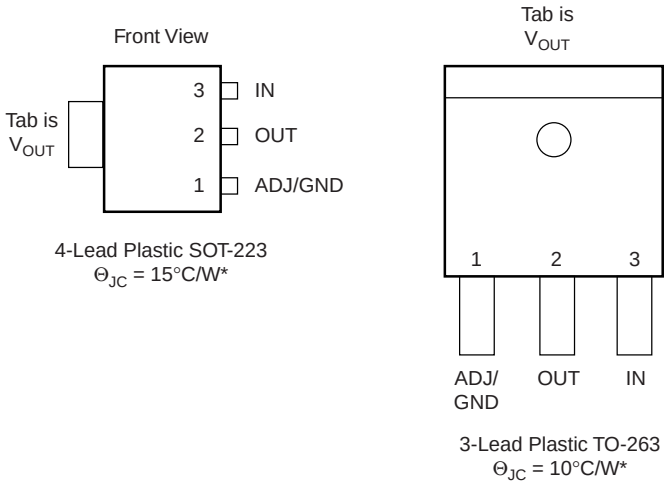
Unlike PNP type regulators where up to 10% of the output current is wasted as quiescent current, the quiescent current of the FAN1086 flows into the load, increasing efficiency.

The FAN1086 series regulators are available in the industry-standard SOT-223 and TO-263 power packages.

Typical Applications



Pin Assignments



*With package soldered to 0.5 square inch copper area over backside ground plane or internal power plane., Θ_{JA} can vary from 30°C/W to more than 50°C/W. Other mounting techniques may provide better thermal resistance than 30°C/W.

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7.5	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

Target Specification

Electrical Characteristics

Operating Conditions: $V_{IN} \leq 7V$, $T_J = 25°C$ unless otherwise specified.

The • denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Reference Voltage[3]	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75V$, $10mA \leq I_{OUT} \leq 1A$	•	1.225 (-2%)	1.250	1.275 (+2%)	V
Output Voltage	$10mA \leq I_{OUT} \leq 1A$					
	FAN1086-2.5, $4V \leq V_{IN} \leq 7V$	•	2.450	2.5	2.550	V
	FAN1086-2.85, $4.35V \leq V_{IN} \leq 7V$	•	2.793	2.85	2.907	V
	FAN1086-3.3, $4.8V \leq V_{IN} \leq 7V$	•	3.234	3.3	3.366	V
	FAN1086-5, $6.5V \leq V_{IN} \leq 7V$	•	4.900	5.0	5.100	V
Line Regulation[1,2]	$(V_{OUT} + 1.5V) \leq V_{IN} \leq 7V$, $I_{OUT} = 10mA$	•		0.005	0.2	%
Load Regulation[1,2]	$(V_{IN} - V_{OUT}) = 2V$, $10mA \leq I_{OUT} \leq 1A$	•		0.05	0.5	%
Dropout Voltage	$\Delta V_{REF} = 1\%$, $I_{OUT} = 1.5A$	•		1.300	1.500	V
Current Limit	$(V_{IN} - V_{OUT}) = 2V$	•	1.6	2.0		A
Adjust Pin Current[3]		•		35	120	µA
Adjust Pin Current Change[3]	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75$, $10mA \leq I_{OUT} \leq 1A$	•		0.2	5	µA
Minimum Load Current	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75$	•	10			mA
Quiescent Current	$V_{IN} = V_{OUT} + 1.25V$	•		4	13	mA
Ripple Rejection	f = 120Hz, C_{OUT} = 22µF Tantalum, $(V_{IN} - V_{OUT}) = 3V$, $I_{OUT} = 1.5A$		60	72		dB
Thermal Regulation	$T_A = 25°C$, 30ms pulse			0.004	0.02	%/W
Temperature Stability		•		0.5		%
Long-Term Stability	$T_A = 125°C$, 1000hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			0.003		%
Thermal Resistance, Juncation to Case	SOT-223			15		°C/W
	TO-263			10		°C/W
Thermal Shutdown	Junction Temperature			155		°C
Thermal Shutdown Hysteresis				10		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output current. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. FAN1086 only.

Target Specification

Target Specification

Typical Performance Characteristics

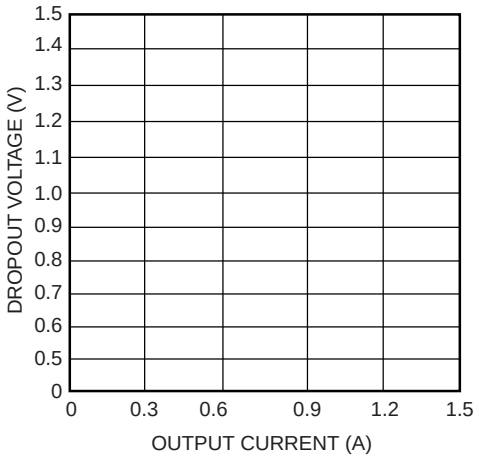


Figure 1. Dropout Voltage vs. Output Current

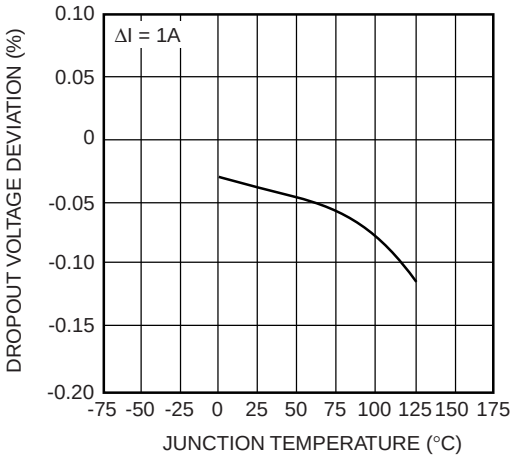


Figure 2. Load Regulation vs. Temperature

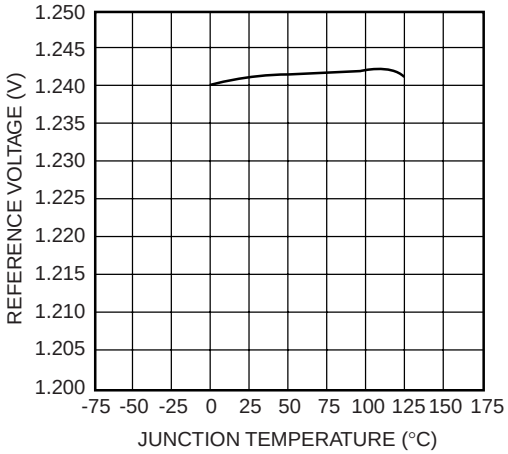


Figure 3. Reference Voltage vs. Temperature

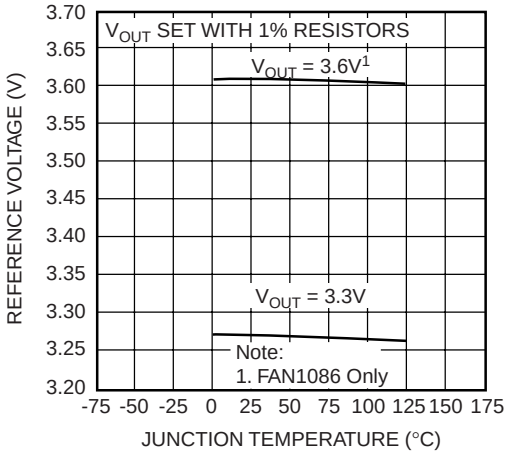


Figure 4. Output Voltage vs. Temperature

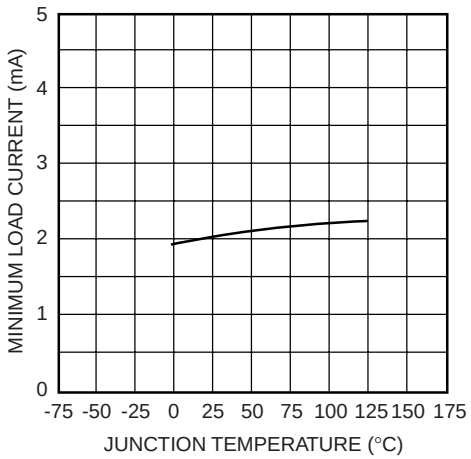


Figure 5. Minimum Load Current vs. Temperature

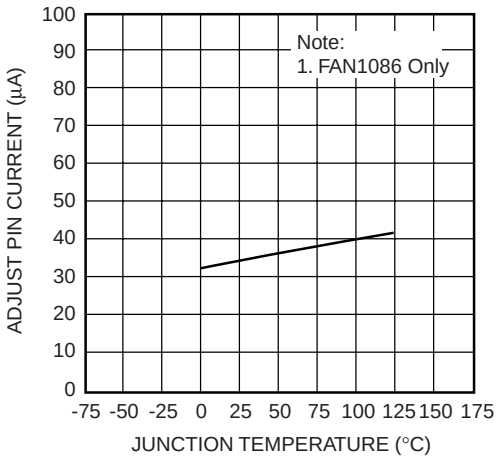


Figure 6. Adjust Pin Current vs. Temperature

Typical Performance Characteristics (continued)

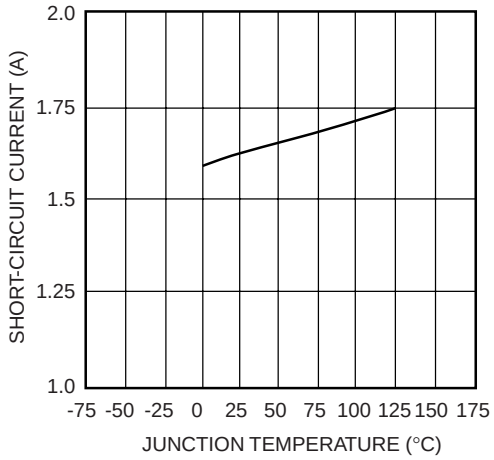


Figure 7. Short-Circuit Current vs. Temperature

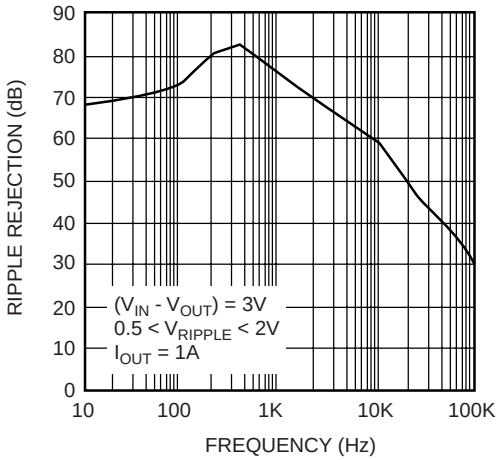


Figure 8. Ripple Rejection vs. Frequency

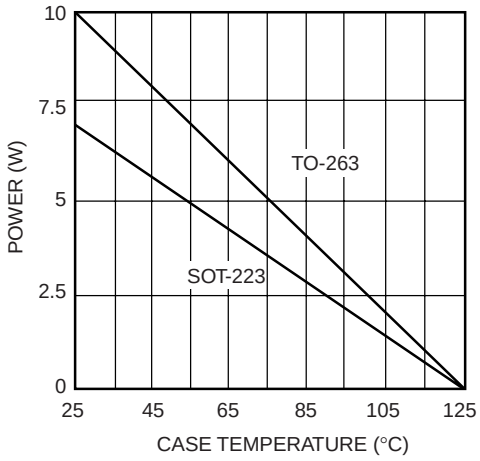


Figure 9. Maximum Power Dissipation

Target Specification

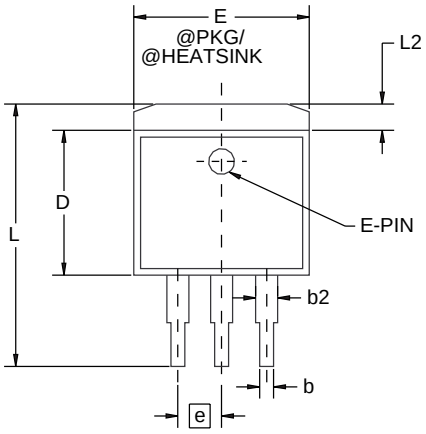
Mechanical Dimensions

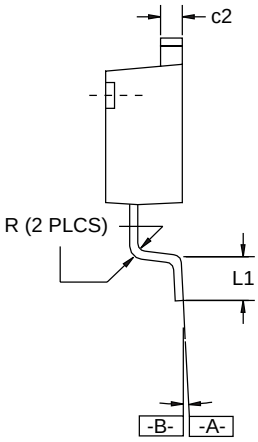
3-Lead TO-263 Package

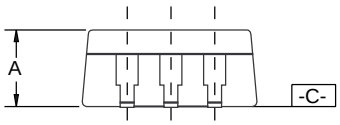
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	10.88	
L1	.090	.100	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.48	
α	0°	8°	0°	8°	

Notes:

1. Dimensions are exclusive of mold flash and metal burrs.
2. Stand off-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimension exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.





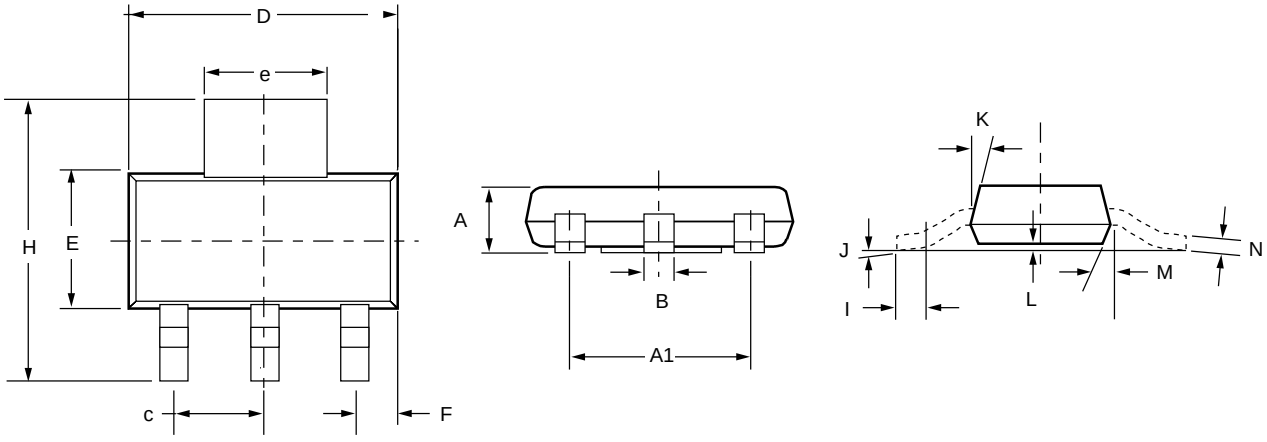


Target Specification

Mechanical Dimensions

4-Lead SOT-223 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.071	—	1.80	
A1	—	.181	—	4.80	
B	.025	.033	.640	.840	
c	—	.090	—	2.29	
D	.248	.264	6.30	6.71	
E	.130	.148	3.30	3.71	
e	.115	.124	2.95	3.15	
F	.033	.041	.840	1.04	
H	.264	.287	6.71	7.29	
I	.012	—	.310	—	
J	—	10°	—	10°	
K	10°	16°	10°	16°	
L	.0008	.0040	.0203	.1018	
M	10°	16°	10°	16°	
N	.010	.014	.250	.360	



Target Specification

Ordering Information

Product Number	Package
FAN1086M	TO-263
FAN1086S	SOT-223
FAN1086M-2.5	TO-263
FAN1086S-2.5	SOT-223
FAN1086M-2.85	TO-263
FAN1086S-2.85	SOT-223
FAN1086M-3.3	TO-263
FAN1086S-3.3	SOT-223
FAN1086M-5	TO-263
FAN1086S-5	SOT-223

Target Specification

11/23/99 0.0m 004
Stock#DS30001117

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAN1581

5A Adjustable/Fixed Ultra Low Dropout Linear Regulator

Features

- Ultra Low dropout voltage, 0.4V typical at 5A
- Remote sense operation
- Fast transient response
- Load regulation: 0.05% typical
- 0.5% initial accuracy
- On-chip thermal limiting
- 5 Pin standard TO-220 and TO-263 packages

Applications

- Pentium® Processors
- PowerPC™, AMD K5 and K6 processors
- Pentium support of GTL+ bus supply
- Low voltage logic supply
- Embedded Processor supplies
- Split plane regulator
- New 2.5V and 1.8V Logic Families

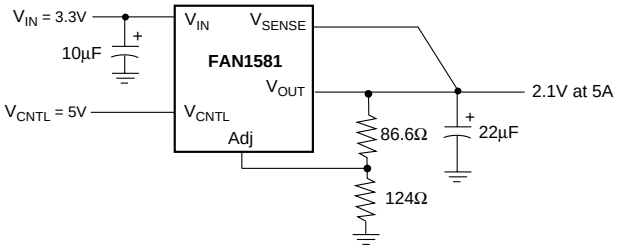
Description

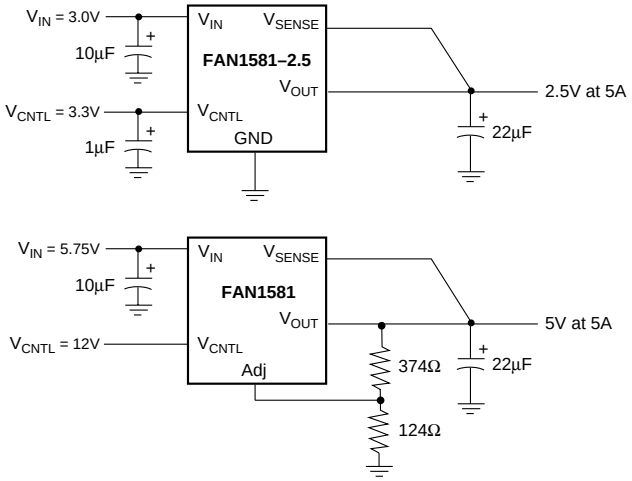
The FAN1581, FAN1581-1.5, and FAN1581-2.5 are ultra-low dropout regulators with 5A output current capability. These devices have been optimized for low voltage applications including V_{TT} bus termination, where transient response and minimum input voltage are critical. The FAN1581 is ideal for low voltage microprocessor applications requiring a regulated output from 1.3V to 5.7V with a power input supply of 1.75V to 6.5V. The FAN1581-1.5 offers fixed 1.5V with 5A current capabilities for GTL+ bus V_{TT} termination. The FAN1581-2.5 offers fixed 2.5V with 5A current capability for logic IC operation and processors while minimizing the overall power dissipation.

Current limit ensures controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

The FAN1581 series regulators are available in the industry-standard 5-Pin TO-220 and TO-263 power packages.

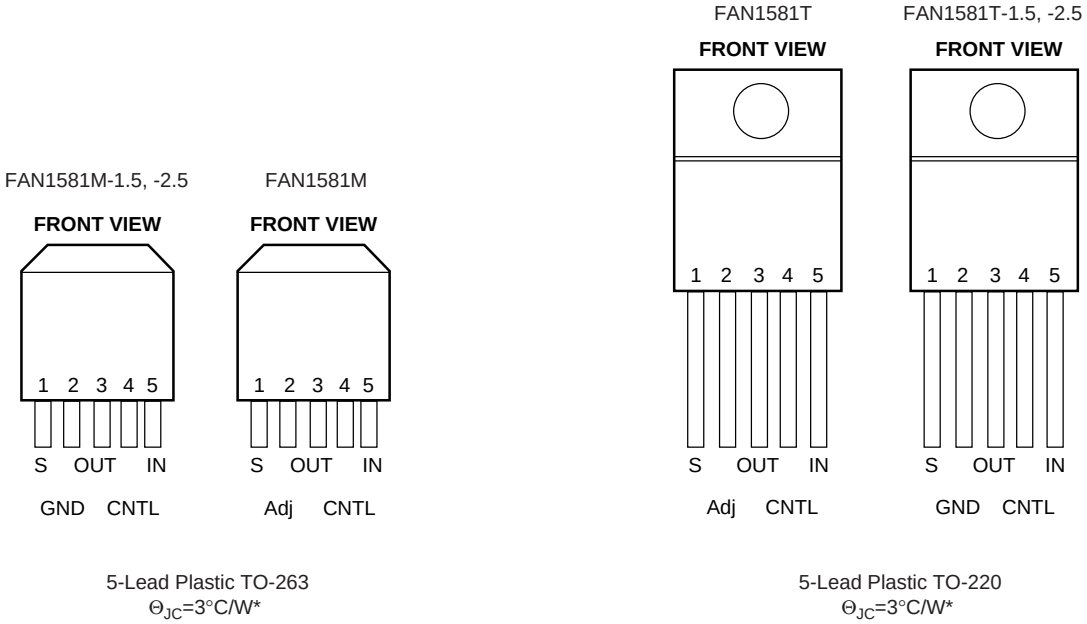
Typical Applications





Preliminary Specification

Pin Assignments



5-Lead Plastic TO-263
Θ_{JC}=3°C/W*

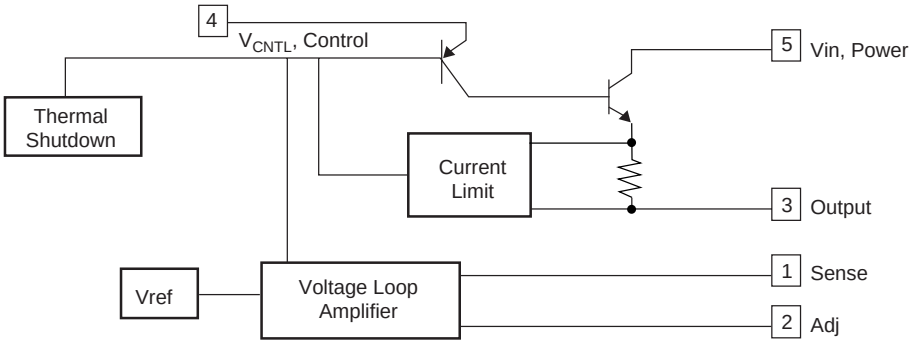
5-Lead Plastic TO-220
Θ_{JC}=3°C/W*

*With package soldered to 0.5 square inch copper area over backside ground plane or internal power plane. Θ_{JA} can vary fom 20°C/W to >40°C/W with other mounting techniques.

Pin Definitions

Pin Number	Pin Name	Pin Function Descrition
1	VSense	**Remote Voltage Sense**. Connect this pin to the load to permit true remote sensing and avoid trace drops.
2	ADJ/GND	**Adjust or Ground.** On the FAN1581, this pin forms the feedback to determine the output voltage. On the FAN1581-1.5 and -2.5, connect this pin to ground.
3	VOUT	**Output Voltage.** This pin and the tab are output.
4	VCNTL	**Control Voltage.** This pin draws small-signal power to control the FAN1581 circuitry. Connect to a voltage higher than VIN, as shown in the applications circuits.
5	VIN	**Input Voltage.**

Internal Block Diagram



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7	V
V_{CNTL}		13.2	V
Operating Junction Temperature Range	0	125	°C
Lead Temperature (Soldering, 10 sec.)		300	°C
Storage Temperature Range	-65	150	°C

Electrical Characteristics

T_J=25°C, V_{OUT} = V_S, V_{ADJ} = 0V unless otherwise specified.
The • denotes specifications which apply over the specified operating temperature range.

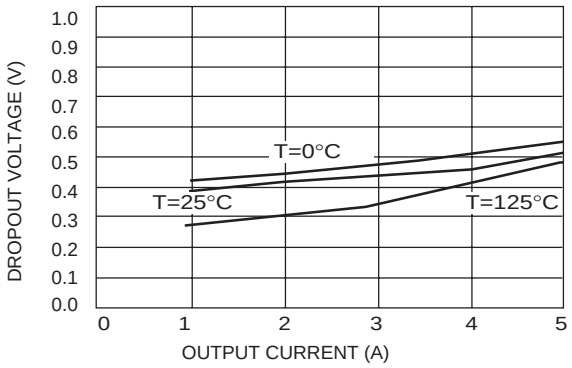
Parameter	Conditions		Min.	Typ.	Max.	Units
Reference Voltage[3]	V_{IN} = 2.0V, V_{CNTL} = 2.75V, I_{OUT} = 10mA		1.243	1.250	1.257	V
Reference Voltage[3]	2.05V ≤ V_{IN} ≤ 5.5V, 2.7V ≤ V_{CNTL} ≤ 12V, 10mA ≤ I_{OUT} ≤ 5A	•	1.237	1.250	1.263	V
Adjustable Output Voltage	3V ≤ V_{IN} ≤ 7V (function of Vout), 10mA ≤ I_{OUT} ≤ 5A	•	Vref	1.5	5.7	V
Output Voltage[4]	3V ≤ V_{IN} ≤ 7V, 10mA ≤ I_{OUT} ≤ 5A	•	1.47	1.5	1.53	V
Output Voltage[5]	5.1V ≤ V_{IN} ≤ 7V, 10mA ≤ I_{OUT} ≤ 5A	•	2.474	2.5	2.526	V
Line Regulation[1,2]	1.75V ≤ V_{IN} ≤ 5.5V, 2.5V ≤ V_{CNTL} ≤ 12V, I_{OUT} = 10mA	•		1	3	mV
Load Regulation[1,2]	V_{IN} = 2.1V, V_{CNTL} = 2.75V, 10mA ≤ I_{OUT} ≤ 5A	•		1	5	mV
Dropout Voltage Minimum V_{CNTL}	V_{IN} = 2.05V, ΔV_{REF} = 1%, I_{OUT} = 5A	•		1.05	1.18	V
Dropout Voltage Minimum V_{IN}	V_{CNTL} = 2.75V, ΔV_{REF} = 1%, I_{OUT} = 5A			0.4	0.5	V
Dropout Voltage Minimum V_{IN}	V_{CNTL} = 2.75V, ΔV_{REF} = 1%, I_{OUT} = 5A	•		0.5	0.6	V
Current Limit	V_{IN} = 2.05V, V_{CNTL} = 2.75V	•	5.2			A
Control Pin Current	V_{IN} = 2.05V, V_{CNTL} = 2.75V, I_{OUT} = 10mA	•		30	120	µA
Adjust Pin Current[3]	V_{IN} = 2.05V, V_{CNTL} = 2.75V	•		50	120	mA
Minimum Load Current	V_{IN} = 3.3V, V_{CNTL} = 5V	•		5.0	10	mA
Ripple Rejection	V_{IN} = 3.75V, V_{CNTL} = 3.75V, f = 120Hz, C_{OUT} = 22µF Tantalum, I_{OUT} = 2.5A		60	80		dB
Thermal Resistance, Junction to Case				3		°C/W
Thermal Regulation	T_A = 25°C, 30ms pulse			0.002	0.02	%/W
Thermal Shutdown				150		°C

Notes:

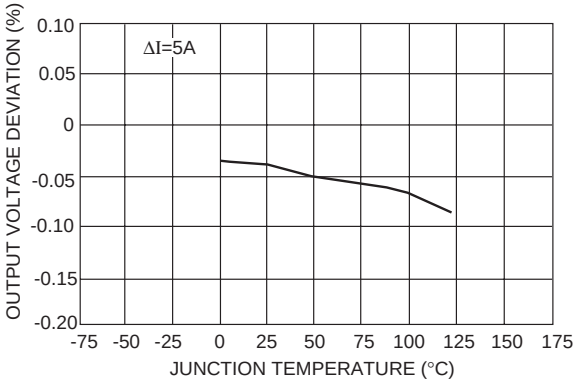
1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output current. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. FAN1581 only.
4. FAN1581-1.5 only.
5. FAN1581-2.5 only.

Preliminary Specification

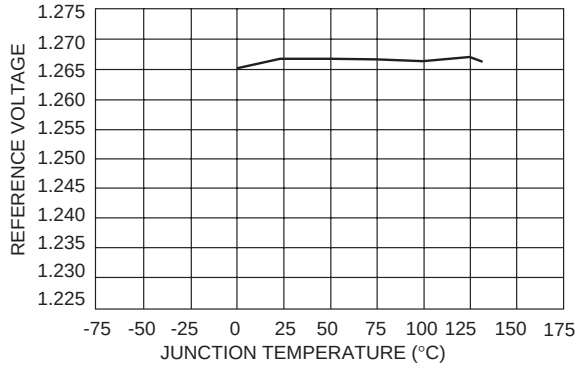
Typical Perfomance Characteristics



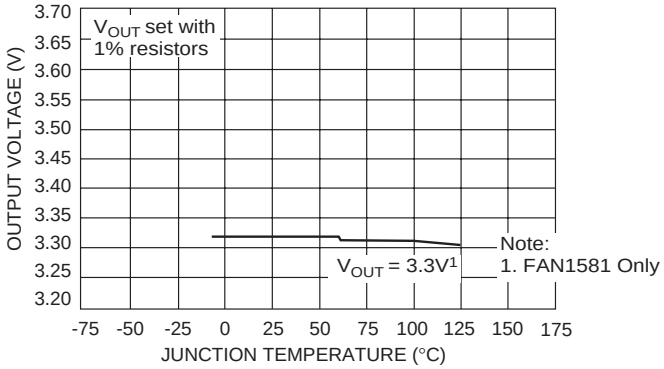
Dropout Voltage vs. Output Current



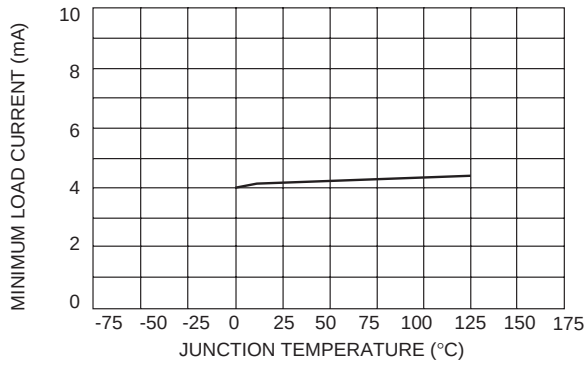
Load Regulation vs. Temperature



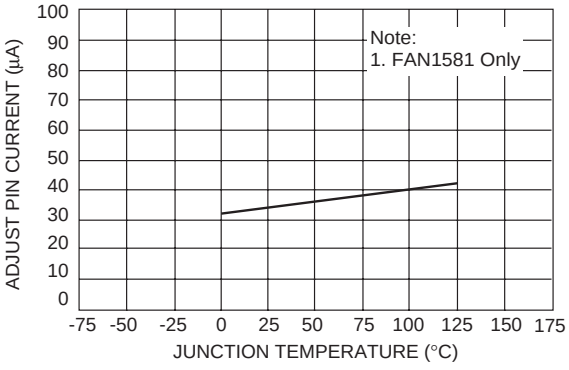
Reference Voltage vs. Temperature



Output Voltage vs. Temperature

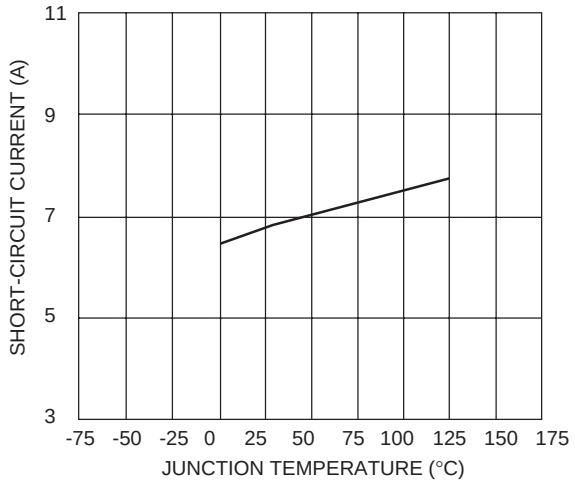


Mimimum Load Current vs. Temperature

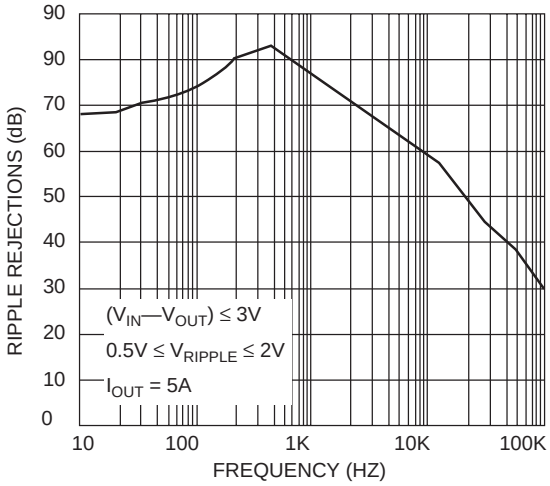


Adjust Pin Current vs. Temperature

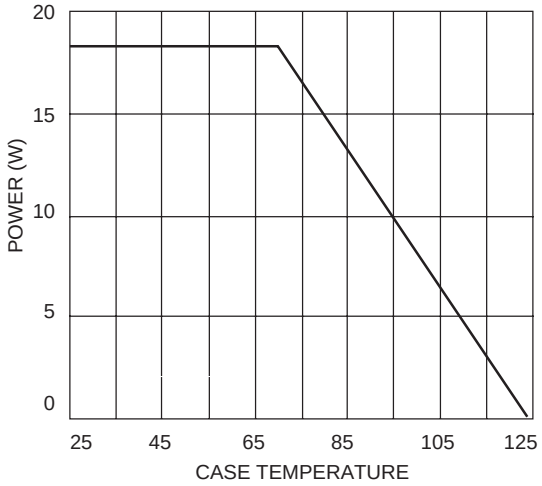
Typical Perfomance Characteristics (continued)



Short-Circuit Current vs.Temeperature



Ripple Rejection vs. Frequency



Maximum Power Dissipation

General

The FAN1581, FAN1581-1.5, and FAN1581-2.5 are three-terminal regulators optimized for GTL+ V_{TT} termination and logic applications. These devices are short-circuit protected, and offer thermal shutdown to turn off the regulator when the junction temperature exceeds about 150°C. The FAN1581 series provides low dropout voltage and fast transient response. Frequency compensation uses capacitors with low ESR while still maintaining stability. This is critical in addressing the needs of low voltage high speed microprocessor buses like GTL+.

Stability

The FAN1581 series requires an output capacitor as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100µF aluminum electrolytic on the output to ensure stability. The frequency compensation of these devices optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <1Ω. It is also recommended to use bypass capacitors such as a 22µF tantalum or a 100µF aluminum on the adjust pin of the FAN1581 for low ripple and fast transient response. When these bypassing capacitors are not used at the adjust pin, smaller values of output capacitors provide equally good results.

Protection Diodes

In normal operation, the FAN1581 series does not require any protection diodes. For the FAN1581, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under short-circuit conditions.

Preliminary Specification

A protection diode between the input and output pins is usually not needed. An internal diode between the input and the output pins on the FAN1581 series can handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input can generate those levels of current; a diode from output to input is then recommended, as shown in Figure 1. Usually, normal power supply cycling or system "hot plugging and unplugging" will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the output, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

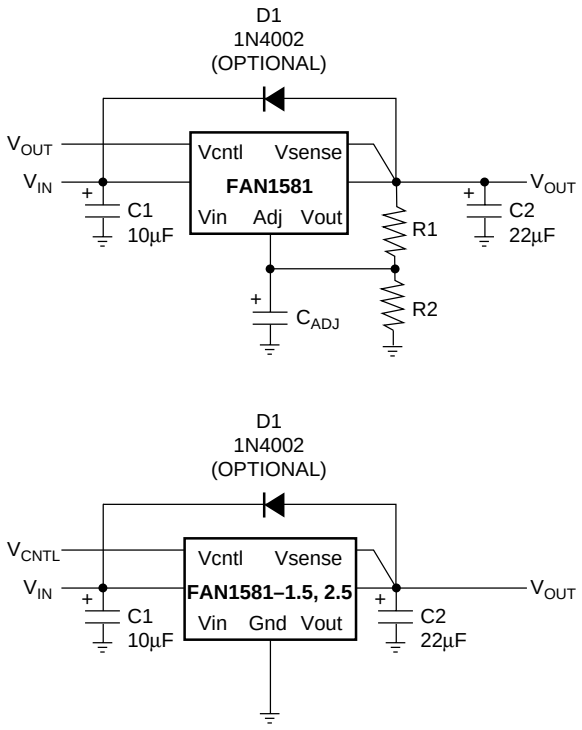


Figure 1. Optional Protection Diode

Ripple Rejection

In applications that require improved ripple rejection, a bypass capacitor from the adjust pin of the FAN1581 to ground reduces the output ripple by the ratio of VOUT/1.25V. The impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1 (typically in the range of 100Ω to 120Ω) in the feedback divider network in Figure 1. Therefore, the value of the required adjust pin capacitor is a function of the input ripple frequency. For example, if R1 equals 100Ω and the ripple frequency equals 120Hz, the adjust pin capacitor should be 22µF. At 10kHz, only 0.22µF is needed.

Output Voltage

The FAN1581 regulator develops a 1.25V reference voltage between the output pin and the adjust pin (see Figure 2). Placing a resistor R1 between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. Normally, this current is the specified minimum load current of 10mA.

The current out of the adjust pin adds to the current from R1 and is typically 35µA. Its output voltage contribution is small and only needs consideration when a very precise output voltage setting is required.

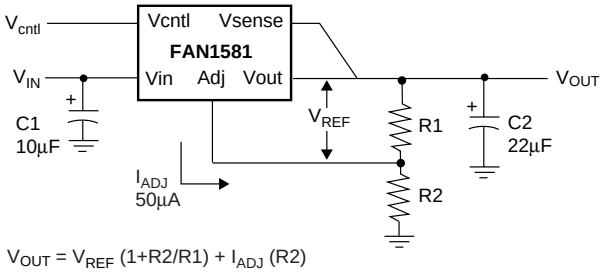


Figure 2. Basic Regulator Circuit

Load Regulation

The FAN1581 family provides true remote sensing, eliminating output voltage errors due to trace resistance. To utilize remote sensing, connect the VSENSE pin directly to the load, rather than at the VOUT pin. If the load is more than 1" away from the FAN1581, it may be necessary to increase the load capacitance to ensure stability.

Thermal Considerations

The FAN1581 series protect themselves under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heat sink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The electrical characteristics section provides a separate thermal resistance and maximum junction temperature for both the control circuitry and the power transistor. Calculate the maximum junction temperature for both sections to ensure that both thermal limits are met.

For example, look at using an FAN1581T-1.5 to generate 5A @ 1.5V ± 2% from a 3.3V source (3.2V to 3.6V).

Assumptions:

- V_{in} = 3.6V worst case
- V_{OUT} = 1.47V worst case
- I_{OUT} = 5A continuous
- T_A = 40°C
- Θ Case-to-Ambient = 5°C/W (assuming both a heatsink and a thermally conductive material)

The power dissipation in this application is:

$P_D = (V_{IN} - V_{OUT}) * (I_{OUT}) = (3.6\text{-}1.47) * (5) = 10.65W$

From the specification table,

$T_J = T_A + (P_D) * (\Theta \text{ Case-to-Ambient} + \Theta_{JC})$
$= 40 + (10.65) * (5 + 3) = 125°C$

The junction temperature is within the maximum rating.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Use of a thermally conductive material at the case-to-heat sink interface is recommended. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance.

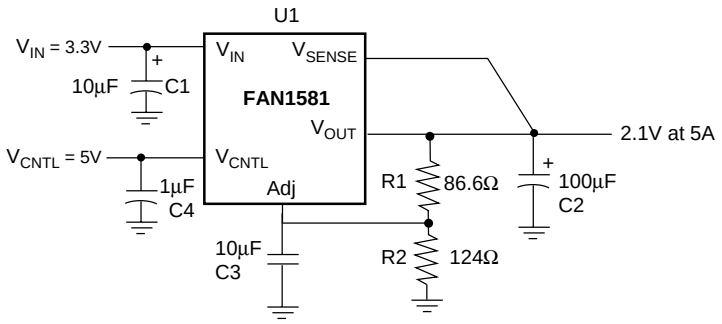


Figure 3. Application Circuit (FAN1581)

Table 1. Bill of Materials for Application Circuit for the FAN1581

Item	Quantity	Manufacturer	Part Number	Description
C1, C3	2	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Xicon	L10V100	100µF, 10V Aluminum
C4	1	Any		1µF Ceramic
R1	1	Generic		86.6Ω, 1%
R2	1	Generic		124Ω, 1%
U1	1	Fairchild	FAN1581T	5A Regulator

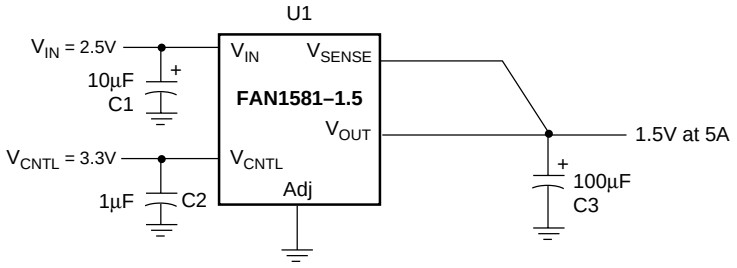


Figure 4. Application Circuit (FAN1581-1.5)

Table 2. Bill of Materials for Application Circuit for the RC1581-1.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Any		1µF Ceramic
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	FAN1581T-1.5	5A Regulator

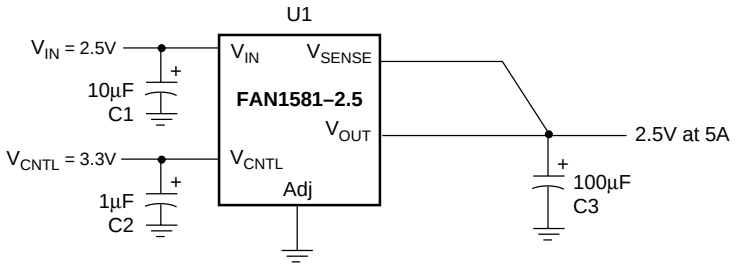


Figure 5. Application Circuit (FAN1581-2.5)

Table 3. Bill of Materials for Application Circuit for the RC1581-2.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Any		1µF Ceramic
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	FAN1581T-2.5	5A Regulator

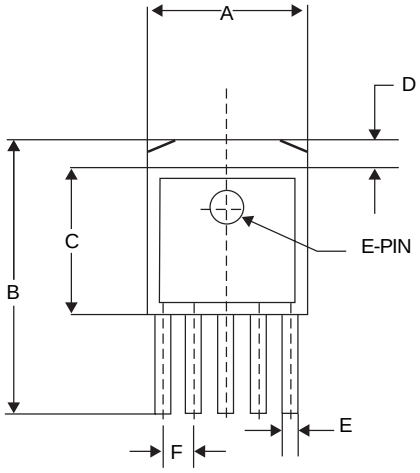
Preliminary Specification

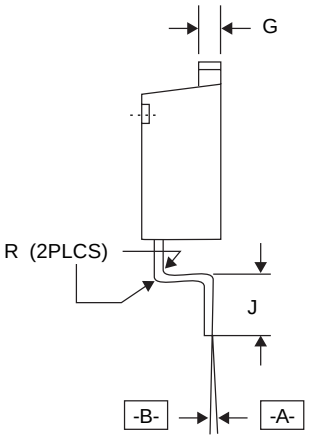
Mechanical Dimensions

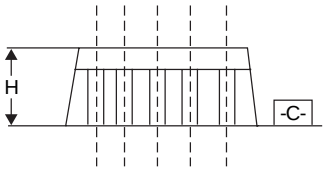
5-Lead TO-263 Package

Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.380	.405	9.65	10.29
B	.575	.625	14.60	15.88
C	.325	.380	8.25	9.66
D	–	.055	–	1.40
E	.020	.039	.50	.99
F	.060	.072	1.52	1.83
G	0.45	.055	1.14	1.40
H	.160	.190	4.06	4.83
J	.090	0.110	2.28	2.80
K	.018	.029	.457	.736
R	.017	.019	0.43	0.48

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum –B-.
3. Foot length is measured with ref. to Datum –A- with lead surface (at inner R).
4. Dimension exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place –C-.







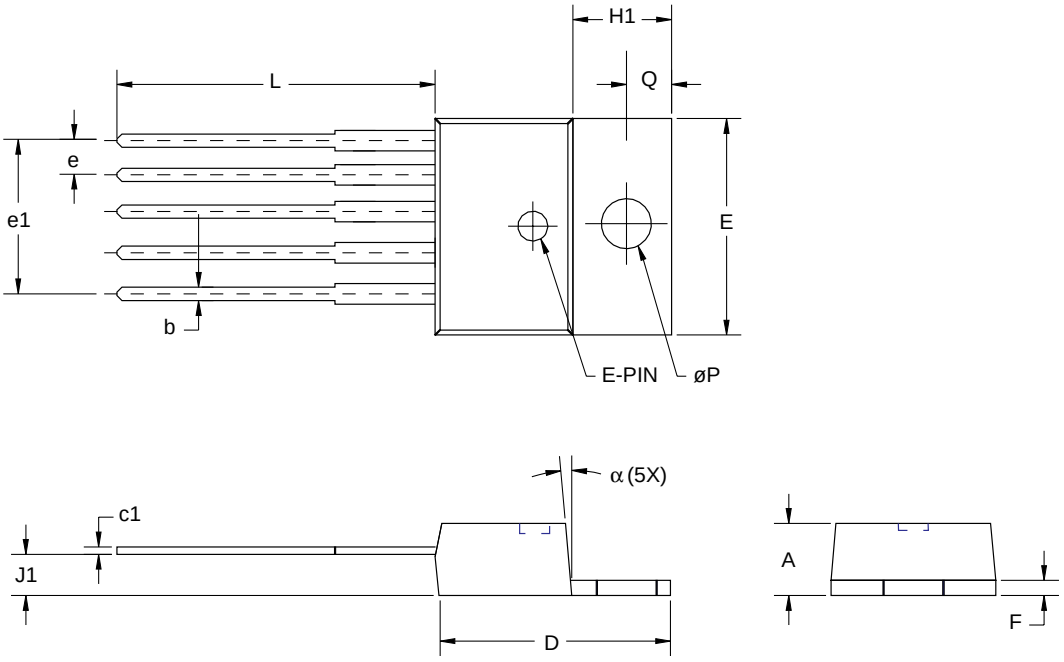
Preliminary Specification

Mechanical Demensions (continued)

5-Lead TO-220 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.140	.190	3.56	4.83	
b	.025	.040	.63	1.02	
c1	.140	.220	.356	.559	
øP	.139	.161	3.53	4.09	
D	.560	.650	14.22	16.51	
E	.380	.420	9.65	10.67	
e	.062	.072	1.57	1.83	
e1	.263	.273	6.68	6.94	
F	.045	.055	1.14	1.40	
H1	.230	.270	5.84	6.87	
J1	.080	.115	2.04	2.92	
L	.500	.580	12.70	14.73	
Q	.100	.135	.254	.343	
α	3°	7°	3°	7°	

Notes:
1. Dimension c1 apply for lead finish.



Ordering Information

Product Number	Package
FAN1581M	TO-263
FAN1581T	TO-220
FAN1581M-1.5	TO-263
FAN1581T-1.5	TO-220
FAN1581M-2.5	TO-263
FAN1581T-2.5	TO-220

Preliminary Specification

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MICROWIRE™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAN1582

3A Adjustable/Fixed Ultra Low Dropout Linear Regulator

Features

- Ultra Low dropout voltage, 0.4V typical at 3A
- Remote sense operation
- Fast transient response
- Load regulation: 0.05% typical
- 0.5% initial accuracy
- On-chip thermal limiting
- 5 Pin standard TO-220 and TO-263 packages

Applications

- Pentium® Processors
- PowerPC™, AMD K5 and K6 processors
- Pentium support of GTL+ bus supply
- Low voltage logic supply
- Embedded Processor supplies
- Split plane regulator
- New 2.5V and 1.8V Logic Families

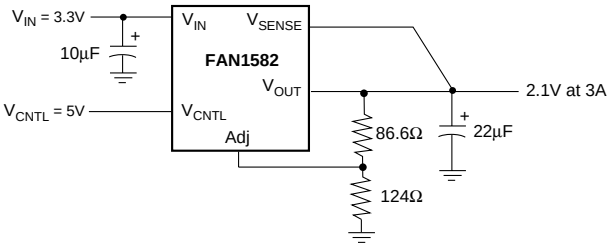
Description

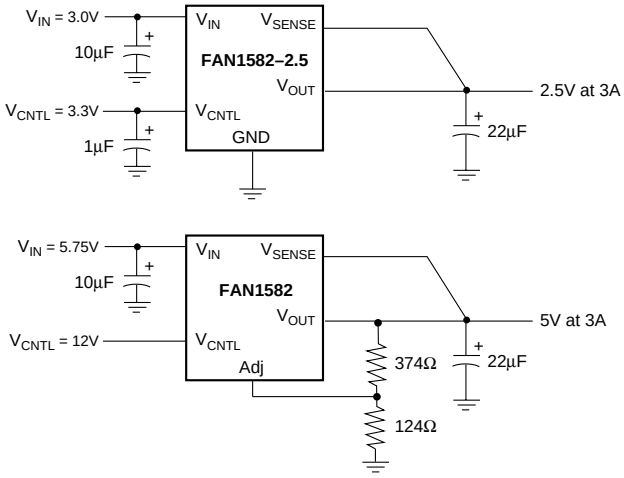
The FAN1582, FAN1582-1.5, and FAN1582-2.5 are ultra-low dropout regulators with 3A output current capability. These devices have been optimized for low voltage applications including V_{TT} bus termination, where transient response and minimum input voltage are critical. The FAN1582 is ideal for low voltage microprocessor applications requiring a regulated output from 1.3V to 5.7V with a power input supply of 1.75V to 6.5V. The FAN1582-1.5 offers fixed 1.5V with 3A current capabilities for GTL+ bus V_{TT} termination. The FAN1582-2.5 offers fixed 2.5V with 3A current capability for logic IC operation and processors while minimizing the overall power dissipation.

Current limit ensures controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

The FAN1582 series regulators are available in the industry-standard 5-Pin TO-220 and TO-263 power packages.

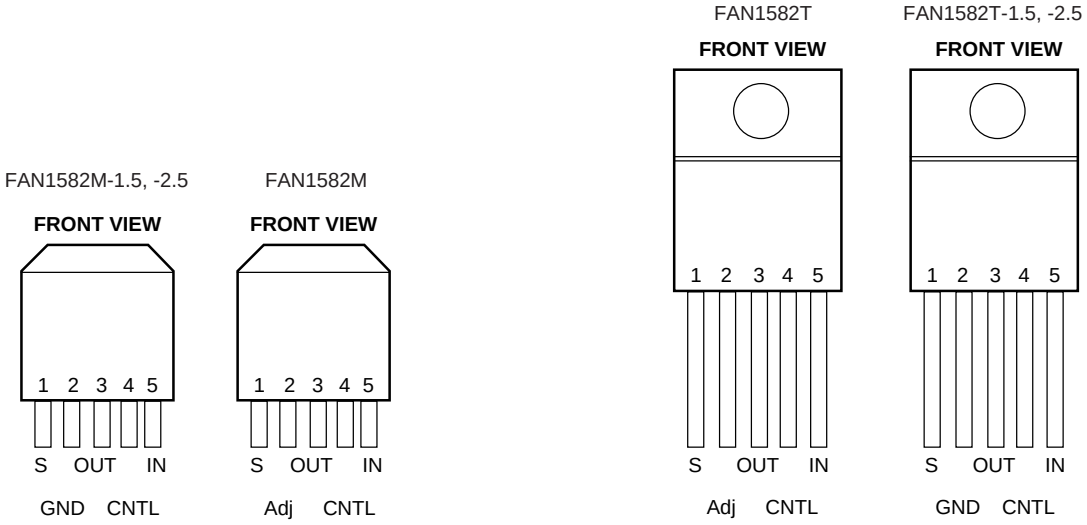
Typical Applications





Preliminary Specification

Pin Assignments



5-Lead Plastic TP-263
Θ_{JC}=3°C/W*

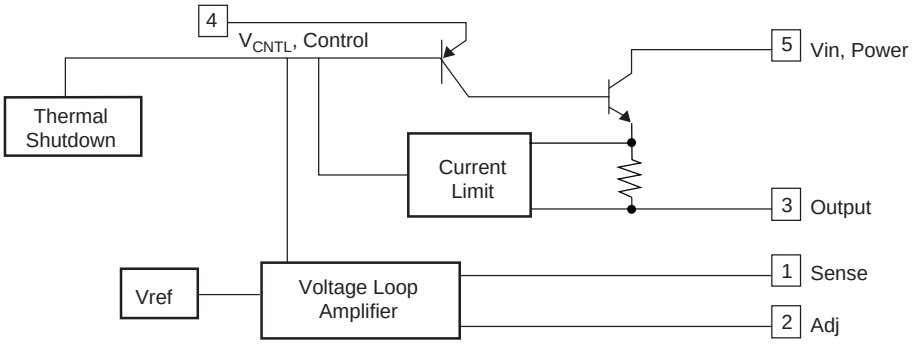
5-Lead Plastic TP-220
Θ_{JC}=3°C/W*

*With package soldered to 0.5 square inch copper area over backside ground plane or internal power plane. Θ_{JA} can vary fom 20°C/W to >40°C/W with other mounting techniques.

Pin Definitions

Pin Number	Pin Name	Pin Function Descrition
1	VSense	**Remote Voltage Sense**. Connect this pin to the load to permit true remote sensing and avoid trace drops.
2	ADJ/GND	**Adjust or Ground.** On the FAN1582, this pin forms the feedback to determine the output voltage. On the FAN1582-1.5 and -2.5, connect this pin to ground.
3	VOUT	**Output Voltage.** This pin and the tab are output.
4	VCNTL	**Control Voltage.** This pin draws small-signal power to control the FAN1582 circuitry. Connect to a voltage higher than VIN, as shown in the applications circuits.
5	VIN	**Input Voltage.**

Internal Block Diagram



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7	V
V_{CNTL}		13.2	V
Operating Junction Temperature Range	0	125	°C
Lead Temperature (Soldering, 10 sec.)		300	°C
Storage Temperature Range	-65	150	°C

Electrical Characteristics

T_J=25°C, V_{OUT} = V_S, V_{ADJ} = 0V unless otherwise specified.
The • denotes specifications which apply over the specified operating temperature range.

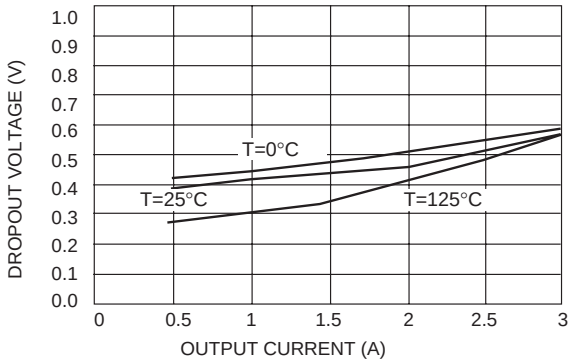
Parameter	Conditions		Min.	Typ.	Max.	Units
Reference Voltage[3]	V_{IN} = 2.0V, V_{CNTL} = 2.75V, I_{OUT} = 10mA		1.243	1.250	1.257	V
Reference Voltage[3]	2.05V ≤ V_{IN} ≤ 5.5V, 2.7V ≤ V_{CNTL} ≤ 12V, 10mA ≤ I_{OUT} ≤ 3A	•	1.237	1.250	1.263	V
Adjustable Output Voltage	3V ≤ V_{IN} ≤ 7V (function of Vout), 10mA ≤ I_{OUT} ≤ 3A	•	Vref	1.5	5.7	V
Output Voltage[4]	3V ≤ V_{IN} ≤ 7V, 10mA ≤ I_{OUT} ≤ 3A	•	1.47	1.5	1.53	V
Output Voltage[5]	5.1V ≤ V_{IN} ≤ 7V, 10mA ≤ I_{OUT} ≤ 3A	•	2.474	2.5	2.526	V
Line Regulation[1,2]	1.75V ≤ V_{IN} ≤ 5.5V, 2.5V ≤ V_{CNTL} ≤ 12V, I_{OUT} = 10mA	•		1	3	mV
Load Regulation[1,2]	V_{IN} = 2.1V, V_{CNTL} = 2.75V, 10mA ≤ I_{OUT} ≤ 3A	•		1	5	mV
Dropout Voltage Minimum V_{CNTL}	V_{IN} = 2.05V, ΔV_{REF} = 1%, I_{OUT} = 3A	•		1.05	1.18	V
Dropout Voltage Minimum V_{IN}	V_{CNTL} = 2.75V, ΔV_{REF} = 1%, I_{OUT} = 3A			0.4	0.5	V
Dropout Voltage Minimum V_{IN}	V_{CNTL} = 2.75V, ΔV_{REF} = 1%, I_{OUT} = 3A	•		0.5	0.6	V
Current Limit	V_{IN} = 2.05V, V_{CNTL} = 2.75V	•	3.1			A
Control Pin Current	V_{IN} = 2.05V, V_{CNTL} = 2.75V, I_{OUT} = 10mA	•		30	120	µA
Adjust Pin Current[3]	V_{IN} = 2.05V, V_{CNTL} = 2.75V	•		50	120	mA
Minimum Load Current	V_{IN} = 3.3V, V_{CNTL} = 5V	•		5.0	10	mA
Ripple Rejection	V_{IN} = 3.75V, V_{CNTL} = 3.75V, f = 120Hz, C_{OUT} = 22µF Tantalum, I_{OUT} = 1.5A		60	80		dB
Thermal Resistance, Junction to Case				3		°C/W
Thermal Regulation	T_A = 25°C, 30ms pulse			0.002	0.02	%/W
Thermal Shutdown				150		°C

Notes:

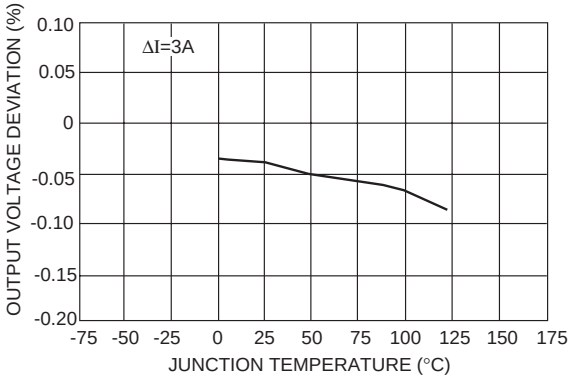
1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output current. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. FAN1582 only.
4. FAN1582-1.5 only.
5. FAN1582-2.5 only.

Preliminary Specification

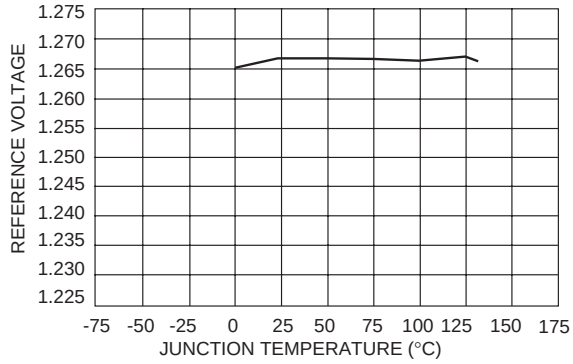
Typical Perfomance Characteristics



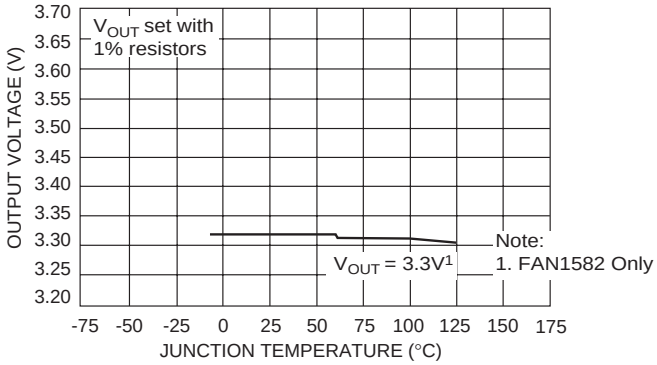
Dropout Voltage vs. Output Current



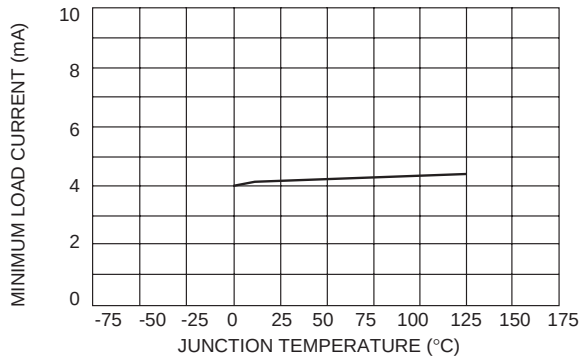
Load Regulation vs. Temperature



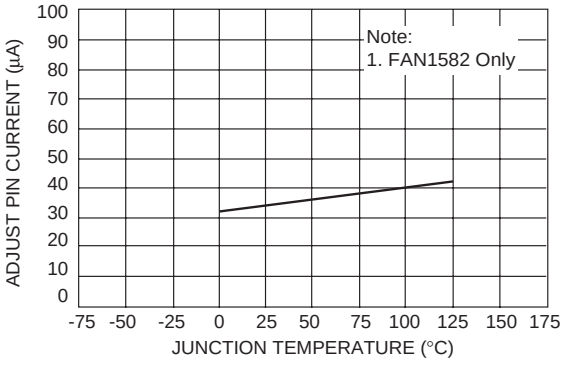
Reference Voltage vs. Temperature



Output Voltage vs. Temperature

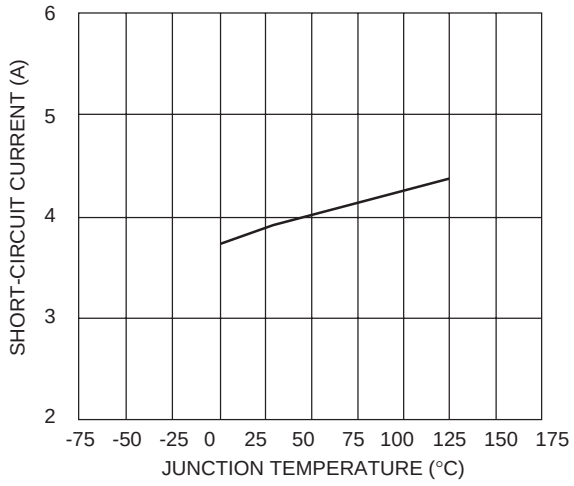


Mimimum Load Current vs. Temperature

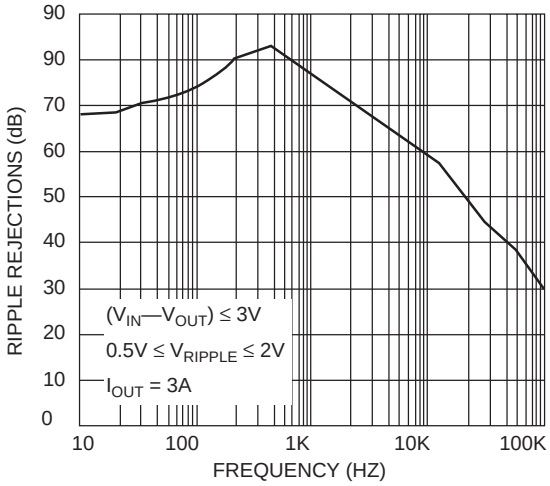


Adjust Pin Current vs. Temperature

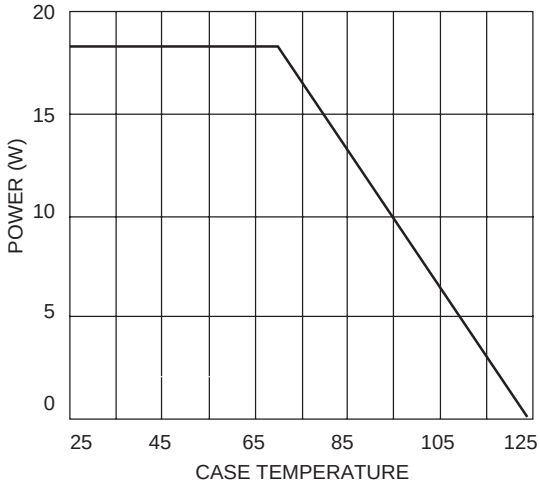
Typical Perfomance Characteristics (continued)



Short-Circuit Current vs.Temeperature



Ripple Rejection vs. Frequency



Maximum Power Dissipation

General

The FAN1582, FAN1582-1.5, and FAN1582-2.5 are three-terminal regulators optimized for GTL+ V_{TT} termination and logic applications. These devices are short-circuit protected, and offer thermal shutdown to turn off the regulator when the junction temperature exceeds about 150°C. The FAN1582 series provides low dropout voltage and fast transient response. Frequency compensation uses capacitors with low ESR while still maintaining stability. This is critical in addressing the needs of low voltage high speed microprocessor buses like GTL+.

Stability

The FAN1582 series requires an output capacitor as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100µF aluminum electrolytic on the output to ensure stability. The frequency compensation of these devices optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <1Ω. It is also recommended to use bypass capacitors such as a 22µF tantalum or a 100µF aluminum on the adjust pin of the FAN1582 for low ripple and fast transient response. When these bypassing capacitors are not used at the adjust pin, smaller values of output capacitors provide equally good results.

Protection Diodes

In normal operation, the FAN1582 series does not require any protection diodes. For the FAN1582, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under short-circuit conditions.

Preliminary Specification

A protection diode between the input and output pins is usually not needed. An internal diode between the input and the output pins on the FAN1582 series can handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input can generate those levels of current; a diode from output to input is then recommended, as shown in Figure 1. Usually, normal power supply cycling or system "hot plugging and unplugging" will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the output, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

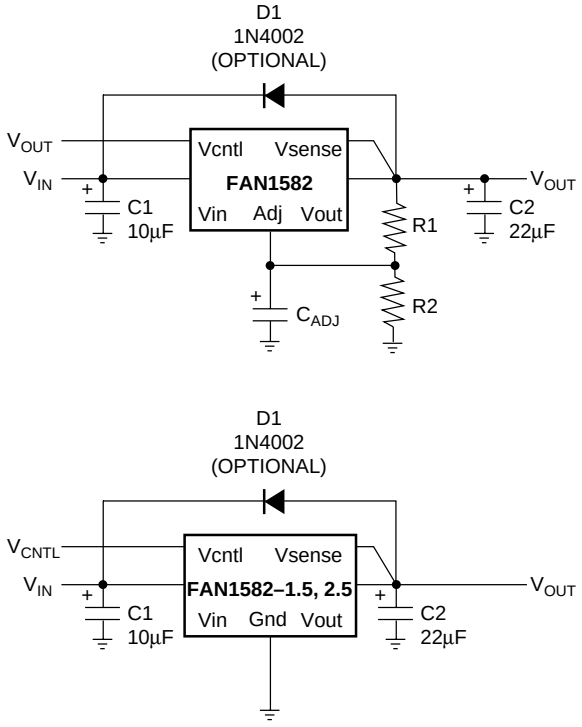


Figure 1. Optional Protection Diode

Ripple Rejection

In applications that require improved ripple rejection, a bypass capacitor from the adjust pin of the FAN1582 to ground reduces the output ripple by the ratio of VOUT/1.25V. The impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1 (typically in the range of 100Ω to 120Ω) in the feedback divider network in Figure 1. Therefore, the value of the required adjust pin capacitor is a function of the input ripple frequency. For example, if R1 equals 100Ω and the ripple frequency equals 120Hz, the adjust pin capacitor should be 22µF. At 10kHz, only 0.22µF is needed.

Output Voltage

The FAN1582 regulator develops a 1.25V reference voltage between the output pin and the adjust pin (see Figure 2). Placing a resistor R1 between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. Normally, this current is the specified minimum load current of 10mA.

The current out of the adjust pin adds to the current from R1 and is typically 35µA. Its output voltage contribution is small and only needs consideration when a very precise output voltage setting is required.

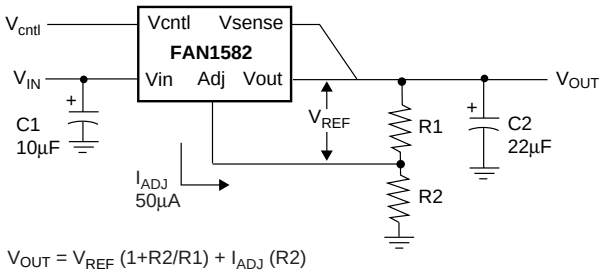


Figure 2. Basic Regulator Circuit

Load Regulation

The FAN1582 family provides true remote sensing, eliminating output voltage errors due to trace resistance. To utilize remote sensing, connect the VSENSE pin directly to the load, rather than at the VOUT pin. If the load is more than 1" away from the FAN1582, it may be necessary to increase the load capacitance to ensure stability.

Thermal Considerations

The FAN1582 series protect themselves under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heat sink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The electrical characteristics section provides a separate thermal resistance and maximum junction temperature for both the control circuitry and the power transistor. Calculate the maximum junction temperature for both sections to ensure that both thermal limits are met.

For example, look at using an FAN1582T-1.5 to generate 3A @ 1.5V ± 2% from a 3.3V source (3.2V to 3.6V).

Assumptions:

- V_{in} = 3.6V worst case
- V_{OUT} = 1.47V worst case
- I_{OUT} = 3A continuous
- T_A = 70°C
- Θ Case-to-Ambient = 5°C/W (assuming both a heatsink and a thermally conductive material)

The power dissipation in this application is:

$P_D = (V_{IN} - V_{OUT}) * (I_{OUT}) = (3.6\text{-}1.47) * (3) = 6.39W$

From the specification table,

$T_J = T_A + (P_D) * (\Theta \text{ Case-to-Ambient} + \Theta_{JC})$
$= 70 + (6.39) * (5 + 3) = 121°C$

The junction temperature is below the maximum rating.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Use of a thermally conductive material at the case-to-heat sink interface is recommended. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance.

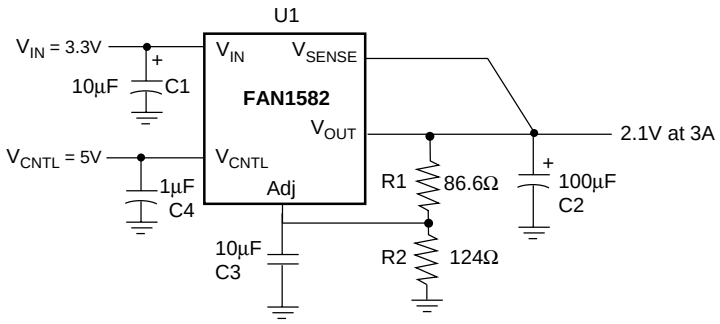


Figure 3. Application Circuit (FAN1582)

Table 1. Bill of Materials for Application Circuit for the FAN1582

Item	Quantity	Manufacturer	Part Number	Description
C1, C3	2	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Xicon	L10V100	100µF, 10V Aluminum
C4	1	Any		1µF Ceramic
R1	1	Generic		86.6Ω, 1%
R2	1	Generic		124Ω, 1%
U1	1	Fairchild	FAN1582T	3A Regulator

Preliminary Specification

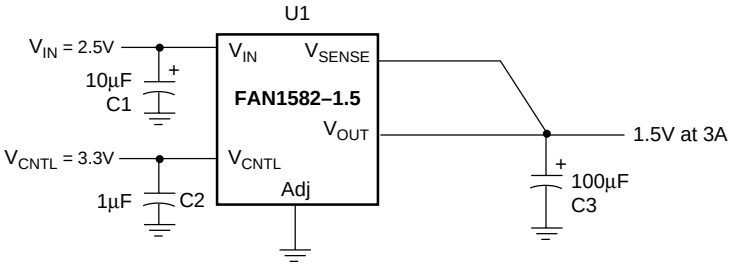


Figure 4. Application Circuit (FAN1582-1.5)

Table 2. Bill of Materials for Application Circuit for the RC1582-1.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Any		1µF Ceramic
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	FAN1582T-1.5	3A Regulator

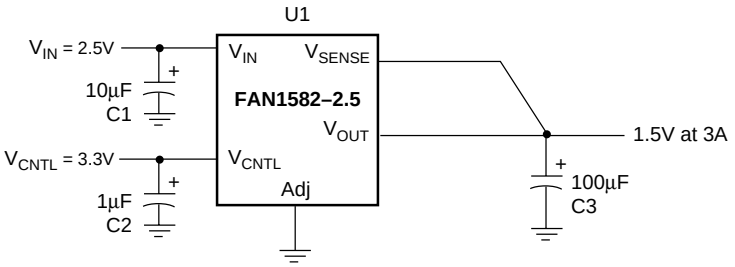


Figure 5. Application Circuit (FAN1582-2.5)

Table 3. Bill of Materials for Application Circuit for the RC1582-2.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2	1	Any		1µF Ceramic
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	FAN1582T-2.5	3A Regulator

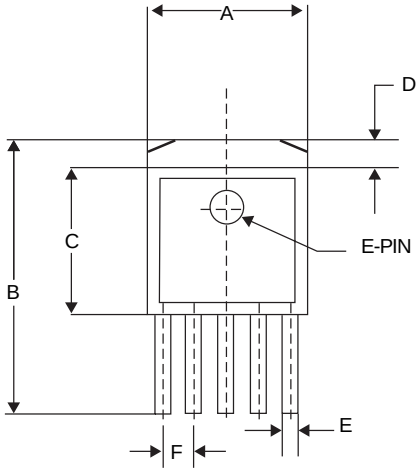
Preliminary Specification

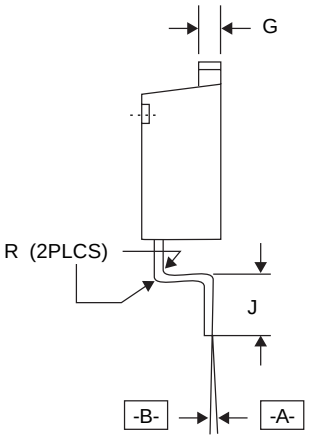
Mechanical Dimensions

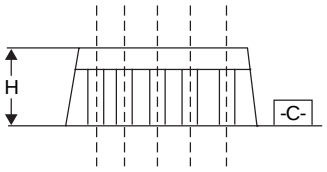
5-Lead TO-263 Package

Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.380	.405	9.65	10.29
B	.575	.625	14.60	15.88
C	.325	.380	8.25	9.66
D	–	.055	–	1.40
E	.020	.039	.50	.99
F	.060	.072	1.52	1.83
G	0.45	.055	1.14	1.40
H	.160	.190	4.06	4.83
J	.090	0.110	2.28	2.80
K	.018	.029	.457	.736
R	.017	.019	0.43	0.48

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum –B-.
3. Foot length is measured with ref. to Datum –A- with lead surface (at inner R).
4. Dimension exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place –C-.







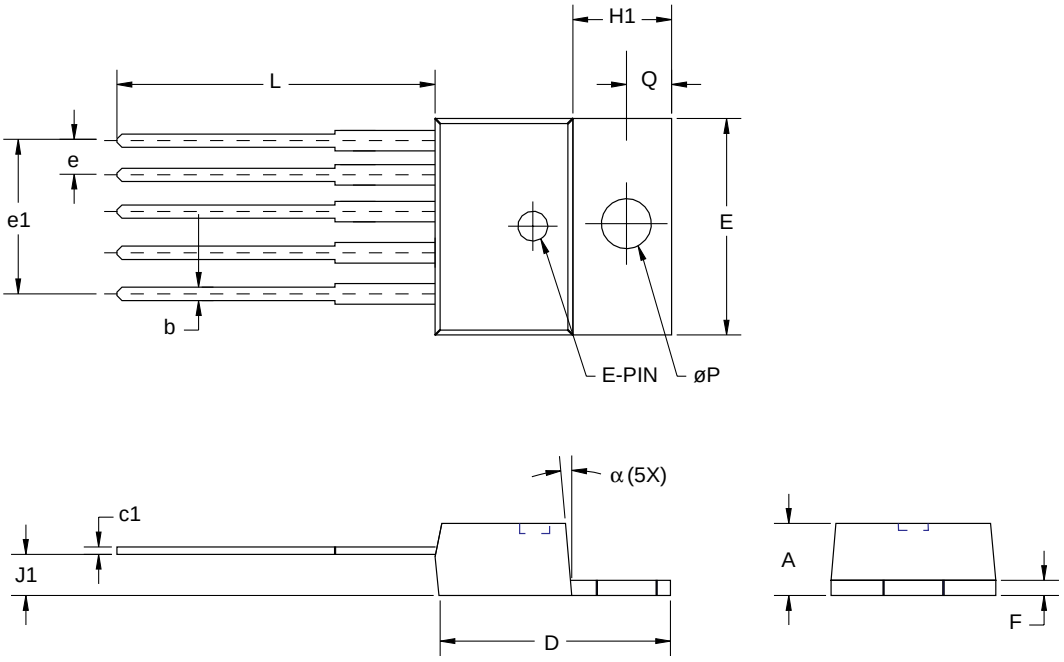
Preliminary Specification

Mechanical Demensions (continued)

5-Lead TO-220 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.140	.190	3.56	4.83	
b	.025	.040	.63	1.02	
c1	.140	.220	.356	.559	
øP	.139	.161	3.53	4.09	
D	.560	.650	14.22	16.51	
E	.380	.420	9.65	10.67	
e	.062	.072	1.57	1.83	
e1	.263	.273	6.68	6.94	
F	.045	.055	1.14	1.40	
H1	.230	.270	5.84	6.87	
J1	.080	.115	2.04	2.92	
L	.500	.580	12.70	14.73	
Q	.100	.135	.254	.343	
α	3°	7°	3°	7°	

Notes:
1. Dimension c1 apply for lead finish.



Ordering Information

Product Number	Package
FAN1582M	TO-263
FAN1582T	TO-220
FAN1582M-1.5	TO-263
FAN1582T-1.5	TO-220
FAN1582M-2.5	TO-263
FAN1582T-2.5	TO-220

Preliminary Specification

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAN4040

Precision Micropower Shunt Voltage Reference

Features

- Fixed 2.500V, 3.300V, 4.096V, 5.000V, 8.192V, 10.000V
- Tolerances to ±0.1% (25°C)
- Low output noise
- Low temperature coefficient
- Small packages
- Extended operating current range

Applications

- Portable equipment
- Disk drives
- Instrumentation
- Audio equipment
- Data acquisition systems

Description

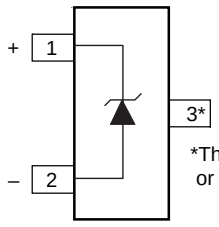
The FAN4040 series of precision shunt references are ideal for space- and cost-sensitive applications. They are available in a variety of fixed output voltages (2.500V, 3.300V, 4.096V, 5.000V, 8.192V, and 10.000V) and with a variety of output voltage tolerances (0.1%, 0.2%, 0.5%, 1%, and 2%). They also have excellent temperature coefficients, to 100ppm/°C for the tighter tolerance grades. The FAN4040 series has an extended operating current range, sinking as much as 25mA.

The FAN4040 series is available in SOT-23, SO-8, and TO-92 packages.

Preliminary Information

Connection Diagrams

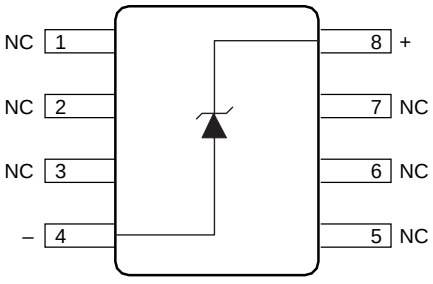
SOT-23



*This pin must be left floating or connected to pin 2.

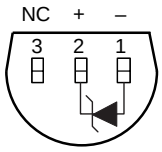
Top View

SO-8



Top View

TO-92



Bottom View

FAN4050

Precision Micropower Shunt Voltage Reference

Features

- Fixed 2.500V, 4.096V, 5.000V, 8.192V, 10.000V
- Tolerances to ±0.1% (25°C)
- Low output noise
- Low temperature coefficient
- Small packages: SSOT-23
- Extended operating current range

Applications

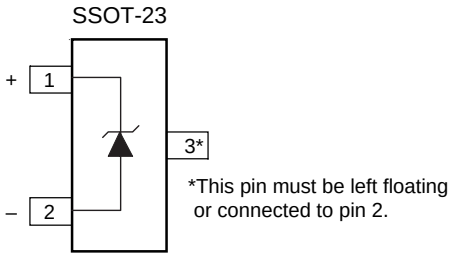
- Portable equipment
- Disk drives
- Instrumentation
- Audio equipment
- Data acquisition systems

Description

The FAN4050 series of precision shunt references are ideal for space- and cost-sensitive applications. They are available in a variety of fixed output voltages (2.500V, 4.096V, 5.000V, 8.192V, and 10.000V) and with a variety of output voltage tolerances (0.1%, 0.2%, and 0.5%). They also have excellent temperature coefficients, 50ppm/°C.

The FAN4050 series is available in the SSOT-23 package.

Connection Diagram



Top View

Advance Specification

Absolute Maximum Ratings[1]

Ratings are over full operating free-air temperature range unless otherwise noted.

Parameter	Min.	Max.	Unit
Continuous cathode current, I_K	-10	20	mA
Power dissipation[2]		280	mW
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

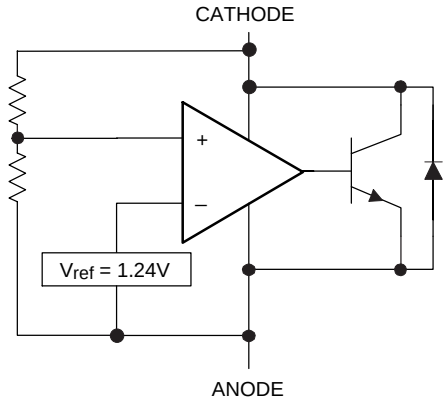
Notes:

1. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
2. It is recommended to connect pin 3 to pin 2 in the SSOT23 package to ensure optimal thermal performance.

Recommended Operating Conditions

Parameter	Min.	Max.	Unit
Continuous cathode current, I_K	0.1	15	mA
Operating temperature range in free air, T_A	-40	85	°C

Equivalent Schematic



Advance Specification

Advance Specification

Guaranteed Electrical Characteristics, FAN4050-2.5

(T_A = 25°C unless otherwise specified, in free air)

The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Limits A	Limits B	Limits C	Units
V_R	Reverse Breakdown Voltage	I_K = 100µA		2.500	2.500	2.500	V*
TCV_R	Reverse Breakdown Voltage Tolerance	I_K = 100µA	 •	±2.5 ±11	±5.0 ±14	±13 ±21	mV mV
I_{RMIN}	Minimum Operating Current		•	65	65	65	µA
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	I_K = 100µA	•	±50	±50	±50	ppm/°C
ΔV_R (ΔI_K)	Reverse Breakdown Voltage Change with Operating Current	$I_{RMIN} \le I_K \le$1mA 1mA ≤ I_K ≤ 15mA	• •	1.2 8.0	1.2 8.0	1.2 8.0	mV mV
Z_{KA}	Reverse Dynamic Impedance	I_K=1mA, f=120Hz, I_{AC}=0.1I_K		0.3	0.3	0.3	Ω*
e_N	Wideband Noise	I_K=100µA, 10Hz ≤ f ≤ 10kHz		41	41	41	μV_{RMS}*
ΔV_R	Reverse Breakdown Voltage Long-term Stability	t=1000hrs, T=25°C, I_K=100µA		120	120	120	ppm*

*Typical.

Guaranteed Electrical Characteristics, FAN4050-4.1

(T_A = 25°C unless otherwise specified, in free air)

The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Limits A	Limits B	Limits C	Units
V_R	Reverse Breakdown Voltage	I_K = 100µA		4.096	4.096	4.096	V*
TCV_R	Reverse Breakdown Voltage Tolerance	I_K = 100µA	 •	±4.1 ±18	±8.2 ±22	±21 ±34	mV mV
I_{RMIN}	Minimum Operating Current		•	73	73	73	µA
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	I_K = 100µA	•	±50	±50	±50	ppm/°C
ΔV_R (ΔI_K)	Reverse Breakdown Voltage Change with Operating Current	$I_{RMIN} \le I_K \le$1mA 1mA ≤ I_K ≤ 15mA	• •	1.2 10	1.2 10	1.2 10	mV mV
Z_{KA}	Reverse Dynamic Impedance	I_K=1mA, f=120Hz, I_{AC}=0.1I_K		0.5	0.5	0.5	Ω*
e_N	Wideband Noise	I_K=100µA, 10Hz ≤ f ≤ 10kHz		93	93	93	μV_{RMS}*
ΔV_R	Reverse Breakdown Voltage Long-term Stability	t=1000hrs, T=25°C, I_K=100µA		120	120	120	ppm*

*Typical.

Guaranteed Electrical Characteristics, FAN4050-5.0

(T_A = 25°C unless otherwise specified, in free air)
The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Limits A	Limits B	Limits C	Units
V_R	Reverse Breakdown Voltage	I_K = 100µA		5.000	5.000	5.000	V*
TCV_R	Reverse Breakdown Voltage Tolerance	I_K = 100µA	 •	±5.0 ±22	±10 ±27	±25 ±42	mV mV
I_{RMIN}	Minimum Operating Current		•	80	80	80	µA
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	I_K = 100µA	•	±50	±50	±50	ppm/°C
ΔV_R (ΔI_K)	Reverse Breakdown Voltage Change with Operating Current	$I_{RMIN} \le I_K \le$1mA 1mA ≤ I_K ≤ 15mA	• •	1.4 12	1.4 12	1.4 12	mV mV
Z_{KA}	Reverse Dynamic Impedance	I_K=1mA, f=120Hz, I_{AC}=0.1I_K		0.5	0.5	0.5	Ω*
e_N	Wideband Noise	I_K=100µA, 10Hz ≤ f ≤ 10kHz		93	93	93	μV_{RMS}*
ΔV_R	Reverse Breakdown Voltage Long-term Stability	t=1000hrs, T=25°C, I_K=100µA		120	120	120	ppm*

*Typical.

Guaranteed Electrical Characteristics, FAN4050-8.2

(T_A = 25°C unless otherwise specified, in free air)
The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Limits A	Limits B	Limits C	Units
V_R	Reverse Breakdown Voltage	I_K = 150µA		8.192	8.192	8.192	V*
TCV_R	Reverse Breakdown Voltage Tolerance	I_K = 150µA	 •	±8.2 ±35	±16 ±43	±41 ±68	mV mV
I_{RMIN}	Minimum Operating Current		•	95	95	95	µA
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	I_K = 150µA	•	±50	±50	±50	ppm/°C
ΔV_R (ΔI_K)	Reverse Breakdown Voltage Change with Operating Current	$I_{RMIN} \le I_K \le$1mA 1mA ≤ I_K ≤ 15mA	• •	2.5 18	2.5 18	2.5 18	mV mV
Z_{KA}	Reverse Dynamic Impedance	I_K=1mA, f=120Hz, I_{AC}=0.1I_K		0.6	0.6	0.6	Ω*
e_N	Wideband Noise	I_K=150µA, 10Hz ≤ f ≤ 10kHz		150	150	150	μV_{RMS}*
ΔV_R	Reverse Breakdown Voltage Long-term Stability	t=1000hrs, T=25°C, I_K=150µA		120	120	120	ppm*

*Typical.

Advance Specification

Guaranteed Electrical Characteristics, FAN4050-10

(T_A = 25°C unless otherwise specified, in free air)

The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Limits A	Limits B	Limits C	Units
V_R	Reverse Breakdown Voltage	I_K = 150µA		10.00	10.00	10.00	V*
TCV_R	Reverse Breakdown Voltage Tolerance	I_K = 150µA	 •	±10 ±43	±20 ±53	±50 ±83	mV mV
I_{RMIN}	Minimum Operating Current		•	103	103	103	µA
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	I_K = 150µA	•	±50	±50	±50	ppm/°C
ΔV_R (ΔI_K)	Reverse Breakdown Voltage Change with Operating Current	$I_{RMIN} \le I_K \le$1mA 1mA ≤ I_K ≤ 15mA	• •	3.5 23	3.5 23	3.5 23	mV mV
Z_{KA}	Reverse Dynamic Impedance	I_K=1mA, f=120Hz, I_{AC}=0.1I_K		0.7	0.7	0.7	Ω*
e_N	Wideband Noise	I_K=150µA, 10Hz ≤ f ≤ 10kHz		150	150	150	μV_{RMS}*
ΔV_R	Reverse Breakdown Voltage Long-term Stability	t=1000hrs, T=25°C, I_K=150µA		120	120	120	ppm*

*Typical.

Advance Specification

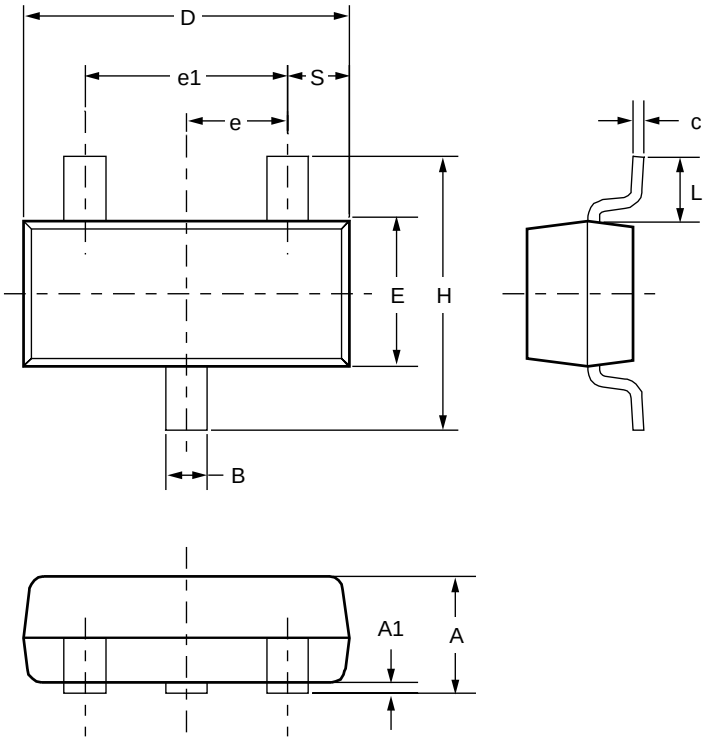
Mechanical Dimensions

SSOT-23 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.035	.044	.89	1.02	
A1	.0005	.004	.013	.10	
B	.015	.020	.37	.51	
c	.003	.007	.085	.18	
D	.110	.120	2.80	3.04	
E	.047	.055	1.20	1.40	
e	.035	.041	.89	1.03	
e1	.070	.080	1.78	2.05	
H	.083	.104	2.10	2.64	
L	.027 BSC		.69 BSC		
S	.018	.024	.45	.60	

Notes:

1. Dimensions are inclusive of plating.
2. Dimensions are exclusive of mold flash & metal burr.
3. Comply to JEDEC TO-236.
4. This drawing is for matrix leadframe only.



Advance Specification

Ordering Information

Example: FAN4050 A I S3-5.0

FAN4050 **A** **I** **S3** **–** **5.0**

Grade	Package	Voltage
0.1% = A	SSOT23 = S3	2.5V = 2.5
0.2% = B		4.096V = 4.1
0.5% = C		5.0V = 5.0
		8.192V = 8.2
		10V = 10.0

SSOT-23 Package Marking Information

Only 3 fields of marking are possible on an SSOT-23. This table gives the meaning of these fields.

Example: F5A

F **5** **A**

Voltage	Grade
2.5V = 2	0.1% = A
4.096V = 4	0.2% = B
5.0V = 5	0.5% = C
8.192V = 8	
10V = 0	

Advance Specification

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MICROWIRE™
POP™
PowerTrench®
QFET™
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Quiet Series™
SuperSOT™-3
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SuperSOT™-8
SyncFET™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAN5061

High Performance Programmable Synchronous DC-DC Controller for Multi-Voltage Platforms

Features

- Programmable output for Vcore from 1.3V to 3.5V using an integrated 5-bit DAC
- Controls adjustable linears for Vtt (1.5V), and Vclock (2.5V)
- Meets VRM specification with as few as 5 capacitors
- Meets 1.550V +40/-70mV over initial tolerance, temperature and transients
- Remote sense
- Active Droop
- Drives N-Channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- 20 pin SOIC package

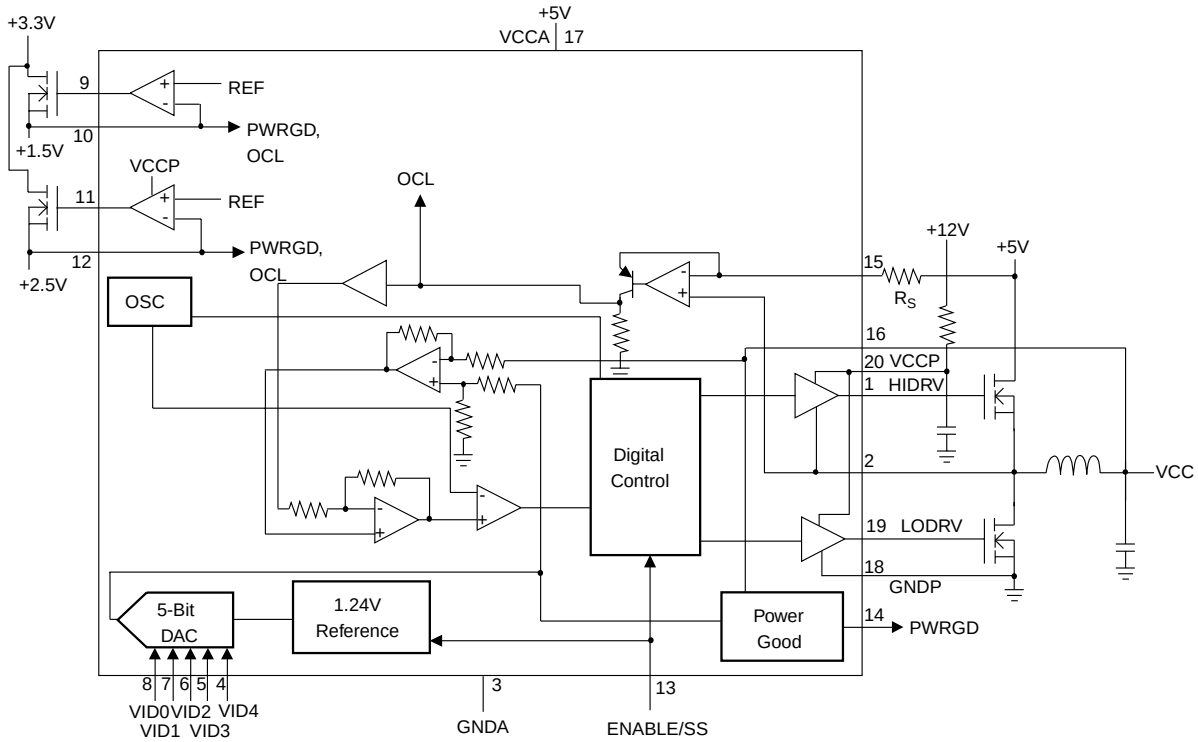
Applications

- Power supply for Pentium® II Camino Platform
- Power supply for Pentium II Whitney Platform
- VRM for Pentium III processor
- Programmable multi-output power supply

Description

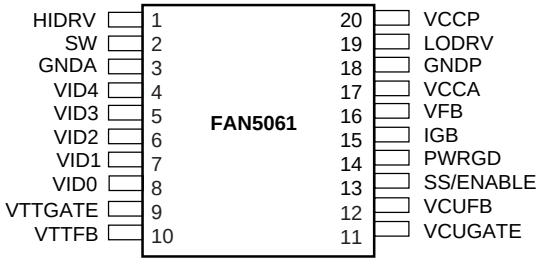
The FAN5061 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable set of output voltages for multi-voltage platforms such as the Intel Camino, and provides a complete solution for the Intel Whitney and other high-performance processors. The FAN5061 features remote voltage sensing, independently adjustable current limit, and Active Droop for optimal converter transient response. The FAN5061 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The FAN5061 uses a high level of integration to deliver load currents in excess of 16A from a 5V

Block Diagram



source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while Active Droop permits exact tailoring of voltage for the most demanding load transients. The FAN5061 includes linear regulator controllers for Vtt termination (1.5V), and Vclock (2.5V), each adjustable with an external divider. The FAN5061 also offers integrated functions including Power Good, Output Enable/Soft Start and current limiting, and is available in a 20 pin SOIC package.

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	HIDRV	**High Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
2	SW	**High side Driver Source and Low side Driver Drain Switching Node.** Together with DROOP and ILIM pins allows FET sensing for Vcc current.
3	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
4-8	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.
9	VTTGATE	**Gate Driver for VTT Transistor.** For 1.5V output.
10	VTTFB	**Voltage Feedback for VTT.**
11	VCKGATE	**Gate Driver for VCK Transistor.** For 2.5V output.
12	VCKFB	**Voltage Feedback for VCK.**
13	ENABLE/SS	**Output Enable.** A logic LOW on this pin will disable all outputs. An internal current source allows for open collector control. This pin also doubles as soft start for all outputs.
14	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if any output voltage is not within ±12% of the nominal output voltage setpoint.
15	IFB	**Vcc Current Feedback.** Pin 15 is used in conjunction with pin 2 as the input for the Vcc current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
16	VFB	**Vcc Voltage Feedback.** Pin 16 is used as the input for the Vcc voltage feedback control loop. See Application Information for details regarding correct layout.
17	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
18	GNDP	**Power Ground.** Return pin for high currents flowing in pin 20 (VCCP).
19	LODRV	**Vcc Low Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
20	VCCP	**Power VCC.** For all FET drivers. Connect to system 12V supply through a 33Ω, and decouple with a 1µF ceramic capacitor.

Preliminary Specification

Absolute Maximum Ratings

Supply Voltages VCCA, VCCP to GND	13.5V
Voltage Identification Code Inputs, VID0-VID4	VCCA
All Other Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-ambient, Θ_{JA}[1]	75°C/W

Note:

1. Component mounted on demo board in free air.

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP		10.8	12	13.2	V

Electrical Specifications

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
VCC Regulator						
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A,V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.397 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C,V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		-4		mV/V
Internal Droop Impedance	I_{LOAD} = 0.8A to 12.5A		13.0	14.4	15.8	KΩ
Maximum Droop				60		mV
Output Ripple	20MHz BW, I_{LOAD} = 18A			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to 18A, V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45	50	60	µA
Efficiency	I_{LOAD} = 18A, V_{OUT} = 2.0V			85		%

Preliminary Specification

Electrical Specifications (Continued)

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Driver Rise & Fall Time	See Figure 3			50		nsec
Output Driver Deadtime	See Figure 3			50		nsec
Duty Cycle			0		100	%
5V UVLO		•	3.74	4	4.26	V
12V UVLO		•	7.65	8.5	9.35	V
Soft Start Current		•	5	10	17	µA
VTT Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$	•	1.425	1.5	1.575	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
VCLK Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$	•	2.375	2.5	2.625	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
Common Functions						
Oscillator Frequency		•	255	310	345	kHz
PWRGD Threshold	Logic HIGH, All Outputs Logic LOW, Any Output	• •	93 88		107 112	$\%V_{OUT}$
Linear Regulator Under Voltage Delay Time	Over Current			30		µsec

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

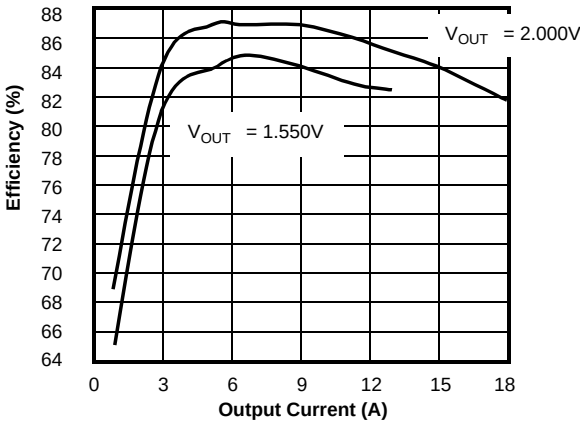
1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

Preliminary Specification

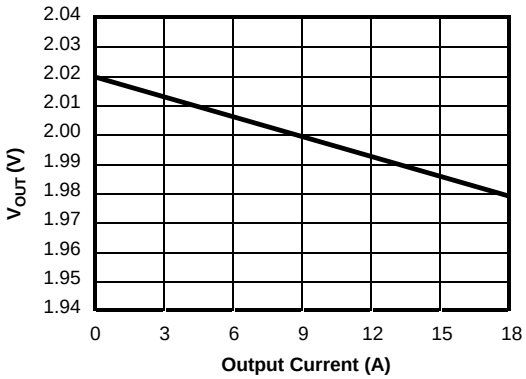
Typical Operating Characteristics

(V_{CCA} = 5V, V_{CCP} = 12V, and T_A = +25°C using circuits in Figure 1, unless otherwise noted.)

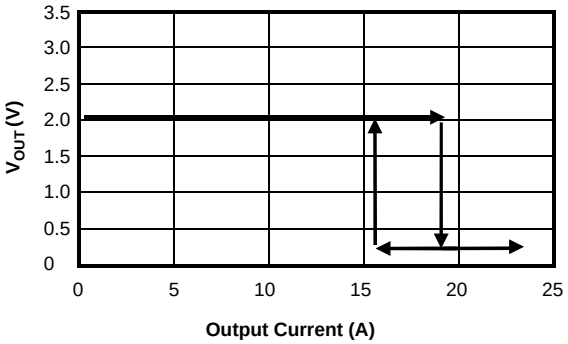
V_{CPU} Efficiency vs. Output Current



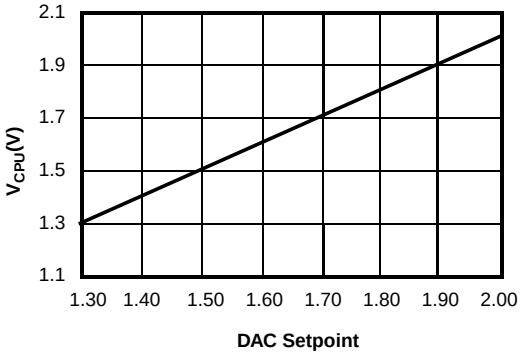
Droop, V_{CPU} = 2.0V, R_D = 8K Ω



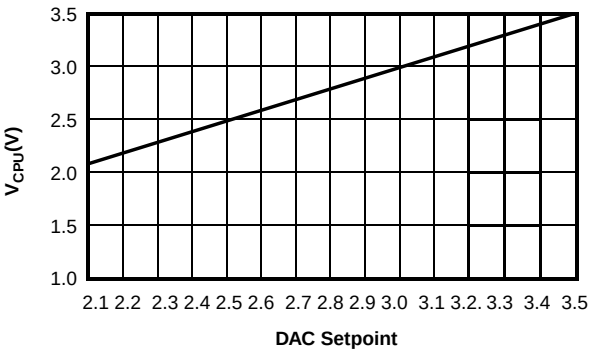
CPU Output Voltage vs. Output Current



Output Programming, VID4 = 0

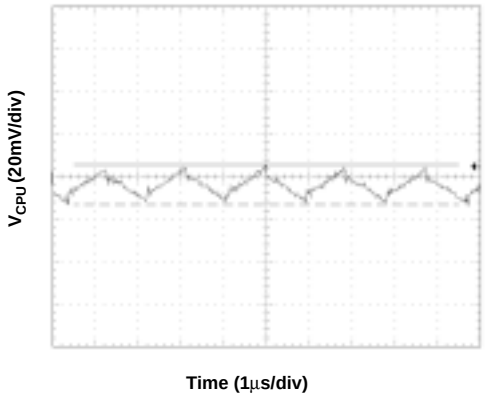


Output Programming, VID4 = 1

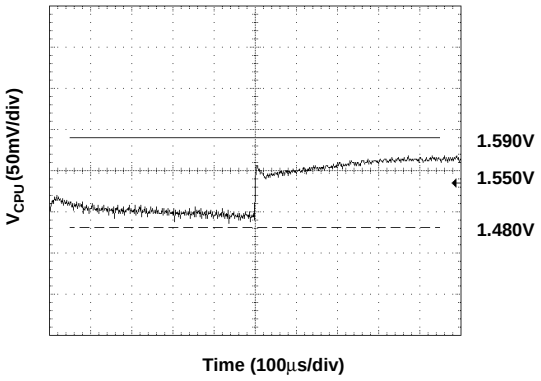


Typical Operating Characteristics (continued)

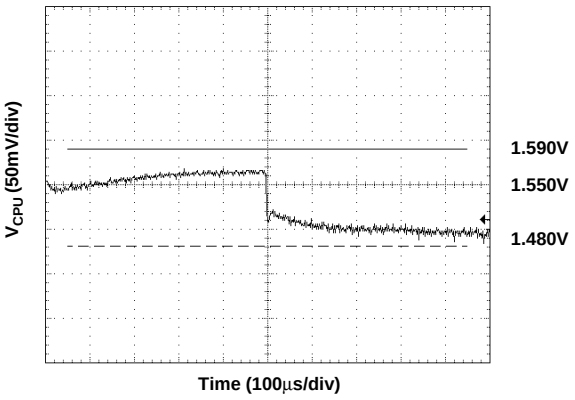
Output Ripple, 2.0V @ 18A



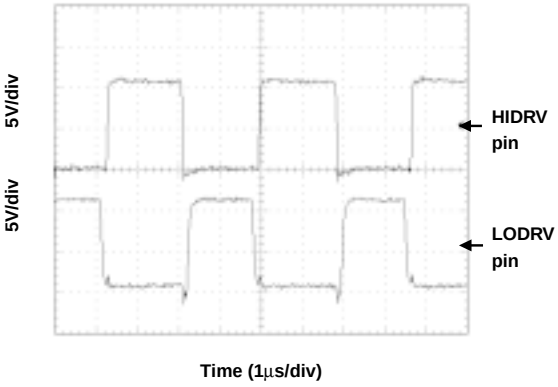
Transient Response, 12.5A to 0.5A



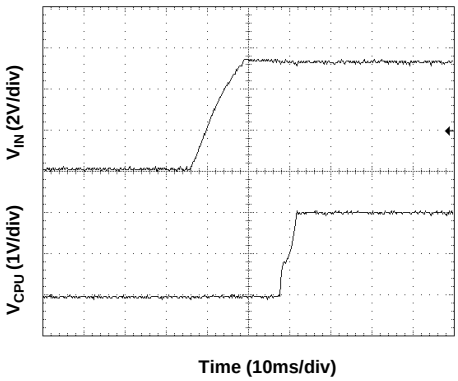
Transient Response, 0.5A to 12.5A



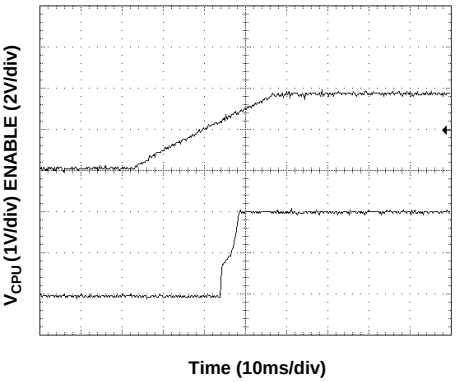
Switching Waveforms, 18A Load



Output Startup, System Power-up



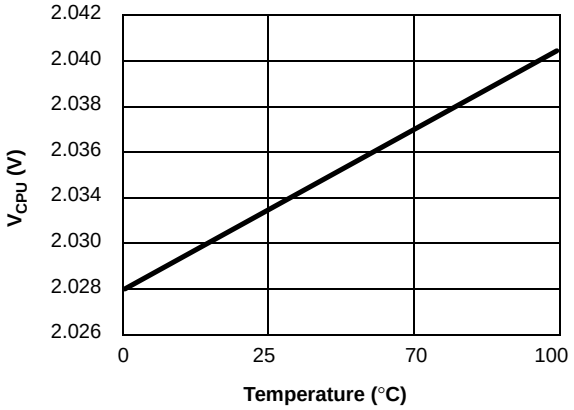
Output Startup from Enable

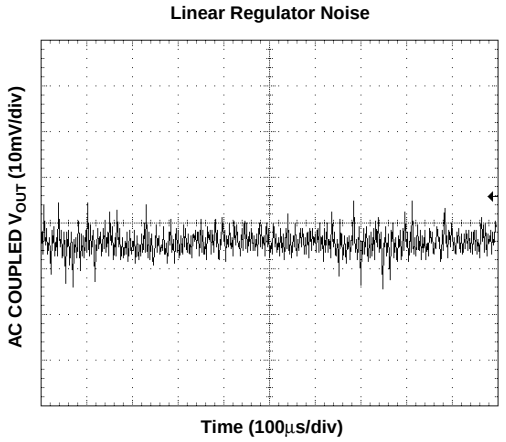


Preliminary Specification

Preliminary Specification

Typical Operating Characteristics (continued)





Application Circuit

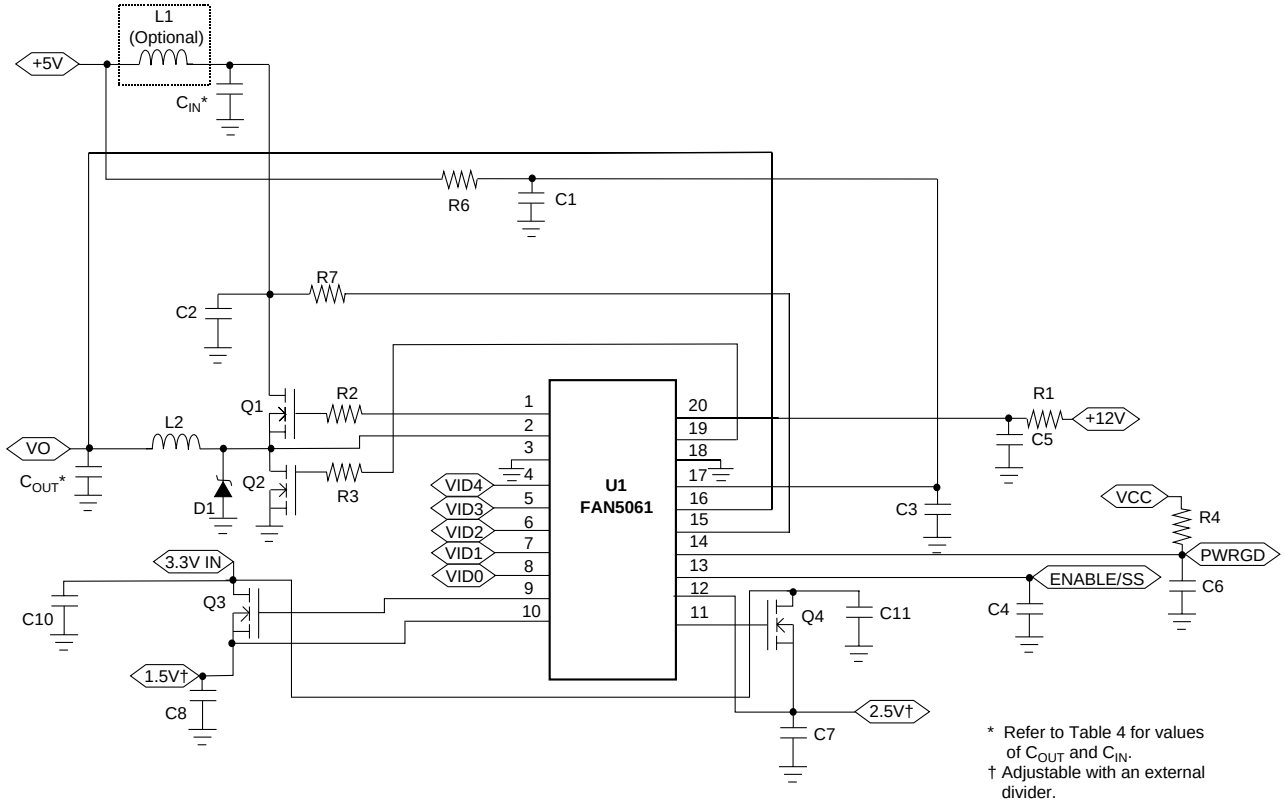


Figure 1. Application Circuit for Katmai/Camino/BX/ZX Motherboards
(Worst Case Analyzed! See Appendix for Details*)*

Table 2. FAN5061 Application Bill of Materials for Intel Katmai/Camino/BX/ZX Motherboards

(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C8-9	Sanyo 6MV1000FA	2	1000µF, 6.3V Electrolytic	
C10-11	Any	2	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 8A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-4	Fairchild FDB4030L	2	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R6	Any	1	10Ω	
R7	Any	1	*	
U1	Fairchild FAN5061M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 17.4A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/Ω should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

*Refer to table for values.

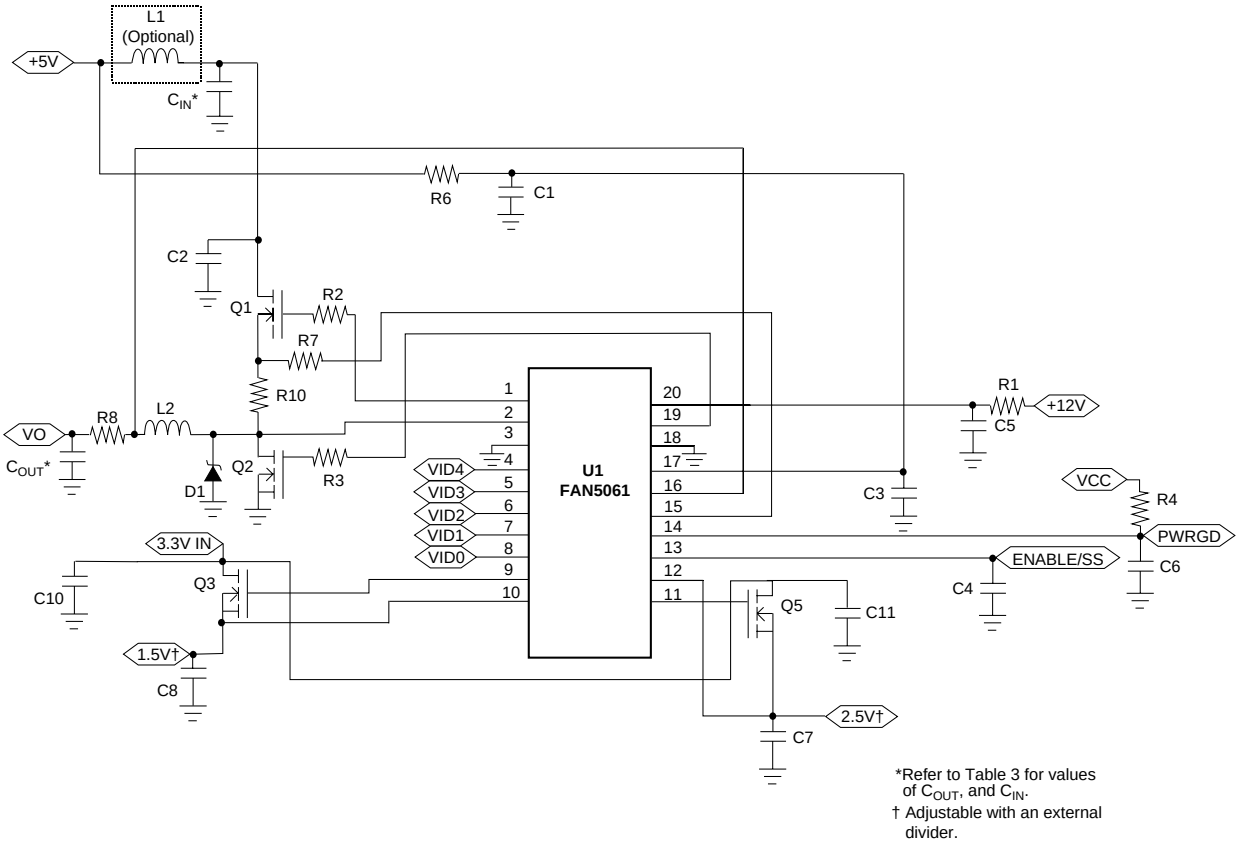


Figure 2. Application Circuit for Coppermine/Camino Motherboards
(Typical Design)

Table 3. FAN5061 Application Bill of Materials for Intel Coppermine/Camino Motherboards
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C8-9	Sanyo 6MV1000FA	2	1000µF, 6.3V Electrolytic	
C10-11	Any	2	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	12	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 5A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 15A Inductor	DCR ~ 3mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-4	Fairchild FDB4030L	2	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R6	Any	1	10Ω	
R7	Any	1	6.24KΩ	
R8	N/A	1	30mΩ	PCB Trace Resistor
U1	Fairchild FAN5061M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 12.5A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/Ω should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

Application Circuit Summary

Table 4 summarizes the worst-case design schematics presented in this section. The basic choices are: A) The processor, B) the chipset used, and C) the use or not of a sense resistor. Depending on board layout and component selection, it may be possible to use fewer output capacitors than shown here. For configurations not shown in this datasheet, consult the Appendix for selection of component values.

Table 4. Recommended Values for CPU-based Applications

Processor	Chipset	C_{IN}	C_{OUT}*	R5, R7 (KΩ)
Coppermine	Whitney	3	4	8.45
Katmai	Camino	4	6	13.0
Mendocino	Whitney	4	5	11.3
Katmai	BX	5	6	11.8

*Output capacitance requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details. See the Appendix to this datasheet for the method of calculation of these components. Pin 4 must be used to remote sense the voltage at the processor to achieve the specified performance.

Test Parameters

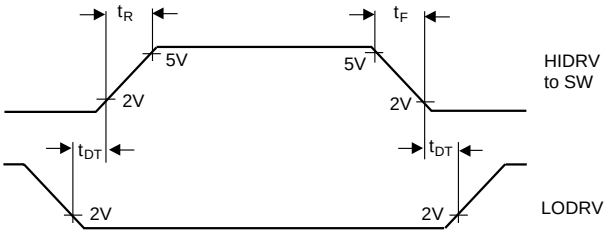


Figure 3. Ouput Drive Timing Diagram

Application Information

The FAN5061 Controller

The FAN5061 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the FAN5061 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The FAN5061 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the FAN5061 Block Diagram on page 1. The FAN5061 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the DROOP (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the DROOP and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the FAN5061 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The FAN5061 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers’ power and ground are separated from the chip’s power and ground for switching noise immunity. The power supply pin, VCCP, is supplied from an external 12V source through a series 33Ω resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the FAN5061 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4

is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V.

Power Good (PWRGD)

The FAN5061 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The Power Good flag provides no other control function to the FAN5061.

Output Enable/Soft Start (ENABLE/SS)

The FAN5061 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to softstart the switching.

Over-Voltage Protection

The FAN5061 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the FAN5061 disables the output drive signal to the external high-side MOSFET. The DC-DC converter returns to normal operation after the output voltage returns to normal levels.

Oscillator

The FAN5061 oscillator section uses a fixed frequency of operation of 300KHz.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:
V_{in} = Input Power Supply
V_{out} = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_O \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:
C_o = The total output capacitance
I_{pp} = Maximum to minimum load transient current
V_{tb} = The output voltage tolerance budget allocated to load transient
D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_O, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The FAN5061 provides significant cost savings for the newer CPU systems that typically run at high supply current.

FAN5061 Short Circuit Current Characteristics

The FAN5061 protects against output short circuit on the core supply by turning off both the high-side and low-side MOSFETs. The FAN5061 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} * R_{DS,\,on}}{I_{Detect}}$$

with $I_{Detect} \approx 50\mu A$, I_{SC} is the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. Alternately, use of a sense resistor in series with the source of the MOSFET eliminates this source of inaccuracy in the current limit.

As an example, Figure 4 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET (R_{DS} = 20mΩ maximum at 25°C * 1.25 at 75°C = 25mΩ) and a 8.2KΩ R_S.

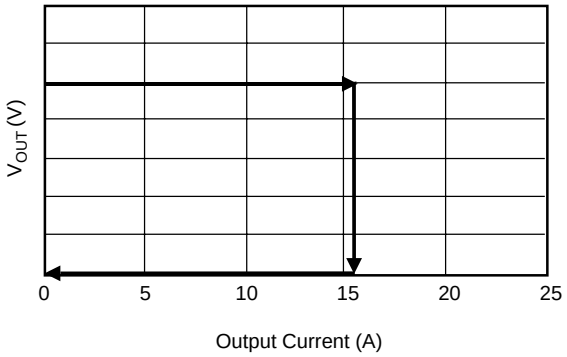


Figure 4. FAN5061 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of 50µA * 8.2KΩ = 410mV, which occurs at 410mV/25mΩ = 16.4A. (Note that this current limit level can be as high as 410mV/15mΩ = 27A, if the MOSFET has typical $R_{DS,on}$ rather than maximum, and is at 25°C).

If the current exceeds this limit for more than 30µsec, the FAN5061 shuts down all of its outputs, including its linear regulators. They remain shut down until power is recycled.

Similarly, if any of the linear regulator outputs are loaded heavily enough that their output voltage drops below 80% of nominal, all FAN5061 outputs, including the switcher, are shut off and remain off until power is recycled.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 5. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 5 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

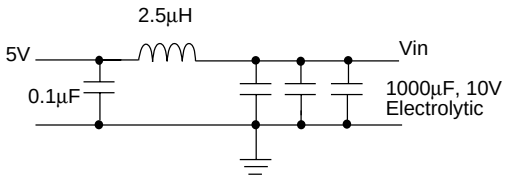


Figure 8. Input Filter

Active Droop™

The FAN5061 includes active droop; as the ouptut current increases, the output voltage drops. This is done in order to allow maximum headroom for transient response of the converter. The current is sensed by measuring the voltage across the high-side MOSFET during its on time. Note that this makes the droop dependent on the temperature of the MOSFET. However, when the formula given for selecting R_S (current limit) is used, there is a maximum droop possible (-40mV), and when this value is reached, additional drop across the MOSFET will not cause any increase in droop—until current limit is reached.

Additional droop can be added to the active droop using a discrete resistor (typically a PCB trace) outside the control loop, as shown in Figure 2. This is typically only required for the most demanding applications, such as for the next generation Intel processor (tolerance = +40/-70mV), as shown in Figure 2.

Remote Sense

The FAN5061 offers remote sense of the output voltage to minimize the output capacitor requirements of the converter. It is highly recommended that the remote sense pin, Pin 16, be tied directly to the processor power pins, so that the effects of power plane impedance are eliminated. Further details on use of the remote sense feature of the FAN5061 may be found in Applications Bulletin AB-24.

Adjusting the Linear Regulators' Output Voltages

Any or all of the linear regulators' outputs may be adjusted high to compensate for voltage drop along traces, as shown in Figure 6.

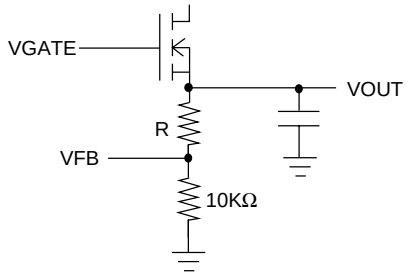


Figure 6. Adjusting the Output Voltage of the Linear Regulator

The resistor value should be chosen as

$$R = 10K\Omega * \left(\frac{V_{out}}{V_{nom}} - 1\right)$$

For example, to get the V_{TT} voltage to be 1.55V instead of 1.50V, use R = 10KΩ * [(1.55/1.50) – 1] = 333Ω.

Using the FAN5061 for Vnorthbridge = 1.8V

Similarly, the FAN5061 can also be used to generate Vnorthbridge = 1.8V by utilizing the AGP regulator as shown in Figure 6: tie the TYPEDET pin to ground, and use R = 2KΩ.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the FAN5061 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the FAN5061 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the FAN5061. That is, traces that connect to pins 1, 2, 19, and 20 (HIDRV, SW, LODRV and VCCP) should be kept far away from the traces that connect to pins 3, 16 and 17.
- Place the 0.1µF decoupling capacitors as close to the FAN5061 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the FAN5061 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-962-7833.

Preliminary Specification

FAN5061 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the FAN5061. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-962-7833 for an evaluation board.

Additional Information

For additional information contact Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-962-7833.

Appendix

Worst-Case Formulae for the Calculation of Cout, R5, and Cin (Circuit of Figure 1 only)

The following formulae design the FAN5061 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, active droop tolerance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

ESR, the ESR of the ouput caps, per cap (44mΩ for the Sanyo parts shown in this datsheet);

R_D, the on-resistance of the MOSFET (20mΩ for the FDB6030);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature).

I_{rms}, the rms current rating of the input caps (2A for the sanyo parts shown in this datasheet.)

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R5 = \frac{I_O * R_D * (1 + \Delta R_D) * 1.10}{50 * 10^{-6}}$$

Number of capacitors needed fo C_{out} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}|}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - 0.004 * V_{nom} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing and the usual caps. We have V_{T+} = $|V_{T-}|$ = 0.134, I_O = 14.2, V_{nom} = 2.000, and ΔR_D = 0.67. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R5 = \frac{14.2 * 0.020 * (1 + 0.67) * 1.0}{50 * 10^{-6}} = 10.4K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134} = 4.66$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.004 * 2.000 + \frac{14400 * 14.2 * 0.020}{18 * 10400 * 1.1}} = 4.28$$

Since X > Y, we choose X, and round up to find we need 5 capacitors for C_{OUT}.

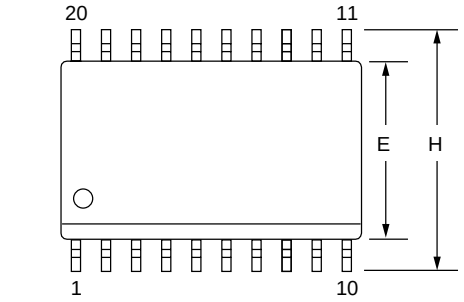
Mechanical Dimension

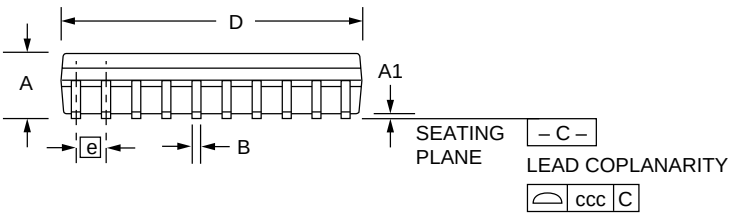
20-Lead SOIC

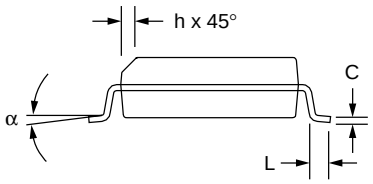
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Specification

Ordering Information

Product Number	Package
FAN5061M	20 pin SOIC

Preliminary Specification

FAN5201

Chemistry Independent Intelligent Battery Charger

Features

- Chemistry independent charging
- SMBus™ 2-wire serial interface controlled
- Independent Voltage, Current and Power DACs
- 6A maximum charging current
- 4–19V battery voltage range
- 24V maximum input voltage
- 5V “keep alive” regulator controller onboard
- 100% maximum duty-cycle
- Synchronous rectification
- System soft start protects during hot plug-ins
- Latched current limit protection
- Output over-voltage protection (crowbar)
- Input under-voltage lockout
- Battery backfeed prevented
- Optimized response for each control loop (current, voltage and power)
- Power down driven by SMBus or by adapter not available or by softstart pin
- Controlled drive of discrete FETs minimizes power dissipation
- Logic signal ACAV indicates presence of AC adapter (adjustable threshold)
- Output current “motorboating” prevented
- True power multiplier

Applications

- Notebooks’ fast chargers
- PDAs
- Hand-held portable instruments

Description

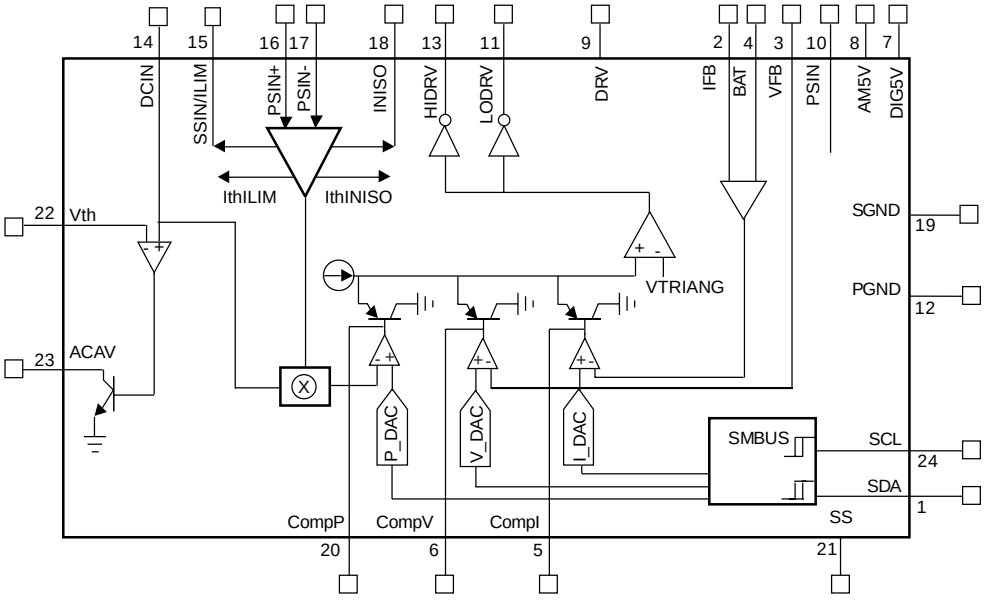
The FAN5201 is a smart battery charger IC controller for Li+ and Ni based battery chemistries. The charger (slave) together with the host controller and smart battery constitutes a smart battery system that communicates via the SMBus protocol, a two wire serial communication system.

An innovative power control loop allows operation from line power and battery charging (with residual power) without exceeding the maximum input power programmed according to the AC adapter power rating.

The FAN5201 is available in one SSOP24 package.

Preliminary Specification

Block Diagram



Preliminary Specification

SMBus Functional Description

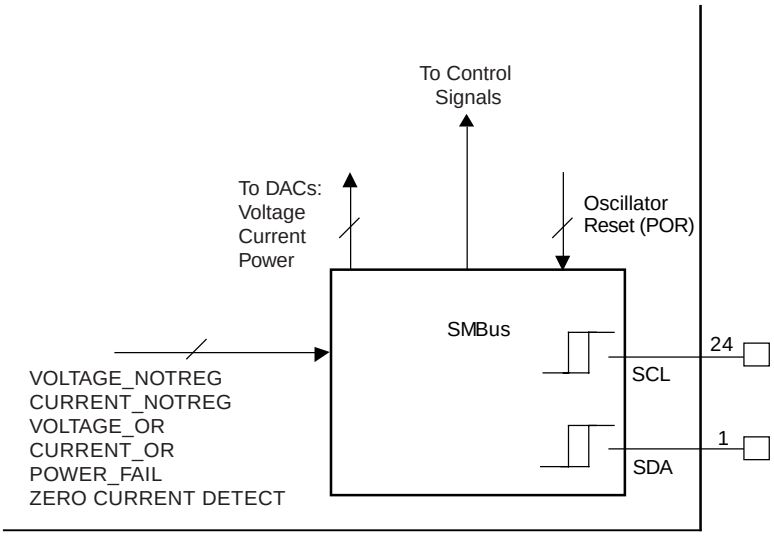
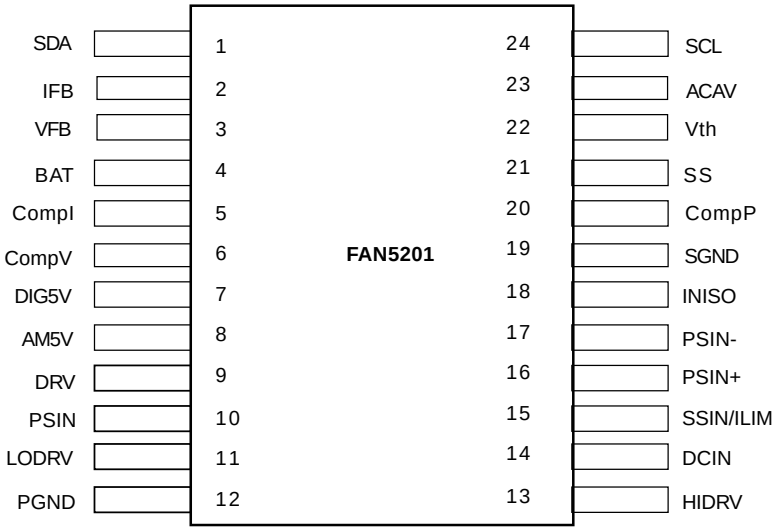


Figure 1. Internal SMBus Configuration

Pin Assignments



Pin Descriptions

Pin Number	Pin Name	Pin Function Description
1	SDA	**Serial Data**. SMBus data I/O.
2	IFB	**Current Feedback.** Output current sense +. Connect this pin to the positive side of a battery current sense resistor.
3	VFB	**Voltage Feedback.** Voltage remote sense feedback. Connect this pin to the battery terminals.
4	BAT	**Battery.** Output current sense -. Connect this pin to the negative side of a battery current sense resistor.
5	CompI	**Current Compensation.** Frequency compensation for current loop.
6	CompV	**Voltage Compensation.** Frequency compensation for voltage loop.
7	DIG5V	**5V Digital Input.** 5V internal power.
8	AM5V	**5V Analog Input.** Connect to 5V power. See Figure 4.
9	DRV	**Drive.** Base (gate) drive for external PNP (P-channel MOSFET).
10	PSIN	**Power Supply.** Power source node, powered either by the AC adapter or by the battery.
11	LODRV	**Low Side FET Driver.** Drive for low side switching MOSFET Q4.
12	PGND	**Power Ground.**
13	HIDRV	**High Side FET Driver.** Drive for high side switching MOSFET Q3.
14	DCIN	**DC Power Input.** Connect to the AC adapter input.
15	SSIN/ILIM	**Soft Start and Current Limit.** Connect to an external MOSFET for limiting inrush and fault current.
16	PSIN+	**Input Power Sense +.** Connect this pin to the positive side of an adapter current sense resistor.
17	PSIN-	**Input Power Sense -.** Connect this pin to the negative side of an adapter current sense resistor.
18	INISO	**Input Isolation Drive.** Q2 gate drive. Attach to a P-channel MOSFET to prevent battery backfeed.
19	SGND	**Signal Ground.** Attach all small signal grounds to this pin, and attach the pin to the ground plane with a single connection.
20	CompP	**Power Compensation.** Frequency compensation for power loop.
21	SS	**Soft Start.** Connect to a capacitor to softstart.
22	Vth	**Voltage Threshold.** Sets the level at which ACAV trips.
23	ACAV	**AC Available.** Open collector output signaling that the AC adapter is present.
24	SCL	**Serial Clock.** SMBus clock input.

Absolute Maximum Ratings[1]

Parameter	Conditions	Min.	Typ.	Max.	Unit
DCIN				30	V
PSIN+, PSIN-				30	V
Ambient Temperature, T_A		0		70	°C
Maximum Power Dissipation	SSOP24, T_J = 125°C		TBD		W

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions **DCIN = 19V, T_A = 0-70°C, unless otherwise specified.**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply and Reference					
DCIN Input Supply Voltage	Internal 5V	8		24	V
	External 5V	6		24	V
DCIN Quiescent Current	Operation			3	mA
	Power Down, Note 1			200	µA
PSIN Current	Operation			300	
	Power Down, Note 1		140	200	µA
5V Accuracy	I < 10mA	-4		4	%
DRV Output Sink Current		1			mA
Switching Regulator					
$V_{bat,min}$	I_{OUT} = 32mA	4			V
Maximum Duty Cycle		100			%
Oscillator Frequency		225	250	275	kHz
HIDRV ON Resistance	High		4	7	Ω
	Low		4	7	Ω
HIDRV High Output, $V_{DCIN} - V_{HI}$	I = 10µA			100	mV
HIDRV Low Output, $V_{DCIN} - V_{LO}$	I = 10µA	5			V
LODRV ON Resistance	High		4	7	Ω
	Low		4	7	Ω
LODRV High Output	I = 10µA, AM5V = DIG5V = %5v	4.5			V
LODRV Low Output				100	mV
Analog Functions					
Input Current Limit Threshold		108		132	mV
Input UVLO		5.4		6.6	V
Input UVLO Hysteresis			400		mV
Vtriang Amplitude, pk-pk			950		mV
Vtriang Mean			2.5		V
Vtriang gain from DCIN			50		mV/V
Psense Amplifier CMRR		60			dB
Psense Amplifier CMRR @ 250kHz		32			dB
VFB Leakage	Operation			30	µA
	Power Down, Note 1			1	

Preliminary Specification

Operating Conditions (Continued) DCIN = 19V, T_A = 0-70°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
BAT, IFB Leakage	Operation			TBD	µA
	Power Down, Note 1			10	µA
Output Overvoltage Threshold		107	110	113	%Vout
Vthreshold ACAV	Rt1 = 9KΩ, Rt2 = 1KΩ	5.4		6.6	V
Vhysteresis ACAV	Rt1 = 9KΩ, Rt2 = 1KΩ		400		mV
Battery POWER_FAIL Threshold		5.4		6.6	V
CURRENT_NOTREG		90		110	%Ireg
VOLTAGE_NOTREG		90		110	%Vreg
Input Isolation Current Threshold	Ith = Vth/RS1	3.6			mV
Backfeed Current Threshold	Ith = Vth/RS2	3.6			mV
Zero Current Detect Threshold			9.7		mV
VOLTAGE_OR Threshold			110		%Vout
CURRENT_OR Threshold		110		112	mV
AC_PRESENT Threshold		5.4		6.6	V
AC_PRESENT Hysteresis			400		mV
Soft Start Current			2		µA
Soft Start Disable	Output disabled			800	mV
Over-temperature Shutdown			150		°C
Digital Functions					
Current DAC Resolution				8	Bits
Current DAC Accuracy		-5		+5	%FS
Current DAC Differential Nonlinearity		-1/2		+1/2	LSB
Current DAC Integral Nonlinearity		-2		+2	LSB
Current DAC Conversion Time				2	msec
Current DAC Voltage Offset		0			mV
Voltage DAC Resolution				8	Bits
Voltage DAC Accuracy		-5		+5	%Vout
Voltage DAC Differential Nonlinearity		-1/2		+1/2	LSB
Voltage DAC Integral Nonlinearity		-2		+2	LSB
Voltage DAC Conversion Time				2	msec
Power DAC Resolution				4	Bits
Power DAC Accuracy		-5		+5	%FS
Power DAC Differential Nonlinearity		-1/2		+1/2	LSB
Power DAC Integral Nonlinearity		-2		+2	LSB
Power DAC Conversion Time				2	msec
Switches Q1, Q2					
SSIN/ILIM Source Current, pk		10			mA
SSIN/ILIM Sink Current, pk		35		65	µA
SSIN/ILIM High Output, $V_{DCIN} - V_{HI}$				100	mV
SSIN/ILIM Low Output, $V_{DCIN} - V_{LO}$	V_{DCIN} = 19V	10		12	V
	V_{DCIN} = 10V	8			V
INISO ON Sink Current				50	µA

Preliminary Specification

Operating Conditions (Continued) DCIN = 19V, T_A = 0-70°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
INISO High Output, $V_{DCIN} - V_{HI}$				100	mV
INISO Low Output, $V_{DCIN} - V_{LO}$	V_{DCIN} = 19V	10		12	V
	V_{DCIN} = 10V	8			V
SMBus					
Data/Clock input low voltage, V_{IL}		-0.3		0.6	V
Data/Clock input high voltage, V_{IH}		1.4		5.5	V
Data/Clock output low voltage, V_{OL}	At I_{PULLUP} MIN			0.4	V
Data/Clock hysteresis, V_{HYS}			200		mV
Input leakage, I_{LEAK}		-1		1	µA
Current through pullup resistor or current source, I_{PULLUP}		100		350	µA
SMB operating frequency, F_{SMB}		10		100	kHz
Bus free time between Stop and Start condition, T_{BUF}		4.7			µsec
Hold time after (repeated) Start condition, $T_{HD:STA}$	After this period, the first clock is generated	4.0			µsec
Repeated Start condition setup time, $T_{SU:STA}$		4.7			µsec
Stop condition setup time, $T_{SU:STO}$		4.0			µsec
Data hold time, $T_{HD:DAT}$		300			nsec
Data setup time, $T_{SU:DAT}$		250			nsec
$T_{TIMEOUT}$	Note 2	25		35	msec
Clock low period, T_{LOW}		4.7			µsec
Clock high period, T_{HIGH}	Note 3	4.0		50	µsec
Cumulative clock low extend time, $T_{LOW:SEXT}$	Note 4			25	msec
Clock/Data fall time, T_F				300	nsec
Clock/Data rise time, T_R				1000	nsec

Notes:

1. 5V DRV Current = 0, SMBus off.
2. A device will timeout when any clock low exceeds this value.
3. T_{HIGH} Max provides a simple guaranteed method for devices to detect bus idle conditions.
4. $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data times and reset itself.

Applications Discussion

Overview

The FAN5201 contains three control loops: a voltage-regulation loop, a current-regulation loop and a power-regulation loop. All three loops operate independently of each other. They are or'red internally to optimize the battery charging while the notebook is drawing power in its normal operation. The voltage-regulation loop monitors the battery to ensure that its voltage is held at the voltage set point (V0). The current-regulation loop monitors current delivered to the battery to ensure that it regulates at the current-limit set point (I0). The power-regulation loop monitors total input power, to both the battery and the notebook, to ensure that total power drawn from the charger never exceeds the maximum power set point (P0). Assuming that there is adequate power available from the charger, the current-regulation loop is in control as long as the battery voltage is below V0. When the battery voltage reaches V0, the current loop no longer regulates, and the voltage-regulation loop takes over. If on the other hand there is not adequate power available from the charger, the power-regulation loop is in control, and limits the charging of the battery in order to guarantee enough power for the notebook. Figure 2 shows the V-I-P characteristic at the battery.

Setting V0, I0 and P0

The FAN5201's voltage-, current-, and power-limits can be set via the Intel System Management Bus (SMBus™) 2-wire serial interface. The FAN5201's logic interprets the serial-data stream from the SMBus interface to set internal digital-to-analog converters (DACs) appropriately. See the FAN5201 Logic section and SMBus Interface Specification for more information.

Analog Section

The FAN5201analog section consists of 1) three transconductance error amplifiers, one for regulating current, one for regulating voltage, and one for regulating system power, 2) a PWM controller, with its associated gate drivers, and 3) miscellaneous control and reference functions, consisting of an AC present signal, 5V reference, inrush current limiter, reverse feed protection, and a soft start circuit.

The FAN5201 uses DACs to set the current, voltage and power levels, which are controlled via the SMBus interface. Since separate amplifiers are used for each of these controls, each of the control loops can be compensated separately for optimum stability and response in each state.

Whether the FAN5201 is controlling the voltage, current or power at any time depends on the battery's state. If there is adequate power available from the charger, and if the battery has been discharged, the FAN5201's output reaches the current-regulation limit before the voltage limit, causing the system to regulate current. As the battery charges, the voltage rises until the voltage limit is reached, and the charger switches to regulating voltage. On the other hand, if there is not enough power available for both the notebook and the battery charging, the FAN5201 regulates charging current at such a level as to respect the maximum power limit. When the voltage limit is reached, the charger will similarly switch to regulating voltage. The transitions from current to voltage regulation, or from power to voltage regulation, are done by the charger, and need not be controlled by the host.

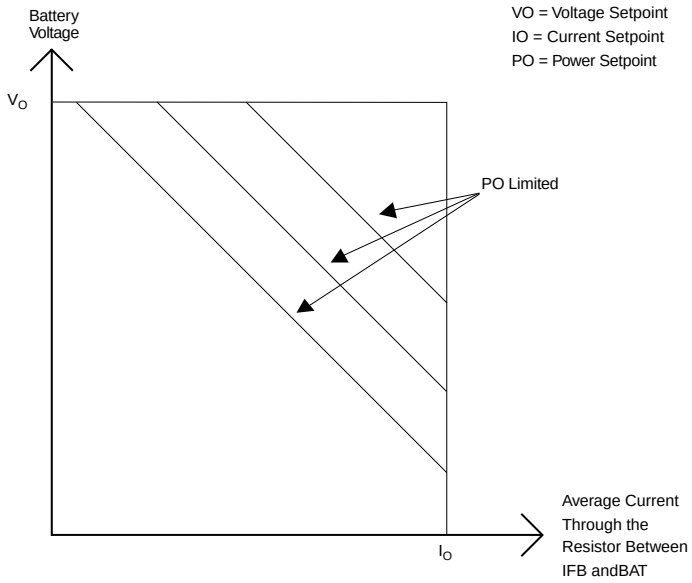


Figure 2. V-I-P Characteristic of FAN5201. If power is available, the battery is charged at a rate I0 until it reaches V0. As power becomes limiting, the charge current is reduced.

Voltage Control Loop

The internal transconductance voltage amplifier controls the FAN5201's output voltage. The battery voltage is fed to the non-inverting input of the amplifier from the VFB pin. The voltage at the amplifier's inverting input is set by an 8-bit DAC, which is controlled by a ChargingVoltage( ) command on the SMBus (See the FAN5201 Logic section and SMBus Interface Specification for more information). The output of the amplifier drives an inverting "or'ring" transistor; the or'ring provides control of the PWM to the lowest of the three amplifiers, while the inversion provides the negative feedback needed for proper control. The ChargingVoltage( ) command of the SMBus provides a 10.000V offset, and 32mV steps, so that the charging voltage can be anywhere from 10.000V to 10.000V + 255 * 32mV = 18.16V. Because a lithium-ion (Li+) battery's typical per-cell voltage is 4.2V maximum, this charger is best suited for 3- and 4-cell batteries. It can also be used for several different cell counts with NiMH batteries.

The voltage amplifier's output is connected to the CompV pin, which compensates the voltage-regulation loop. Typically, a series-resistor/capacitor combination is used to form a pole-zero pair. The pole introduced rolls off the gain starting at low frequencies. The zero provides AC gain at mid-frequencies. The output capacitor of the switcher then rolls off the mid-frequency gain to below 1 to guarantee stability, before encountering the zero introduced by the output capacitor's ESR. Further information on loop stabilization is available in Applications Bulletin AB-18.

Current Control Loop

The internal transconductance current amplifier controls the battery current while the charger is regulating current. Battery current is sensed by monitoring the voltage across a sense resistor (pins IFB and BAT) with an amplifier that removes the common mode battery voltage. The battery current is fed to the non-inverting input of the amplifier. The voltage at the amplifier's inverting input is set by an 8-bit DAC, which is controlled by a ChargingCurrent( ) command on the SMBus (See the FAN5201 Logic section and SMBus Interface Specification for more information). The output of the amplifier drives an inverting "or'ring" transistor; the or'ring provides control of the PWM to the lowest of the three amplifiers, while the inversion provides the negative feedback needed for proper control. The ChargingCurrent( ) command of the SMBus provides 32mA steps with an 18mΩ sense resistor, so that the charging current can be anywhere from 0.000A to 255 * 32mA = 8.16A.

The current amplifier's output is connected to the CompI pin, which compensates the current-regulation loop. Typically, a series-resistor/capacitor combination is used to form a pole-zero pair. The pole introduced rolls off the gain starting at low frequencies. The zero provides AC gain at mid-frequencies. The output capacitor of the switcher then rolls off the mid-frequency gain to below 1 to guarantee stability, before encountering the zero introduced by the output capacitor's ESR. Further information on loop stabilization is available in Applications Bulletin AB-18.

Power Control Loop

The internal transconductance power amplifier controls the system's total power consumption (notebook plus battery charging). Input voltage is monitored on pin DCIN, and input current is sensed by monitoring the voltage across a sense resistor (pins PSIN+ and PSIN-) with an amplifier that removes the common mode input voltage. These two signals are then multiplied together with an analog multiplier, and the result is fed to the non-inverting input of the amplifier. The voltage at the amplifier's inverting input is set by a 4-bit DAC, which is controlled by a ChargingPower( ) command on the SMBus (See the FAN5201 Logic section and SMBus Interface Specification for more information). The output of the amplifier drives an inverting "or'ring" transistor; the or'ring provides control of the PWM to the lowest of the three amplifiers, while the inversion provides the negative feedback needed for proper control. The ChargingPower( ) command of the SMBus provides a 25W offset, and 5W steps, so that the total power drawn can be anywhere from 25W to 25W + 15 * 5W = 100W.

The power amplifier's output is connected to the CompP pin, which compensates the power-regulation loop. Typically, a series-resistor/capacitor combination is used to form a pole-zero pair. The pole introduced rolls off the gain starting at low frequencies. The zero provides AC gain at mid-frequencies. The output capacitor of the switcher then rolls off the mid-frequency gain to below 1 to guarantee stability, before encountering the zero introduced by the output capacitor's ESR. Further information on loop stabilization is available in Applications Bulletin AB-18.

A sudden surge in power required by the notebook will result in a momentary overload on the AC adapter. This has no ill effects, because the power loop recovery time is much shorter than the adapter's thermal time constant, and the minimum adapter output voltage equals the battery voltage, which is sufficient to run the notebook.

PWM Controller

The battery voltage or current or input power is controlled by the pulse-width-modulated (PWM) DC-DC converter controller. This controller drives two external MOSFETs, an N- and a P-channel, which switch the voltage from the input source. This switched voltage feeds an inductor, which filters the switched rectangular wave. The controller sets the pulse width of the switched voltage so that it supplies the desired voltage or current to the battery. The heart of the PWM controller is its multi-input comparator. This comparator compares the lowest of three input signals with a ramp, to determine the pulse width of the switched signal, setting the battery voltage or current. The three signals being or'red together are the current-sense amplifier's output, the voltage-error amplifier's output, and the power-error amplifier's output.

When the current-sense amplifier is in control of the PWM, the comparator adjusts the duty cycle of the switches, regulating the average battery current and keeping it proportional to the error voltage. The current is averaged, rather than peak, since the current sense resistor is between the output capacitor and the battery. Since the average battery current is nearly the same as the peak current, the controller acts as a transconductance amplifier, reducing the effect of the inductor on the output filter LC formed by the output inductor and the output capacitance. This makes stabilizing the circuit easy, since the output filter changes from a complex second-order RLC to a first-order RC. To preserve the inner current-control loop's stability, slope compensation is also fed into the comparator. This damps out perturbations in the pulse width at duty ratios greater than 50%. At heavy loads, the PWM controller switches at a fixed frequency and modulates the duty cycle to control the battery current. At light loads, the DC current through the inductor is not sufficient to prevent the current from going negative through the synchronous rectifier (Figure 2, Q4). The controller monitors the current through the sense resistor; when it drops to below 200mA, the synchronous rectifier turns off to prevent negative current flow.

When the voltage error amplifier is in control of the PWM, the comparator adjusts the duty cycle of the switches, regulating the battery voltage and keeping it proportional to the error voltage. In this mode, the control loop is a standard voltage-mode control, and the only requirement to guarantee stability is that the loop gain be rolled off below 0dB before the LC resonant frequency.

When the power error amplifier is in control of the PWM, the comparator adjusts the duty cycle of the switches, regulating the total power drawn from the charger. The loop determines whether the total power available from the wall adapter is sufficient to provide both the load and battery charging needs. If not, the charging power to the battery is reduced by the amount needed to keep the total demand within the AC-DC output power limit of the adapter.

The PWM controller also implements voltage feedforward. This means that the gain of the control loops are adjusted inversely proportionally to the input voltage: as the input voltage increases, loop gain is decreased. This improves the audio susceptibility of the converter, and in particular, means that the bandwidth of each of the loops is relatively independent of the AC adapter voltage. Feedforward is accomplished by modulating the amplitude of the ramp signal.

MOSFET Drivers

The FAN5201 drives external MOSFETs to regulate battery voltage or current, a high-side P-channel and a low-side N-channel for synchronous rectification. Use of a P-channel MOSFET for the high-side switch permits operation without charge-pumping and its attendant external components. The synchronous rectifier behaves like a diode, but with a smaller voltage drop to improve efficiency. A small dead time is added between the time that the high-side MOSFET turns off and the synchronous rectifier turns on, and vice versa. This prevents shoothrough currents (currents that flow through both MOSFETs during the brief time that one is turning on and the other is turning off). A schottky rectifier from the source to the drain of Q4 prevents the synchronous rectifier's body diode from conducting. The body diode typically has slower switching-recovery times, so allowing it to conduct would degrade efficiency.

Control and Reference Functions

The FAN5201 has a number of additional analog functions to enhance overall system performance. The ACAV is an open collector signal that can be used to determine the presence of the AC charger; its threshold is set by an external resistor divider attached the Vth pin.

A 5V keep alive linear regulator receives power either from the AC adapter via Q1 or from the battery (PSIN pin). This regulator can provide up to 10mA to power memory during a system shutdown.

Protection Circuitry

The FAN5201 protects against a variety of possible fault or problem conditions.

Input Protection

Inrush current can be a problem during hot plug-in if in front of the switching regulator a large capacitor is used to decouple noise. Conceivably, the inrush could be high enough to trip on overcurrent protection in the AC adapter. The FAN5201 provides the means for limiting inrush current to any desired value: The SSIN/ILIM pin provides a sink current of 65µA maximum to turn on the gate of the P-channel MOSFET Q1, so that selecting a gate-source capacitance on Q1 will slow its turn-on time to any desired speed, thus restricting the amount of inrush current.

The charger has its own local soft start, which controls the maximum duty cycle of the PWM. The softstart time is set by selecting a capacitor attached to the SS pin. The softstart pin can also be used for a hard shutdown, by pulling it to ground.

While the AC adapter is not present, the FAN5201 shuts itself off, using an UVLO set at 6.0V.

If the AC adapter is connected to the FAN5201 circuit but is not plugged in, the adapter could present a load to the battery. The FAN5201 prevents this by turning off Q2 (attached to the INISO pin) if the input current falls below 200mA (with an 18mΩ sense resistor). However, this function is disabled until the softstart pin reaches steady state.

Output Protection

If input current exceeds the design of the FAN5201 (6A with an 18mΩ sense resistor) the IC latches off Q1, disconnecting the circuitry from input power within a few microseconds.

If one AC adapter is connected when the battery is not present, the overcurrent limit does not disable the converter because Q1 acts as an inrush current limit.

If the battery voltage exceeds certain levels, internal protection in the battery may open. To prevent this, the FAN5201 latches off Q1, Q3 and Q4 if the output voltage exceeds approximately 110% of the setpoint.

The power converter is a synchronous buck for efficiency. This topology is actually two-quadrant, and could potentially draw current from the battery, boosting it high enough to override the AC adapter. To prevent this backfeed, the FAN5201 turns off the synchronous rectifier if the current into the battery drops below 200mA (with an 18mΩ sense resistor), utilizing instead the paralleled schottky.

If the internal overvoltage switch in the battery were to open due to a high charge current producing a high voltage (due to battery ESR), the voltage loop would take over. With the voltage loop in control, the battery switch would close, and the current could surge high until the current control loop comes out of saturation. The FAN5201 prevents this type of oscillation by means of a special loop controlling the error amplifier of the current loop.

Battery Conditioning

With switch B1 off (see Figure 5), the notebook load can be applied to the batteries even in the presence of the DC adapter. This permits deep discharge of the batteries as part of the battery conditioning process.

Battery Present

The presence of the battery can be detected by the host microcontroller.

Logic Section

The FAN5201 uses serial data to control its operation. The serial interface is compliant with the SMBus specification (see “System Management Bus Specification”, Rev. 1.08). Charger functionality is compatible with an extended subset of the Intel/Duracell Smart Charger Specification for a level 2 charger. The FAN5201 uses the SMBus Read-Word, Write-Word, and Block-Read protocols to communicate with the host system that monitors the battery. The FAN5201 never initiates communication on the bus; it only receives commands and responds to queries for status information. Figure 9 shows examples of the SMBus Write-Word and Read-Word protocols. Each communication with the FAN5201 begins with a start condition that is defined as a falling edge on SDA with SCL high. The device address follows the start condition. The FAN5201 device address is 0001001b (b indicates a binary number). Note that the address is only seven bits, and the binary representation uses R/W as its least significant bit.

Programming a µP Interface for the FAN5201

The µP programmer must bear in mind that the FAN5201 operates as a slave device to the host µP; all communications to the battery are *via* the host. Thus, in particular, the ChargingCurrent(), ChargingVoltage(), and AlarmWarning() commands (and thermistor signals for Ni based batteries) must all be passed to the µP. There is no way to send them directly to the charger.

Another important aspect for the programmer to be aware of is that at power-up, all of the internal registers of the FAN5201 are zeroed. Thus, in order to have the FAN5201 turn on, it is necessary to write to all of the DACs. It is also recommended to write to the Control Signals Word before writing to the DACs.

With these suggestions in mind, a possible flowchart for the µP interface to the FAN5201 would be as shown in Figure 3. In the first step, the battery charge requests are read; after this the FAN5201 can be programmed. First, the FAN5201 is left in Power Down until the programming has been successful. Next, Charging Power, Current, and Voltage are set; the FAN5201 will not operate until all three have been written. The µP next checks that all of the data has been correctly written; if not, the programming sequence is retried. Finally, the Power Down signal is turned off.

Application Schematics and BOMs

Figure 4 shows the FAN5201 in a single battery pack system. Figure 5 shows the FAN5201 in a two battery pack system. In a two battery system, the host microcontroller must poll to determine the state of each battery; and then a selector must control the switches. Figure 4 shows a typical Smart Battery system: for Ni based chemistries the temperature information is handled directly by the µC. The µC continuously monitors the SMBus; in case of communications breakdown the µC detects this and takes appropriate action. For a NiMH battery, a hardware overtemperature protection can be implemented using a comparator on the thermistor line, and turning the softstart pin off.

Notice that Q1 through Q4 are drawn with the associated intrinsic diode in Figure 4 and Figure 5.

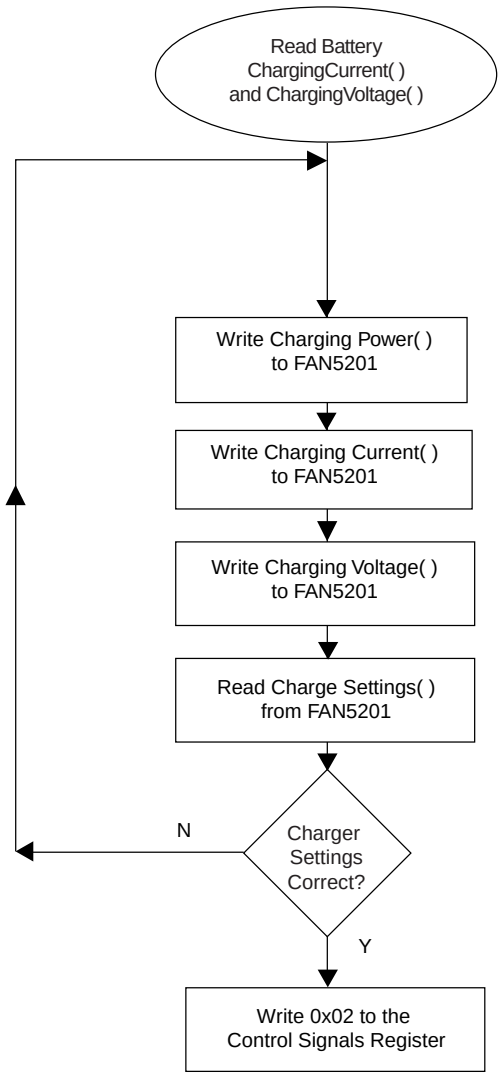


Figure 3. Suggested Flowchart for FAN5201 Startup

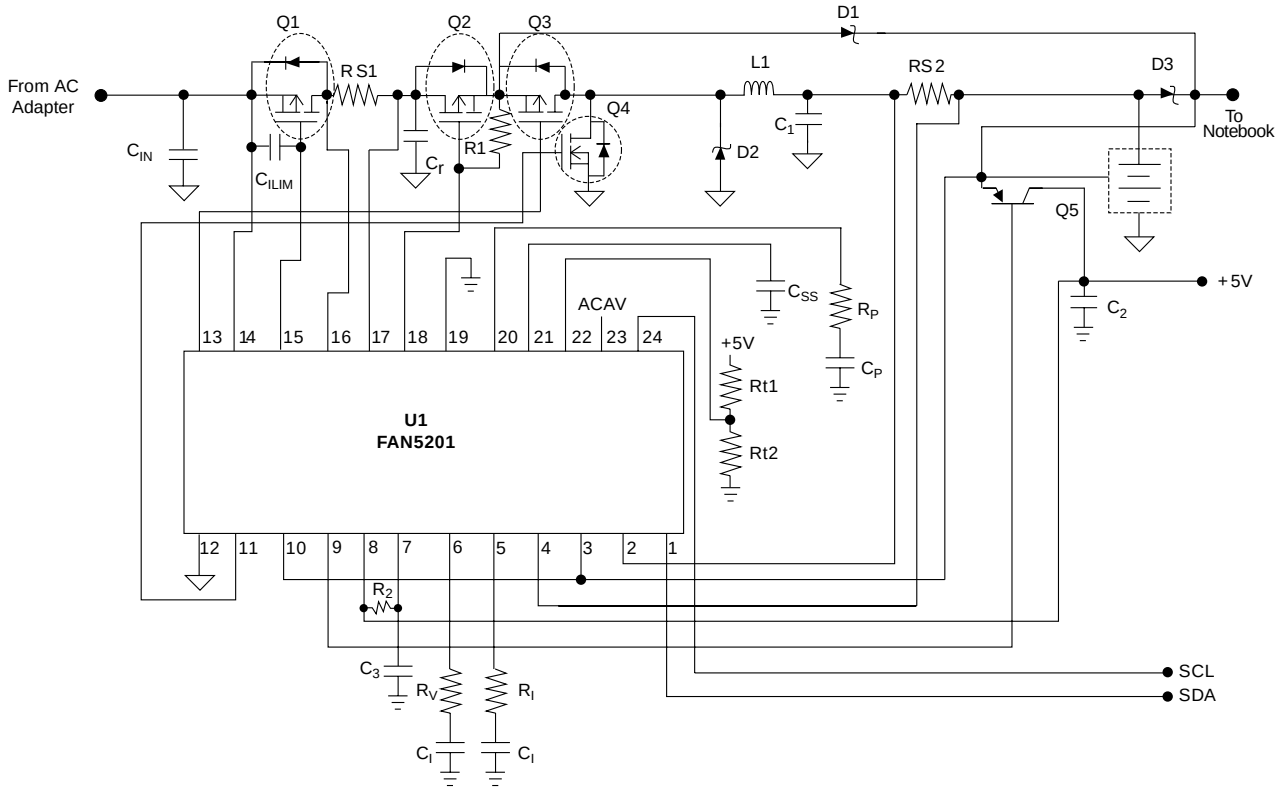


Figure 4. Single Battery Pack System

Table 1. Bill of Materials for Single Battery Pack System (8A maximum current)

Reference	Manufacturer	Manufacturer's P/N	Quantity	Description
C_V, C_I, C_{ILIM}			3	100nF 20% 50V Ceramic Chip Cap
C_1,C_r	AVX	TPSV107*020R0085	2	100µF 20V 85mΩ Tantalum Chip Cap
C_{SS}			1	10nF 20% 50V Ceramic Chip Cap
C2–3			2	10µF, 10V Tantalum Chip Cap
R_V			1	10KΩ 1% 1/10W
Rt1			1	9.09KΩ 1% 1/10W
Rt2, R_I			1	1KΩ 1% 1/10W
RS1-2	Dale	WSL-2512-R018	2	18mΩ 1W SM
R1			1	100KΩ 1/10W
C_P			1	970nF Ceramic Chip cap
R_P, R2			2	10Ω 1/10W
L1	Dale	IHSM-7832-5.6µH	1	5.6µH 6A 25mΩ SM Inductor
Q1-2	Fairchild	NDS8435A	2	30V 23mΩ SO8 P-channel
Q3	Fairchild	FDS9435A	1	30V 50mΩ SO8 P-channel
Q4	Fairchild	FDS6612A	1	30V 10mΩ SO8 N-channel
Q5		FZT704CT	1	100V 2A SOT223 PNP Darlington
D1-3	Motorola	MBRD835L	3	35V 8A Schottky
U1	Fairchild	FAN5201	1	SSOP24 Controller

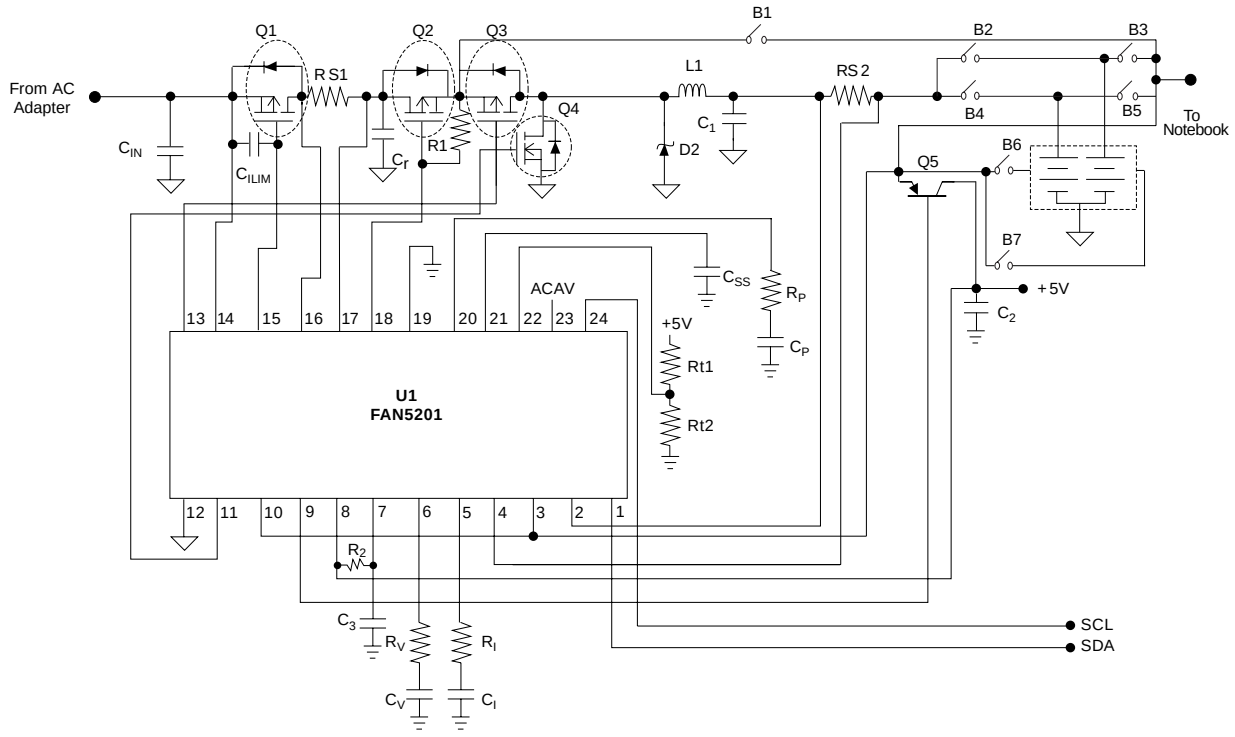


Figure 5. Two Battery Pack System

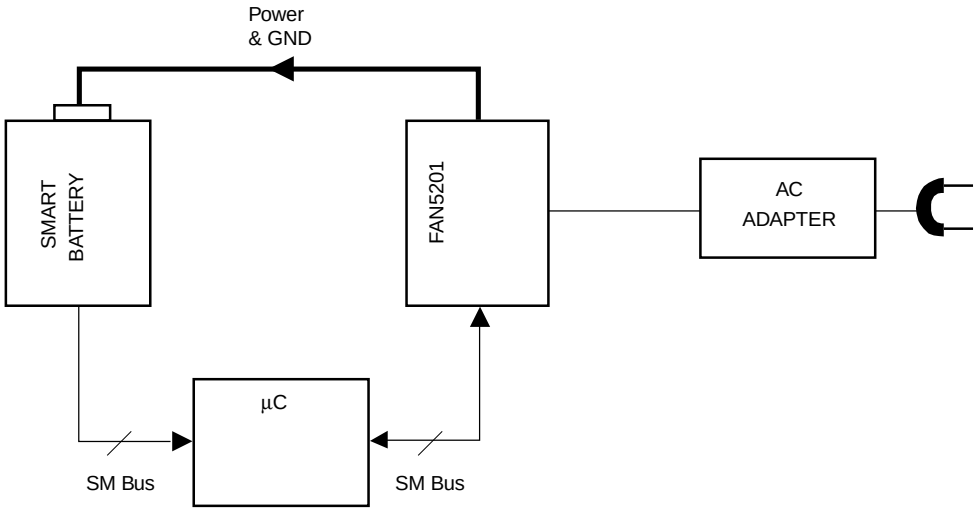


Figure 6. Typical Smart Battery System

SMBus Interface Specification

The FAN5201 is designed to fit in a system whose center is a microcontroller acting as an SMBus host. The host receives charging requests and other signals from a Smart Battery, and sends charging requests to the FAN5201 charger, in the process providing the necessary translations. The FAN5201 acts as a slave only. There is no direct communication between the charger and the battery. Note that the FAN5201 is NOT intended to be fully compliant with the Intel/Duracell Smart Battery System Specification. This document specifies ALL of the FAN5201's SMBus interface.

Slave Address

0001001b

Power On

The FAN5201 powers on with all DACs set to zero. All DACs must be written to before charging can begin. At power on, the Zero Current Bit is 0.

Supported Communications—Write Section (µC to IC)

Charging Current

The host sends the desired charging rate in mA.

- SMBus Protocol: Write Word
- Command Code: 0x14

Table 2. Charging Current Input and Output

Input	
Unsigned 2-Byte	Desired Charging Current
Units	mA
LSB	Bit 5
MSB	Bit 12
Output	
Scale	255 Steps (from 0 to full-scale)
Resolution	32mA (with 18mΩ sense resistor)

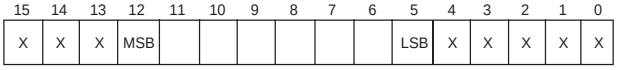


Figure 7. Charging Current Input and Output Word

For example, 0x0200 sets a charge current of 512mA by outputting (16/255) * FS, where FS = 8160mA.

Charging Voltage

The host sends the desired charging voltage in mV with an offset of 10V.

- SMBus Protocol: Write Word
- Command Code: 0x15

Table 3. Charging Voltage Input and Output

Input	
Unsigned 2-Byte	Desired Charging Voltage
Units	mV
LSB	Bit 5
MSB	Bit 12
Output	
Scale	255 Steps (from 0 to full-scale)
Resolution	32mV

Figure 8. Charging Voltage Input and Output Word

For example, 0x0200 sets a charging voltage of 10.512V by outputting (16/255) * FS +10V, where FS = 8.160V.

Charging Power

The host sends the maximum power available from the AC adapter in 5W increments with an offset of 25W.

- SMBus Protocol: Write Word
- Command Code: 0x17

Table 4. Charging Power Input and Output

Input	
Unsigned 2-Byte	Maximum Charging Power
Units	5W
LSB	Bit 0
MSB	Bit 3
Output	
Scale	15 Steps (from 0 to full-scale)
Resolution	5W (with 18mΩ sense resistor)

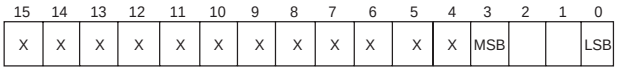


Figure 9. Charging Power Input and Output Word

For example, 0x0005 sets maximum charge power at 50W by outputting (5/15) * FS +25W, where FS = 75W.

Control Signals

The host sends a signal to set the IC into power down mode, and to reset the zero current flag.

When Power Down is sent to the IC, only the 5V linear regulator and the SMBus are on, all other systems are turned off.

The SMBus continues to latch incoming information in Power Down.

Zero Current Reset true (=1) resets the ZERO_CURRENT bit (in the charger status word) to 0 = valid. In order for the ZERO_CURRENT bit to function again, the Zero Current Reset bit must be set false (= 0) after this, otherwise the ZERO_CURRENT bit will remain in the valid state regardless of battery current.

- SMBus Protocol: Write Word
- Command Code: 0x18

Table 5. Control Signals

Field	Bit	Support
Power Down/Normal	1	0/1
Zero Current Reset	2	1 = TRUE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	ZCR	PD	X

Figure 10. Control Signals Word

For example, 0x0006 sets the IC in normal operation, and the zero current bit is reset.

Supported Communications—Read Section (µC to IC)

Charger Status

The host uses this command to read the charger's status bits.

VOLTAGE_NOTREG is set if the battery voltage is outside +10% of the programmed charging voltage.

CURRENT_NOTREG is set if the battery current is outside +10% of the programmed charging current.

ZERO_CURRENT is zero if the battery current is less than 200mA (with an 18mΩ sense resistor).

CURRENT_OR is zero if the battery current is >6A.

VOLTAGE_OR is zero if the battery voltage is >110% of the programmed charging voltage.

POWER_FAIL is set if the battery voltage is <8.5V.

- SMBus Protocol: Read Word
- Command Code: 0x13

Table 6. Charger Status Read

Field	Bit	Support
CHARGE_INHIBITED	0	Always 0, charger enabled
MASTER_MODE	1	Always 0, slave mode
VOLTAGE_NOTREG	2	0 = in regulation
CURRENT_NOTREG	3	0 = in regulation
LEVEL_2/3	4	Not supported
ZERO_CURRENT	5	0 = valid
CURRENT_OR	6	0 = valid
VOLTAGE_OR	7	0 = valid
THERMISTOR_OR	8	Not supported
THERMISTOR_COLD	9	Not Supported
THERMISTOR_HOT	10	Not Supported
THERMISTOR_UR	11	Not Supported
ALARM_INHIBITED	12	Not Supported
POWER_FAIL	13	0 = Voltage OK
BATTERY_PRESENT	14	Not Supported
AC_PRESENT	15	Always 1, charger present

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	X	0/1	X	X	X	X	X	0/1	0/1	0/1	X	0/1	0/1	0

Figure 11. Charger Status Word

For example, a normal operation charger might set this word to 0x8028 to show that the AC adapter is present, power is on, voltage is being regulated, and current is above minimum.

Charger Settings

The host uses this command to read the charger's settings.

- SMBus Protocol: Block Read
- Command Code: 0x3F

Table 7. Charger Settings Read

Field	Byte
Byte Count	Always set to 0x08
Charger Current Low Byte	1
Charger Current High Byte	2
Charger Voltage Low Byte	3
Charger Voltage High Byte	4
Charger Power Low Byte	5
Charger Power High Byte	6
Control Signal Low Byte	7
Control Signal High Byte	8

Non-Supported Communications

The following features are specified in the Intel/Duracell Smart Charger Specification, but are not directly supported by the FAN5201.

Thermistor Interface

Interface to the thermistor occurs exclusively through the host.

Typical Battery Communications

Charging current and voltage requests are intercepted by the host, which transmits them to the charger.

Critical Battery Communications

Overcharge and overtemperature communications are sent to the host, which transmits commands to the charger.

Bus Errors

Unsupported commands, data unavailable, busy or bad data are not transmitted to the host. The FAN5201 signals errors by witholding ACKnowledge (see protocols). It does not support any reads of error registers.

AlarmWarnings()

Alarm warnings are sent to the host, which transmits commands to the charger.

Chargermode() Settings

The ChargerMode() write command is unsupported. The command's effects may be obtained by sending the appropriate commands to the charger.

175 seconds Timeout

Supported by the host, not by the IC. Furthermore, it is recommended that a watchdog timer be used in conjunction with the host processor, to assure that the timeout is not affected by infinite software loops.

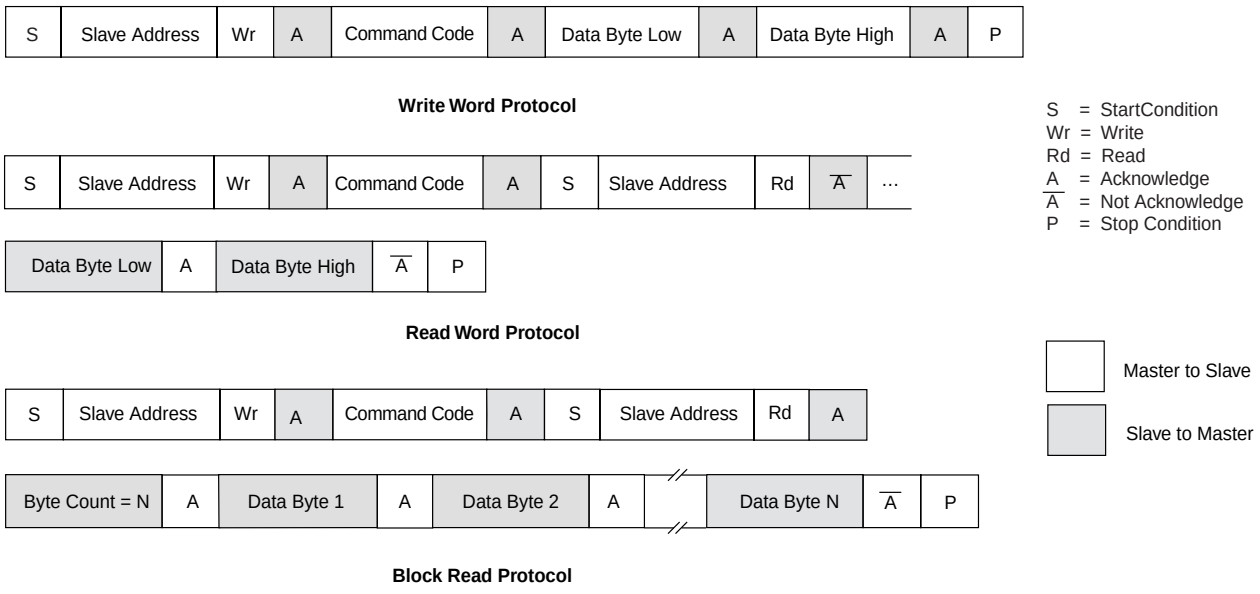


Figure 12. Read and Write Protocols

Timing Diagram

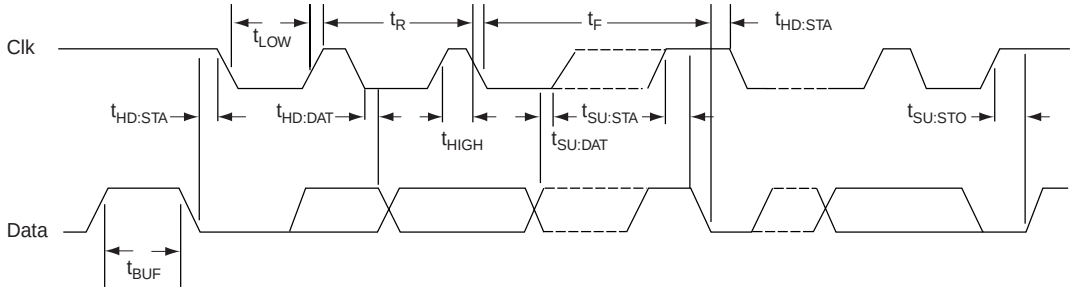


Figure 13. SMBus Timing Diagram

Preliminary Specification

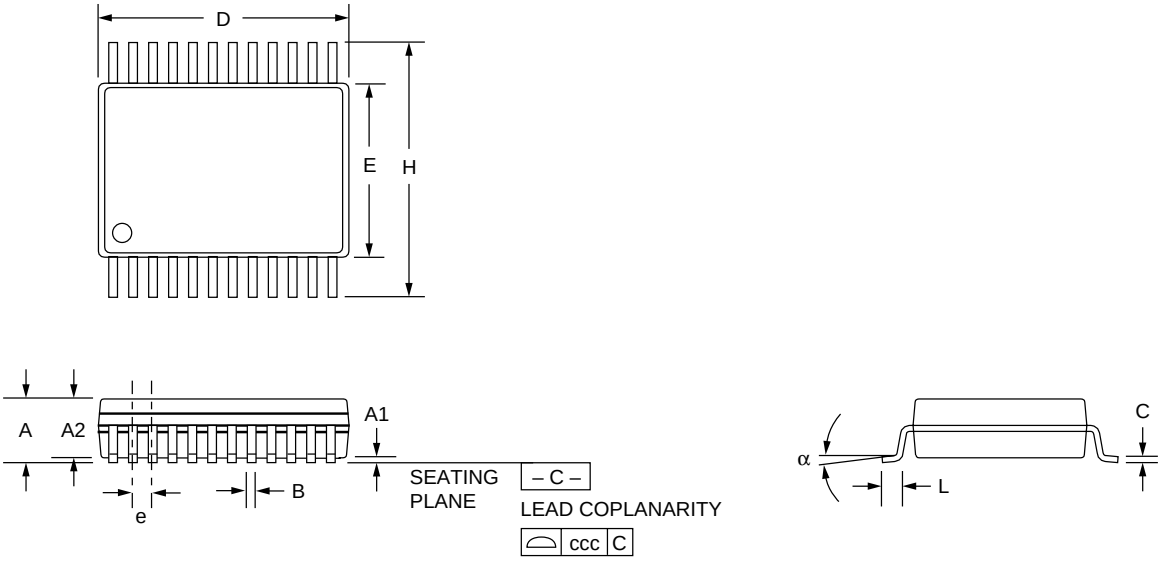
Mechanical Dimensions

24-Lead SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.078	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.010	.015	0.22	0.38	5
c	.0035	.010	0.09	0.25	5
D	.311	.335	7.90	8.50	2, 4
H	.291	.323	7.40	8.20	
E	.197	.220	5.00	5.60	2
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Preliminary Specification

Ordering Information

Product Number	Package
FAN5201MSA	24 Lead SSOP

Preliminary Specification

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAN8024D (KA3024D)

4-CH Motor Drive IC

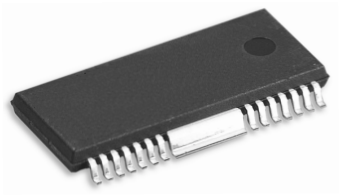
Features

- 2-Channel BTL driver with current feedback
- 2-Channel BTL DC motor driver
- Built-in thermal shutdown circuit
- Built-in mute circuit
- Operating supply voltage: 4.5~13.2V
- Corresponds to 3.3V or 5V DSP

Description

The FAN8024D is a monolithic IC, suitable for a 2-ch BTL DC motor driver and a 2-ch motor driver with current feedback which drives the focus and tracking actuator of a CD-media system.

28-SSOPH-375

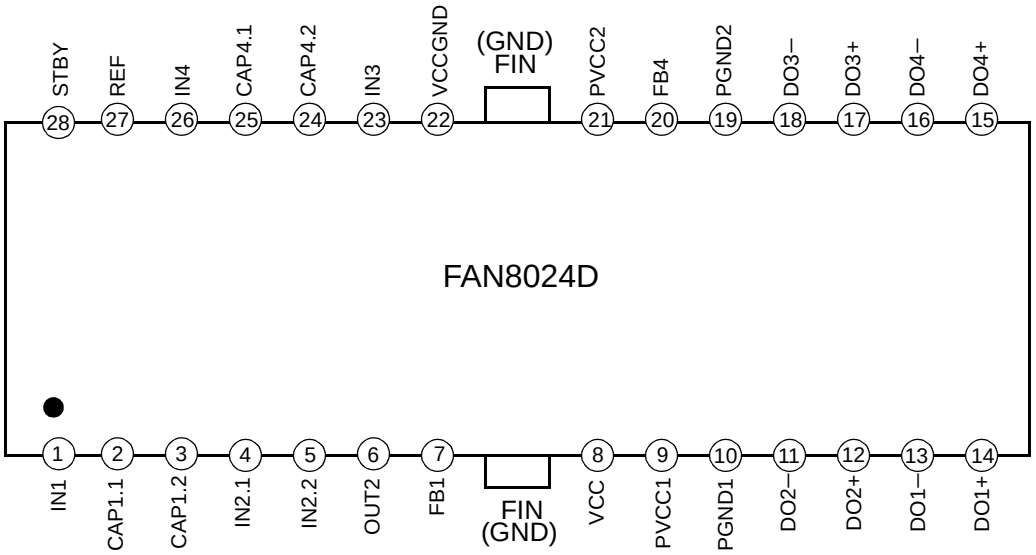


DC MOTOR DRIVE IC

Typical Applications

- Compact disk ROM
- Compact disk RW
- Digital video disk ROM
- Digital video disk RW
- Other compact disk media

Pin Assignments

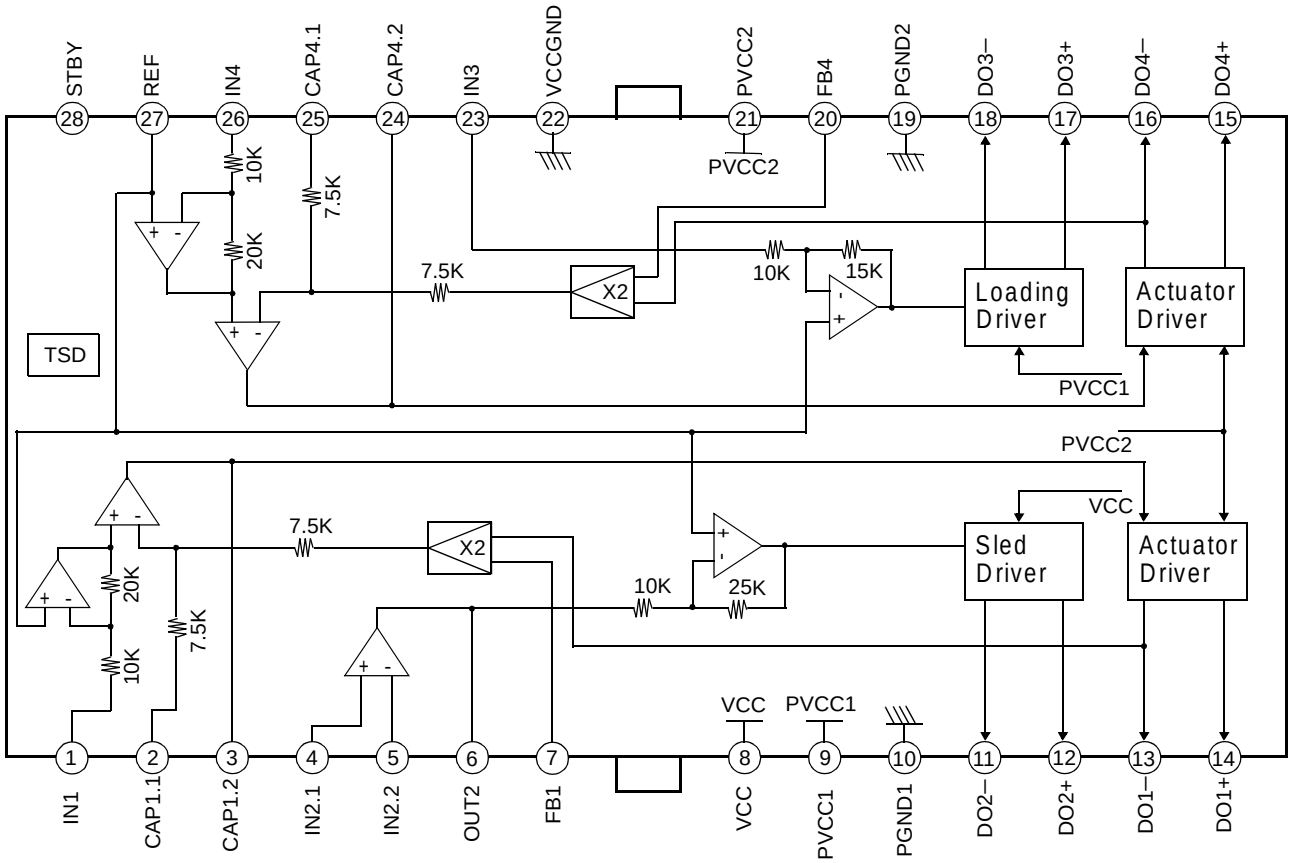


DC MOTOR DRIVE IC

Pin Definitions

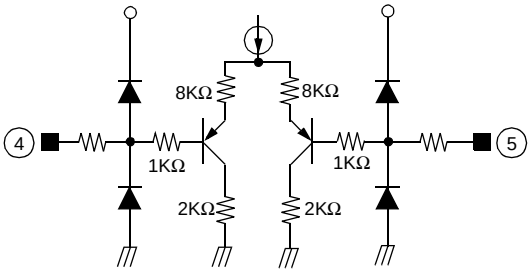
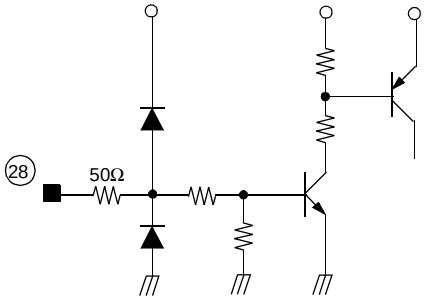
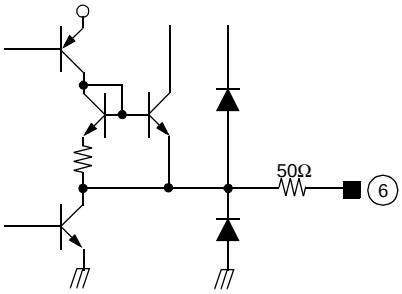
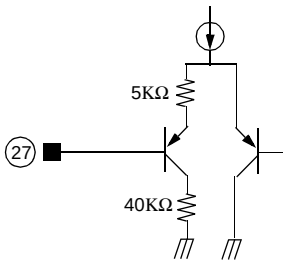
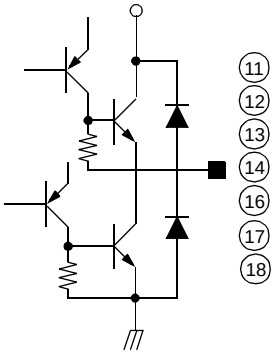
Pin Number	Pin Name	I/O	Pin Function Description
1	IN1	I	CH1 input
2	CAP1.1	-	Connection with capacitor
3	CAP1.2	-	for CH1
4	IN2.1	I	OP-AMP CH2 input(+)
5	IN2.2	I	OP-AMP CH2 input(-)
6	OUT2	O	OP-AMP CH2 output
7	FB1	I	Feedback for CH1
8	VCC	-	Signal Vcc
9	PVCC1	-	Power Supply 1
10	PGND1	-	Power Ground 1
11	DO2–	O	Drive2 Output (-)
12	DO2+	O	Drive2 Output (+)
13	DO1–	O	Drive1 Output (-)
14	DO1+	O	Drive2 Output (+)
15	DO4+	O	Drive4 Output (+)
16	DO4–	O	Drive4 Output (-)
17	DO3+	O	Drive3 Output (+)
18	DO3–	O	Drive3 Output (-)
19	PGND2	-	Power Ground 2
20	FB4	-	Feedback for CH4
21	PVCC2	-	Power Supply 2
22	VCCGND	-	Vcc ground
23	IN3	I	CH3 input
24	CAP4.2	-	Connection with capacitor
25	CAP4.1	-	for CH4
26	IN4	I	CH4 input
27	REF	I	Bias voltage input
28	STBY	I	Stand-by input

Internal Block Diagram



DC MOTOR DRIVE IC

Equivalent Circuits

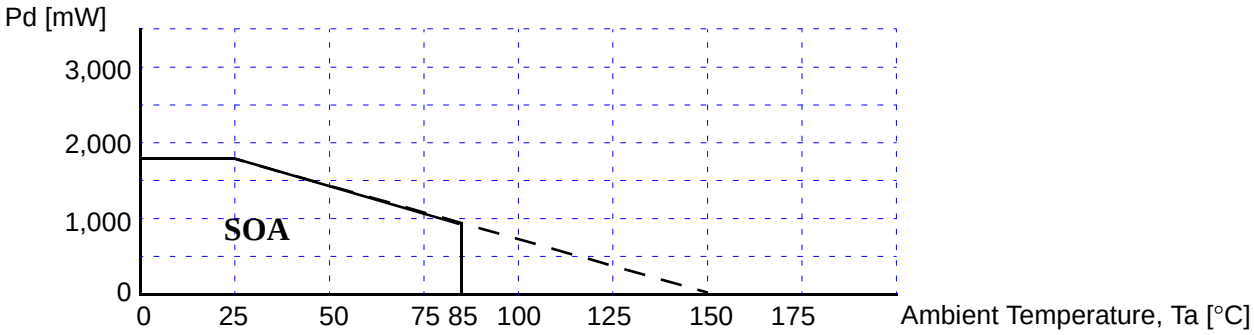
ERROR AMP INPUT	STAND-BY INPUT
	
ERROR AMP OUTPUT	**SIGNAL REFERENCE INPUT**
	
POWER AMP OUTPUT	
	

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V_{CCmax}	15	V
Power dissipation	P_D	@1.7	W
Operating temperature range	T_{OPR}	-35 ~ +85	°C
Storage temperature range	T_{STG}	-55 ~ +150	°C

Notes:

1. When mounted on a 50mm × 50mm × 1mm PCB (Phenolic resin material).
2. Power dissipation reduces 13.6mW/°C for using above Ta = 25°C
3. Do not exceed P_D and SOA(Safe operating area).



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{cc}	4.5	-	13.2	V

Electrical Characteristics

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 12V, $PV_{CC}1,2$ = 5V & the other conditions & nomenclatures follow the test circuit)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Quiescent Current1	I_{CC1}	Stand-by off	-	18	27	mA
Quiescent Current1	I_{CC2}	Stand-by on	-	-	0.5	mA
Stand-by On Voltage	V_{STon}		-	-	0.5	V
Stand-by Off Voltage	V_{SToff}		2.0	-	-	V
ACTUATOR DRIVE PART						
Output Offset Current	$I_{OO1,4}$	VIN1,4 set to BIAS	-6	0	+6	mA
Maximum Output Voltage1	$V_{OM1,4}$	VIN1,4 = 4.5V	3.6	4.0	-	V
Transconductance	$G_{M1,4}$	VIN1,4 = 100mVp-p, f=1kHz	1.5	1.7	1.9	A/V
PRE OP–AMP (SLED DRIVER)						
Common mode Input Range	V_{OOM}	SW1 & SW2 set to position 2, VIN2 sweep from 0V to 12V	0	-	11.0	V
Input Bias Current	I_B	SW1 & SW2 set to position 1	-300	-30	-	nA
Low Level Output Voltage	V_{OL}	SW1=>posit. 2, SW2=>posit. 1 VIN2 is 2.0V & VIN5 is 3.0V	-	0.1	0.3	V
Output Source Current	I_{SOURCE}	SW1 set to position 2 SW2 & SW3 set to position 1 VIN2 is 3.0V & VIN5 is 2.0V	1	4	-	mA
Output Sink Current	I_{SINK}	SW3 set to position 2 VIN2 is 2.0V & VIN5 is 3.0V	5	10	-	mA
SLED DRIVE PART						
Output Offset Voltage of Input OP-Amp	V_{OF2}	SW1=>posit. 2, SW2=>posit. 1 VIN 2 & VIN5 set to BIAS	-100	0	+100	mV
Maximum Output Voltage2	V_{OM2}	SW1 & SW2 set to position 2 VIN2 set to 4.5V	10.0	10.9	-	V
Closed loop Voltage Gain1	G_{VLO2}	VIN2 = 100mVp-p, f=1kHz SW2 & SW1 set to position 2	18.0	20.0	22.0	dB
Loading DRIVE PART						
Output Offset Voltage1	V_{OF3}	VIN3 set to BIAS	-50	0	50	mV
Maximum Output Voltage 3	V_{OM3}	VIN3 set to 4.5V	3.6	4.0	-	V
Closed loop Voltage Gain 2	G_{VLO3}	VIN3 = 100mVp-p, f=1KHz	13.5	15.5	17.5	dB

Application Information

1. REFERENCE INPUT & STAND-BY FUNCTION

- Reference input (PIN 27)
  The applied voltage at the reference input pin must be between 1.4V and 6.5V, when V_{CC}=8.5V.
- Stand-by input (PIN 28)
  The following input conditions must be satisfied for the normal stand-by function.

Stand-by input voltage	Below 0.5V or OPEN	Stand-by function is activated so the bias block and the power block are disabled
Stand-by input voltage	Above 2.0V	Normal operation

2. PROTECTION FUNCTION

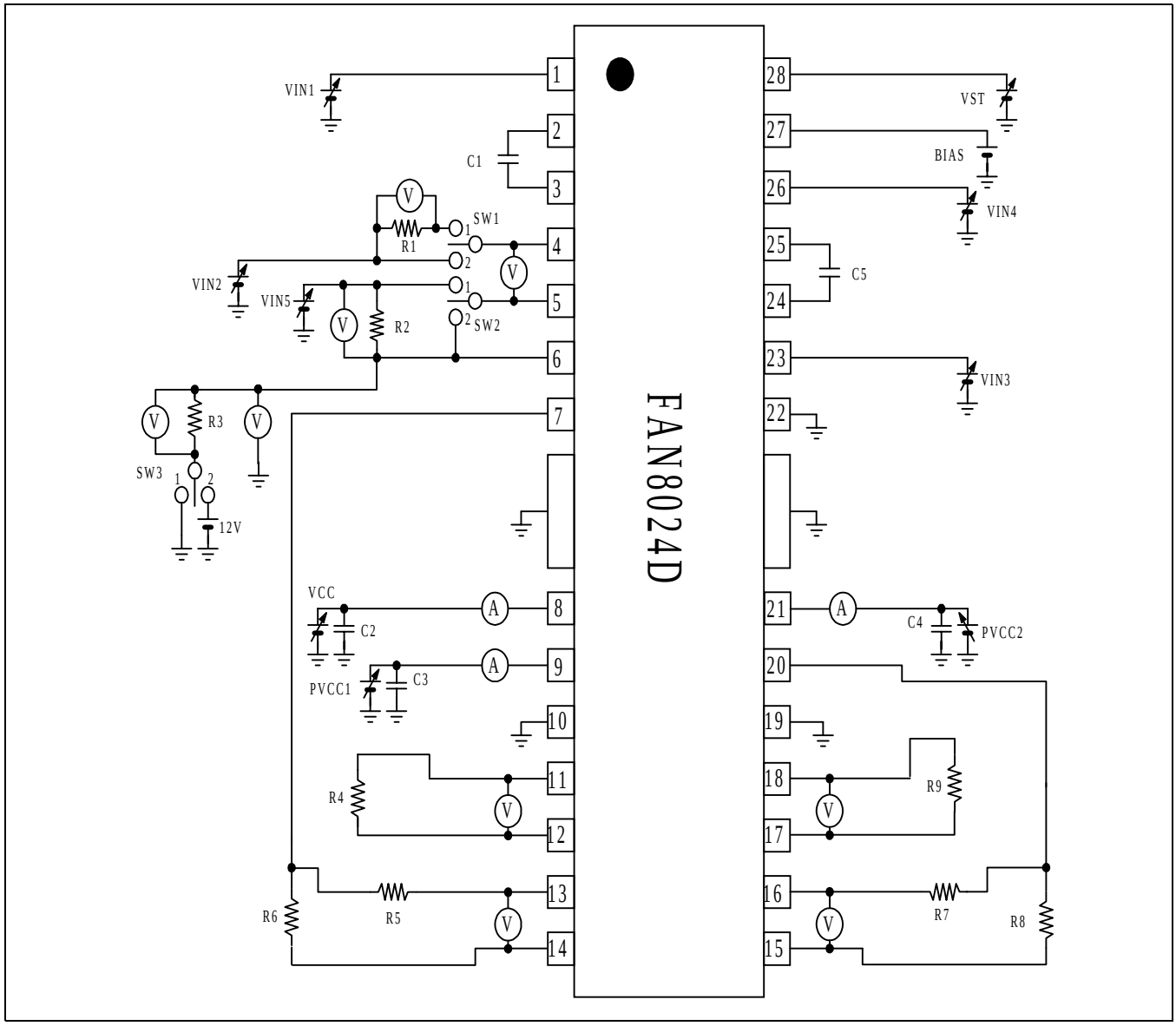
Thermal shutdown (TSD)

If the chip temperature rises above 175°C, the thermal shutdown (TSD) circuit is activated and the output circuit is in the mute state, that is off state. The TSD circuit has a temperature hysteresis of 25°C

3. SEPARATION OF POWER SUPPLY

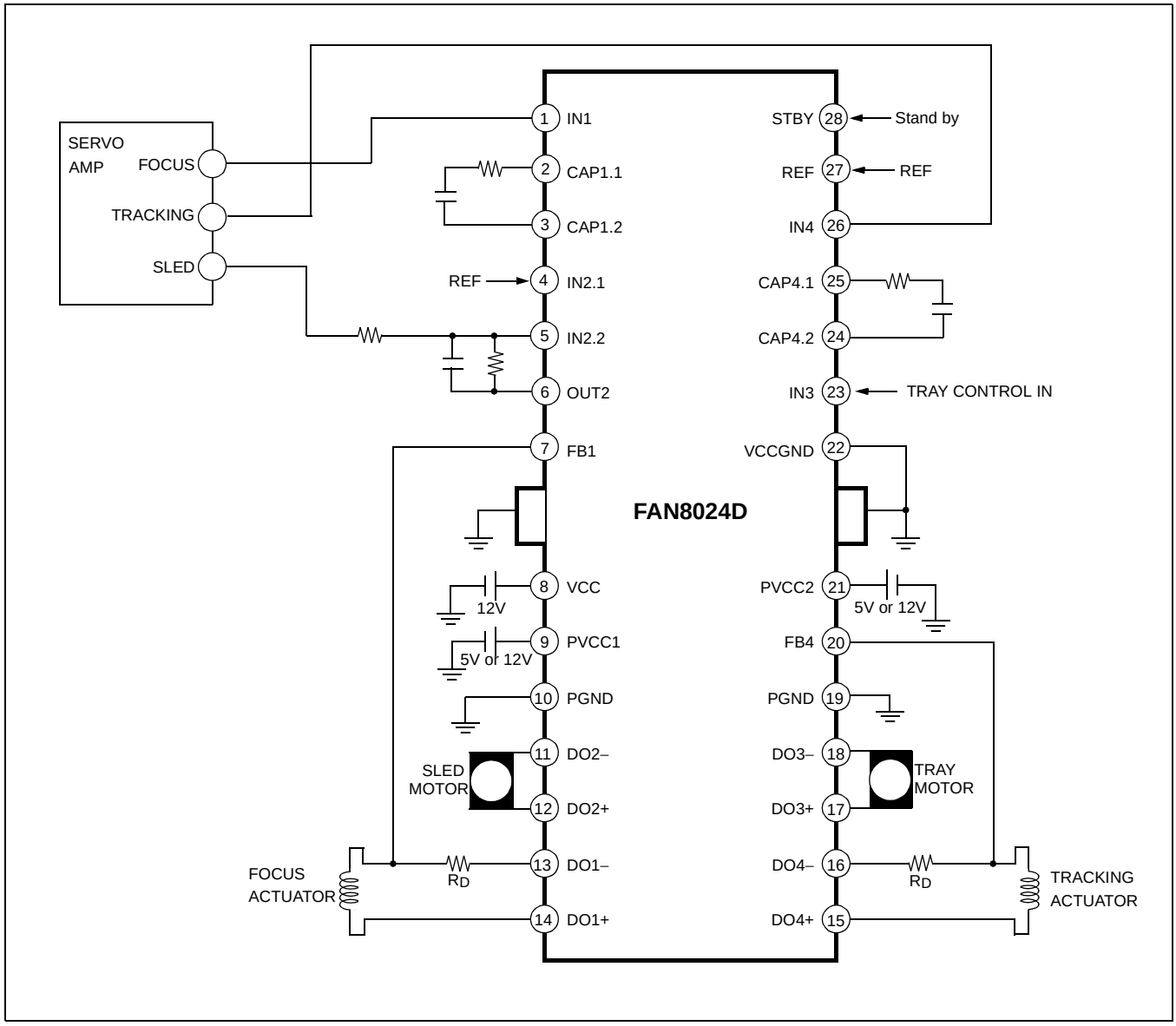
- PV_{cc1} (PIN 9)
  PV_{cc1} is the power for loading driver. The range is between 5V ~ 12V.
- PV_{cc2} (PIN 21)
  PV_{cc2} is the power supply for actuator driver that include focus and tracking actuator. The range is between 5V ~ 12V
- V_{cc} (PIN 8)
  V_{cc} pin supplies power for sled driver and signal logic part. The voltage applied to V_{cc} must be higher than PV_{cc1} and PV_{cc2} at least 1V

Test Circuits



Symbol	Value	Symbol	Value	Symbol	Value
R1	1MΩ	R6	5Ω	C2	10uF
R2	1MΩ	R7	4Ω	C3	10uF
R3	50Ω	R8	5Ω	C4	10uF
R4	8Ω	R9	8Ω	C5	100pF
R5	4Ω	C1	100pF	BIAS	2.5V

Typical Application Circuits



Ordering Information

Device	Package	Operating Temp.
FAN8024D	28-SSOPH-375	-35 °C ~ 85 °C
FAN8024DTF	28-SSOPH-375	-35 °C ~ 85 °C

DC MOTOR DRIVE IC

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAN8026D (KA3026D)

4-CH Motor Drive IC

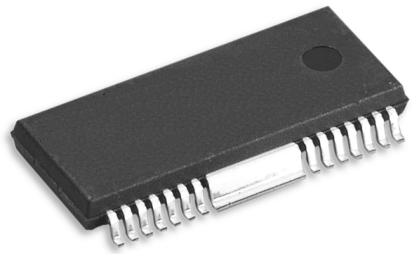
Features

- 3-Channel BTL driver
- 1-Channel forward-Reverse control DC motor driver
- Built-in thermal shutdown circuit
- Built-in mute circuit
- Operating supply voltage: 4.5~13.2V
- Corresponds to 3.3V or 5V DSP

Description

The FAN8026D is a monolithic integrated circuit, suitable for a 1-ch (forward.reverse) control DC motor driver and a 3-ch motor driver which drives the focus actuator,tracking actuator, and sled motor of a CD system.

28-SSOPH-375

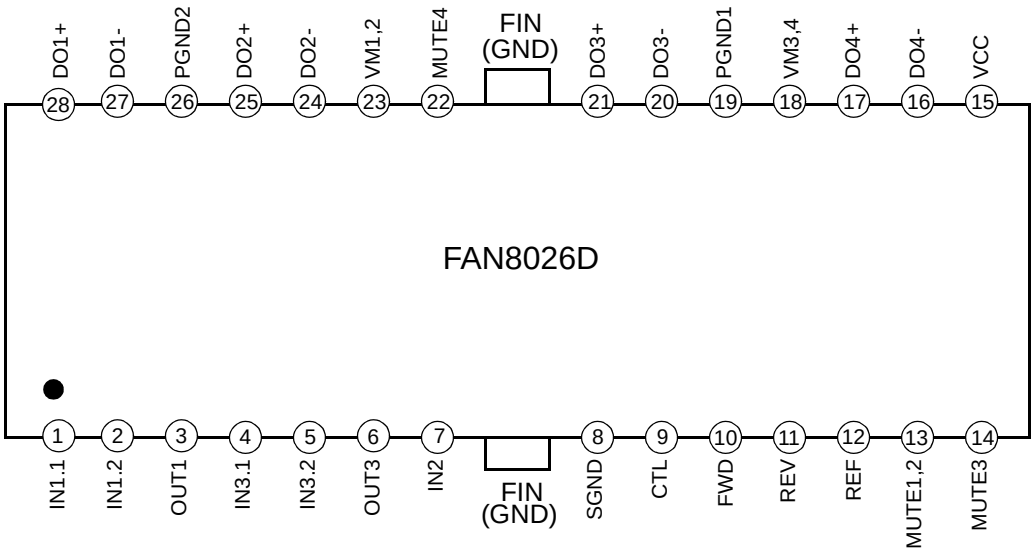


DC MOTOR DRIVE IC

Typical Applications

- Compact disk player
- Digital video disk player
- Mini disk player

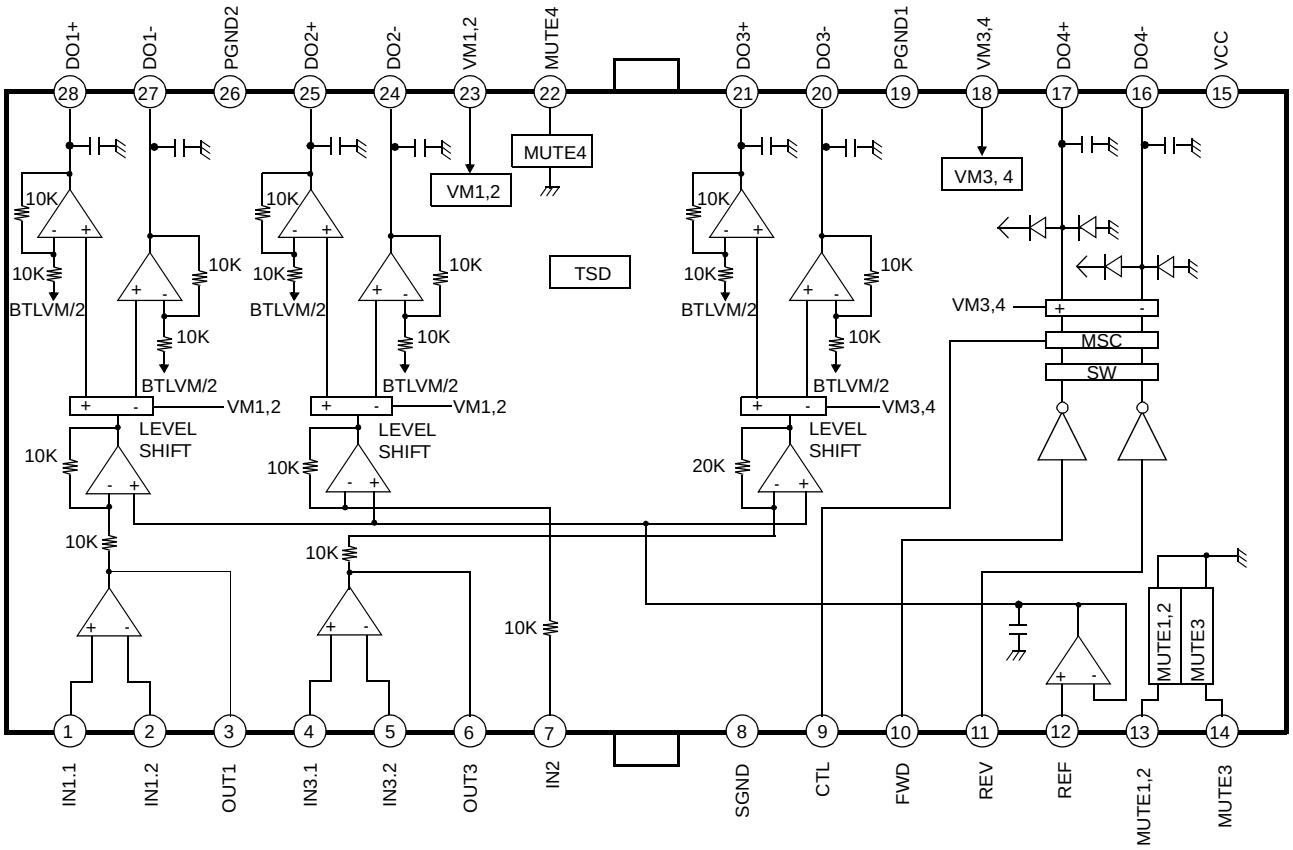
Pin Assignments



Pin Definitions

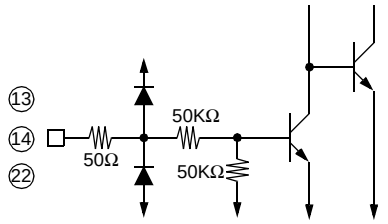
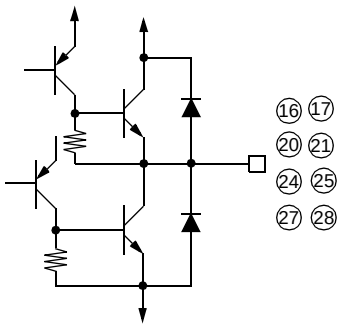
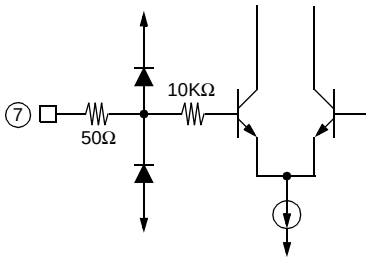
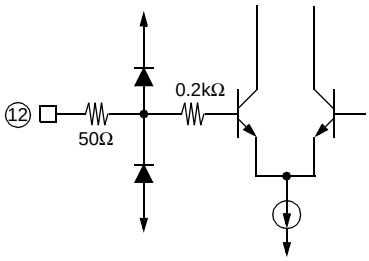
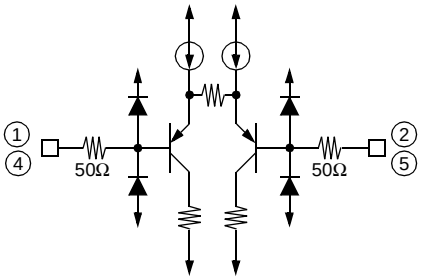
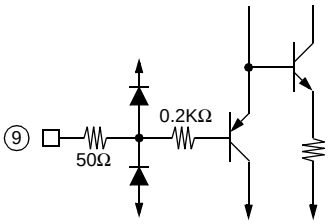
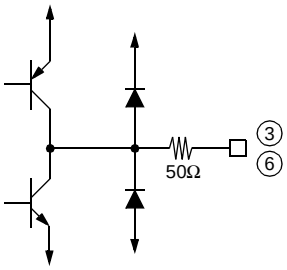
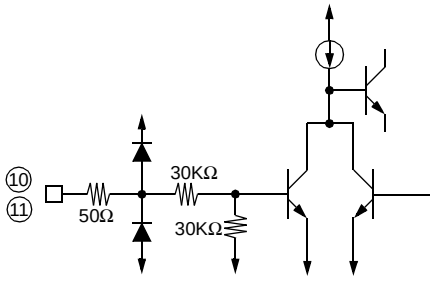
Pin Number	Pin Name	I/O	Pin Function Descrition
1	IN1.1	I	OP-AMP CH1 Input (+)
2	IN1.2	I	OP-AMP CH1 Input (-)
3	OUT1	O	OP-AMP CH1 Output
4	IN3.1	I	OP-AMP CH3 Input (+)
5	IN3.2	I	OP-AMP CH3 Input (-)
6	OUT3	O	OP-AMP CH3 Output
7	IN2	I	OP-AMP CH2 Input
8	SGND	-	Signal Ground
9	CTL	I	CH4 Motor Speed Control
10	FWD	I	CH4 Forward
11	REV	I	CH4 Reverse
12	REF	I	Bias Voltage Input
13	MUTE1,2	I	CH1, 2 Mute
14	MUTE3	I	CH3 Mute
15	V_{CC}	-	Signal V_{CC}
16	DO4-	O	Drive4 Output (-)
17	DO4+	O	Drive4 Output (+)
18	VM3, 4	-	BTL CH3, 4 Power V_{CC}
19	PGND1	-	CH3, 4 Power Ground
20	DO3-	O	Drive3 Output (-)
21	DO3+	O	Drive3 Output (+)
22	MUTE4	-	CH4 Mute
23	VM1,2	-	BTL CH1, 2 Power V_{CC}
24	DO2-	O	Drive2 Output (-)
25	DO2+	O	Drive2 Output (+)
26	PGND2	-	CH1,2 Power Ground
27	DO1-	O	Drive1 Output (-)
28	DO1+	O	Drive1 Output (+)

Internal Block Diagram



DC MOTOR DRIVE IC

Equivalent Circuits

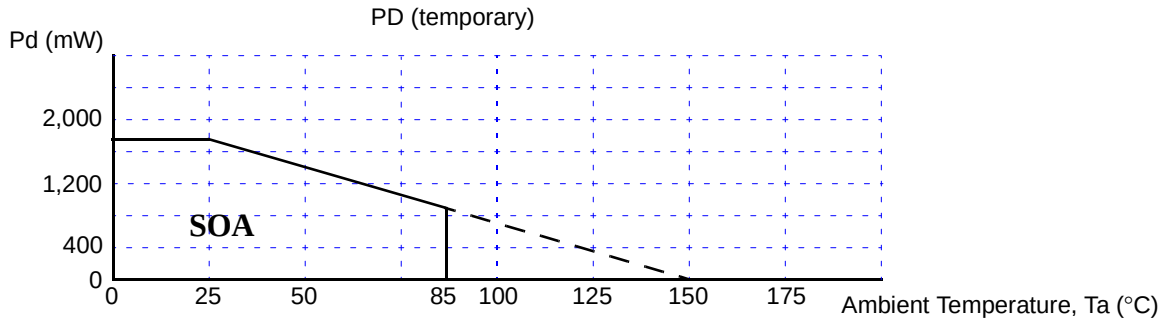
MUTE INPUT	POWER OUTPUT
	
CH2 LEVEL SHIFT INPUT	**SIGNAL REFERENCE INPUT**
	
ERROR AMP INPUT	**LOADING CONTROL INPUT**
	
ERROR AMP OUTPUT	**LOADING LOGIC INPUT**
	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V_{CCmax}	15	V
Power dissipation	P_d	1.7	W
Operating temperature range	T_{opr}	-35 ~ +85	°C
Storage temperature range	T_{stg}	-55 ~ +150	°C

Notes:

1. When mounted on a 50mm × 50mm × 1mm PCB (Phenolic resin material).
2. Power dissipation reduces 13.6mW/°C for using above Ta = 25°C
3. Do not exceed Pd and SOA(Safe operating area).



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	-	13.2	V

Electrical Characteristics

(Unless otherwise specified, Ta = 25 °C, V_{CC} = VM1,2 = VM3,4 = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Quiescent Current	I_{CC}	Vin = 0V	-	8	12	mA
CH Mute On Current	$Imute_{CH}$	Pin 13, Pin14, Pin22 = GND	-	1	3	mA
CH Mute On Voltage	$Vmon_{CH}$	Pin13, Pin14, Pin22 = Variation	-	-	0.5	V
CH Mute Off Voltage	$Vmoff_{CH}$	Pin13, Pin14, Pin22 = Variation	2	-	-	V
DRIVE PART						
Input Offset Voltage	Vio		-20	-	+20	mV
Output Offset Voltage	Voo	Vin = 2.5V	-40	-	+40	mV
Maximum Output Voltage1	Vom1	Vcc=8V, RL = 8Ω (CH1, 2)	4	5.7	-	V
Maximum Output Voltage2	Vom2	Vcc=12V, RL = 24Ω (CH3)	7	9	-	V
Closed Loop Voltage Gain1	Gvc1	f = 1KHz, Vin = 0.1Vrms (CH1, 2)	10.5	12	13.5	dB
Closed Loop Voltage Gain2	Gvc2	f = 1KHz, Vin = 0.1Vrms (CH3)	16	18	20	dB
Ripple Rejection Ratio	RR	Vin = 0.1Vrms, f = 120Hz	-	60	-	dB
Slew Rate	SR	Vo = 2Vp-p, f = 120KHz	-	0.8	-	V/us
ERROR OP AMP PART						
Input Offset Voltage	Vofop		-10	-	+10	mV
Input Bias Current	Ibop		-	-	300	nA
High Level Output Voltage	Vohop	Vcc=8V	7.2	7.6	-	V
Low Level Output Voltage	Volop	Vcc=8V	-	0.2	0.5	V
Output Sink Current	Isink	RL = 1KΩ	2	4	-	mA
Output Source Current	Isource	RL = 1KΩ	2	4	-	mA
Open Loop Voltage Gain	Gvo	Vin = -75dB, f = 1KHz	-	75	-	dB
Ripple Rejection Ratio	RRop	Vin = -20dB, f = 120Hz	-	65	-	dB
Slew Rate	Srop	f = 120KHz, 2Vp-p	-	1	-	V/us
Common Mode Rejection Ratio	CMRR	Vin = -20dB, f = 1KHz	-	80	-	dB
Common Mode Input Range	Vicm		-0.3	-	4.5	V
TRAY DRIVE PART (VCC = VM34 = 8V, RL = 45Ω)						
Input High Level Voltage	Vih		2	-	-	V
Input Low Level Voltage	Vil		-	-	0.5	V
Output Voltage1	Vo1	Vcc=8V, Vctl = 6V	5.2	6.0	6.8	V
Output Voltage2	Vo2	Vcc=13V, Vctl = 8.5V	7.5	8.5	9.5	V
Output Load Regulatoin	ΔV_{RL}	Vctl = 3.5V	-	300	700	mV
Output Offset Voltage1	Voo1	Vin = 5V, 5V	-10	-	+10	mV
Output Offset Voltage2	Voo2	Vin = 0V, 0V	-10	-	+10	mV

Application Information

1. REFERENCE INPUT

Pin 12 (REF) is a reference Input pin.

1) Reference Input
The applied voltage at the reference input pin must be between 1.5 (V) and 6.5 (V), when Vcc = 8V.

2. SEPARATED CHANNEL MUTE FUNCTION

These pins are used for individual channel mute operation.

1) When the mute pins (pin13,14 and 22) are Low level, the mute circuits are enabled and the output circuits are muted.

2) When the voltage of the mute pins (pin13,14 and 22) are High level, the mute circuits are disabled and the output circuits operate normally.

3) If the chip temperature rises above 175 °C, then the thermal shutdown (TSD) circuit is activated and the output circuits are muted.
Mute1, 2 (pin13) - CH1, 2 mute control input pin.
Mute3 (pin14) - CH3 mute control input pin.
Mute4 (pin22) - CH4 mute control input pin.

3. PROTECTION FUNCTION

Thermal Shutdown (TSD)

1) If the chip temperature rises above 175 °C the thermal shutdown (TSD) circuit is activated and the output circuit is in the Mute state, that is Off state.
The TSD circuit has a temperature hysteresis of 25 °C.

4. FOCUS, TRACKING ACTUATOR, SLED MOTOR DRIVE PART

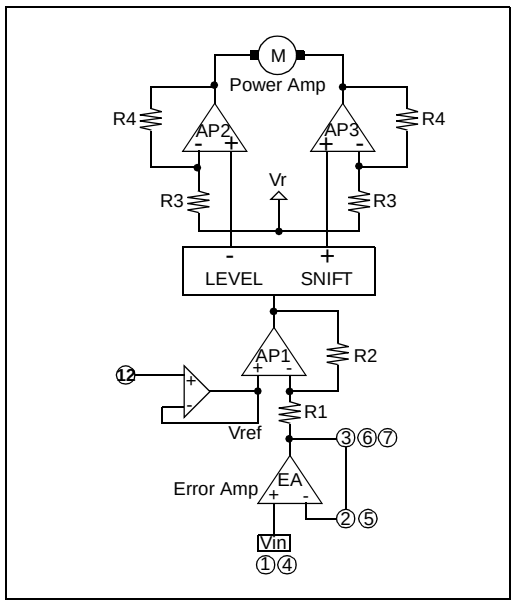
1) The reference voltage REF is given externally through pin 12.

2) The error amp output signal is amplified by R2/R1 times and then fed to the level shift circuit.

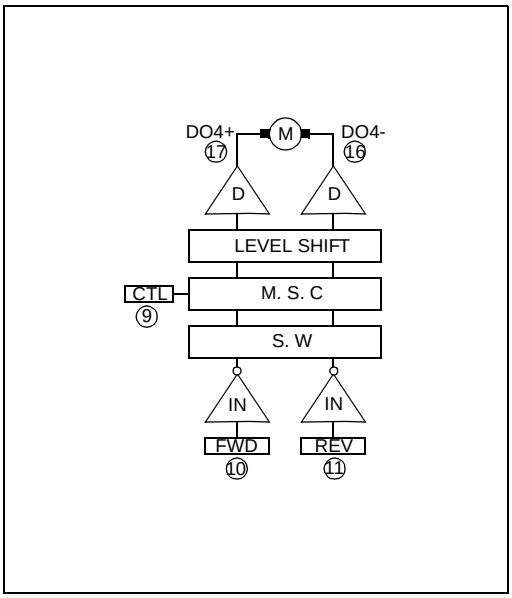
3) The level shift circuit produces the differential output voltages and drives the two output power amplifiers.
Since the differential gain of the output amplifiers is equal to $2 \times (1+ R4/R3)$, the output signal of the error amp is amplified by $(R2/R1) \times 2 \times (1+R4/R3)$.

4) If the total gain is insufficient, the input error amp can be used to increase the gain.

5) The bias voltage (Vr) is about a half of the supply voltage(VM).



5. TRAY MOTOR DRIVE PART



1) Rotational Direction Control

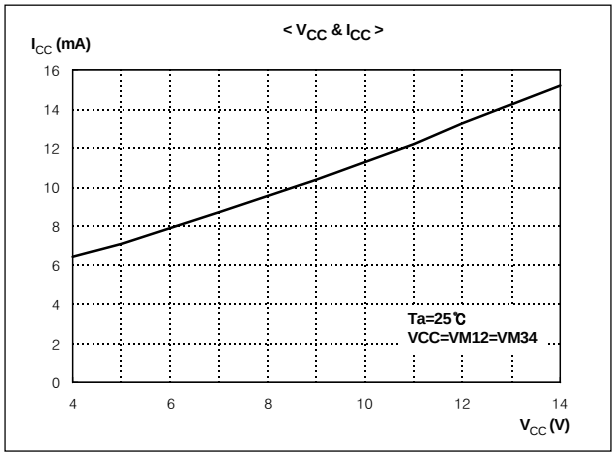
- The forward and reverse rotational direction is controlled by FWD (pin 10) and REV (pin 11) inputs. Conditions are as follows.
- Vr(Power reference voltage) is (VM34-VBE) / 2

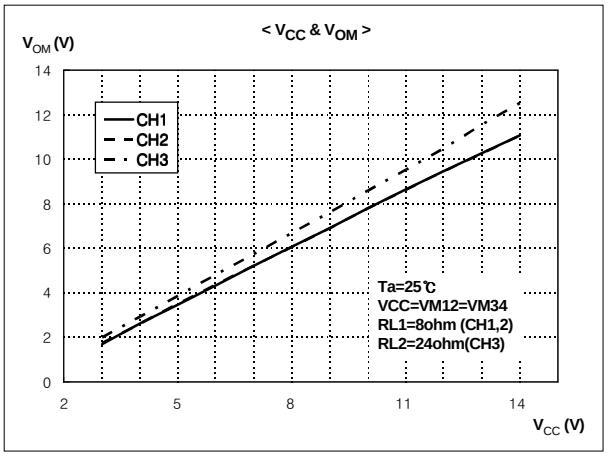
Input		Output		
FWD	**REV**	**DO4+**	**DO4-**	**State**
H	H	Vr	Vr	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	Vr	Vr	Brake

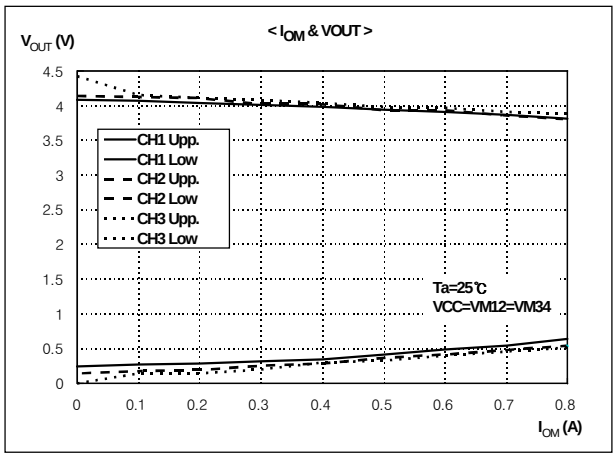
2) Motor Speed Control

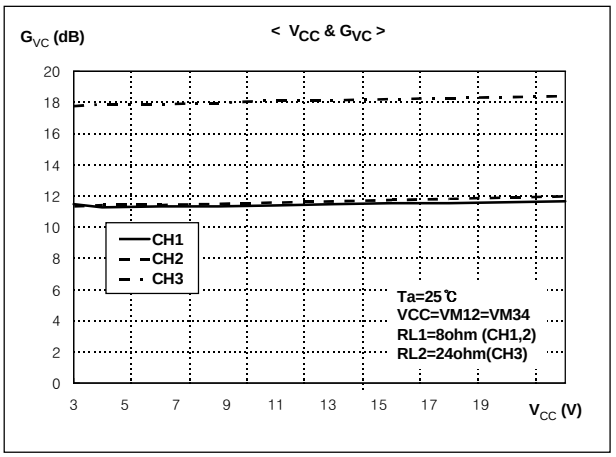
- The motor speed is proportional to the difference voltage between the pin17(DO4+) and the pin16(DO4-).
- By applying the voltage to the pin9 of CTL, the motor speed can be controlled and it is linearly proportional to the applied control voltage.
- When both VM3,4 and Vcc are 8V, and the applied control voltage is higher than 7V, the motor speed is not proportional to the control voltage but the motor speed becomes constant.
- If the pin9 is opened,the motor torque becomes maximum.
- The maximum output swing is 6.0V, when VM3,4 and Vcc are 8V.

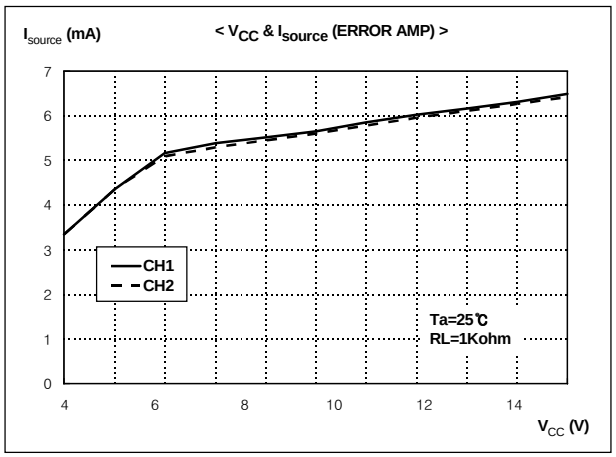
Typical Performance Characteristics

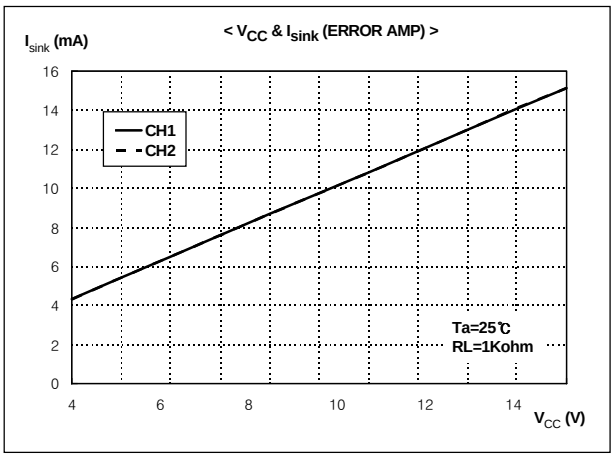






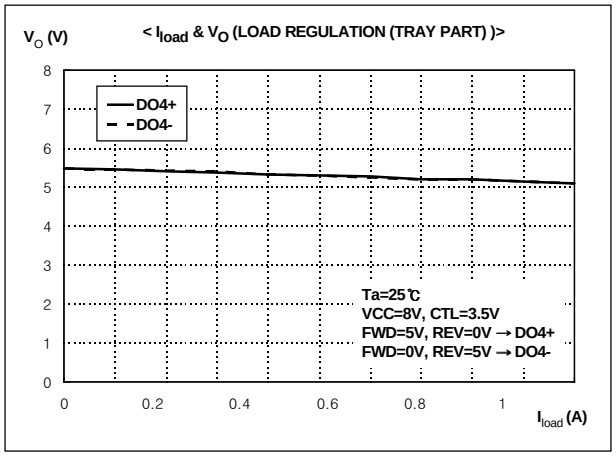


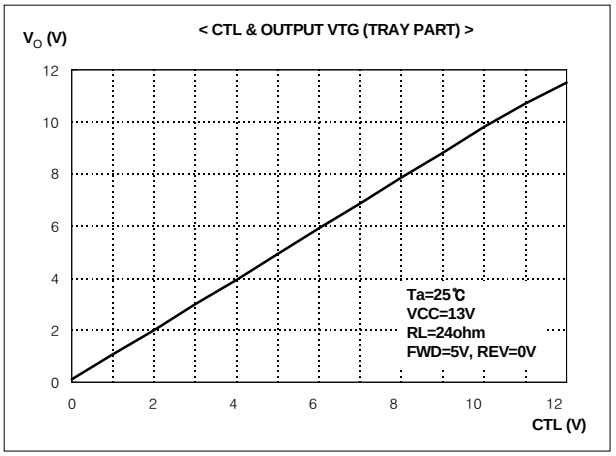


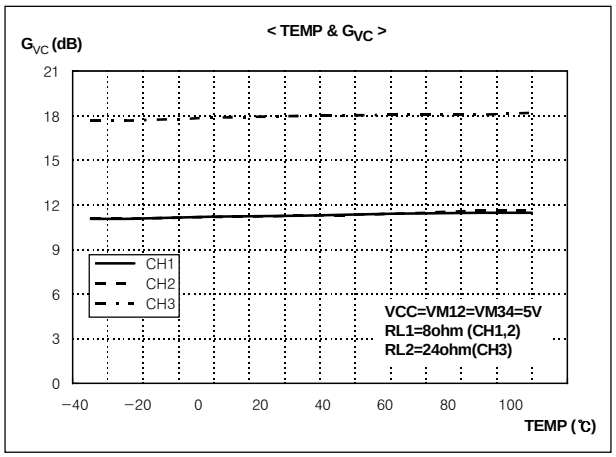


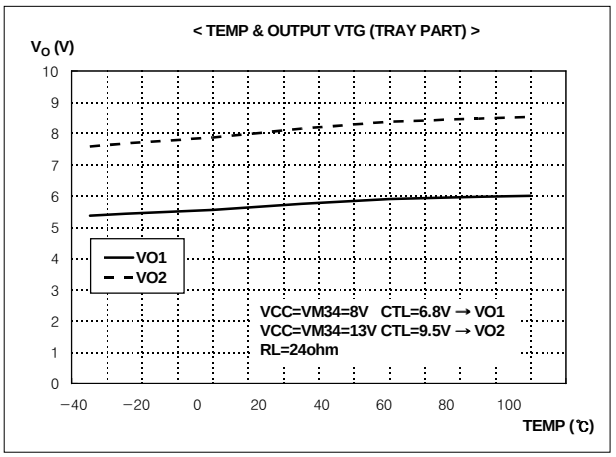
DC MOTOR DRIVE IC

Typical Performance Characteristics (Continued)

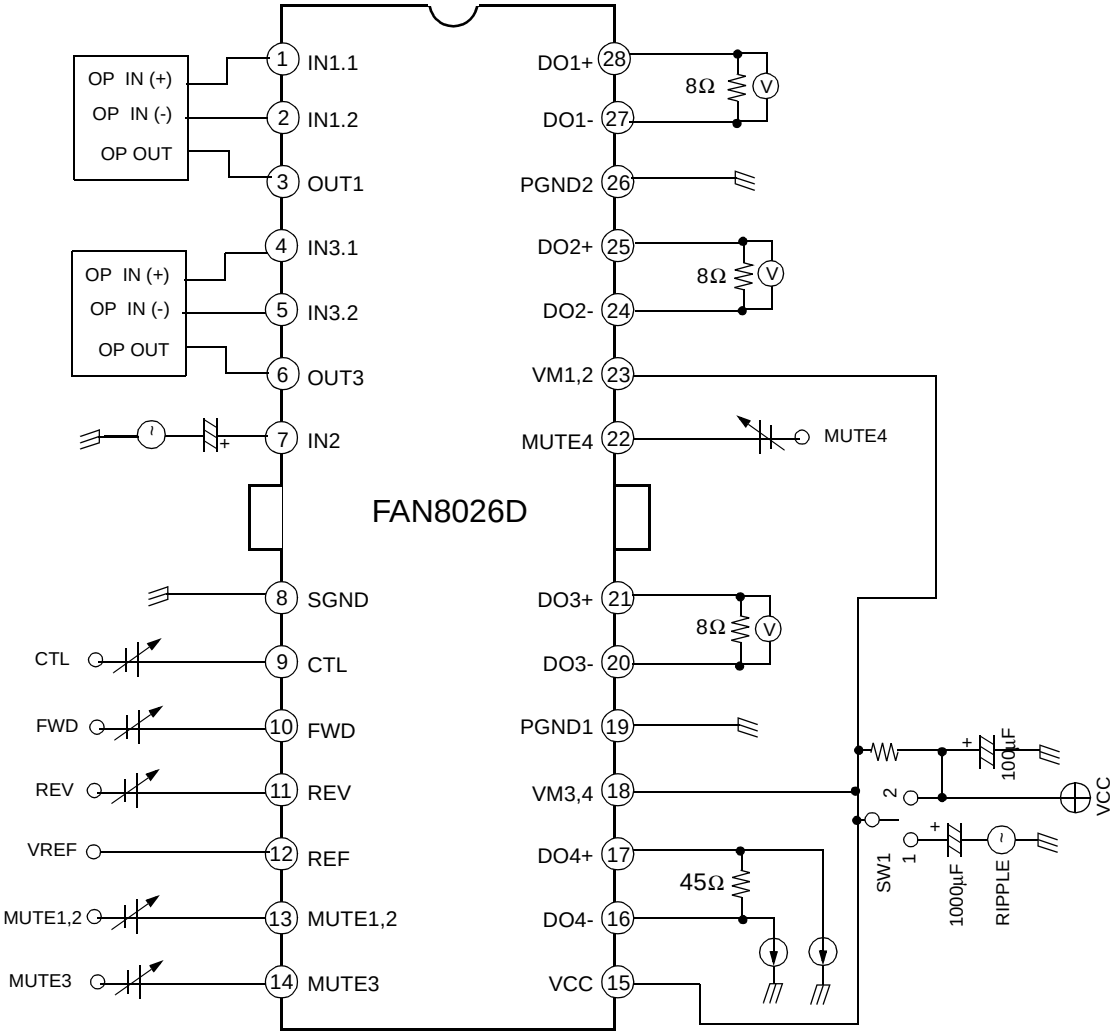


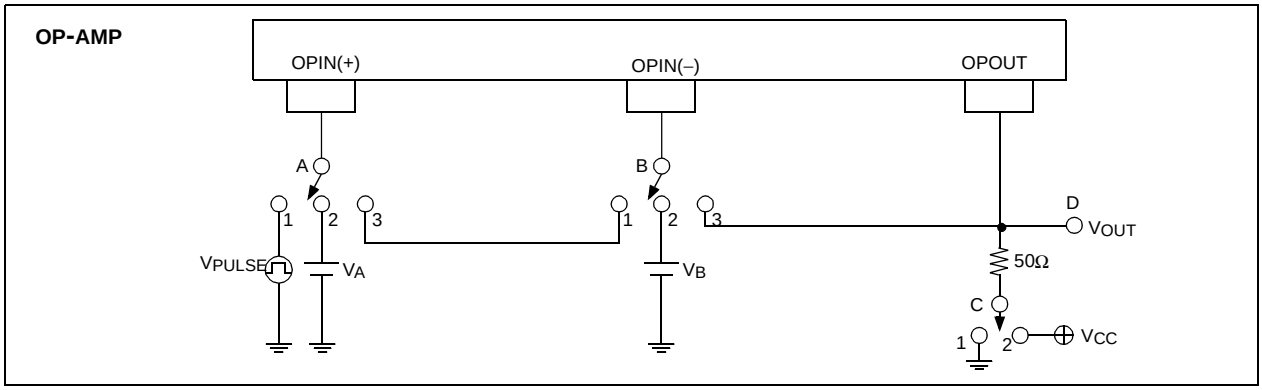






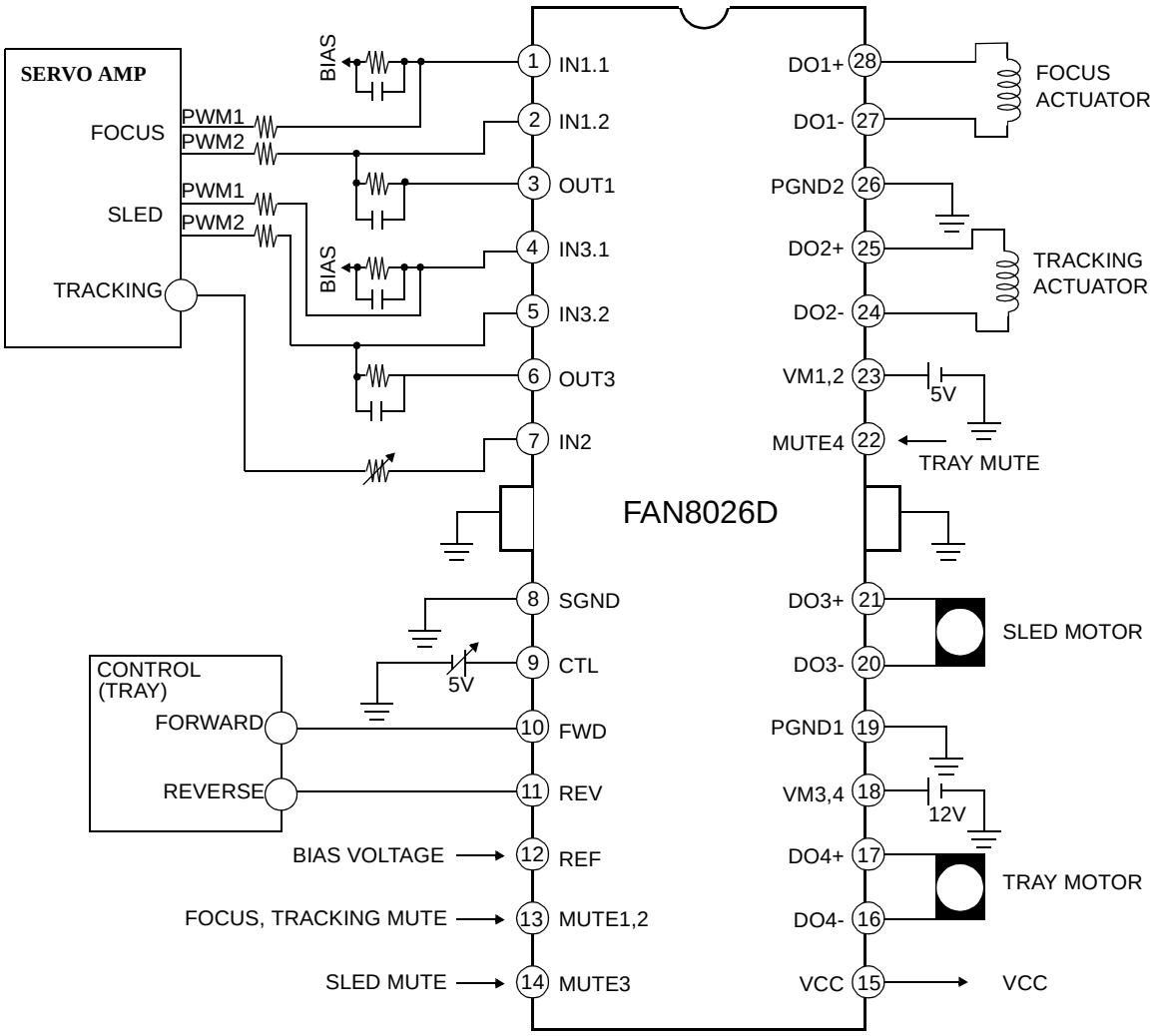
Test Circuits





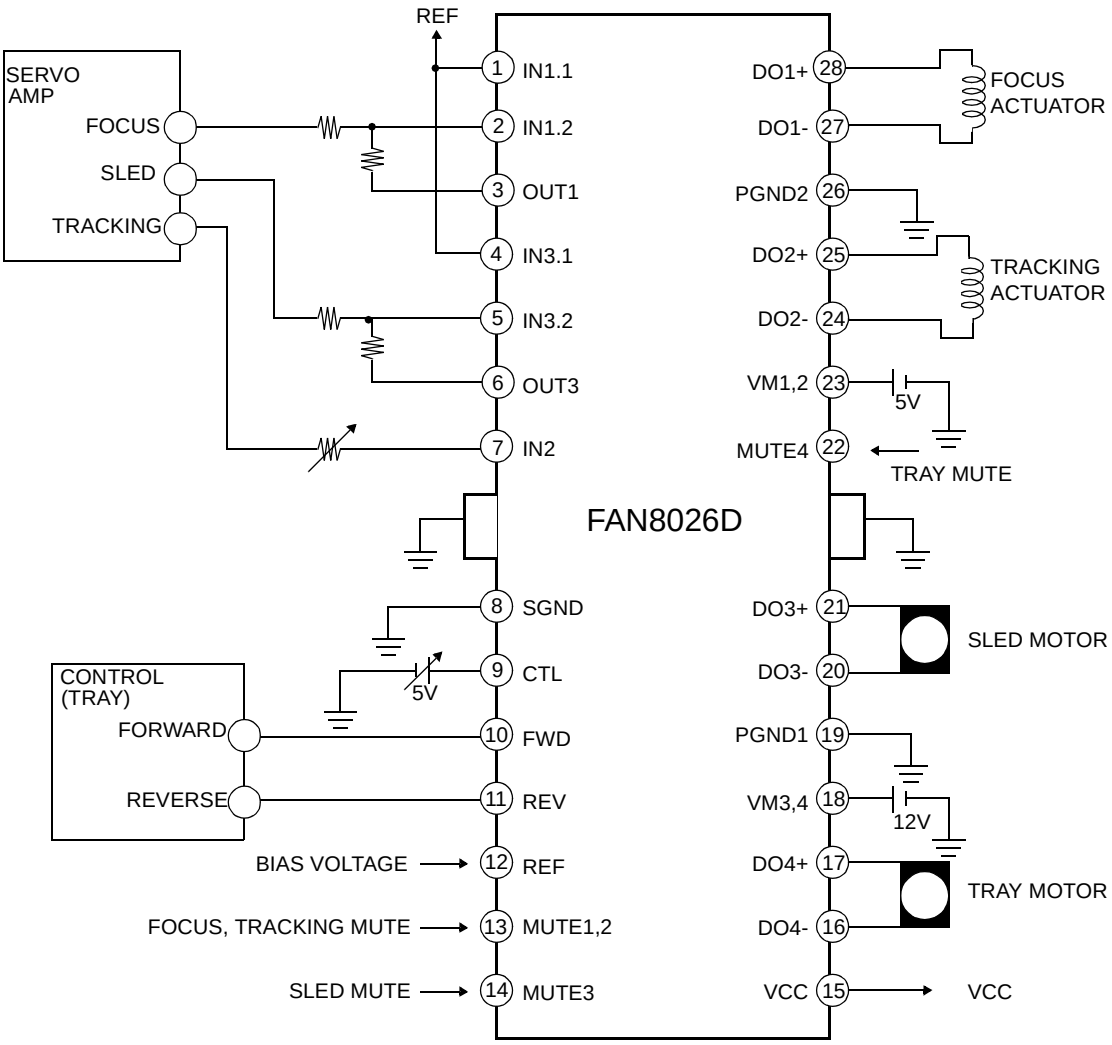
Typical Application Circuits 1

(Diffential PWM Control Mode)



Typical Application Circuits 2

(Voltage Control Mode)



Ordering Information

Device	Package	Operating Temperature
FAN8026D	28-SSOPH-375	-35 °C ~ 85 °C
FAN8026DTF	28-SSOPH-375	-35 °C ~ 85 °C

DC MOTOR DRIVE IC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAN8037 (KA3037)

7-CH Motor Drive IC

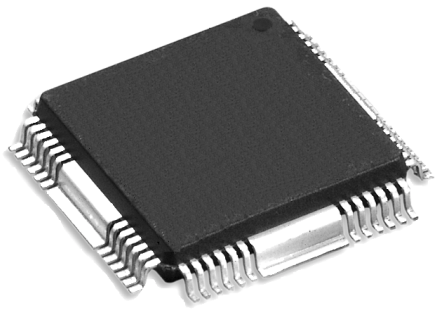
Features

- 4-CH balanced transformerless (BTL) driver
- 3-CH (forward - reverse) control DC motor driver
- Operating supply voltage (4.5 V ~ 13.2 V)
- Built-in thermal shut down circuit (TSD)
- Built-in all channel mute circuit
- Built-in power save mode circuit
- Built-in stand by mode circuit
- Built-in variable regulator

Description

The FAN8037 is a monolithic integrated circuit suitable for a 7-ch motor driver which drives the tracking actuator, focus actuator, sled motor, tray motor, changer motor, panel motor and, spindle motor of the CDP/CAR-CD systems.

48-QFPH-1414

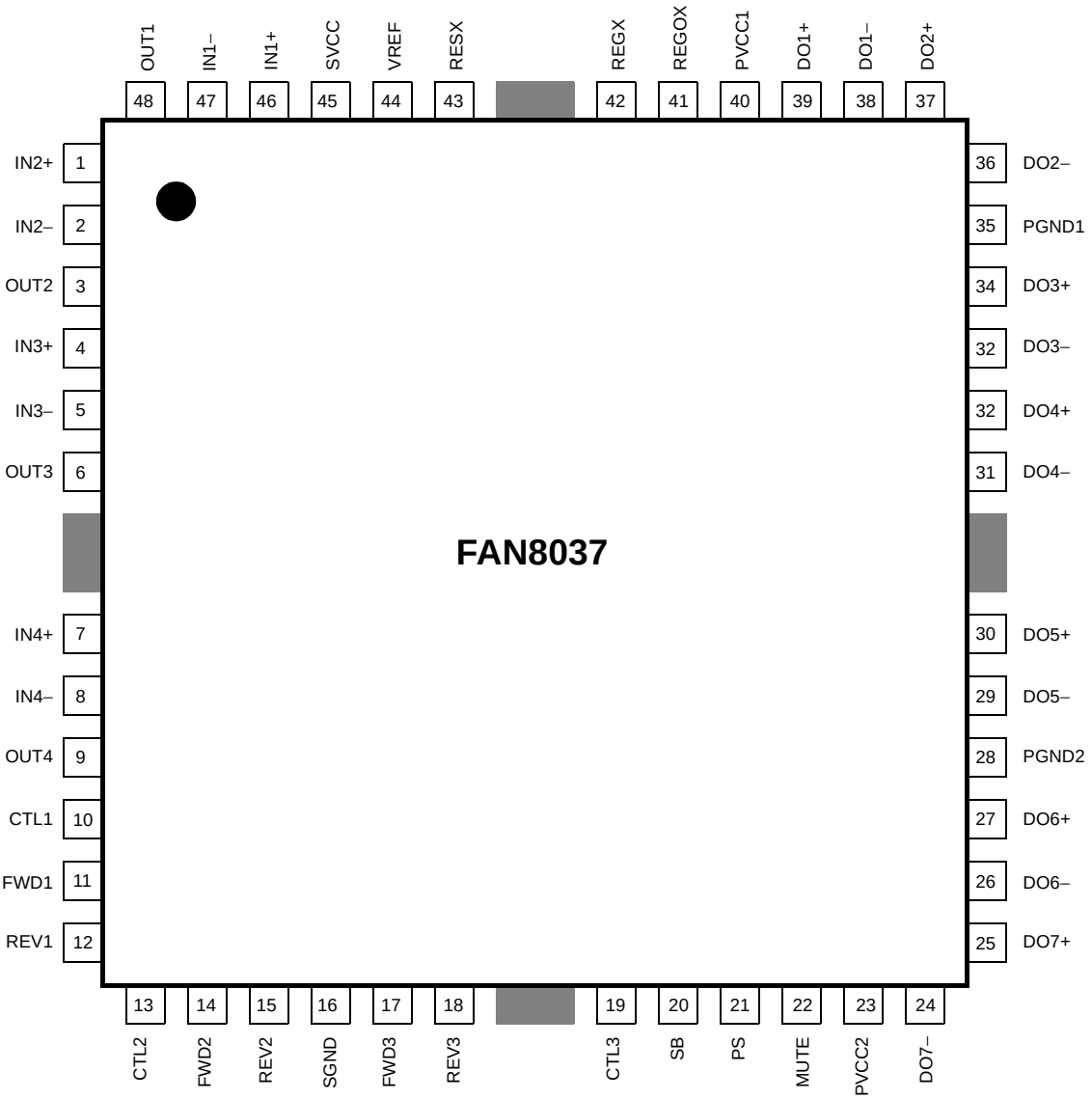


DC MOTOR DRIVE IC

Typical Application

- Compact disk player (Tray, Changer)
- Video compact disk player (Tray, Changer)
- Car compact disk player (Tray, Changer)
- Mixing with compact disk player and mini disk player (Tray, Changer, Panel)

Pin Assignments



DC MOTOR DRIVE IC

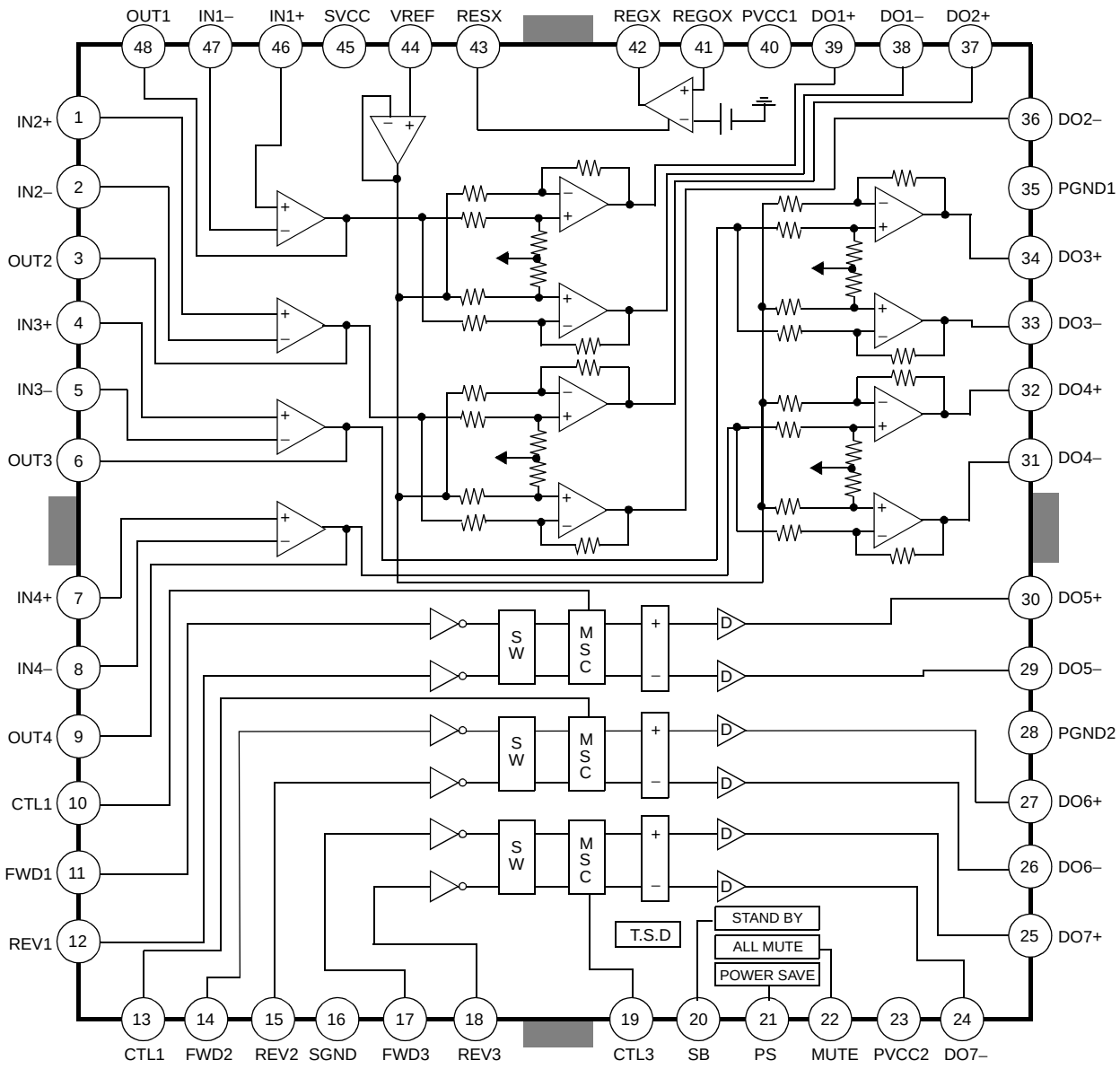
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Descrition
1	IN2+	I	CH2 op-amp input (+)
2	IN2–	I	CH2 op-amp inut (–)
3	OUT2	O	CH2 op-amp output
4	IN3+	I	CH3 op-amp input (+)
5	IN3–	I	CH3 op-amp input (–)
6	OUT3	O	CH3 op-amp output
7	IN4+	I	CH4 op-amp input (+)
8	IN4–	I	CH4 op-amp input (–)
9	OUT4	O	CH4 op-amp output
10	CTL1	I	CH5 motor speed control
11	FWD1	I	CH5 forward input
12	REV1	I	CH5 reverse input
13	CTL2	I	CH6 motor speed control
14	FWD2	I	CH6 forward input
15	REV2	I	CH6 reverse input
16	SGND	-	Signal groung
17	FWD3	I	CH7 forward input
18	REV3	I	CH7 reverse input
19	CTL3	I	CH7 motor speed control
20	SB	I	Stand by
21	PS	I	Power save
22	MUTE	I	All mute
23	PVCC2	-	Power supply voltage (For CH5, CH6, CH7)
24	DO7–	O	CH7 drive ouptut (–)
25	DO7+	O	CH7 drive output (+)
26	DO6–	O	CH6 drive output (–)
27	DO6+	O	CH6 drive output (+)
28	PGND2	-	Power ground2 (FOR CH5, CH6, CH7)
29	DO5–	O	CH5 drive output (–)
30	DO5+	O	CH5 drive output (+)
31	DO4–	O	CH4 drive output (–)
32	DO4+	O	CH4 drive output (+)

Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Descrition
33	DO3–	O	CH3 drive output (–)
34	DO3+	O	CH3 drive output (+)
35	PGND1	-	Power ground 1 (FOR CH1, CH2, CH3, CH4)
36	DO2–	O	CH2 drive output (–)
37	DO2+	O	CH2 drive output (+)
38	DO1–	O	CH1 drive output (–)
39	DO1+	O	CH1 drive output (+)
40	PVCC1	-	Power supply voltage (FOR CH1, CH2, CH3, CH4)
41	REGOX	I	Regulator feedback input
42	REGX	O	Regulator output
43	RESX	I	Regulator reset input
44	VREF	I	Bias voltage input
45	SVCC	-	Signal supply voltage
46	IN1+	I	CH1 op-amp input (+)
47	IN1–	I	CH1 op-amp input (–)
48	OUT1	O	CH1 op-amp output

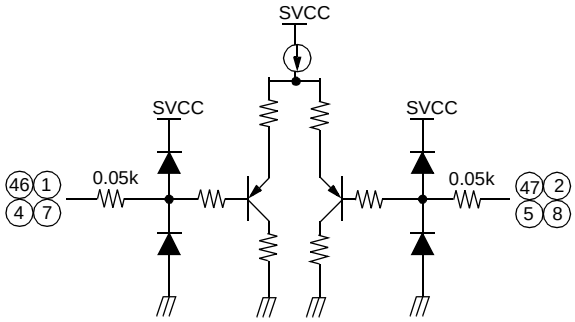
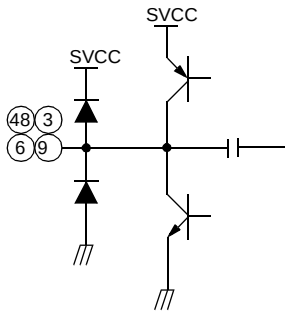
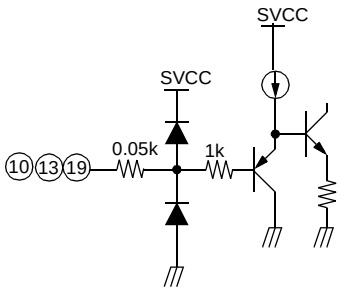
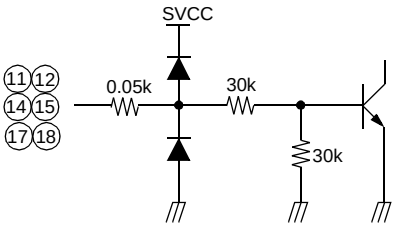
Internal Block Diagram



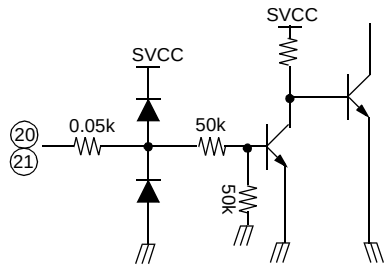
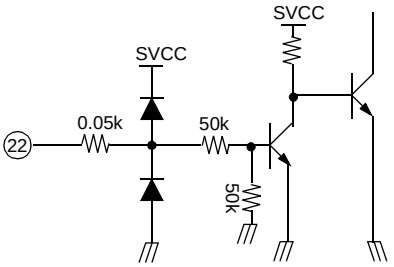
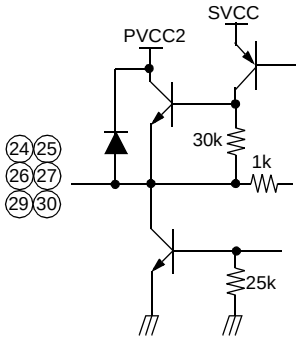
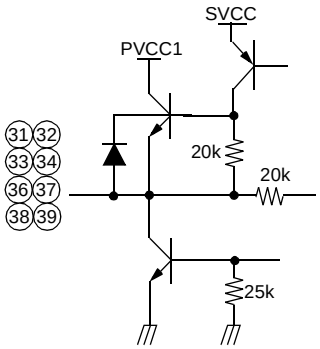
Notes:

1. SW = Logic switch
2. MSC = Motor speed control
3. D = Output driver

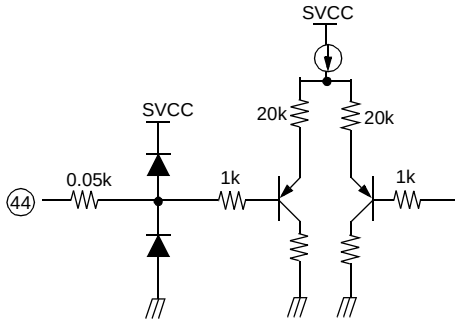
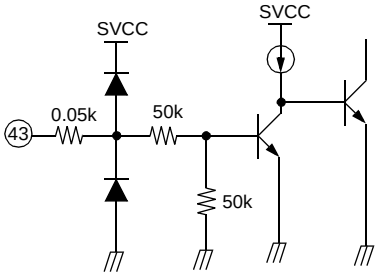
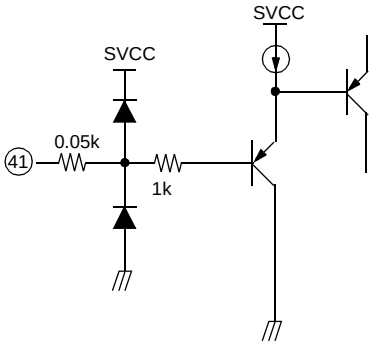
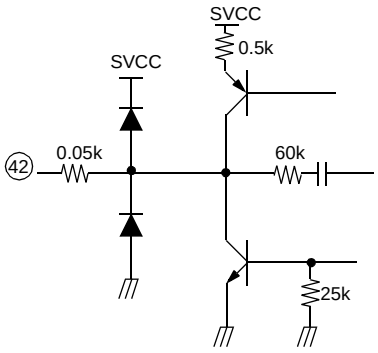
Equivalent Circuits

Description	Pin No.	Internal circuit
Input OPIN (+) OPIN (–)	46,47,1,2 4,5,7,8	
Input opout	48,3,6,9	
CTL	10,13,19	
Logic drive FWD input REV input	11,12, 14,15, 17,18	

Equivalent Circuits (Continued)

Description	Pin No.	Internal circuit
Power save Standby	20,21	
Mute	22	
Logic drive output	24, 25 26, 27 29,30	
4-CH drive output	31, 32 33, 34 36, 37 38, 39	

Equivalent Circuits (Continued)

Description	Pin No.	Internal circuit
Ref	44	
RESX	43	
REG0X	41	
REGX	42	

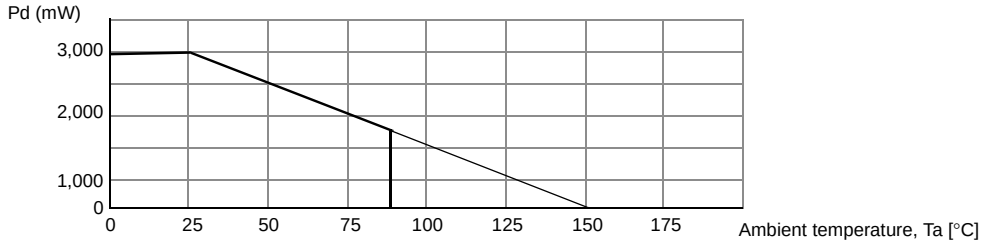
DC MOTOR DRIVE IC

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	$SVCC_{MAX}$	18	V
	PVCC1	18	V
	PVCC2	18	V
Power Dissipation	P_D	3[note]	W
Operating Temperature	T_{OPR}	–35 ~ +85	°C
Storge Temperature	T_{STG}	–55 ~ +150	°C
Maximum Output Current	I_{OMAX}	1	A

Notes:

1. When mounted on 70mm × 70mm × 1.6mm PCB
2. Power dissipation reduces 24mW/°C for using above T_A = 25°C
3. Do not exceed P_D and SOA



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	SVCC	4.5	-	13.2	V
	PVCC1	4.5	-	SVCC	V
	PVCC2	4.5	-	SVCC	V

Electrical Characteristics

(SV_{CC} = PV_{CC1} = PV_{CC2} = 8V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Quiescent circuit current	I_{CC}	Under no-load	15	25	35	mA
Power save on current	I_{PS}	Pin21=GND	-	1	2	mA
Stand by on voltage	V_{SBON}	Pin20=Variation	-	-	0.5	V
Stand by off voltage	V_{SBOFF}	Pin20=Variation	2	-	-	V
Power save on voltage	V_{PSON}	Pin21=Variation	-	-	0.5	V
Power save off voltage	V_{PSOFF}	Pin21=Variation	2	-	-	V
All mute on voltage	V_{MON}	Pin22=Variation	-	-	0.5	V
All mute off voltage	V_{MOFF}	Pin22=Variation	2	-	-	V
DRIVER PART (R_L=8Ω)						
Output offset voltage	V_{OO}	V_{IN}=2.5V	−80	-	+80	mV
Maximum output voltage 1	V_{OM1}	V_{CC}=PV_{CC1}=PV_{CC2}=8V, R_L=8Ω	5.5	6.5	-	V
Maximum output voltage 2	V_{OM2}	V_{CC}=PV_{CC1}=PV_{CC2}=13V, R_L=24Ω	10.5	11.5	-	V
Closed-loop voltage gain	A_{VF}	V_{IN}=0.1Vrms	10.5	12	13.5	dB
Slew rate	SR	Square, Vout=4Vp-p,f=120kHz	-	2	-	V/μs
INPUT OPAMP PART						
Input offset voltage	V_{OF}	-	−30	-	+30	mV
Input bias current	I_B	-	-	-	300	nA
High level output voltage	V_{OH}	R_L=Open	7.2	7.7	-	V
Low level output voltage	V_{OL}	R_L=Open	-	0.2	0.5	V
Output sink current	I_{SINK}	R_L=50Ω	2	4	-	mA
Output source current	I_{SOURCE}	R_L=50Ω	2	4	-	mA
Open loop voltage gain	G_{VO}	V_{IN}=−75dB	-	70	-	dB
Slew rate	SR	Square, Vout=2Vp-p, f=120kHz	-	2.5	-	V/μs

Electrical Characteristics (Continued)

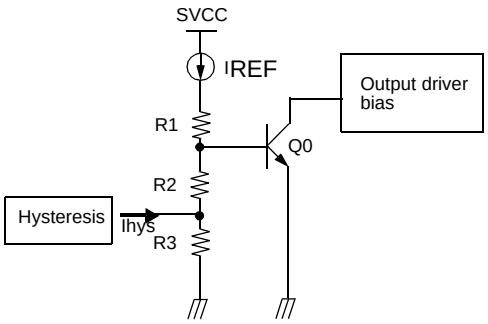
(SV_{CC} = PV_{CC1} = PV_{CC2} = 8V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
TRAY, CHANGER,PANEL DRIVE PART (R_L=45Ω)						
Input high level voltage	V_{IH}	-	2	-	-	V
Input low level voltage	V_{IL}	-	-	-	0.5	V
Output voltage 1	V_{O1}	V_{CC}=8V, V_{CTL}=3V, R_L=8Ω	-	5	-	V
Output voltage 2	V_{O2}	V_{CC}=8V, V_{CTL}=3V, R_L=45Ω	-	6	-	V
Output voltage 3	V_{O3}	V_{CC}=13V, V_{CTL}=4.5V, R_L=45Ω	-	9	-	V
Output load regulation	ΔV_{RL}	V_{CTL}=3V, I_L=100mA → 400mA	-	300	700	mV
Output offset voltage 1	V_{OO1}	V_{IN}=5V, 5V	–40	-	+40	mV
Output offset voltage 2	V_{OO2}	V_{IN}=0V, 0V	–40	-	+40	mV
VARIABLE REGULATOR PART						
Load regulation	ΔV_{RL}	I_L=0 → 200mA	–40	0	+10	V
Line regulation	ΔV_{CC}	I_L=200mA, V_{CC}=6V → 9V	–20	0	+30	mV
Regulator output voltage 1	V_{REG1}	I_L=100mA	4.75	5.0	5.25	V
Regulator output voltage 2	V_{REG2}	I_L=100mA	3.135	3.3	3.465	V
Regulator reset on voltage	Reson	Pin43=Varivation	-	-	0.5	V
Regulator reset off voltage	Resoff	Pin43=Varivation	2	-	-	V

Application Information

1. THERMAL SHUTDOWN

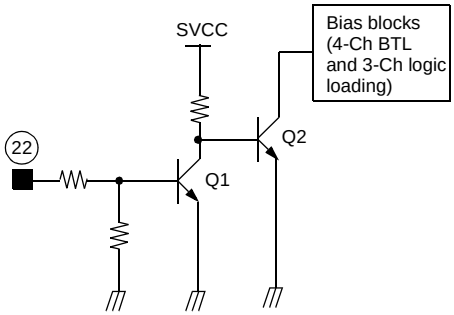
- When the chip temperature reaches to 175°C, then the TSD circuit is activated.
- This shut down the bias current of the output drivers, and all the output drivers are in cut-off state. Thus the chip temperature begin to decrease.
- when the chip temperature falls to 150°C, the TSD circuit is deactivated and the output drivers are normally operated.
- The TSD circuit has the hysteresis temperature of 25°C.



2. ALL MUTE FUNCTION

- When the pin22 is high, the TR Q1 is turned on and Q2 is off, so the bias circuit is enabled. On the other hand, when the pin22 is Low (GND) , the TR Q1 is turned off and Q2 is on, so the bias circuit is disabled.
- That is, this function will cause all the output drivers to be in mute state.
- Truth table is as follows;

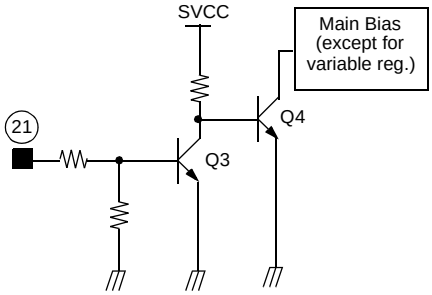
Pin#22	FAN8037
HIGH	MUTE-OFF
LOW	MUTE-ON



3. POWER SAVE FUNCTION

- When the pin21 is high, the TR Q3 is turned on and Q4 is off, so the bias circuit is enabled. On the other hand, when the pin21 is Low (GND) , the TR Q3 is turned off and Q4 is on, so the bias circuit is disabled.
- That is, this function will cause all the circuit blocks of the chip except for the variable regulator to be in the off state. thus the low power quiescent state is established
- Truth table is as follows;

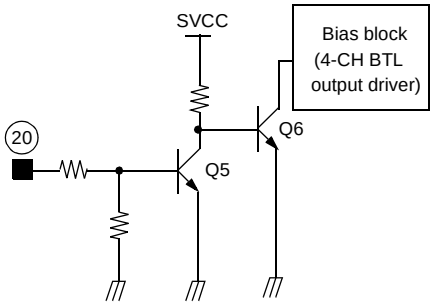
Pin#21	FAN8037
HIGH	POWER SAVE OFF
LOW	POWER SAVE ON



4. STANDBY FUNCTION

- When the pin20 is high, the TR Q5 is turned on and Q6 is off, so the bias circuit is enabled. On the other hand, when the pin20 is Low (GND) , the TR Q5 is turned off and Q6 is on, so the bias circuit is disabled.
- That is, this function will cause the output drivers of the 4-CH BTL part(Focus, Tracking, Spindle, Sled) to be in off state.
- Truth table is as follows

Pin#20	KA3037
HIGH	STANDBY OFF
LOW	STANDBY ON



5. REGULATOR & RESET FUNCTION

The regulator and reset circuits are illustrated in the figure 1.

- The external circuit is composed of the PNP transistor(KSB772), capacitor(about 33μF) and 2 feedback resistors.
- The capacitor is used as a ripple eliminator and should have good temperature characteristics.
- The regulator output voltage is decided as follows.
  $V_{REG} = (1+R1/R2) \times 2.5$
- When the voltage of the pin 43 (Vreset) is high, the regulator circuit operates normally. If the voltage of pin 43 is low, the regulator circuit is disabled .

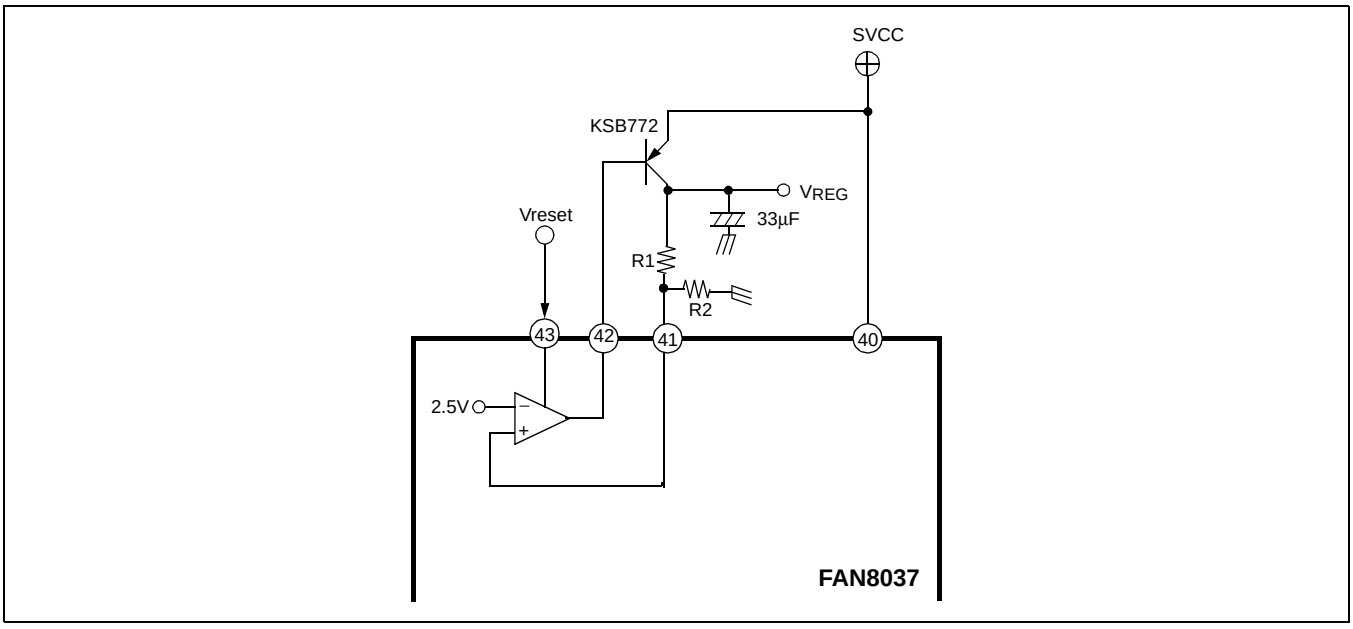
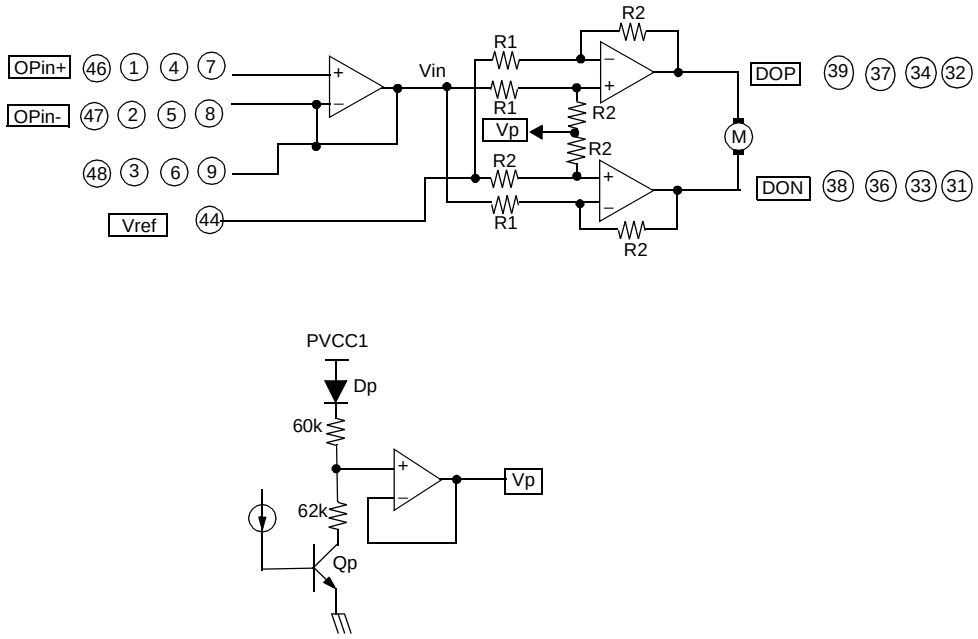


Figure 1. Regulator circuit

6. FOCUS, TRACKING ACTUATOR, SPINDLE, SLED MOTOR DRIVE PART



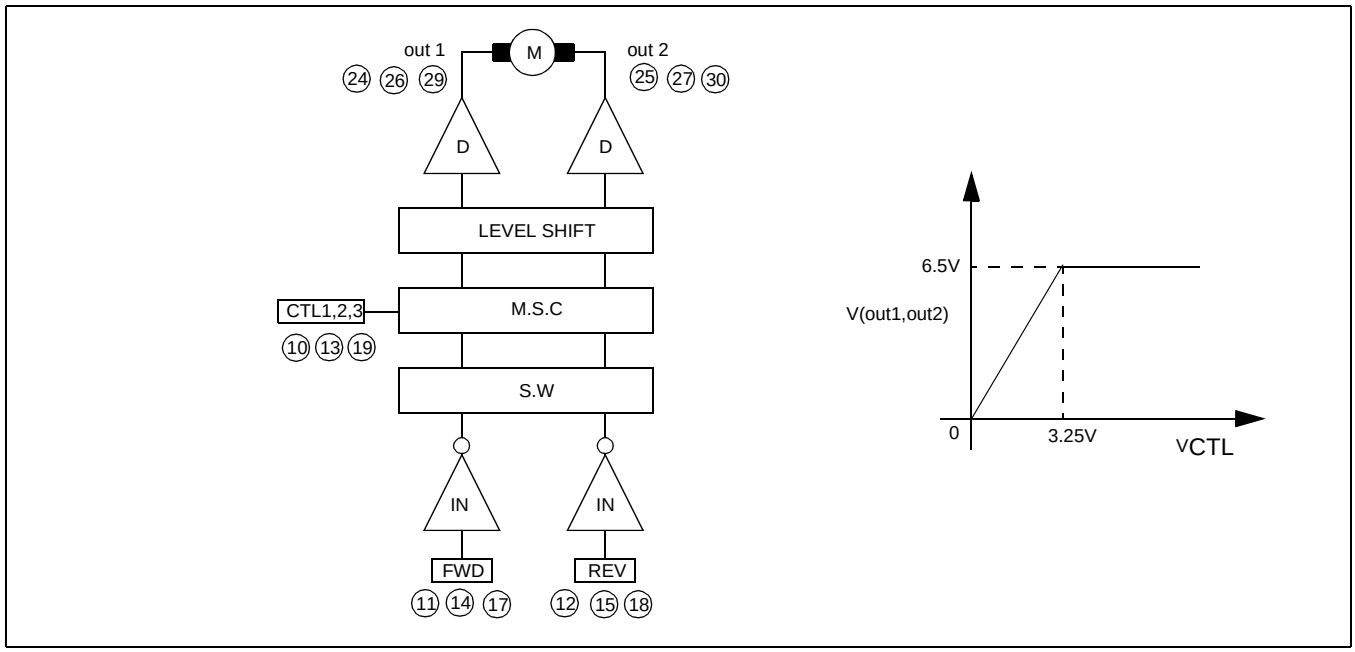
- The voltage, Vref is the reference voltage given by the external bias voltage of the pin 44.
- The input signal (Vin) through pins 46,1,4 and 7 is amplified one time and then fed to the output stage. (assume that input opamp was used as a buffer)
- The total closed loop voltage gain is as follows

$$Vin = Vref + \Delta V$$
$$DOP = Vp + 2\Delta V$$
$$DON = Vp - 2\Delta V$$
$$Vout = DOP - DON = 4\Delta V$$
$$Gain = 20\log\frac{Vout}{\Delta V} = 20\log 4 = 12dB$$

- If you want to change the total closed loop voltage gain, you must use the input opamp as an amplifier
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage Vp is expressed as ;

$$Vp = (PVCC1 - VDp - VcesatQp) \times \frac{62k}{60k + 62k} + VcesatQp$$
$$= \frac{PVCC1 - VDp + VcesatQp}{1.97} + VcesatQp \quad \text{----------} \quad (1)$$

7. TRAY, CHANGER,PANEL MOTOR DRIVE PART



- Rotational direction control
  The forward and reverse rotational direction is controlled by FWD (pin 11,14, 17) and REV (pin 12,15,18) and the input conditions are as follows.

INPUT		OUTPUT		
FWD	**REV**	**OUT 1**	**OUT 2**	**State**
H	H	Vp	Vp	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	-	-	Hign impedance

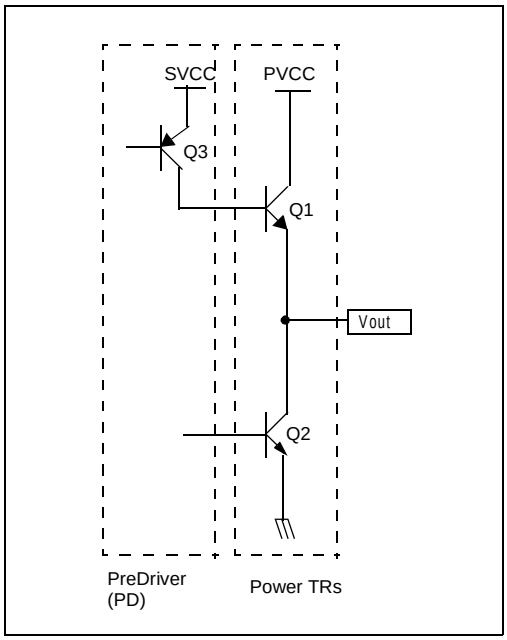
- Where Vp(Power referencd voltage) is approximately about 3.75V at PVCC2=8V) acording to equation (1).
- Where out1 pins are pins24,26,29 and out2 pins are pins25,27,30
- Motor speed control (When SVCC=PVCC2=8V)
  - The almost maximum torque is obtained when the pins (10,13 and 19 (CTL1, 2, 3)) are open.
  - If the voltage of the pins (10,13 and 19 (CTL1, 2, 3)) are 0V, the motor will not operate.
  - When the control voltage of the pins 10,13 and 19 (CTL1, 2, 3) are between 0 and 3.25V, the differential output voltage(V(out1,out2)) is about two times of control voltage. Hence, the control to the differential output gain is two.
  - When the control voltage is greater than 3.25V, the output voltage is saturated at the 6.5V because of the output swing limitation.

8. BOOTSTRAPPED OPERATION

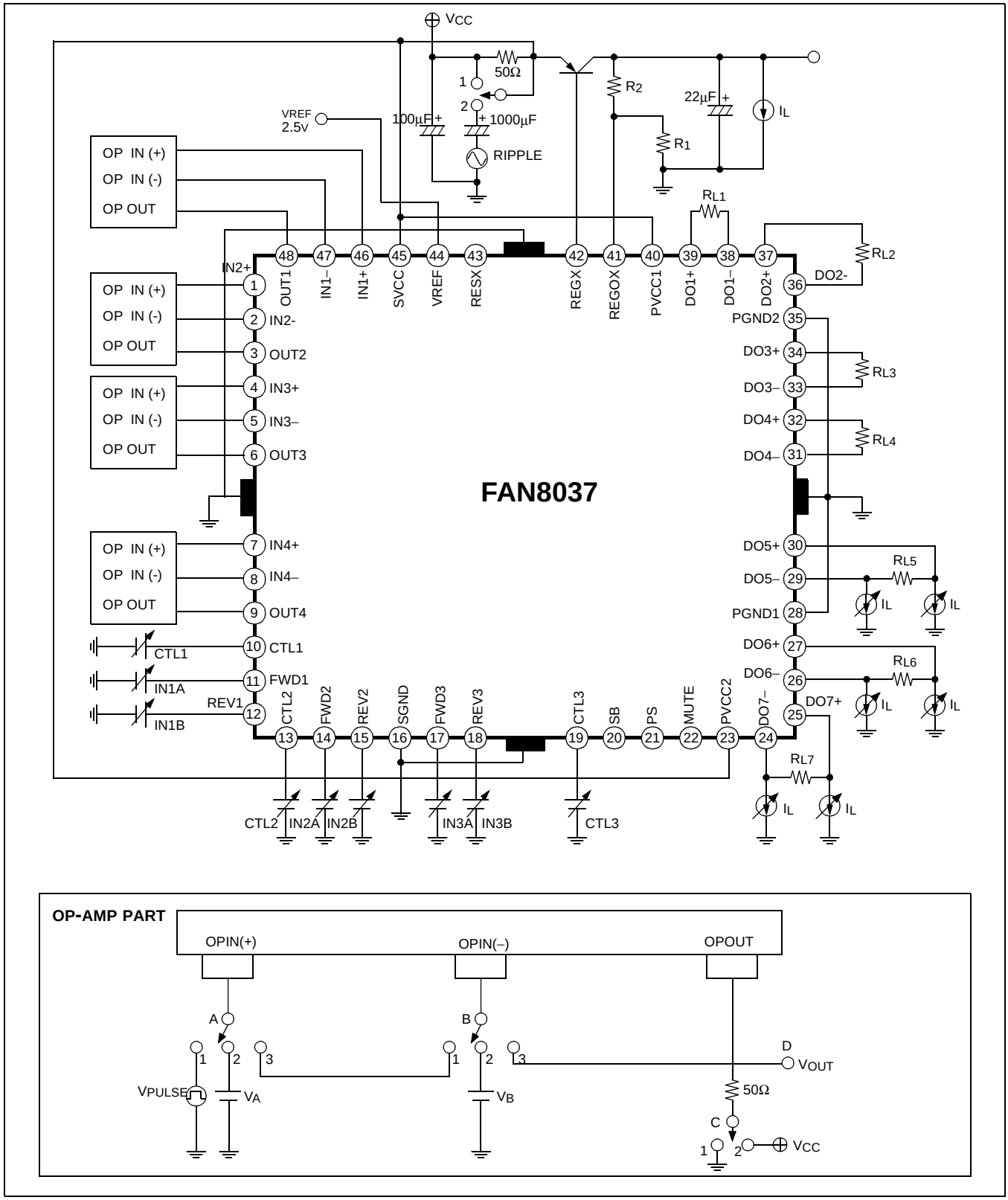
- Our IC has two kinds of power supplies, the power supply , SVCC is for predrivers and the other circuit blocks(SVCC), and PVCC1 and PVCC2 is for the power transistors.
- When SVCC=PVCC*n (n*=1,2), no bootstapped operation occurs. Thus the single-ended maximum output voltage is about to

$$SVCC - (VcesatQ3 + Vbe1) \cong SVCC - 1V$$

- If larger output swing is requied, use the bootstrap function. When $SVCC > PVCCn + 1V$ the bootsrap function is operated.
- In the mode, the single-ended maximum output voltage is about to $PVCCn - VcesatQ1 \cong PVCCn - 0.5$; hence wide output dynamic range can be obtained.

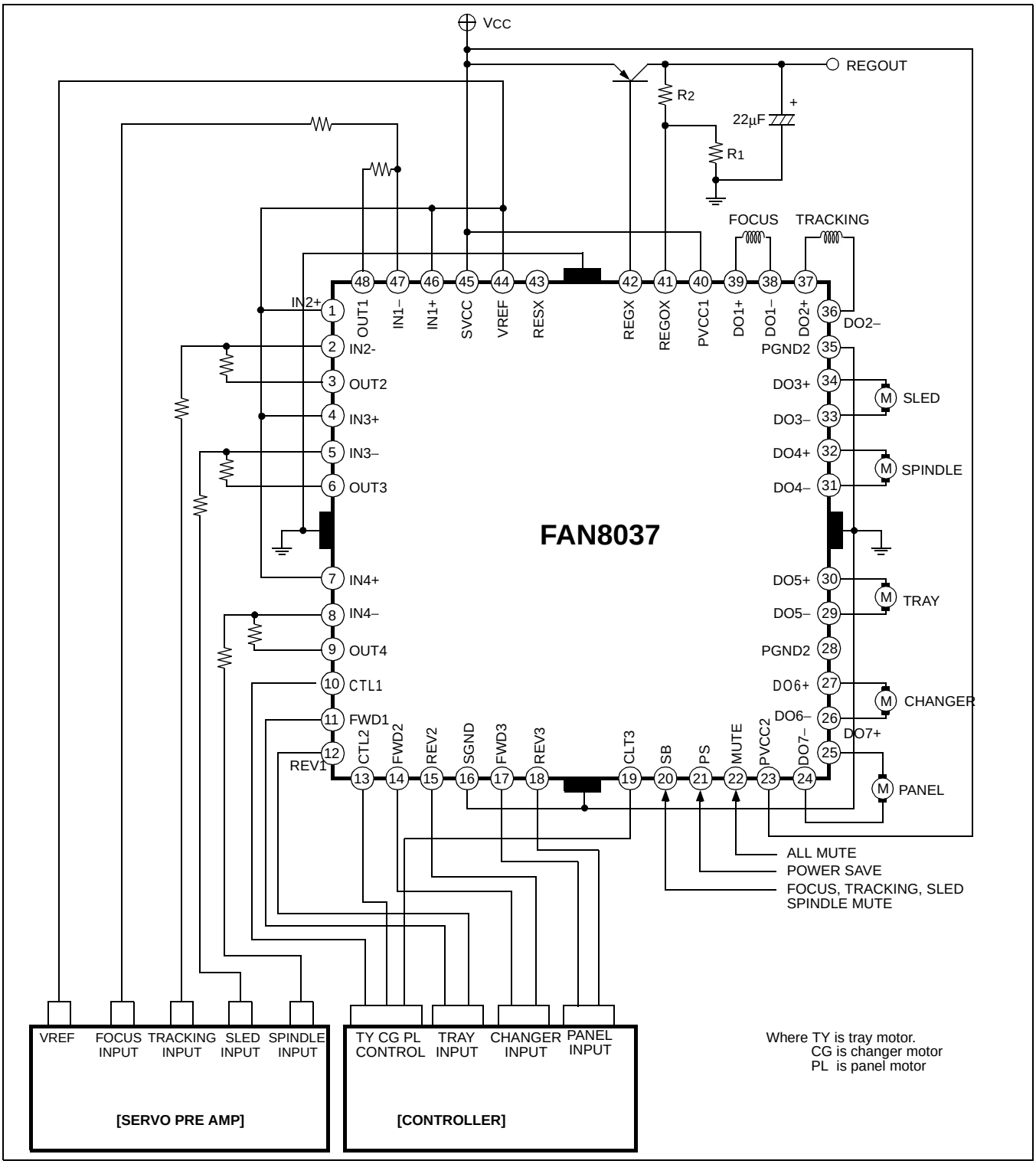


Test Circuits



Typical Application Circuits 1

[Voltage control mode]

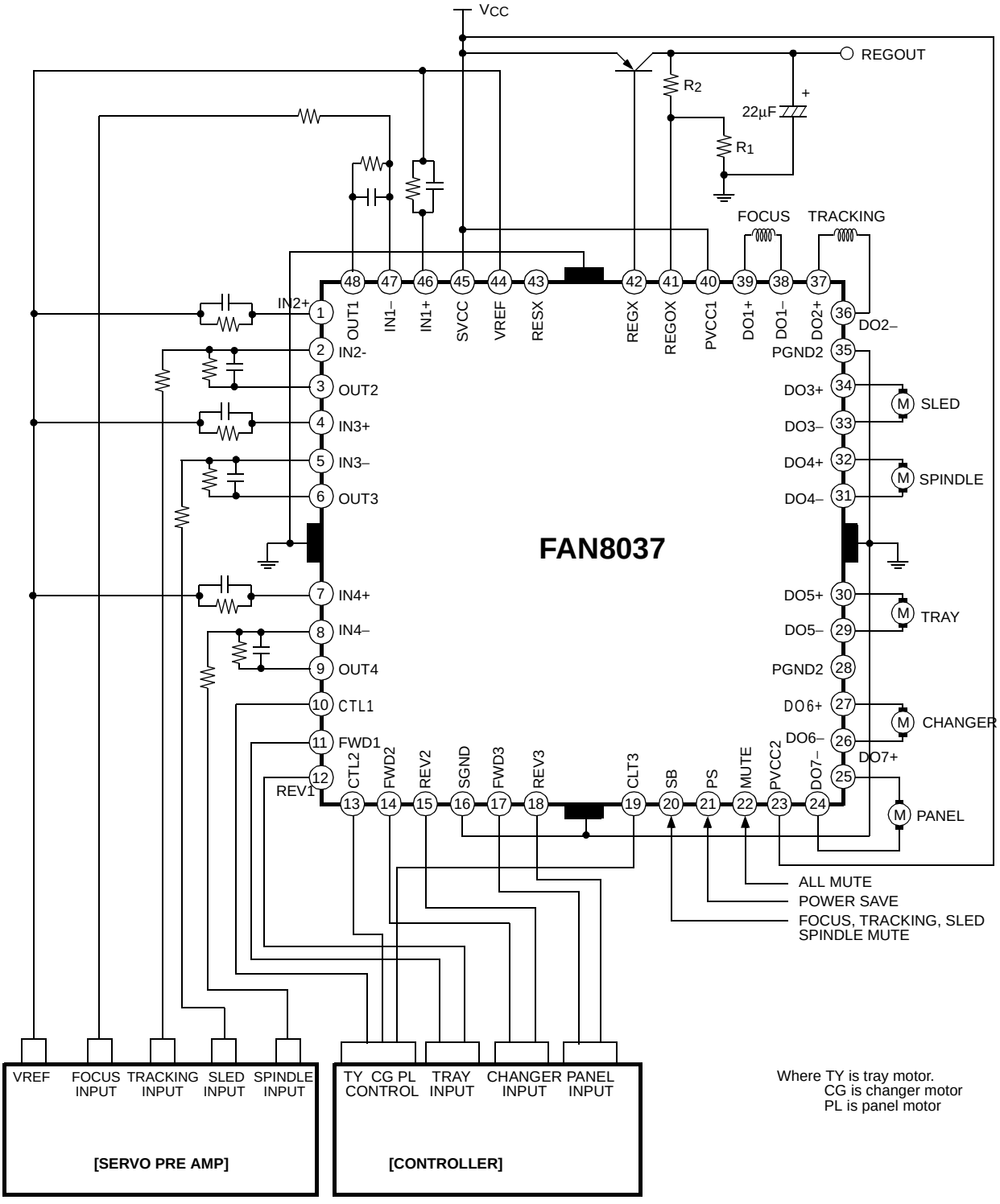


Notes:

Radiation pin is connected to the internal GND of the package.
Connect the pin to the external GND.

Typical Application Circuits 2

[Differential PWM control mode]



Notes:

Radiation pin is connected to the internal GND of the package.
Connect the pin to the external GND

Ordering Information

Device	Package	Operating Temperature
FAN80037	48-QFPH-1414	–35°C ~ +85°C

DC MOTOR DRIVE IC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAN8038 (KA3038)

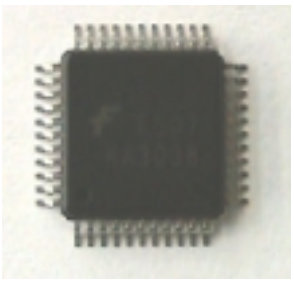
4-CH Motor Drive IC

Features

- 4-CH H-Bridge driver
- Built-in DC/DC converter controller circuit
- Built-in Reset circuit
- Built-in Battery charging circuit
- Built-in Voltage drop detector
- Built-in Thermal shutdown circuit
- Built-in general OP-AMP
- Low power consumption
- Built-in Power controller circuit

Description

FAN8038 is Monolithic IC for portable CD player.

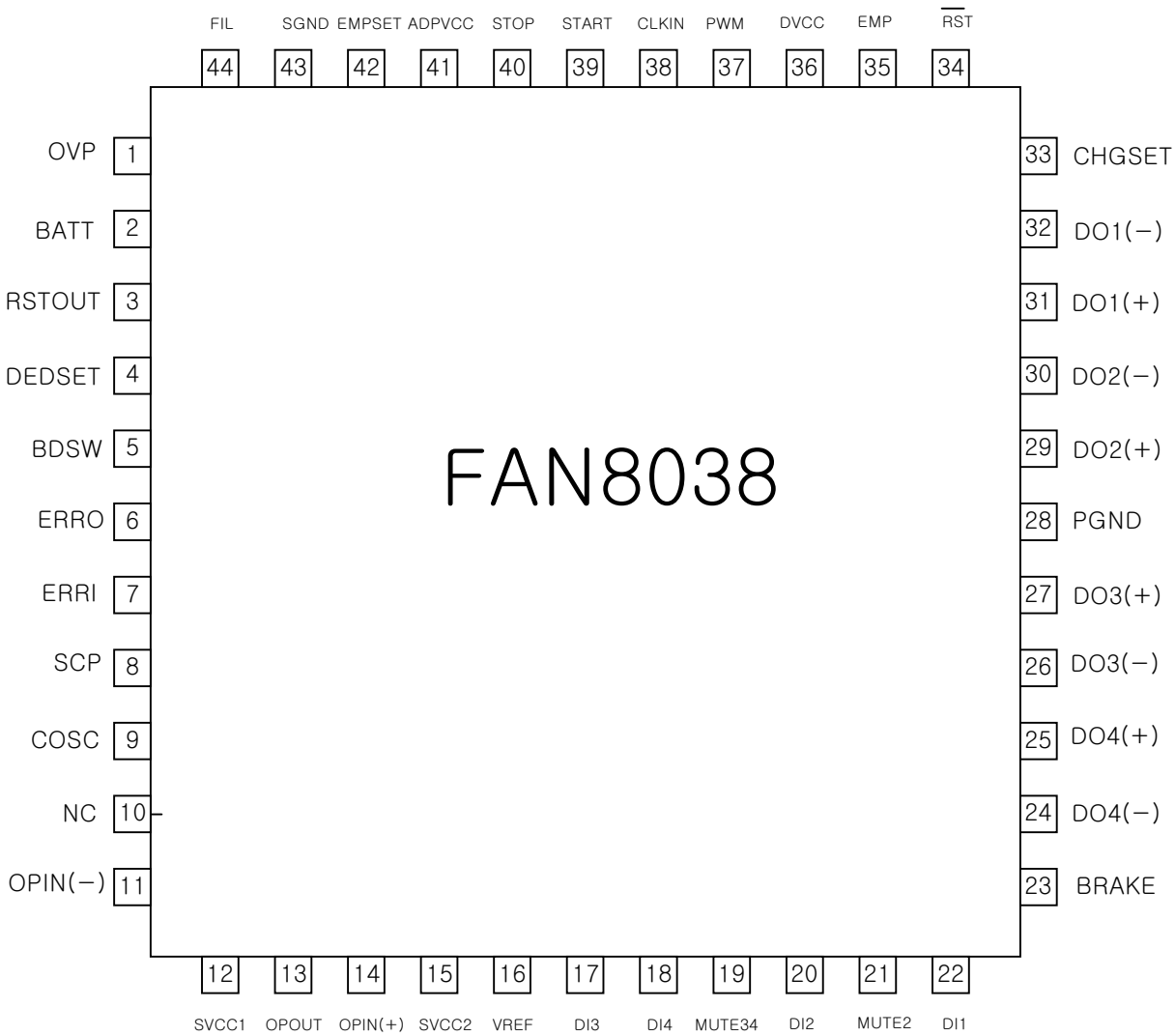


Typical application

- Portable compact disk player
- Diskman
- Mini-Disk

DC MOTOR DRIVE IC

Pin Assignments

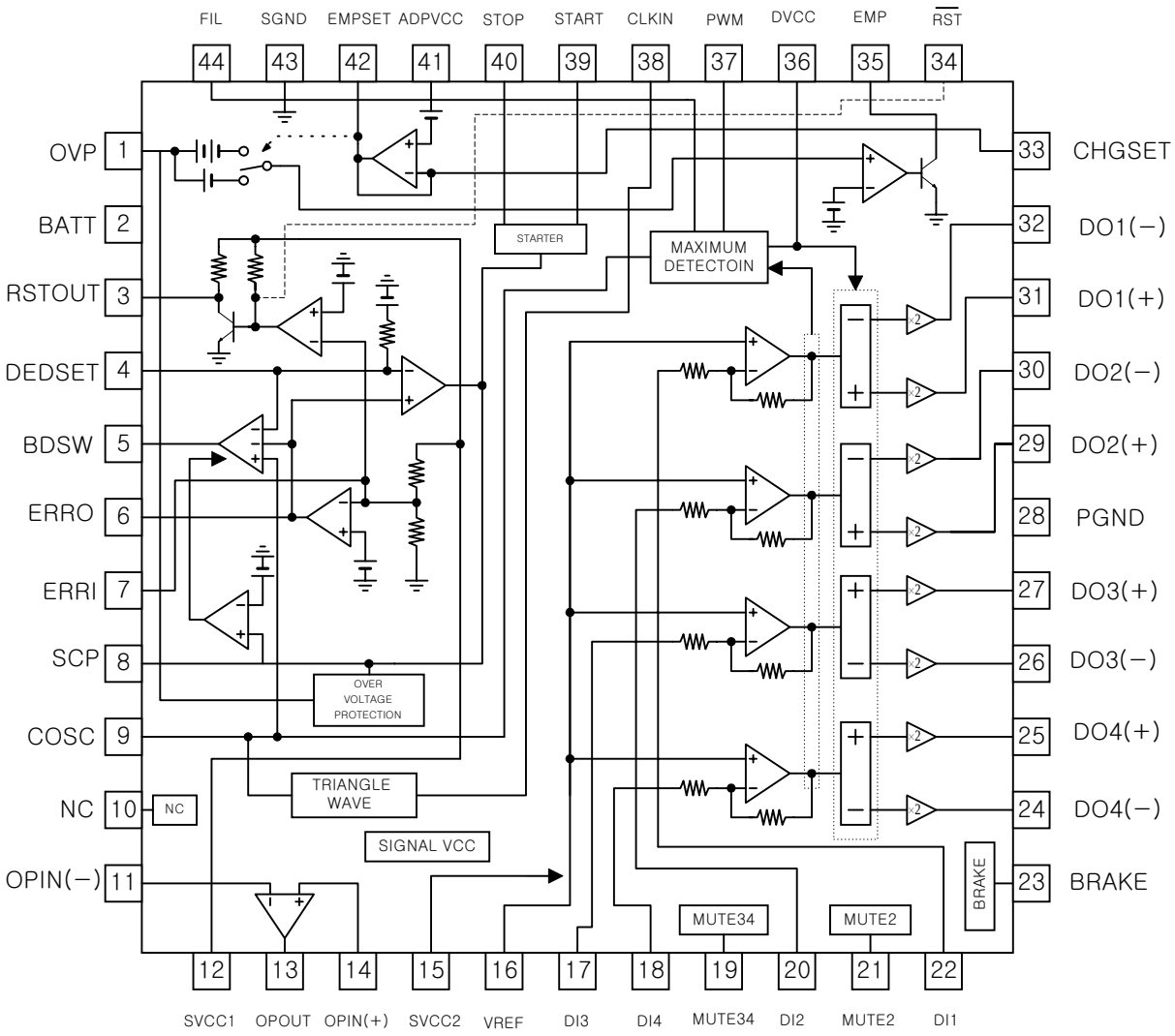


DC MOTOR DRIVE IC

Pin Definitions

Pin Number	Pin Name	Pin Function Descrition
1	OVP	Battery power supply mode
2	BATT	Battery power supply
3	RSTOUT	RSTOUT detection output
4	DEDSET	DEDSET time setting
5	BDSW	Booster transistor drive
6	ERRO	Error amp output
7	ERRI	Error amp input
8	SCP	Short circuit protection setting
9	COSC	Triangular wave output
10	N.C	No connection
11	OPIN(–)	Op-amp negative input
12	SVCC1	control circuit power supply
13	OPOUT	Op-amp output
14	OPIN(+)	Op-amp positive input
15	SVCC2	Pre-drive power supply
16	VREF	Reference voltage
17	DI3	CH3 control signal input
18	DI4	CH4 control signal input
19	MUTE34	CH3, 4 mute
20	DI2	CH2 control signal input
21	MUTE2	CH2 mute
22	DI1	CH1 control signal input
23	BRAKE	CH1 Brake
24	DO4(-)	CH4 negative output
25	DO4(+)	CH4 positive output
26	DO3(-)	CH3 negative output
27	DO3(+)	CH3 positive output
28	PGND	Power unit power ground
29	DO2(+)	CH2 positive output
30	DO2(-)	CH2 negative output
31	DO1(+)	CH1 positive output
32	DO1(-)	CH1 negative output
33	CHGSET	Charge current setting
34	RST	RSTOUT inverting output
35	EMP	Empty detection output
36	DVCC	H-bridge power supply
37	PWM	PWM transistor drive
38	CLKIN	External clock input
39	START	Boost DC/DC converter starting
40	STOP	Boost DC/DC converter off
41	ADPVCC	Charging circuit power supply
42	EMPSET	Empty dection level converting
43	SGND	Signal ground
44	FIL	PWM phase compensation

Internal Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V_{CC}	13.2	V
Maximum output current	I_O	500	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	–35 ~ +85	°C
Stroage temperature	T_{STG}	–55 ~ +150	°C

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charging circuit power supply voltage	ADPVCC	3.0	4.5	8.0	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Control Circuit Power Supply voltage	SVCC	2.7	3.2	5.5	V
PRE-DRIVER V_{CC}	SVCC2	2.7	3.2	5.5	V
Output Voltage	VM	-	PWM	BATT	V
Operating Temperature	Ta	-10	25	70	°C

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, VREF=1.6V, ADPVCC=0V, fCLKIN=88.2KHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
COMMON SECTION						
BATT stand-by current	I_{ST}	BATT=10.5V,SVCC1,2=VREF=0V	-	-	5	µA
BATT supply current (No load)	I_{BATT}	DVCC=0.45V, MUTE34=3.2V	-	2.5	3.5	mA
SVCC supply current (NO load)	I_{SVCC1}	DVCC=0.45V, MUTE34=3.2V, ERRI=0V	-	3.0	3.5	mA
SVCC2 supply current (No load)	I_{SVCC2}	DVCC=0.45V, MUTE34=3.2V	-	3.5	5.0	mA
ADPVCC supply current (No load)	I_{ADPVCC}	ADPVCC=4.5V, ROUT=OPEN	-	0.2	1.0	mA
H-DRIVE PART						
Voltage gain CH1, 3, 4 CH2	$G_{VC}134$ $G_{VC}2$	-	12 21.5	14 23.5	16 24.5	dB
Gain error by polarity	ΔG_{VC}	-	–2	0	2	dB
Input pin resistance CH1,3,4 CH2	$R_{DI}134$ $R_{DI}2$	IN=1.7 & 1.8V	9 6	11 7.5	13 9	KΩ
Maximum output voltage	V_{OUT}	RL=8Ω, DVCC=BATT=4V, IN=0 ~ 3.2V	1.9	2.1	-	V
Saturation voltage (Lower)	V_{SAT1}	IO=–300mA, IN=0 & 3.2V	-	240	400	mV
Saturation voltage (Upper)	V_{SAT2}	IO=300mA, IN=0 & 3.2V	-	240	400	mV
Input offset voltage	V_{IO}	-	–8	0	8	mV
Output offset voltage CH1,3,4 CH2	$V_{OO}134$ $V_{OO}2$	VREF=IN=1.6V	–70 –130	0 0	70 130	mV
DEAD zone	V_{DB}	-	–30	0	30	mV
Brake1 on voltage	V_{M1ON}	DI1=1.8V	2.0	-	-	V
Brake1 off voltage	V_{M1OFF}	DI1=1.8V	-	-	0.8	V
MUTE2 on voltage	V_{M2ON}	DI2=1.8V	2.0	-	-	V
MUTE2 off voltage	V_{M2OFF}	DI2=1.8V	-	-	0.8	V
MUTE34 on voltage	V_{M34ON}	DI3=DI4=1.8V	-	-	0.8	V
MUTE34 off voltage	V_{M34OFF}	DI3=DI4=1.8V	2.0	-	-	V
VREF on voltage	V_{REFON}	INn=1.8V(N=1, 2, 3, 4)	1.2	-	-	V
VREF off voltage	V_{REFOFF}	INn=1.8V(N=1, 2, 3, 4)	-	-	0.8	V
BRAKE1 brake current	I_{BRAKE}	brake current	4	7	10	mA

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
PWM POWER SUPPLY DRIVING						
PWM sink current	I_{PWM}	DI1=2.1V	10	13	17	mA
DVCC level shift voltage	V_{SHIF}	DI1=1.8V, DVCC-OUT1F	0.35	0.45	0.55	V
DVCC leak current	I_{DLK}	DVCC=9V, SVCC1,2=BATT=0V	-	0	5	µA
PWM amp transfer gain	G_{PWM}	DI1=1.8V, DVCC=1.2V ~ 1.4V	1/60	1/50	1/40	1/KΩ
DC/DC CONVERTER						
ERROR AMP						
SVCC1 pin threshold voltage	V_{S1TH}	-	3.05	3.20	3.35	V
ERRO pin output voltage H	V_{EOH}	ERRI=0.7V, IO=–100µA	1.4	1.6	-	V
ERRO pin output voltage L	V_{EOL}	ERRI=1.3V, IO=100µA	-	-	0.3	V
SHORT CIRCUIT PROTECTION						
SCP pin voltage	V_{SCP}	ERRI=1.3V	-	0	0.1	V
SCP pin current 1	I_{SCP1}	ERRI=0.7V	6	10	16	µA
SCP pin current 2	I_{SCP2}	ERRI=1.3V, OFF=0V	12	20	32	µA
SCP pin current 3	I_{SCP3}	ERRI=1.3V, BATT=9.5V	12	20	32	µA
SCP pin impedance	R_{SCP}	-	175	220	265	KΩ
SCP pin threshold voltage	V_{SCPTH}	ERRI=0.7V, COSC=470PF	1.10	1.20	1.30	V
Over-voltage protection detect	V_{OVP}	OVP Voltage	9.5	10	10.5	V
TRANSISTOR DRIVING						
BDSW pin output voltage 1H	V_{SW1H}	BATT=COSC=1.5V =SVCC2=0V, 10mA	0.78	0.98	1.13	V
BDSW pin output voltage 2H	V_{SW2H}	COSC=0V, IO=–10mA, ERRI=0.7V SCP=0V	1.0	1.5	-	V
BDSW pin output voltage 2L	V_{SW2L}	CT=2V, IO=1-mA	-	0.3	0.45	V
BDSW pin oscillating reequency 1	f_{SW1}	COSC=470pF, =SVCC2=0V	65	80	95	KHz
SW pin oscillating reequency 2	f_{SW2}	COSC=470pF, CLKIN=0V	60	70	82	KHz
BDSW pin oscillating reequency 3	f_{SW3}	COSC=470pF	-	88.2	-	KHz
BDSW pin minimum pulse width	T_{SWMIN}	COSC=470pF, ERRO=0.5 → 0.7V	0.01	-	0.6	µs
Pulse duty start	D_{SW1}	COSC=470PF, SVSS1,SVCC2=0V	40	50	60	%
MAX. pulse duty at self-running	D_{SW2}	COSC=470pF, ERR0=0.8V, CLKIN=0V	50	60	70	%
MAX. pulse duty at CLKIN synchronization	D_{SW3}	ERR0=0.8V, COSC=470pF	45	55	65	%

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
DEAD TIME						
DEDSET pin impedance	R_{DEDSET}	-	52	65	78	KΩ
DEDSET pin output voltage	V_{DEDSET}	-	0.78	0.88	0.98	V
INTERFACE						
STOP pin threshold voltage	V_{STOPTH}	ERRI=1.3V	2.0	-	-	V
STOP pin bias current	I_{STOP}	OFF=0V	75	95	115	μA
START pin on threshold voltage	V_{STATH1}	SVCC1,SVCC2=0V, COSC=2V	1.3	-	-	V
START pin off threshold voltage	V_{STATH2}	SVCC1,SVCC2=0V, COSC=2V	-	-	2.1	V
START pin bias current	I_{START}	START=0V	13	16	19	μA
CLKIN pin threshold voltage H	$V_{CLKINTH H}$	-	2.0	-	-	V
CLKIN pin threshold voltage L	$V_{CLKINTH L}$	-	-	-	0.8	V
CLKIN pin bias current	I_{CLKIN}	CLKIN=3.2V	-	-	10	μA
START CURCUIT						
Starter switching voltage	V_{SSV}	SVCC1,SVCC2=0V → 3.2V START=0V	2.3	2.5	2.7	V
Starter switching hysteresis width	V_{SSHS}	START=0V	130	200	300	mV
Discharge release voltage	V_{DIS}	-	1.63	1.83	2.03	V
RESET CIRCUIT						
SVCC1 RESET threshold voltage ratio	R_{RSTOTH}	-	85	90	95	%
RESET detection hysteresis width	V_{RSTHS}	-	25	50	100	mV
RSTOUT pin output voltage	V_{RSTO}	IO=1mA, SVCC1,SVCC2=2.8V	-	-	0.5	V
RSTOUT pin pull up resistance	R_{RSTO}	-	72	90	108	KΩ
RST pin output voltage 1	V_{RST1}	IO=−1mA, SVCC1,SVCC2=2.8V	2.0	-	2.4	V
RST pin output voltage 2	V_{RST2}	IO=−1mA, SVCC1,SVCC2=0V	2.0	-	2.4	V
RST pin pull up resistance	R_{RST}	-	77	95	113	KΩ

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
OP-AMP						
Input bias current	I_{BIAS}	IN(+)=1.6V	-	-	300	nA
Input offset voltage	V_{OFOP}	IN(+)=1.6V	–5.5	0	5.5	mV
High level output voltage	V_{OHOP}	RL=OPEN	2.8	-	-	V
Low level output voltage	V_{OLOP}	RL=OPEN	-	-	0.2	V
Output drive current (Source)	V_{SOURCE}	50Ω GND	-	–6.5	–3.0	mA
Output drive current (Sink)	V_{SINK}	50Ω SVCC	0.4	0.7	-	mA
Open loop voltage gain	GVO	VIN=–75dB, F=1KHz	-	70	-	dB
Slew rate	SR	-	-	0.5	-	V/μs
BATTERY CHARGING CURCUIT						
CHGSET pin bias voltage	V_{CHGSET}	ADPVCC=4.5V, CHGSET=1.8KΩ	0.71	0.81	0.91	V
CHGSET pin output resistance	R_{CHGSET}	ADPVCC=4.5V	0.75	0.95	1.20	KΩ
EMPSET pin leak current 1	I_{EMPSET}	ADPVCC=4.5V, CHGSET=OPEN	-	-	1.0	μA
EMPSET pin leak current 2	I_{EMPSET}	ADPVCC=0.6V, CHGSET=1.8KΩ	-	-	1.0	μA
EMPSET pin saturation voltage	V_{EMPSET}	ADPVCC=4.5V, IO=300mA, CHGSET=0Ω	-	0.45	1.0	V
EMPTY DETECTION						
EMP detection voltge 1	V_{EMPT1}	V_{EMPSET}=0V	2.1	2.2	2.3	V
EMP detection voltge 2	V_{EMPT2}	I_{EMPSET}=–2μA	1.7	1.8	1.9	V
EMP detection hysteresis voltage 1	V_{EMHS1}	V_{EMPSET}=0V	25	50	100	mV
EMP detection hysteresis voltage 2	V_{EMHS2}	I_{EMPSET}=–2μA	25	50	100	mV
EMP pin output voltage	V_{EMP}	IO=1mA, OVP=1V	-	-	0.5	V
EMP pin output leak current	I_{EMPLK}	OVP=2.4V	-	-	1.0	μA
OVP pin input resistance	R_{OVP}	V_{EMPSET}=0V	17	23	27	KΩ
OVP pin leak current	I_{OVPLK}	SVCC1=SVCC2=0V, OVP=4.5V	-	-	1.0	V
EMP_SET pin detection voltage	V_{EMPSET}	V_{EMPSET}=BATT-$_{EMPSET}$, OVP=2V	1.5	-	-	V
EMP_SET pin detection current	I_{EMPSET}	EMPSET	–2	-	-	μA

Application Information

1. MUTE FUNCTION

- When The BRAKE Pin is low is normal opration (high is CH1 mute on).
- When The Mute2 Pin is low is normal opration (high is CH2 mute on).
- When The Mute34 Pin is high is normal opration (low is CH3,4 mute on).

2. VREF DROP MUTE (FIGURE 1)

- When the Voltage of the mute pin is above 1V, the mute circuit is stopped and the output circuit is.

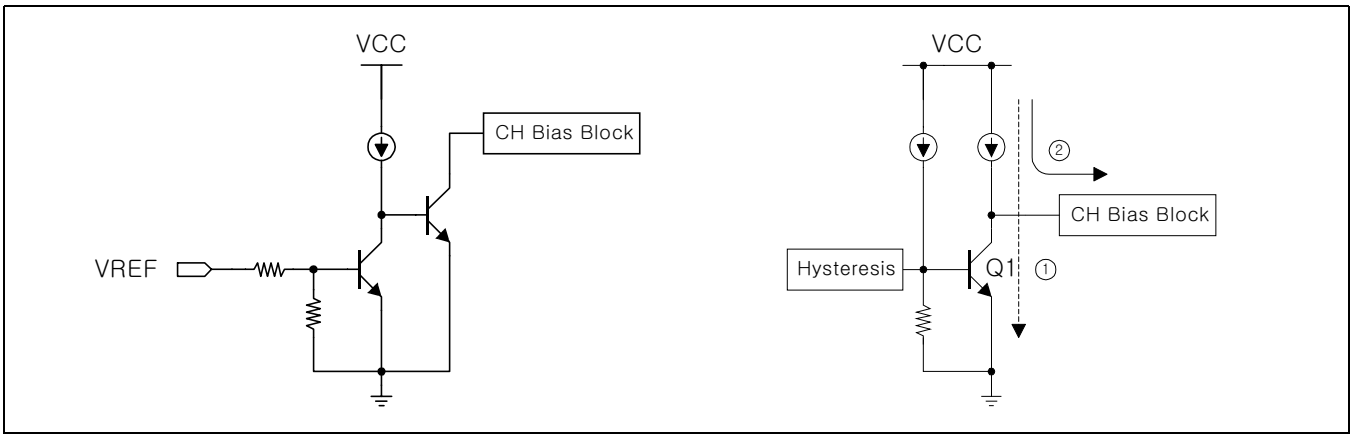


Figure 1. VREF Drop MUTE Circuit

Figure 2. TSD Circuit

3. THERMAL SHUTDOWN(FIGURE 2)

- If the chip temperature rises above 150°C, then the thermal shutdown (TSD) circuit is activated and the output circuit will be mute.

4. H-BRIDGE DRIVER (4-CHANNELS)

Driver input resistance is 10KΩ of CH1, CH3, CH4 and input resistance of CH2 is 7.5KΩ.

Driver gain can obtain under -mentioned

CH1, 3, 4: $GV = 20\log\left|\frac{55K}{11K + R}\right|$

CH2 $GV = 20\log\left|\frac{110K}{7.5K + R}\right|$

R is External resistance.

5. SWITCHING REGULATED POWER SUPPLY DRIVE

- This circuit detects a maximum output value of 4CH drivers and then generates PWM Signal.
- External Component is PNP-Tr, Coil, Schottky Diodeand Capacitor .

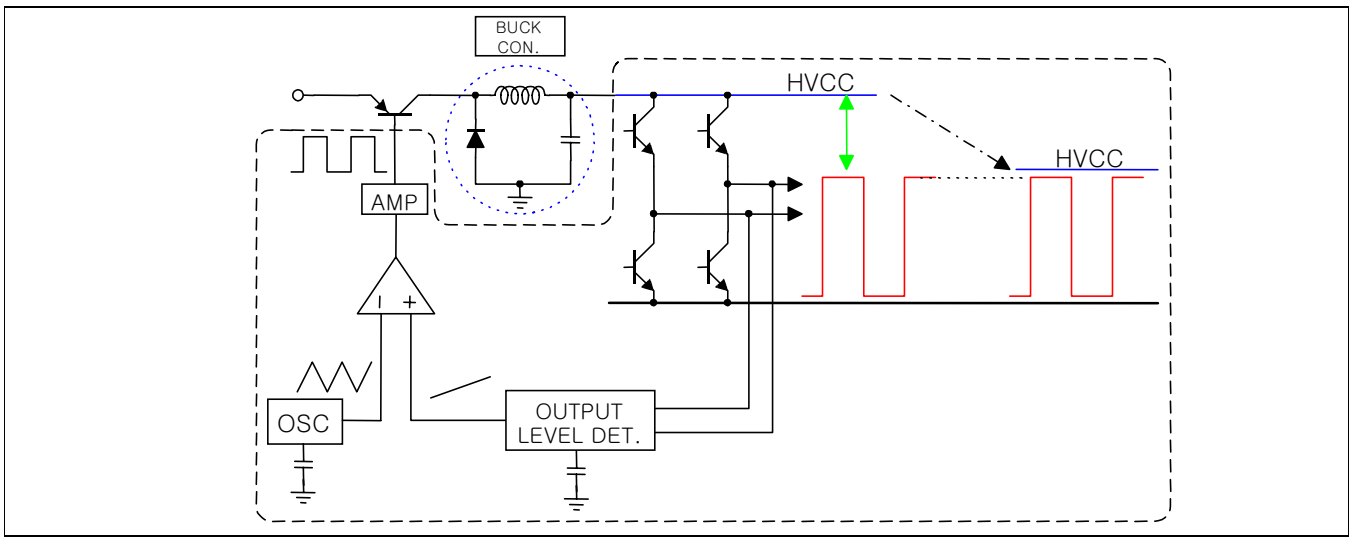


Figure 1. Switching Regulated Power Supply

6. DC/DC CONVERTER CONTROL CIRCUIT

- Booster circuit needs External component. and the voltage() is defined as follows.

$$SVCC1 = 1.267 \times \frac{\frac{R1 \cdot R3}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}}$$

R1 = Resistor1
R2 = Resistor2
R3 = 30KΩ
R4 = 30.5KΩ

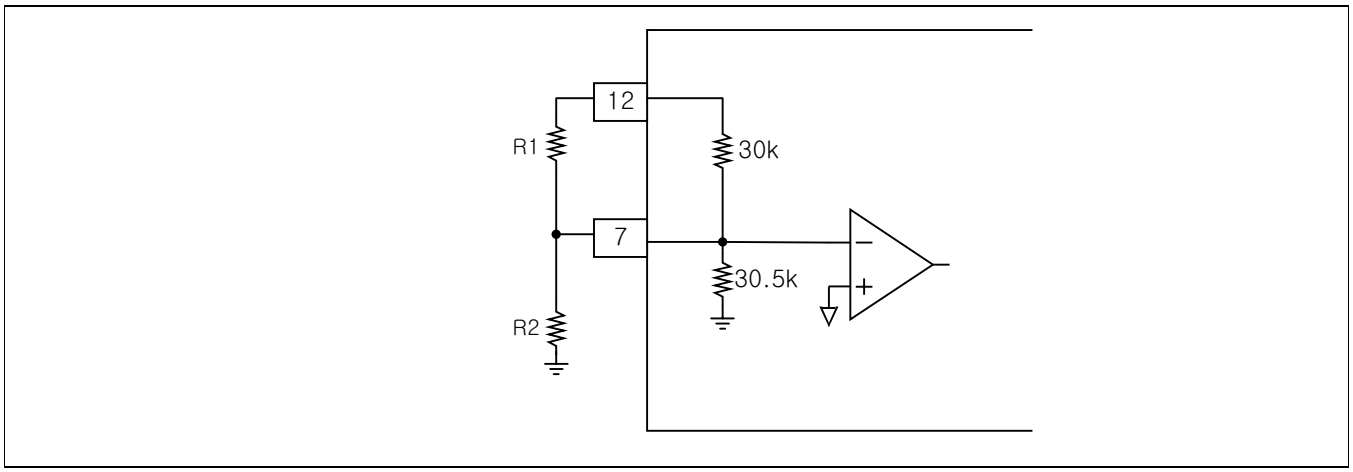


Figure 2. Output Voltage

- Short Circuit Protection function when GND and is short, ERRI become LOW and ERRO HIGH and it makes capacitor charging. fanally AMP3 is OFF.(figure 5)

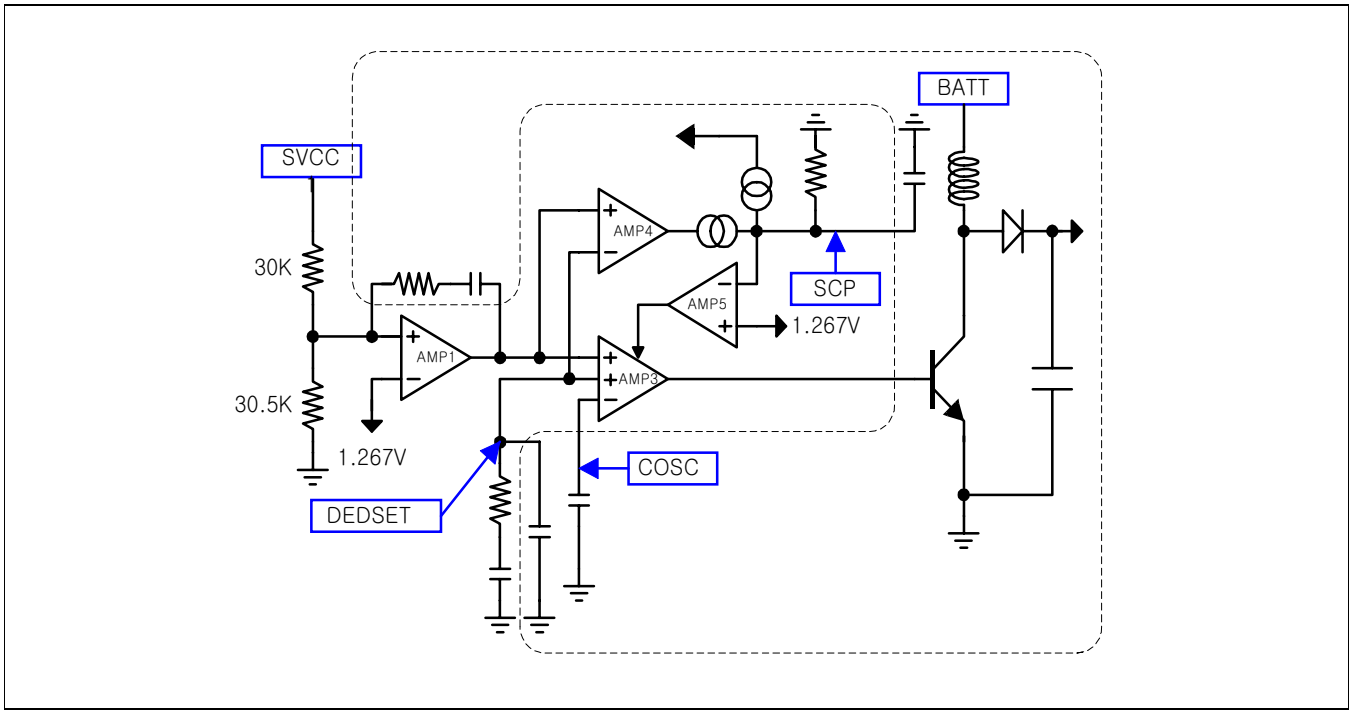


Figure 3. DC/DC Converter Control Circuit

Switching off time depen on a capacitor of the SCP . and the equation is as follow.

$$t = C_{SCP} \times \frac{V_{TH}}{I_{SCP}} \qquad (V_{TH} = 1.25V,\ I_{SPRT} = 10\mu A)$$

- Max Duty can be controlled resistor. the equation is as follow.

$$t = C_{DEDSET} \times R \qquad (R = 65K\Omega)$$

- Capacitor of the SCP terminal can control disable switiching time and it can be calculated by as follow equation.

$$t = C_{SCP} \times \frac{V_{TH}}{I_{STOP}} \qquad (V_{TH} = 1.25V,\ I_{OFF} = 20\mu A)$$

- Over Voltage Protection BATT Voltage is over 9.7V charging SCP terminal Capacitor, it reach to V_{TH} SW terminal signal is OFF the equation is as follow

$$t = C_{SCP} \times \frac{V_{TH}}{I_{HV}} \qquad (V_{TH} = 1.25V,\ I_{HV} = 20\mu A)$$

- If Output Voltage of RSTOUT Circuit DC/DC Conver is over than 90%, RSTOUT terminal turn to HIGH and Hysteresis is 50mV. and RSTOUT stste is ON.

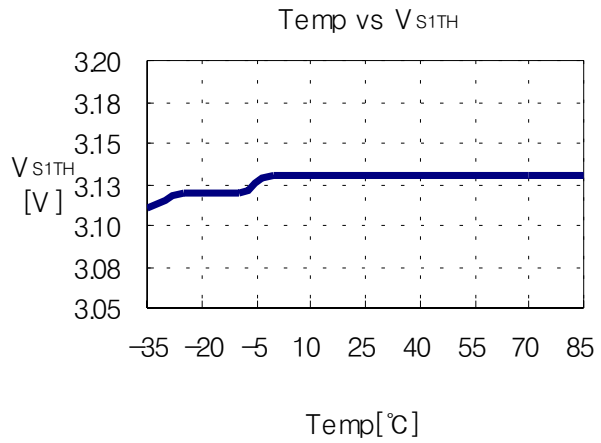
7. EMPTY DETECTING CIRCUIT.

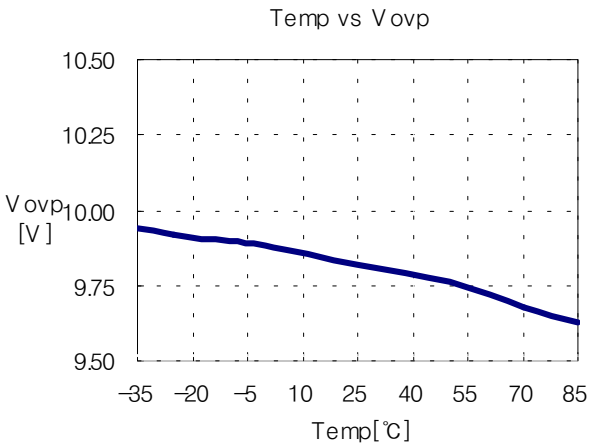
EMPSET	Detect Voltage	Hysteresis	Mode
LOW	2.2V	50mV	Battery Mode
HIGH-Z	1.8V	50mV	Adapter Mode

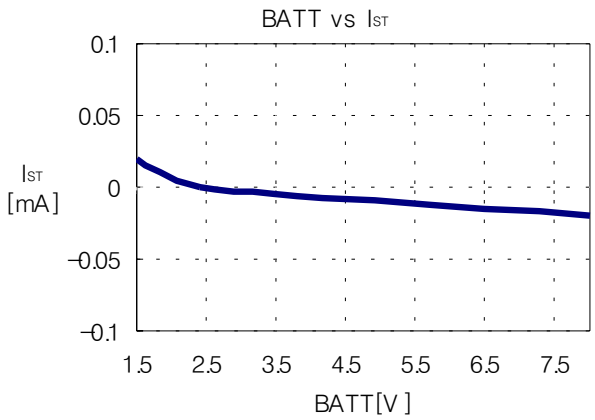
8. BATTERY CHARGING CIRCUIT

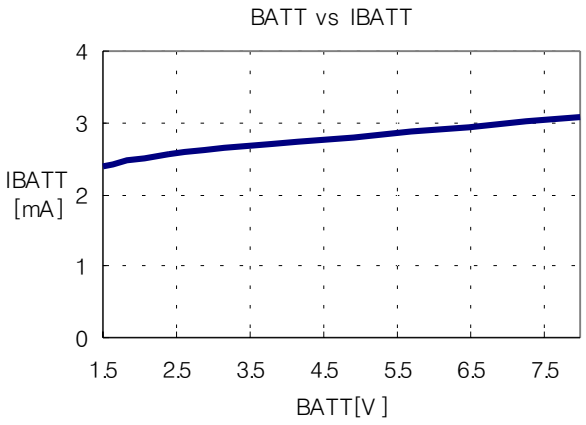
- the battery charger circuit is separated from any other block .
- TSD operate at 150°C. Hysteresis is 30°C

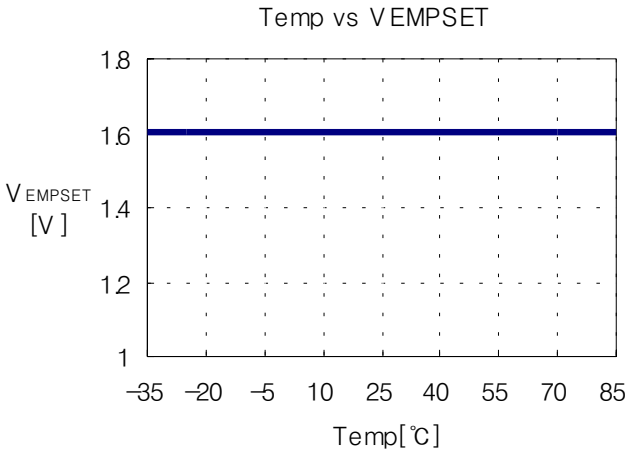
Typical Perfomance Characteristics

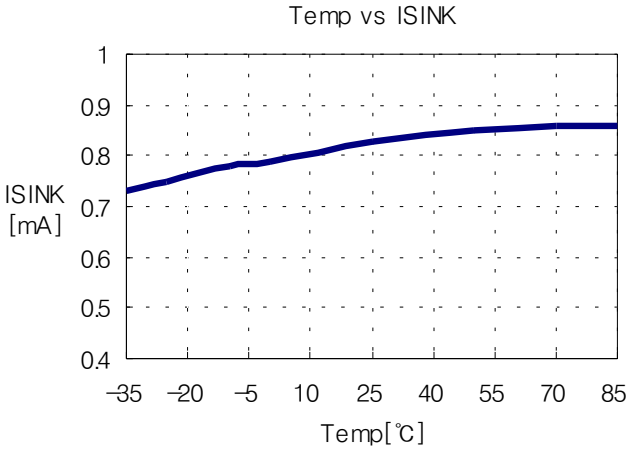




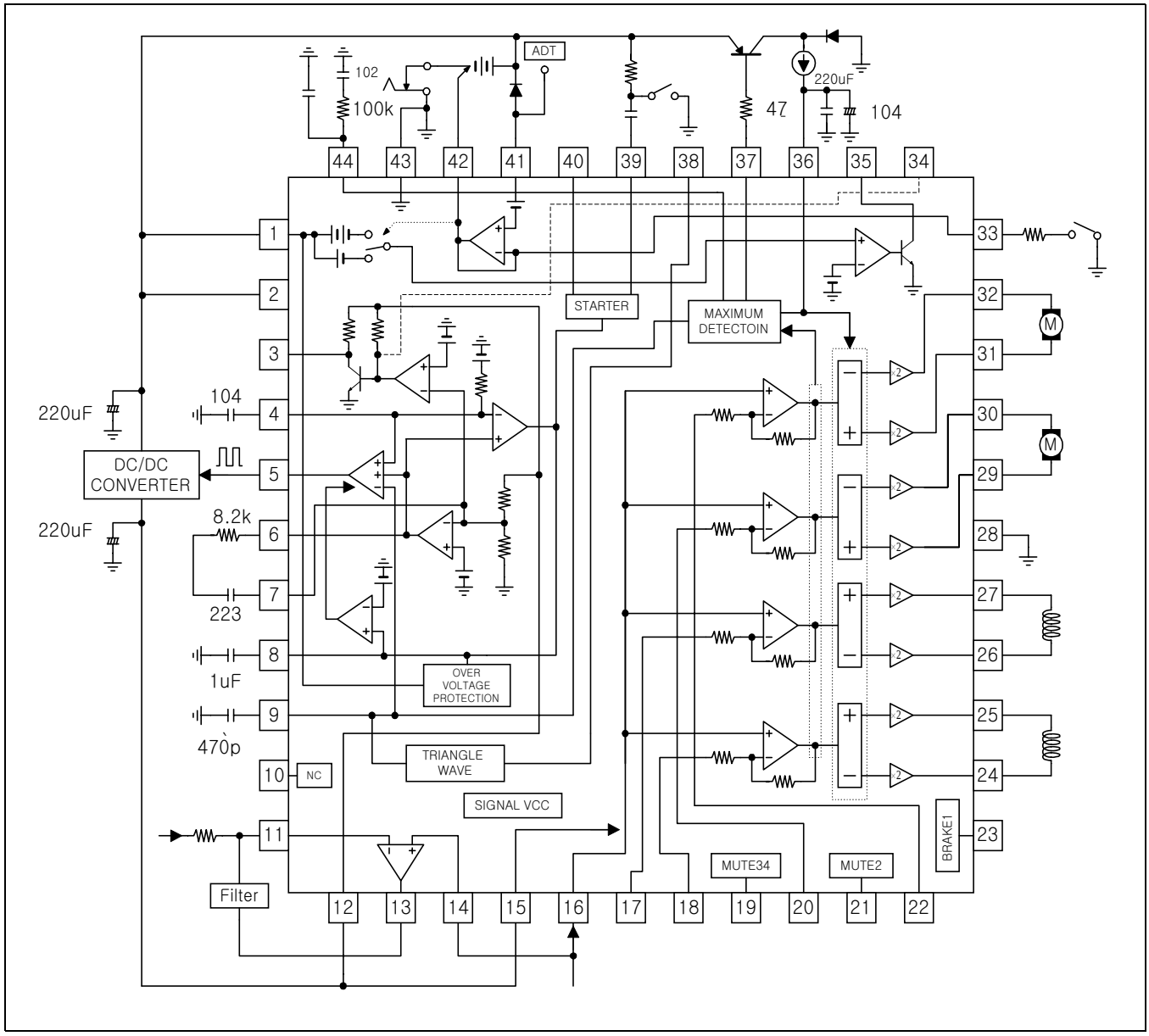








Typical Application Circuits



Ordering Information

Device	Package	Operating Temperature
FAN8038	44-QFP-1010B	–35°C ~ +85°C

DC MOTOR DRIVE IC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAN8725 (KA3025)

Spindle and 5-CH Driver

Features

Common

- Built-in thermal shutdown circuit (TSD)
- Built-in power save circuit
- 3 Independent voltage source
- Corresponds to 3.3V or 5V DSP

Spindle

- Built-in hall bias
- Built-in FG signal output circuit
- Built-in rotational direction detecting circuit
- Built-in protection circuit for reverse rotation
- Built-in short brake circuit

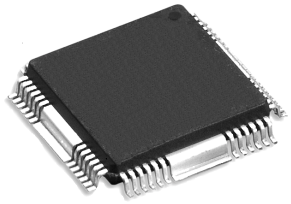
BTL (5-channel)

- Built-in 5-CH balanced transformerless (BTL) driver
- Built-in Level shift circuit
- Independent voltage sources
  - VM2 = CH1,CH2 / VM3 = CH3, CH4 ,CH5

Description

The FAN8725 is a monolithic IC suitable for a 3-phase BLDC spindle motor driver and 5-ch motor drivers which drives the focus actuator, tracking actuator, loading motor, stepping motor driver of the CD-media systems.

48-QFPH-1414

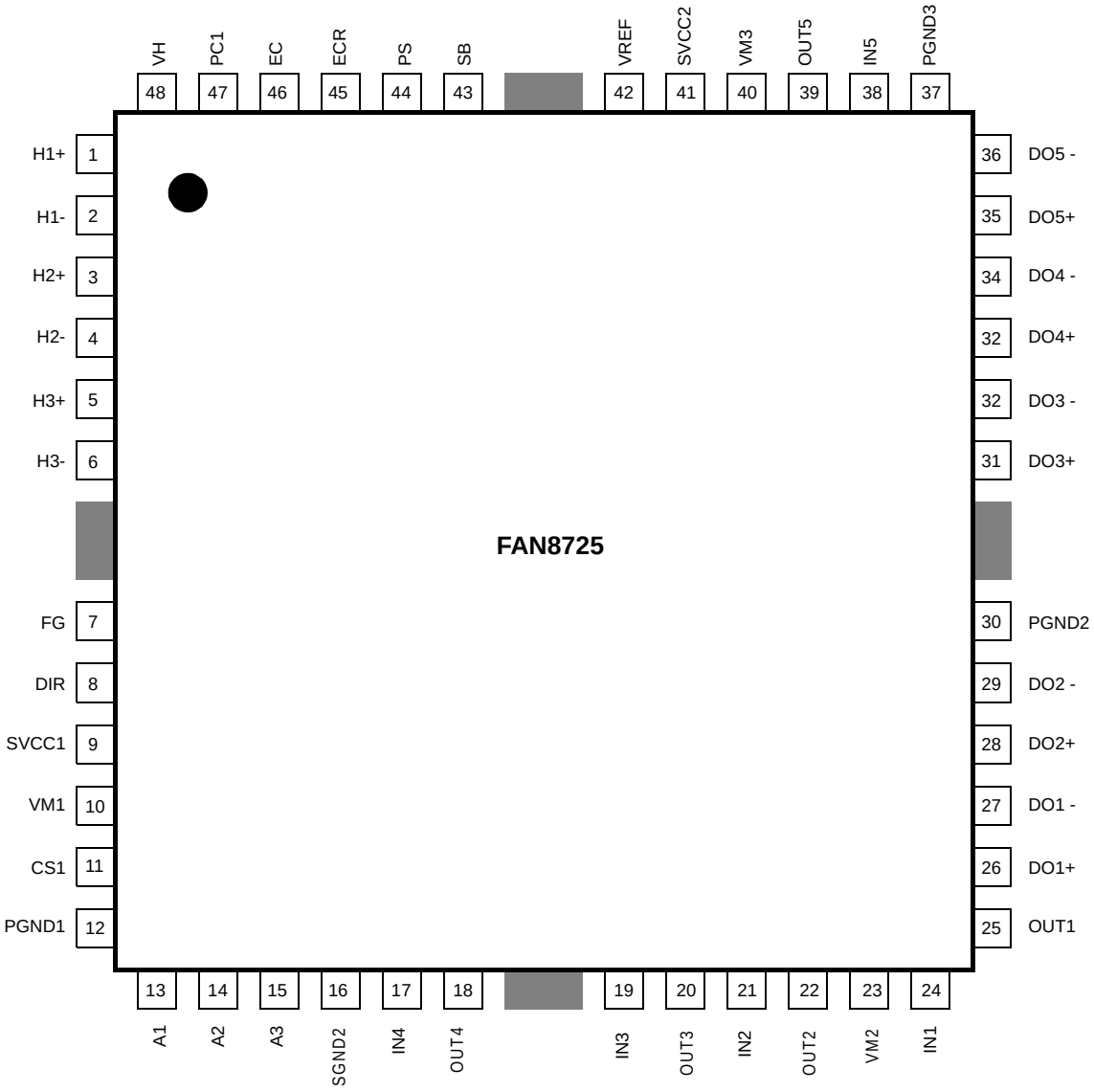


CD-MEDIA ONE CHIP IC

Typical Applications

- Compact disc ROM
- Digital video disc ROM
- Compact disc recorderable
- Digital video disc player
- Compact disc player

Pin Assignments



Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	H1-	I	Hall 1(-) input
2	H1+	I	Hall 1(+) input
3	H2+	I	Hall 2(-) input
4	H2-	I	Hall 2(+) input
5	H3+	I	Hall 3(-) input
6	H3-	I	Hall 3(+) input
7	FG	O	Frequency Generator output
8	DIR	O	Rotation direction output
9	SVCC1	-	Spindle Signal supply voltage
10	VM1	-	Spindle power supply
11	CS1	I	Spindle current sense
12	PGND1	-	Spindle power ground
13	A1	O	3-phase output1
14	A2	O	3-phase output2
15	A3	O	3-phase output3
16	SGND2	-	CH signal ground
17	IN4	I	OP-Amp CH 4 input(-)
18	OUT4	O	OP-Amp CH 4 output
19	IN3	I	OP-Amp CH 3 input(-)
20	OUT3	O	OP-Amp CH 3 output
21	IN2	I	OP-Amp CH 2 input(-)
22	OUT2	O	OP-Amp CH 2 output
23	VM2	-	CH1/CH2 power supply
24	IN1	I	OP-Amp CH 1 input(-)
25	OUT1	O	OP-Amp CH 1 output
26	DO1+	O	Channel 1 output (+)
27	DO1 -	O	Channel 1 output (–)
28	DO2+	O	Channel 2 output (+)
29	DO2 -	O	Channel 2 output (–)
30	PGND2	-	CH1/CH2 power ground
31	DO3+	O	Channel 3 output (+)
32	DO3 -	O	Channel 3 output (–)
33	DO4+	O	Channel 4 output (+)

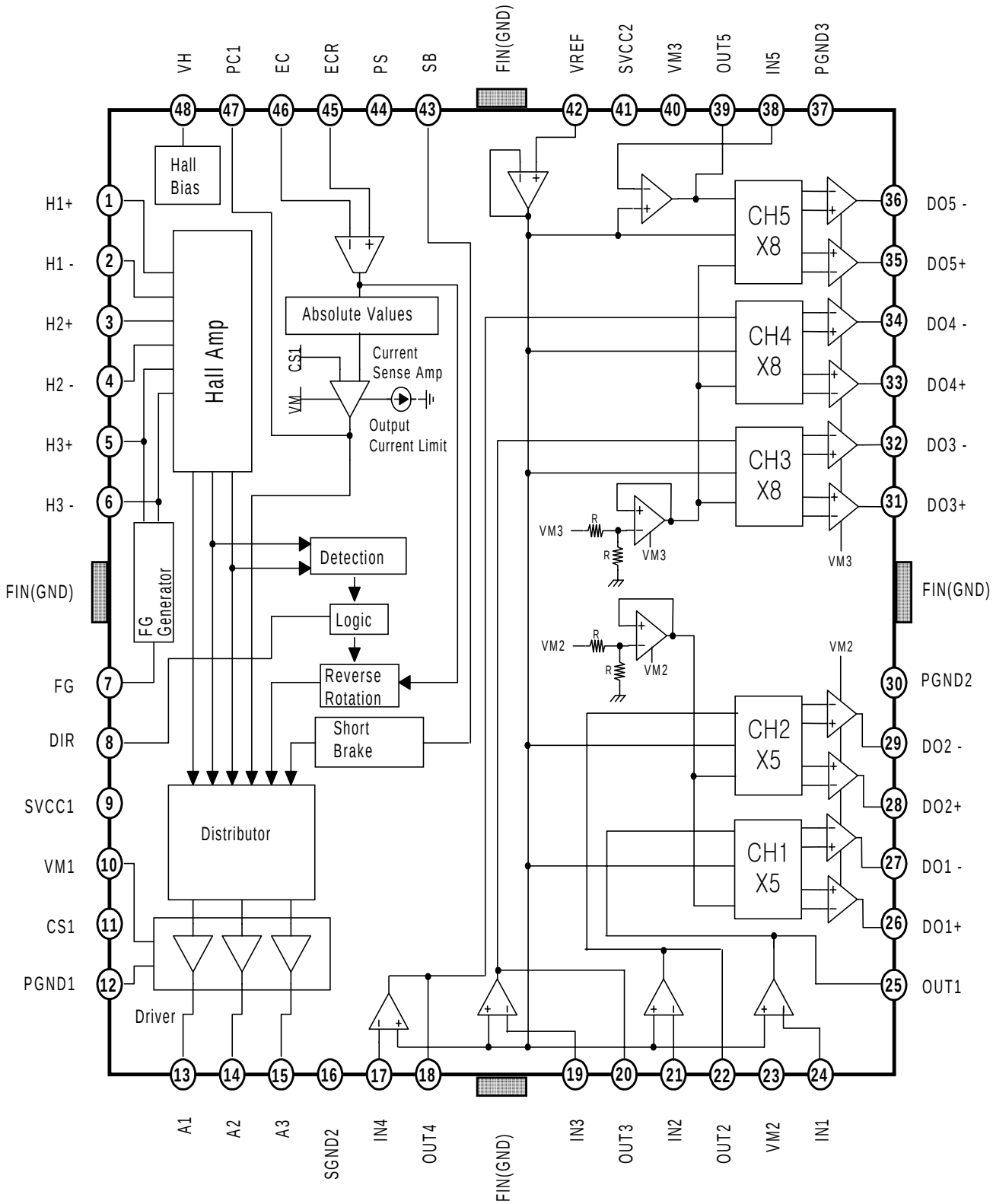
Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Description
34	DO4 -	O	Channel 4 output (–)
35	DO5+	O	Channel 5 output (+)
36	DO5-	O	Channel 5 output (–)
37	PGND3	-	CH3/CH4/CH5 power ground
38	IN5	I	OP-Amp CH 5 input(-)
39	OUT5	O	OP-Amp CH 5 output
40	VM3	-	CH3/CH4/CH5 power supply
41	SVCC2	-	CH Signal supply voltage
42	VREF	I	BTL reference voltage
43	SB	I	Short brake
44	PS	I	Power save
45	ECR	I	Torque control reference
46	EC	I	Torque control
47	PC1	-	Phase compensation capacitor
48	VH	I	Hall bias

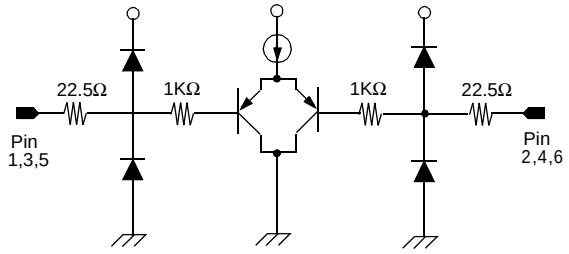
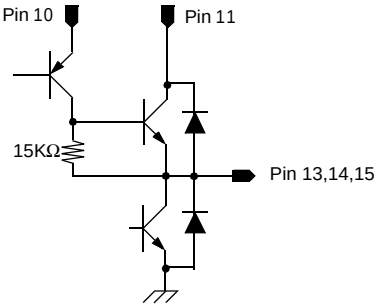
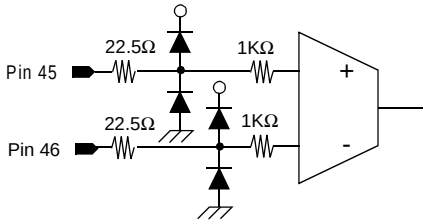
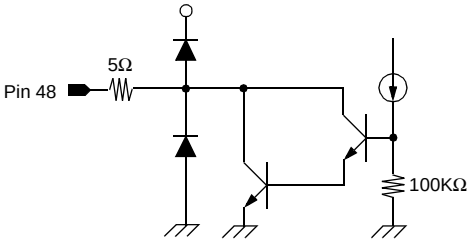
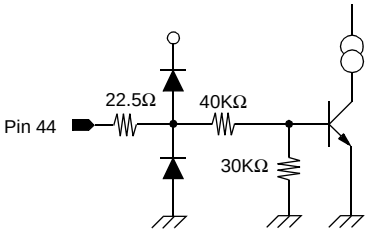
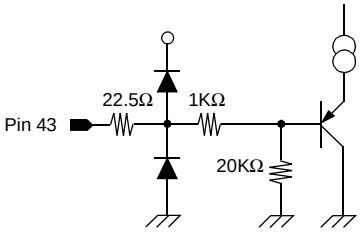
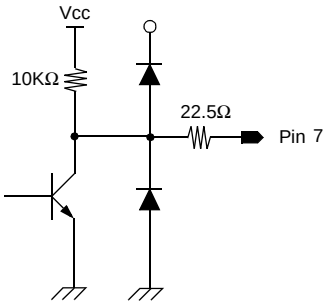
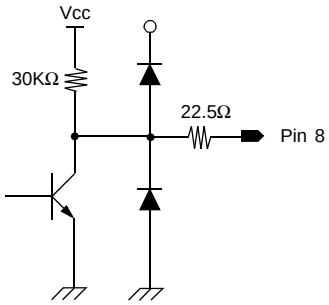
Notes:

BTL drive part symbol(+,- outputs of drives) is determined according to the polarity of input pin.
(For example, if the voltage of pin 24 is high, the output of pin 26 is high)

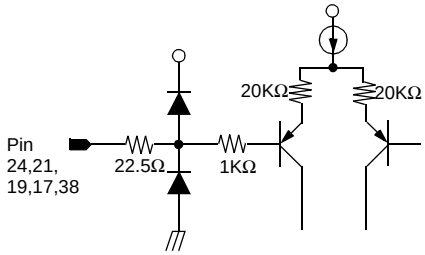
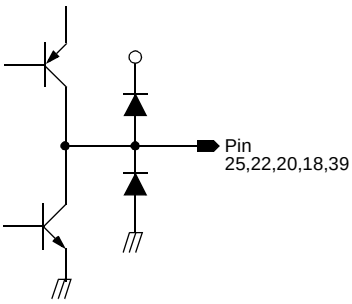
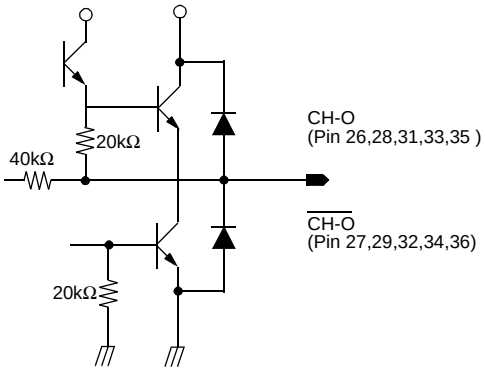
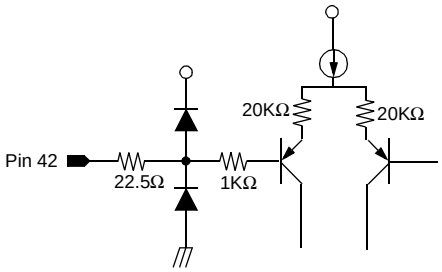
Internal Block Diagram



Equivalent Circuits (Spindle Part)

HALL INPUT	DRIVER OUTPUT
	
TORQUE CONTROL INPUT	**HALL BIAS INPUT**
	
POWER SAVE INPUT	**SHORT BRAKE INPUT**
	
FG OUTPUT	**DIR OUTPUT**
	

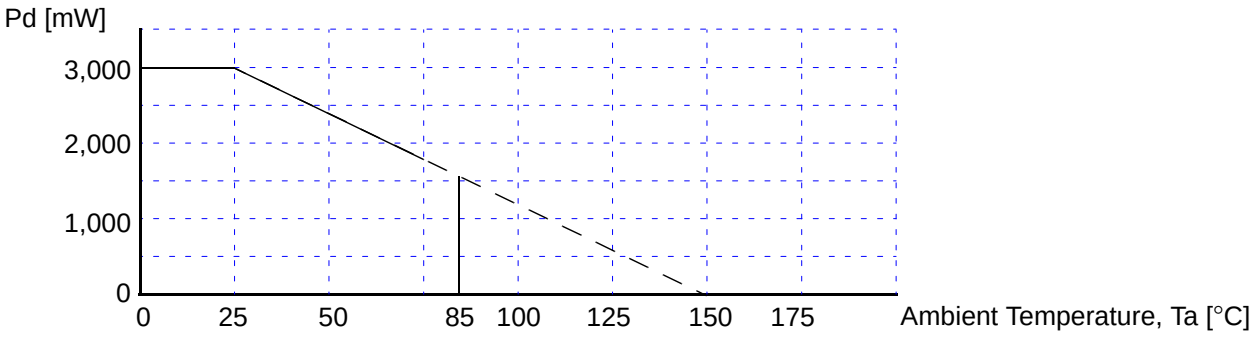
Equivalent Circuits (BTL Part)

OP-AMP INPUT	OP-AMP OUTPUT
	
DRIVE OUTPUT	**VREF**
	

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage (Spindle Signal)	SV_{CC1max}	7	V
Supply Voltage (BTL Signal)	SV_{CC2max}	15	V
Supply Voltage (Spindle Motor)	V_{M1max}	15	V
Supply Voltage (BTL CH1/2)	V_{M2max}	15	V
Supply Voltage (BTL CH3/4/5)	V_{M3max}	15	V
Power Dissipation	P_D	@3.0	W
Operating Temperature Range	T_{OPR}	-20 ~ +75	°C
Storage Temperature Range	T_{STG}	-55 ~ +150	°C
Maximum Output Current (Spindle Part)	I_{Omaxa}	1.3	A
Maximum Output Current (BTL Part)	I_{Omaxb}	0.6	A

@: 1. When mounted on 70mm × 70 mm × 1.6mm PCB (Phenolic resin material)
2. Power dissipation is reduced 24 mW/°C for using above Ta=25°C
3. Do not exceed P_D and SOA(Safe Operating Area).



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage (Spindle Signal)	SV_{CC1}	4.5	–	5.5	V
Operating Supply Voltage (BTL Signal)	SV_{CC2}	10.8	–	13.2	V
Operating Supply Voltage (Spindle Motor)	V_{M1}	10.8	–	13.2	V
Operating Supply Voltage (BTL CH1/2)	V_{M2}	4.5	–	SV_{CC2}	V
Operating Supply Voltage (BTL CH3/4/5)	V_{M3}	4.5	–	SV_{CC2}	V

Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
FULL CHIP						
Quiescent Circuit Current 1	I_{CC1}	FULL CHIP (PS=0V)	–	0	0.2	mA
Quiescent Circuit Current 2	I_{CC2}	SPINDLE (PS=5V)	–	5	10	mA
Quiescent Circuit Current 3	I_{CC3}	BTL (PS=5V)	–	20	30	mA
POWER SAVE						
On Voltage Range	V_{PSon}	L-H Circuit On	2.5	–	Vcc	V
Off Voltage Range	V_{PSoff}	H-L Circuit Off	–	–	1.0	V
HALL BIAS						
Hall Bias Voltage	V_{HB}	I_{HB}=20mA	0.4	1.0	1.8	V
HALL AMP						
Hall Bias Current	I_{HA}		–	0.5	2	uA
Common Mode Input Range	V_{HAR}		1.5	–	4.0	V
Minimum in Level	V_{INH}		100	–	–	mVpp
H1 Hysteresis	V_{HYS}		5	20	40	mVpp
TORQUE CONTROL						
Ecr In Voltage Range	E_{CR}		0.2	–	4.0	V
Ec In Voltage Range	E_C		0.2	–	4.0	V
Offset Voltage (-)	E_{Coff-}	E_C =1.9V	-80	-50	-20	mV
Offset Voltage (+)	E_{Coff+}	E_{CR} =1.9V	20	50	80	mV
E_C In Current	E_{Cin}	E_C=1.9V	-3	-0.5	–	uA
E_{CR} In Current	E_{CRin}	E_{CR}=1.9V	-3	-0.5	–	uA
In/output Gain	G_{EC}	E_{CR}=2.5V, R_{CS}=0.5Ω	0.56	0.70	0.84	A / V
FG						
FG Output Voltage (H)	V_{FGh}	I_{FG}= -10uA	4.5	4.9	V_{CC}	V
FG Output Voltage (L)	V_{FHl}	I_{FG}=10uA	–	–	0.5	V
Duty(Reference Value)		R_{CS}=0.5Ω		50		%
OUTPUT BLOCK						
Saturation Voltage (upper TR)	V_{Oh}	I_O= -300mA	–	1.0	1.4	V
Saturation Voltage (lower TR)	V_{Ol}	I_O=300mA	–	0.4	0.7	V
Torque Limit Current	I_{TL}	R_{CS}=0.5Ω	560	700	840	mA
DIRECTION DETECTOR						
DIR Output Voltage (H)	V_{DIRh}	I_{FG}=-10uA	4.5	4.7		V
Dir Output Voltage (L)	V_{DIRl}	I_{FG}=10uA	–	–	0.5	V
SHORT BRAKE						
On Voltage Range	V_{SBon}		2.5	–	V_{CC}	V
Off Voltage Range	V_{SBoff}		0	–	1.0	V

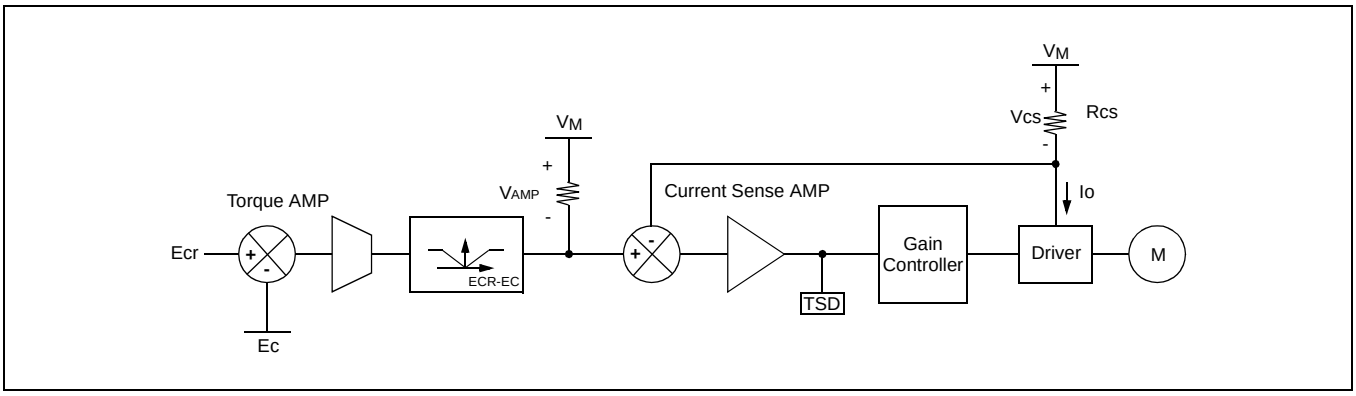
Electrical Characteristics (Continued)

BTL Drive Part (Ta=25°C, SV_{CC2}=12V, V_{M2}=5V, V_{M3}=12V, R_L=8, 24Ω)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CH1/CH2						
Output Offset Voltage1,2	$V_{OF1/2}$		-95	–	95	mV
Maximum Output Voltage1,2	$V_{OM1/2}$	V_{M2}=5V,RL=8Ω	3.6	4.0	–	V
Voltage Gain	$G_{VC1/2}$	V_{IN}=0.1Vrms, 1kHz	12.0	14.0	16.0	dB
CH3/CH4/CH5						
Output Offset Voltage3,4,5	$V_{OF3/4/5}$		-95	–	95	mV
Maximum Output Voltage3,4,5	$V_{OM3/4/5}$	V_{M3}=12V,RL=24Ω	8.4	10.5	–	V
Voltage Gain	$G_{VC3/4/5}$	V_{IN}=0.1Vrms, 1kHz	16.0	18.0	20.0	dB
OP-AMP PART						
Common Mode Input Range	V_{ICM}		0	–	11.0	V
Input Bias Current	I_B		-300	-30		nA
Low Level Output Voltage	V_{CL}			0.2	0.5	V
High Level Output Voltage	V_{OH}		10.0	11	–	V
Output Driving Source Current	I_{SOURCE}		1	4.0	–	mA
Output Driving Sink Current	I_{SINK}		5	10	–	mA

Application Information

1. TORQUE CONTROL & OUTPUT CURRENT CONTROL

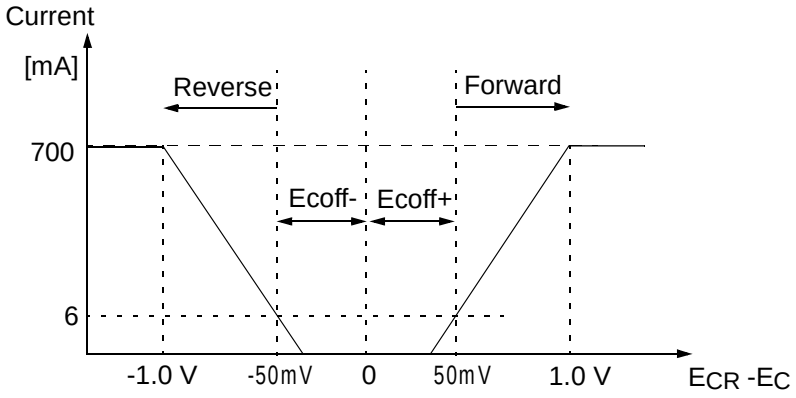


1) By amplifying the voltage difference between Ec and Ecr from Servo IC, the Torque Sense AMP produces the input (V_{AMP}) for the Current Sense AMP.

2) The output current (I_O) is converted into the voltage (V_{CS}) through the sense resistor (R_{CS}) and compared with the V_{AMP}. By the negative feedback loop, the sensed output voltage, VCS is equal to the input V_{AMP}. Therefore, the output current (I_O) is linearly controlled by the input V_{AMP}.

3) As a result, the signals, E_C and E_{CR} can control the velocity of the Motor by controlling the output current (I_O) of the Driver.

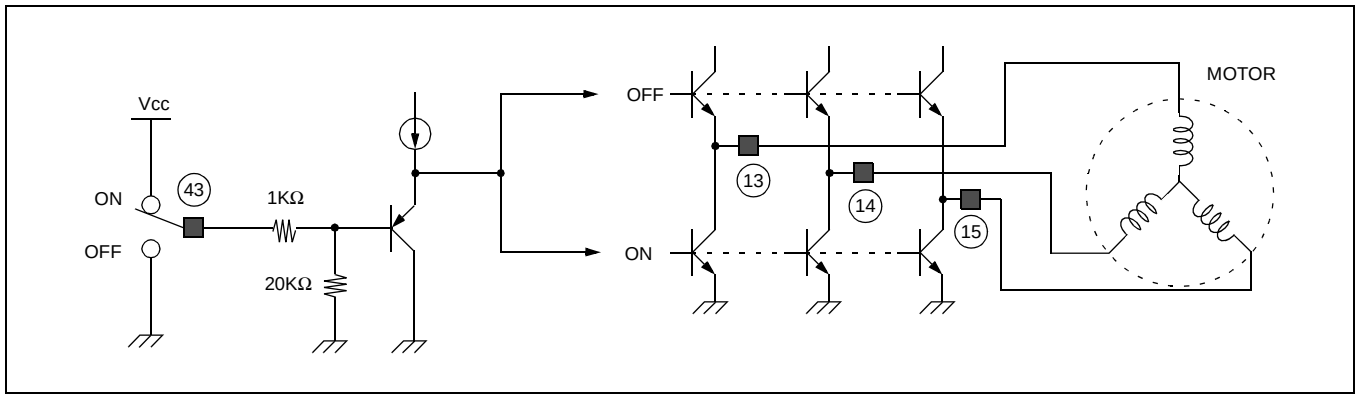
4) The range of the torque voltage is as shown below.



	Rotation
$E_{CR} > Ec$	Forward rotation
$E_{CR} < Ec$	Stop after detecting reverse rotation

The input range of E_{CR}, E_C is 0.2 V ~ 4.0 V (R_{CS} = 0.5[Ω])

2. SHORT BRAKE



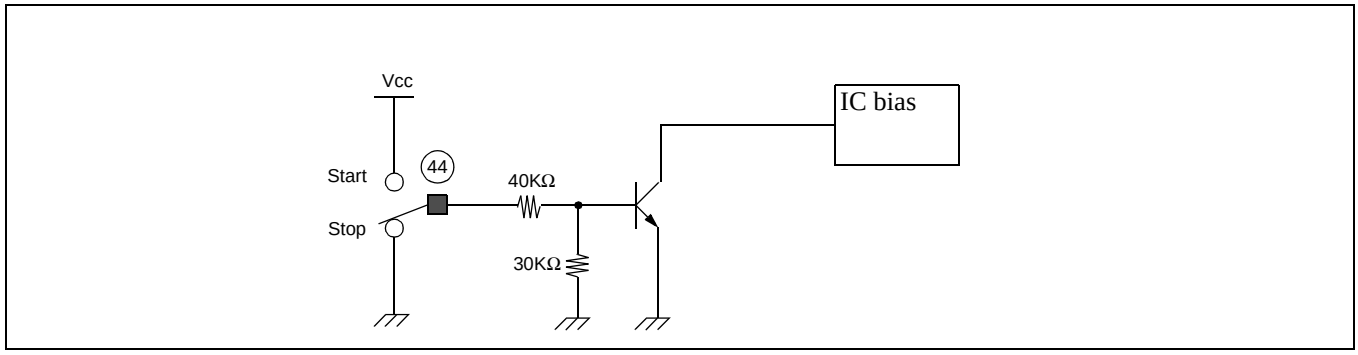
Pin # 43	Short Brake
HIGH	ON
LOW	OFF

When the pick-up part moves from the inner to the outer spindle of the CD, the Brake function of the reverse voltage is commonly employed to decrease the rotating velocity of the Spindle Motor.

However, if the Spindle Motor rotates rapidly, the Brake function of the reverse voltage may produce much heat at the Drive IC.

To remove this shortcoming and to enhance the braking efficiency, the Short Brake function is added to FAN8725. When the Short Brake function is activated, all upper Power TRs turn off and all lower Power TRs turn on, so as to make the rotating velocity of the motor slow down. But FG and DIR functions continue to operate normally.

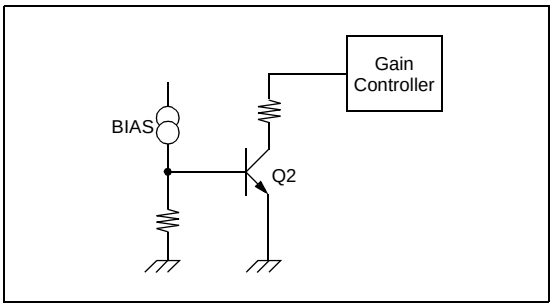
3. POWER SAVE



Pin # 44	Power Save
HIGH	Operate
LOW	Sleep mode

When PS function is activated, the chip is deactivated.

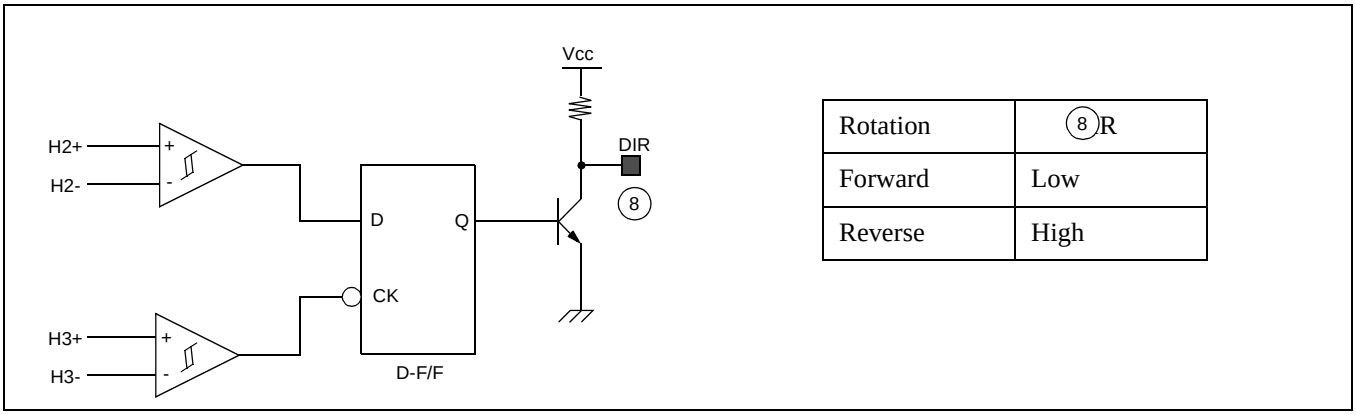
4. TSD (THERMAL SHUTDOWN)



When the chip temperature rises up to about 175C(degree), the Q2 turns on so that the output driver will be shutdown. When the chip temperature falls off to about 150C(degree), then the Q2 turns off so that the driver is to operate normally. Thus, TSD has the temperature hysteresis of about 25C(degree).

-- The TSD circuit shuts down all the power drives(spindle and BTL power drives) excluding both CH1 and CH2 power drives(actuator part).

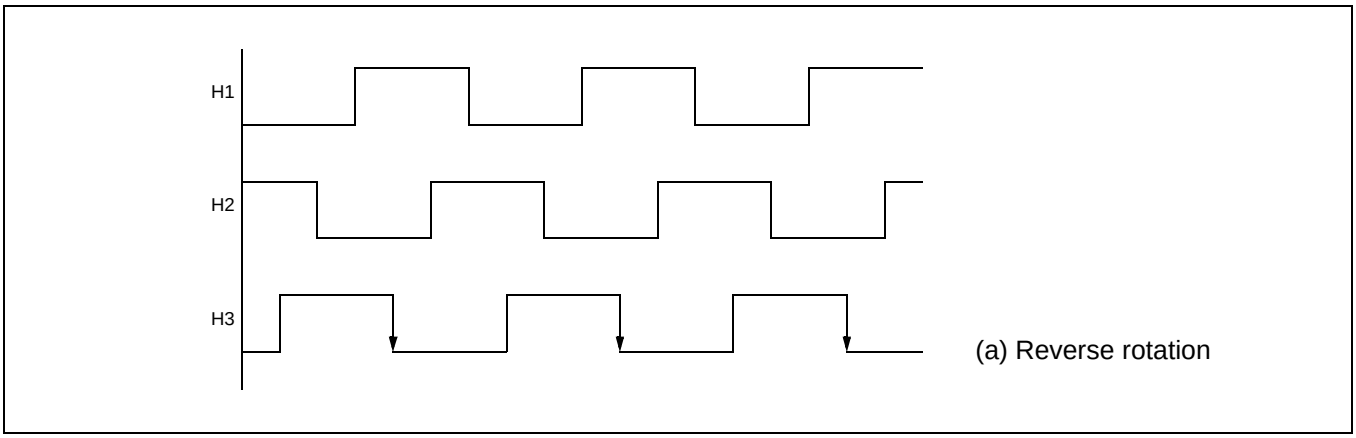
5. ROTATIONAL DIRECTION DETECTION



Rotation	⑧R
Forward	Low
Reverse	High

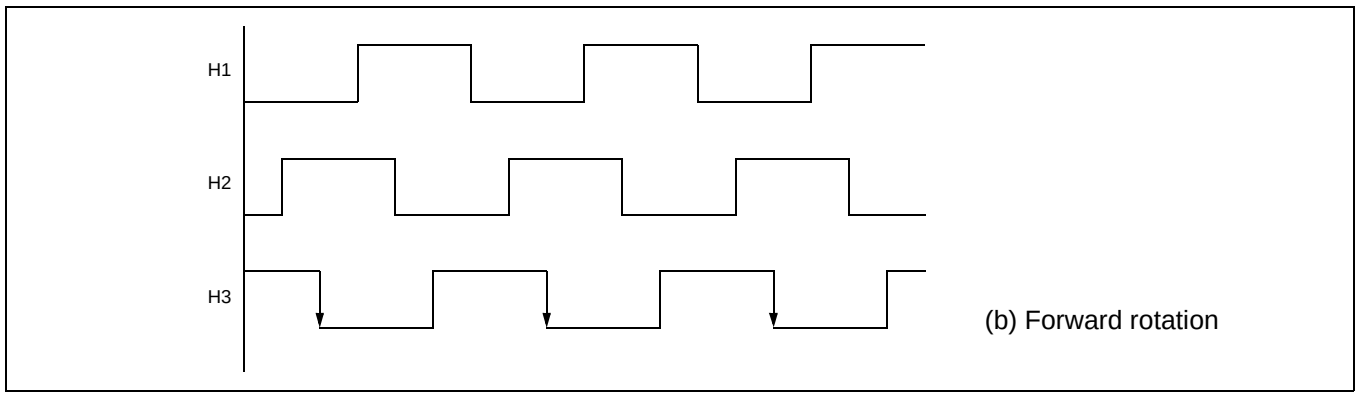
1) The forward and the reverse rotations of the CD are simply detected by using the D-F/F and the truth table is shown in the above table.

2) The rotational direction of the CD can be explained by the output waveform of the Hall sensors. Let the three outputs of Hall sensors be H1, H2 and H3 respectively.
When the spindle rotates in reverse direction, the Hall sensor output waveform are shown in Fig.(a). Thus the phases ordered in H1→H2→H3 with a 120° phase difference.



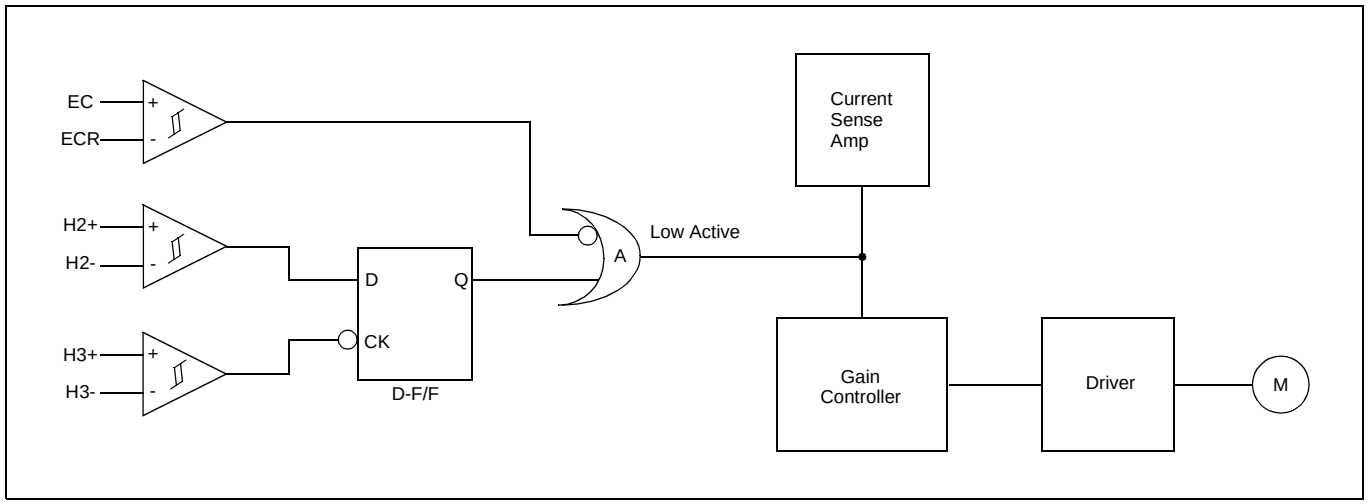
(a) Reverse rotation

On the other hand, if the spindle rotates in forward rotation, the phase relationship is H3ÆH2ÆH1 as shown in Fig.(b)



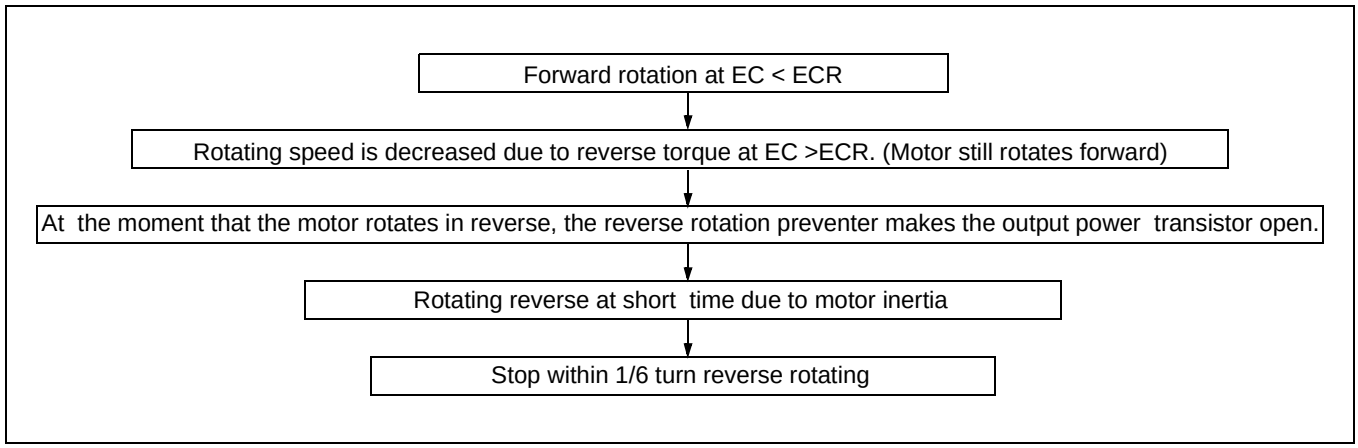
Therefore, the output of the rotational direction detector is Low, when the spindle rotates forward, while HIGH as in the case of the reverse rotation.

6. REVERSE ROTATION PREVENTION



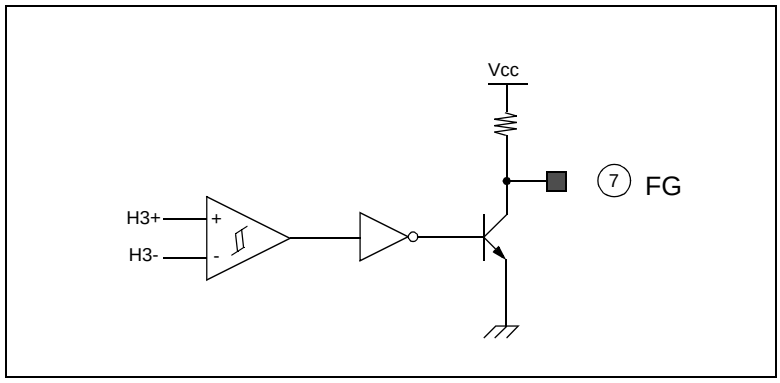
1) When the output of the OR Gate, A is LOW, it steers all the output current of the current sense Amp makes the current delivered to the Gain Controller zero. Thus the output current of the Driver becomes zero and the motor is stopped.

2) As in the state of the forward rotation, the D-F/F output, Q is HIGH and the motor rotates normally. At this state, if the control input is changed such that EC>ECR, then the motor rotates slowly more and more by the reverse commutation in the Driver. At the moment that the motor rotates in reverse direction, the D-F/F output becomes Low and the OR Gate output, thus, becomes LOW. This prevents the motor from rotating in reverse direction. The operation principle is shown in the table and the flow chart.

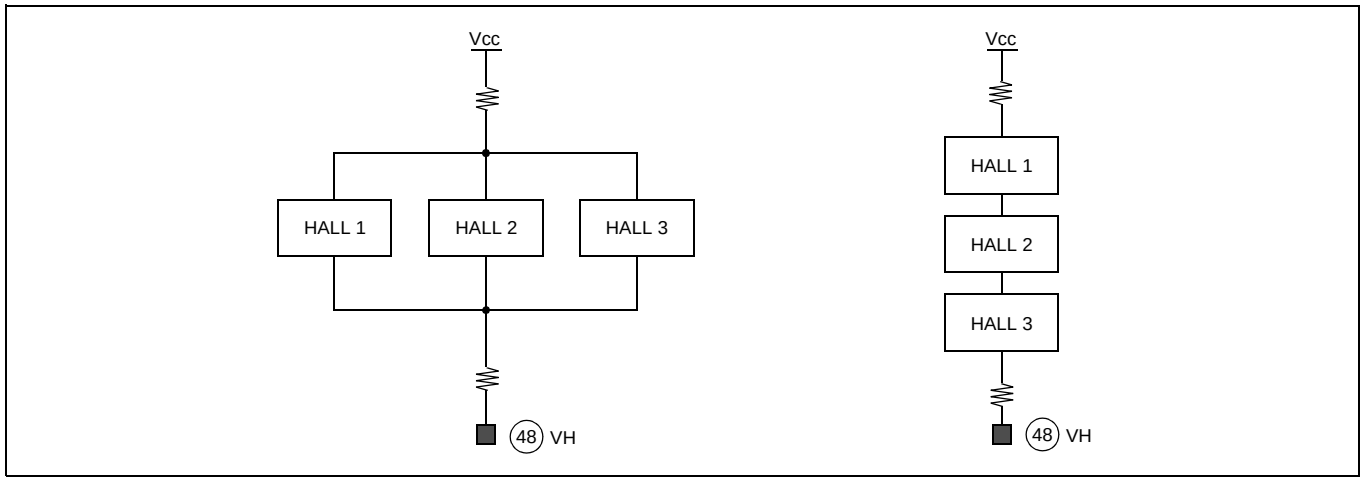


Rotation	H2	H3	D-F/F (Q)	Reverse Rotation Preventer	
				$E_{CR}>E_C$	$E_C>E_{CR}$
Forward	H	H→L	H	Forward	-
Reverse	L	H→L	L	-	Brake and Stop

7. FG OUTPUT

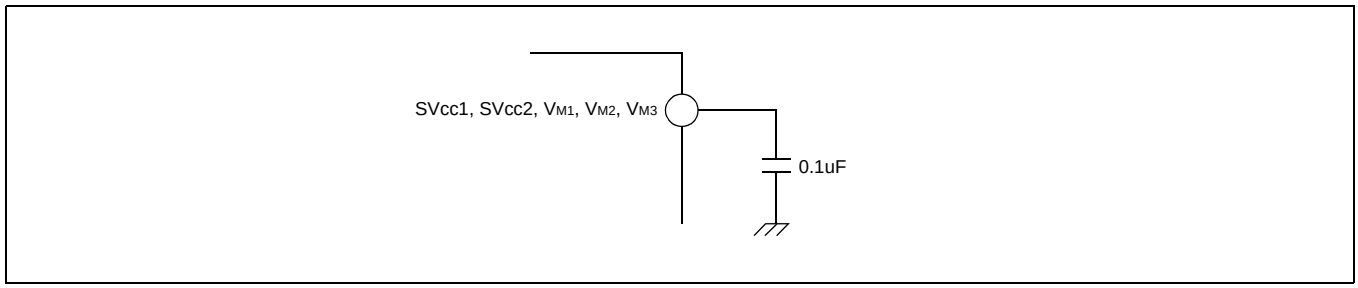


8. HALL SENSOR CONNECTION



9. CONNECT A BYPASS CAPACITOR, FROM ALL THE SUPPLY VOLTAGE SOURCES TO GROUND.

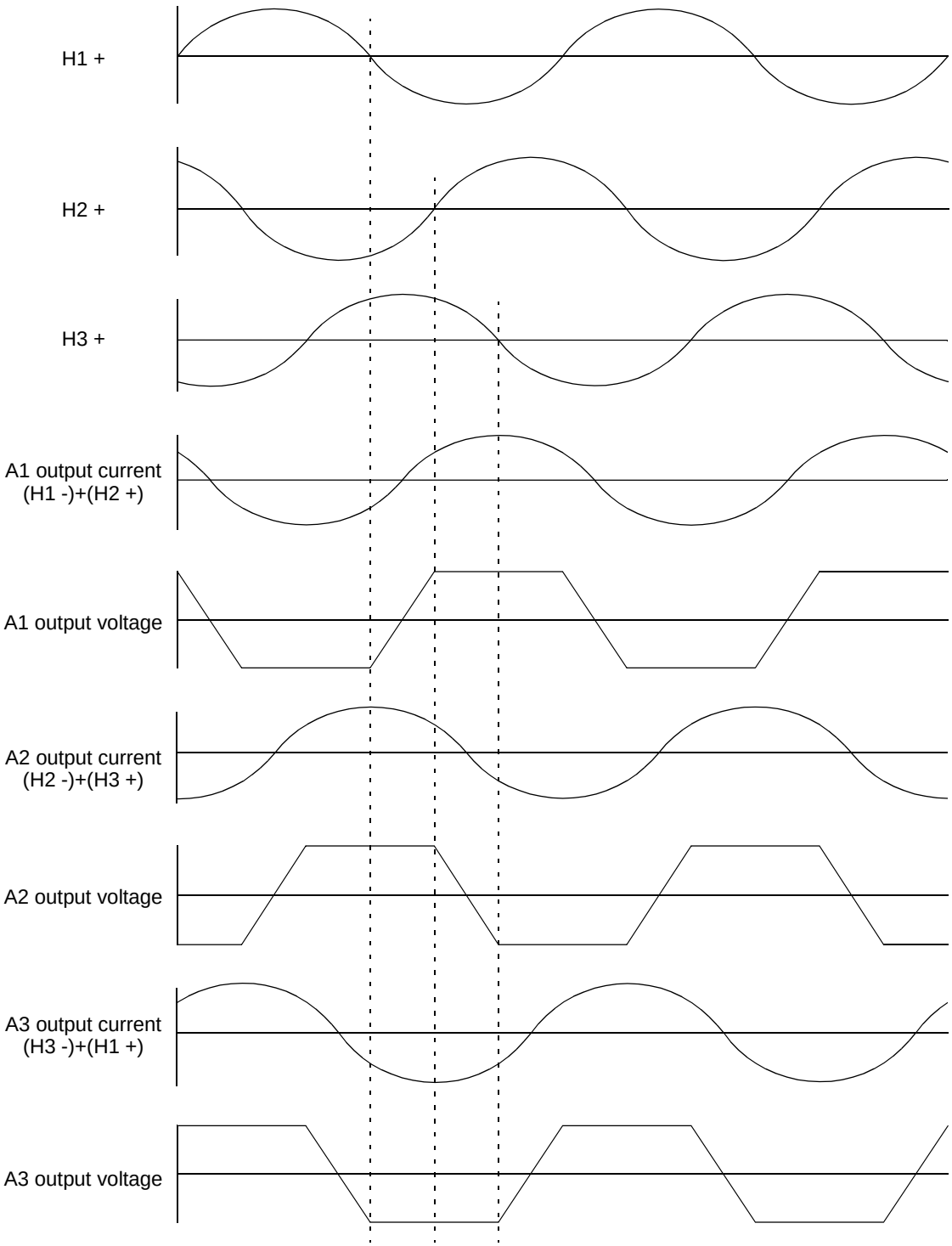
(Typically 0.1uF, or even higher)



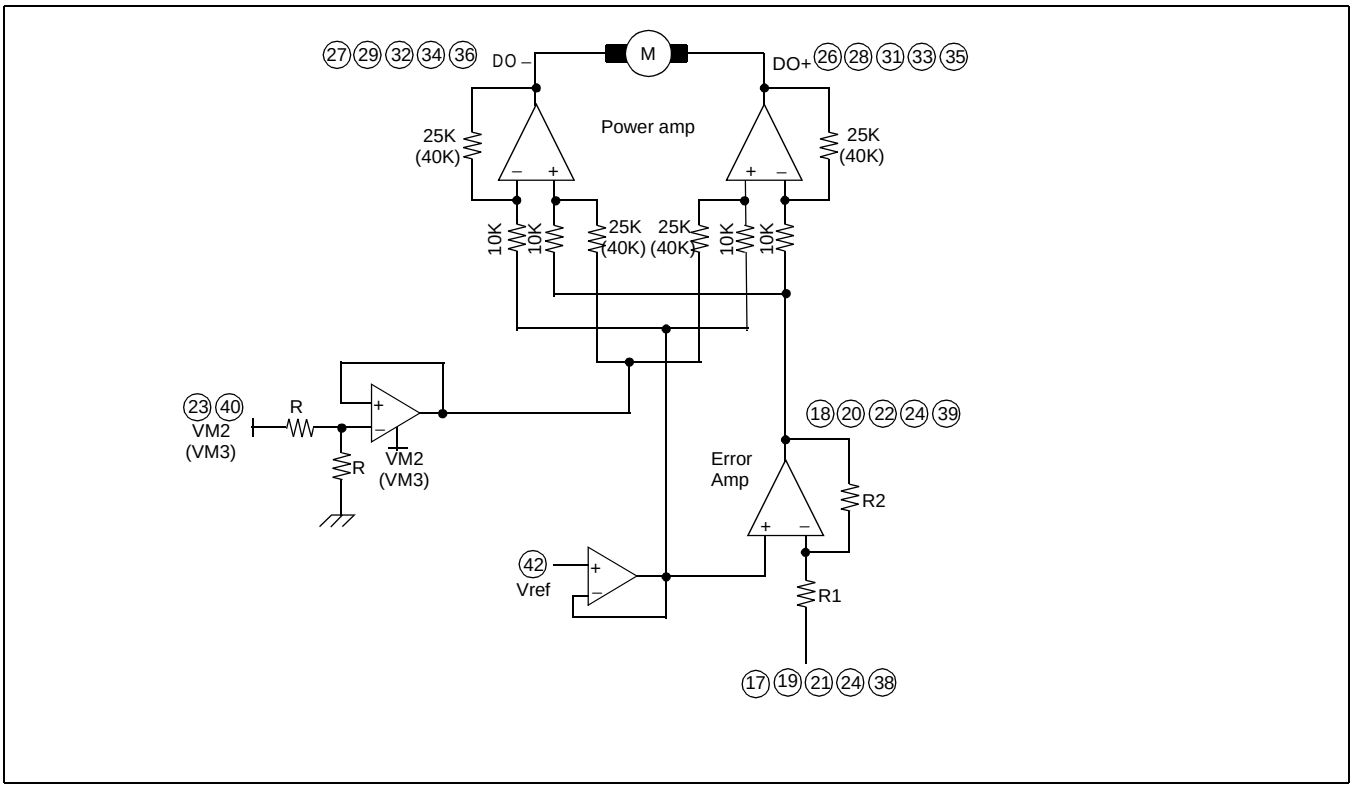
10. THE HEAT RADIATION FIN IS CONNECTED TO THE INTERNAL GND OF THE PACKAGE.

Connect the FIN to the external GND.

11. INPUT-OUTPUT TIMING CHART

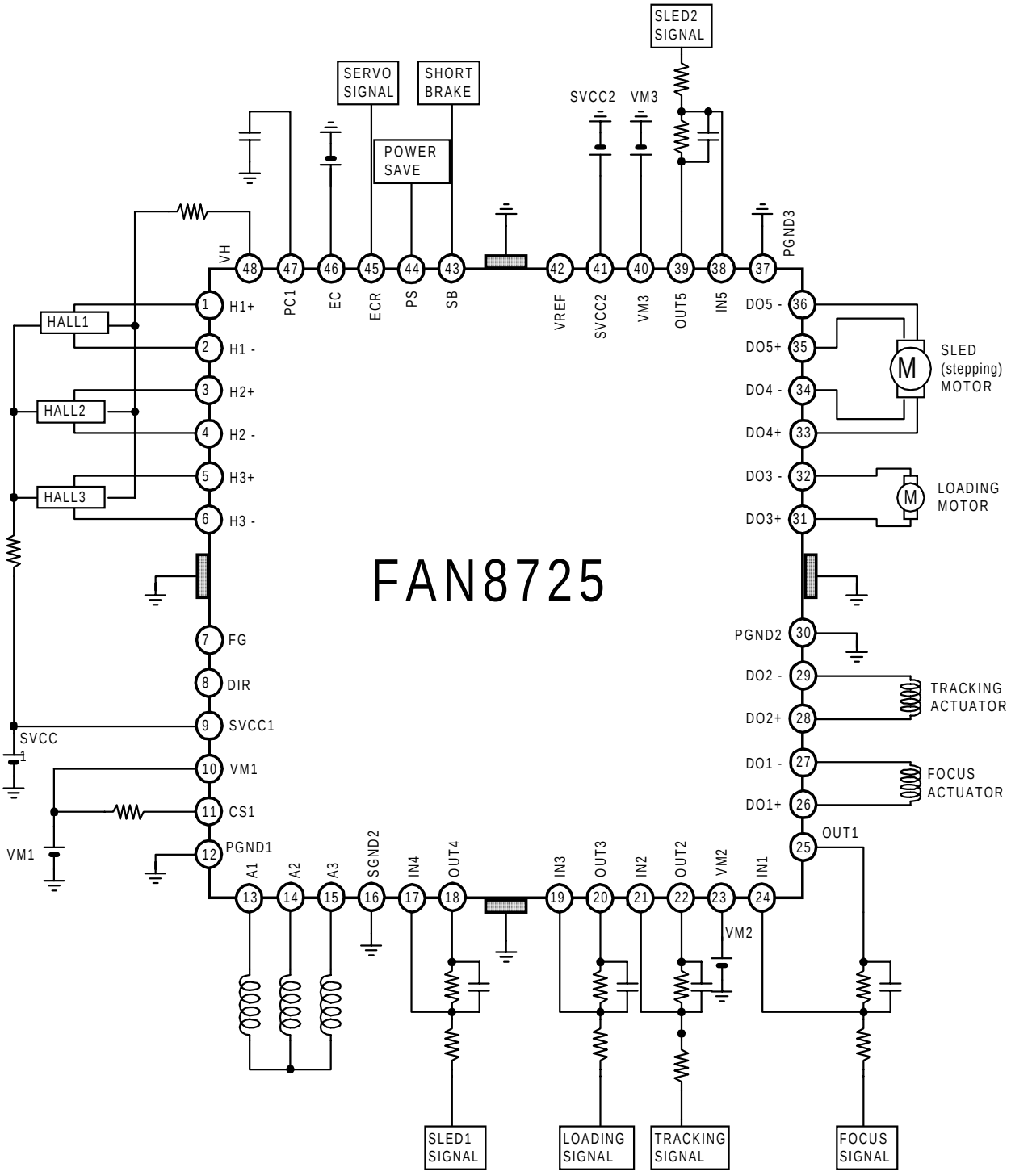


12. BTL DRIVE PART



- The reference voltage REF is given externally through pin 42.
- The error amp output signal is amplified by R2 / R1 times and then fed to the power amp part.
- The power amp part produces the differential output voltages and drives the two output power amplifier circuit.
- Since the differential gain of the output amplifiers of CH1/CH2 is equal to $2 \times (25K / 10K)$, the output signal of the error amp is amplified by $(R2 / R1) \times 5$.
- Since the differential gain of the output amplifiers of CH3/CH4/CH5 is equal to $2 \times (40K / 10K)$, the output signal of the error amp is amplified by $(R2 / R1) \times 8$.
- If the total gain is insufficient, the input error amp can be used to increase the gain.
- The CH1/CH2 are generally used as actuator drive part so this channels are not affected by TSD circuit.

Typical Application Circuits



Ordering Information

Device	Package	Operating Temperature
FAN8725	48-QFPH-1414	–35°C ~ +85°C

CD-MEDIA ONE CHIP IC

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAN8800 (KA3162)

Single IGBT Gate Driver

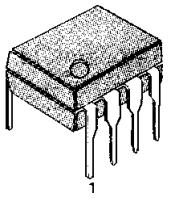
Features

- High Current Output: 1.0A Source and 2.0A Sink
- Protection against Overcurrent and Short circuit
- CMOS Compatible Input and Fault Status Indicator
- Programmable Fault-Out Duration Time
- Built in Slow Turn-off Circuit Under Fault Condition
- Undervoltage Lockout Optimized for IGBTs
- Negative Gate Drive Capability
- Suitable for Integration in Power Modules
- -40 to 105°C Operating Temperature

Description

The FAN8800 is a monolithic integrated circuit designed for driving single IGBT with De-saturation and undervoltage protection. It is suitable for driving discrete and module IGBTs, and further, it offers a cost effective solution for driving power MOSFETs. The integrated fault feedback notifies the controller when the IGBT is shutdown due to a De-saturation or a over current condition.

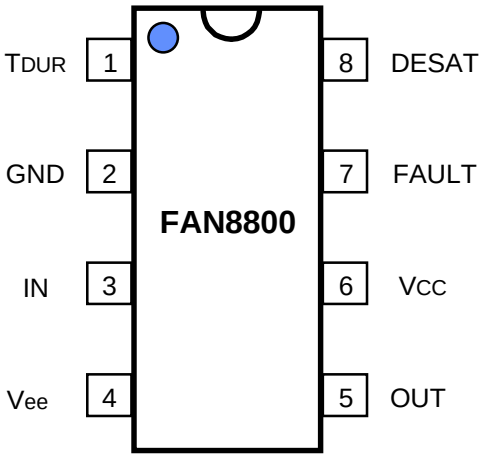
8-DIP



Typical Applications

- Gate drive for single insulated gate bipolar TR
- Gate drive for single MOSFET

Pin Assignments

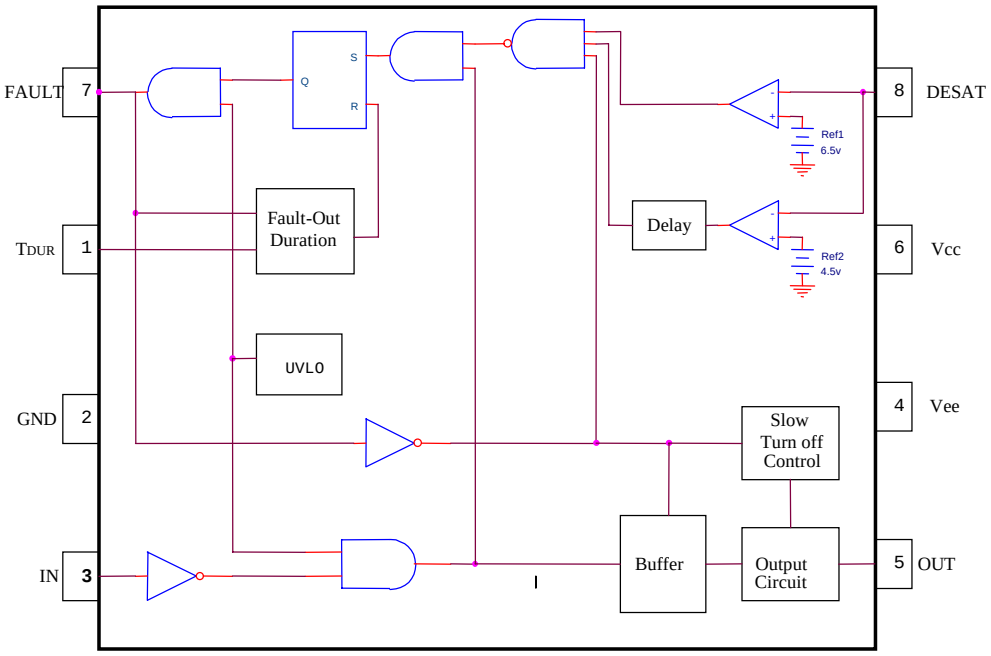


(Top View)

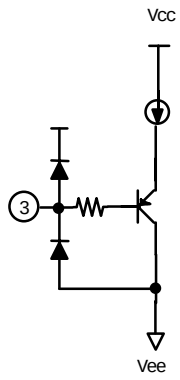
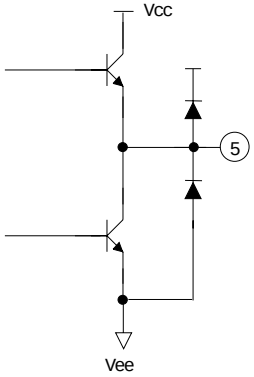
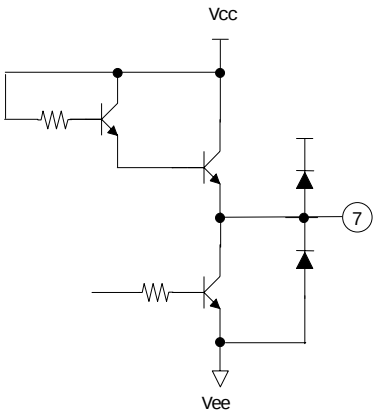
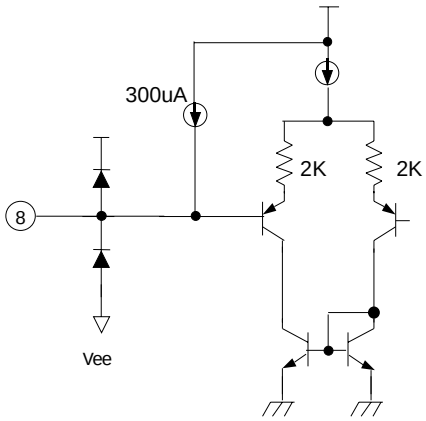
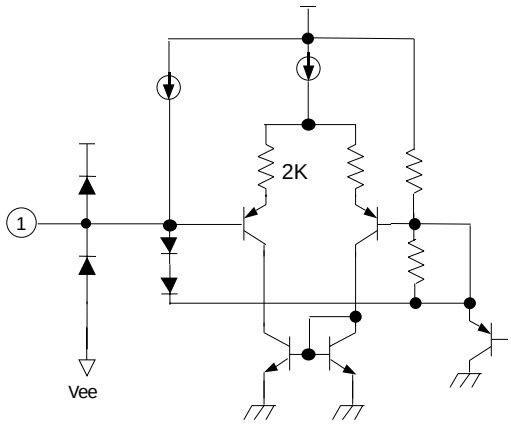
Pin Definitions

Pin Number	Pin Name	Pin Function Descrition
1	TDUR	Fault Output Duration(Adjustment Capacitor for Fault-Out Duration)
2	GND	Ground
3	IN	Inverting gate drive voltage output (Vout) control input
4	Vee	Gate drive voltage output
5	OUT	Output supply voltage (Negative)
6	V_{CC}	Output supply voltage (Positive)
7	FAULT	Fault Output. FAULT changes from a logic low state to a logic high output when a fault condition is detected.
8	DESAT	De-saturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 6.5v while the IGBT is on, FAULT output is changed from a logic low state to a logic high state.

Internal Block Diagram



Equivalent Circuits

Driver Input	Driver Output
	
Fault Out	**Desat**
	
T_{DUR}	
	

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC} - Vee	36	V
Output Source Current Output Sink Current	I_O	1.0 2.0	A
Fault Output Source Current Fault Output Sink Current	IF_O	25 10	mA
Input Voltage	Vin	Vee - 0.3 to V_{CC}	V
De-saturation Voltage	V_{DESAT}	-0.3 to V_{CC}	V
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @Ta =25°C	PD	0.56	W
Operating Ambient Temperature Range	T_{OPR}	-40 to 105	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C

Recommened Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max	Unit
Total Supply Voltage	V_{CC}	+13	+15	+18	V
Operating Power Supply Voltage	Vee	-13	-15	-18	V
Operating Ambient Temperature	Ta	-40	25	105	°C

Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
LOGIC INPUT						
High Input Threshold Voltage	V_{IH}	-	-	2.7	3.2	V
Low Input Threshold Voltage	V_{IL}	-	1.2	2.3	-	
DRIVE OUTPUT						
Low Output Voltage	V_{OL}	Isink=1.0A	-	2.0	2.4	V
High Output Voltage	V_{OH}	Isource=500mA	12	14	-	
FAULT OUTPUT						
Low Fault Output Voltage	V_{FL}	Isink=5.0A	-	0.2	1.0	V
High Fault Output Voltage	V_{FH}	Isource=20mA	11	13.5	-	
UVLO						
Start-up Voltage	V_{CCST}	-	11	11.5	12	V
Disable Voltage	V_{CCDI}	-	10	10.5	11	V
UVLO Hysteresis	H_Y	-	0.9	1.0	11.1	V
DESATURATION INPUT						
De-saturation Current Source	I_{CHG}	Vin=0V, V_{DESAT}=0V	210	300	380	µA
Discharge Current	I_{DSCHG}	Vin=Vcc, V_{DESAT}=Vcc	1.0	2.5	-	mA
OCP and SCP						
OCP Voltage Reference	V_{OCP}	-	4.0	4.5	5.0	µA
SCP Voltage Reference	V_{SCP}	-	5.8	6.5	7.3	mA
POWER SUPPLY						
Standby Current	I_{CCST}	Vin = High, Output open	-	14	20	mA
Operating Current	I_{CCOP}	CL=1.0nF, f=20kHz	-	20	30	mA
Propagation Delay Time to High Output Level	T_{PLH}	Rg=0, CL=1.0nF f=10kHz, Duty Cycle=50%	-	0.35	0.7	µs
Propagation Delay Time to Low Output Level	T_{PHL}		-	0.35	0.7	µs
Rise Time	Tr		-	50	100	ns
Fall Time	Tf		-	50	100	ns
OCP Delay Time	T_{OCP}		50	80	120	µs
SCP Delay Time	T_{SCP}		-	0.3	1.0	µs
Fault Output Duration Time	T_{DUR}	Cdur=2.7nF	100	170	320	µs
Slow turn-off time	T_{SLOW}	CL=4.7nF	0.8	2.0	5.0	µs

Application Information

1. FAULT-OUT DURATION TIME (T_{DUR})

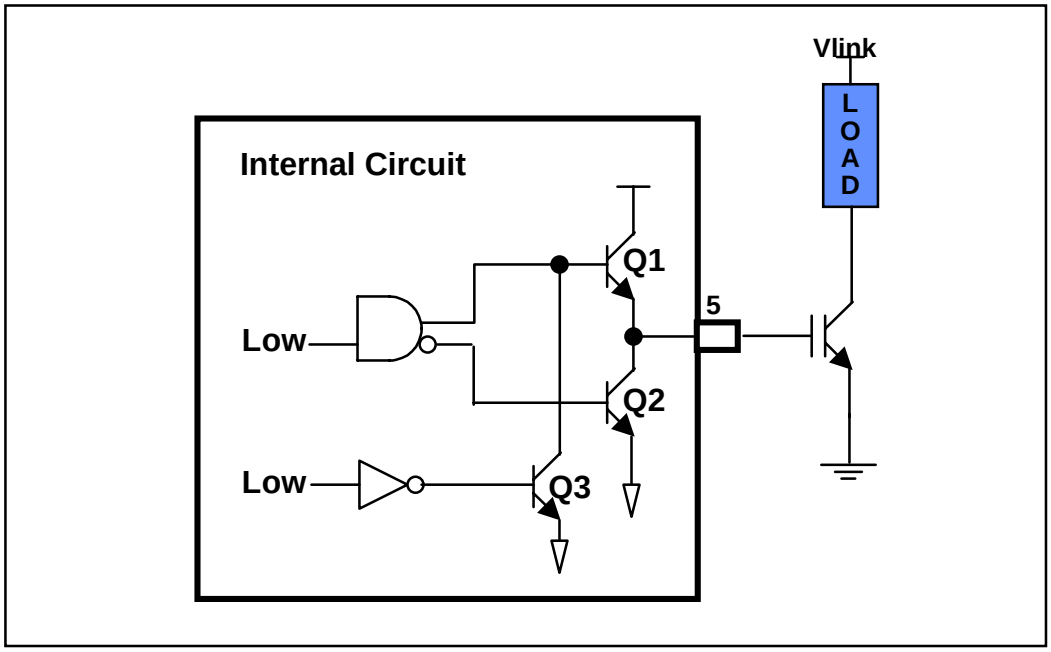
1) Two modes in Fault-Out Duration.

- OCP mode
  Fault-Out Duration operates after T_{OCP}.
- SCP mode
  If Vpin8 is over 6.5V, Fault-Out Duration will operate after T_{SCP}.

2) T_{DUR} (It can be adjusted by external capacitor (C_{DUR}) is

$$T_{DUR} = C_{DUR}/55\mu A \times (5V - 1.4V)$$
$$= 2.7nF/55\mu A \times (5V - 1.4V)$$
$$= 176\mu s$$

2. SLOW TURN-OFF (T_{SLOW})



1) When SCP (Short Circuit Protection) is operated, Q3 turns on and Q2 turns on.

2) In the upper condition, Q2 flows the constant current of 35mA.

3) The capacitance of IGBT as the load is discharging by 35mA, that is Slow Turn-off.

4) Slow Turn-off time is

$$T_{SLOW} = C_{IGBT}/35mA \times (V5max - V5min)$$
$$= 4.7nF/35mA \times (15V - 1V)$$
$$= 1.9\mu s$$

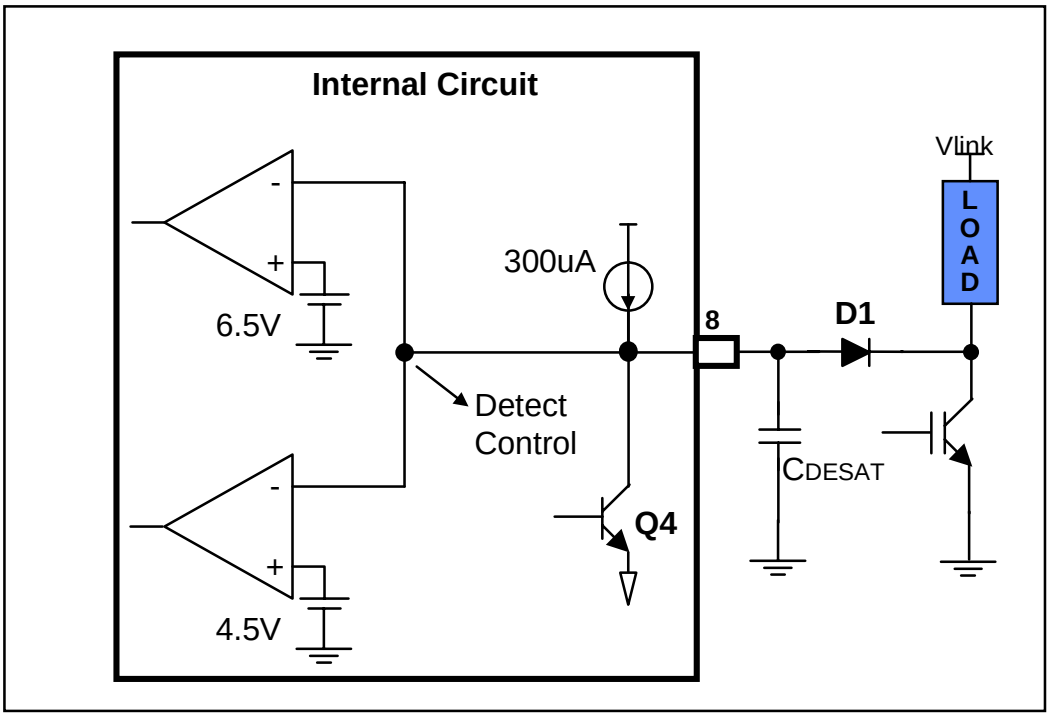
3. OCP DELAY TIME (T_{OCP})

1) If the saturation detector(DESAT or Vpin8) is 4.5V < Vpin8 < 6.5V, the Fault-Out signal will be high after T_{OCP}.

2) T_{COP} (This value is fixed internally) is

$$T_{OCP} = 50pF/3\mu A \times 5V$$
$$= 83\mu s$$

4. CHARGE TIME IN THE DE-SATURATION DETECTION



1) When the signal of Drive Output (Vpin5) is high, Q4 turns on and it is operated De-saturation Detection Mode in upper figure. In this mode, when it detects the voltage of collector- emitter terminal of IGBT through D1.

   If Vce(sat) + Vf of D1 $\geq$ 4.5V, it is operated OCP Mode.
   If Vce(sat) + Vf of D1 $\geq$ 6.5V, it is operated SCP Mode.

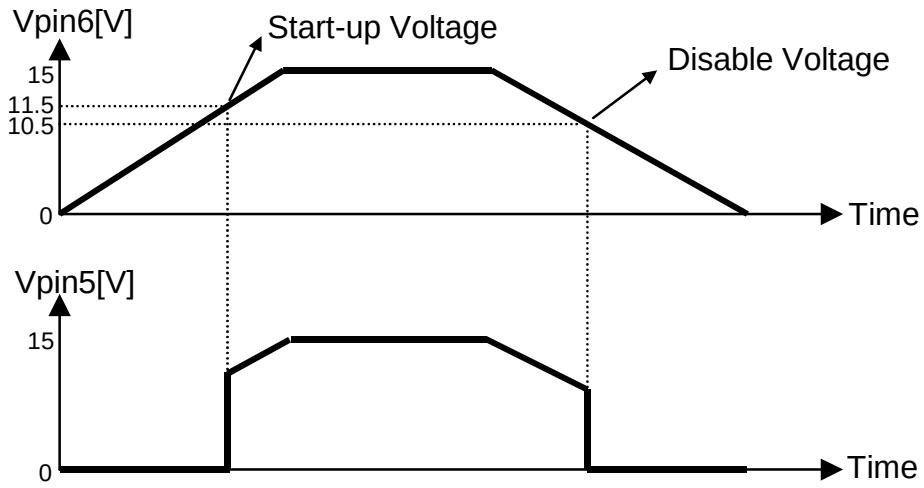
   When the input signal of IGBT is from low-state to high-state, Q4 turns off and it is operated De-saturation Detection Mode. On this times, the voltage of collector-emitter terminal of IGBT is not saturation-state yet.
   This period is said On Time Delay (Td (on)).
   Here, the operation of C_{DESAT} is following ; When C_{DESAT} is charged by current source of 300uA and so it prevents operating error for Td (on) of IGBT.

2) Slope of Vpin8 is

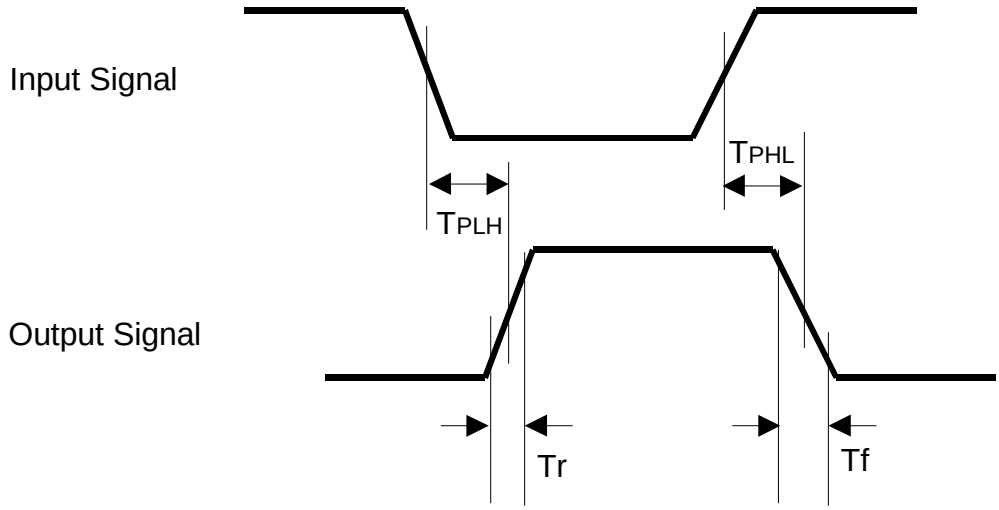
$$\Delta V/\Delta T = 300\mu A/C_{DESAT}$$

Timing Chart

UVLO Operation

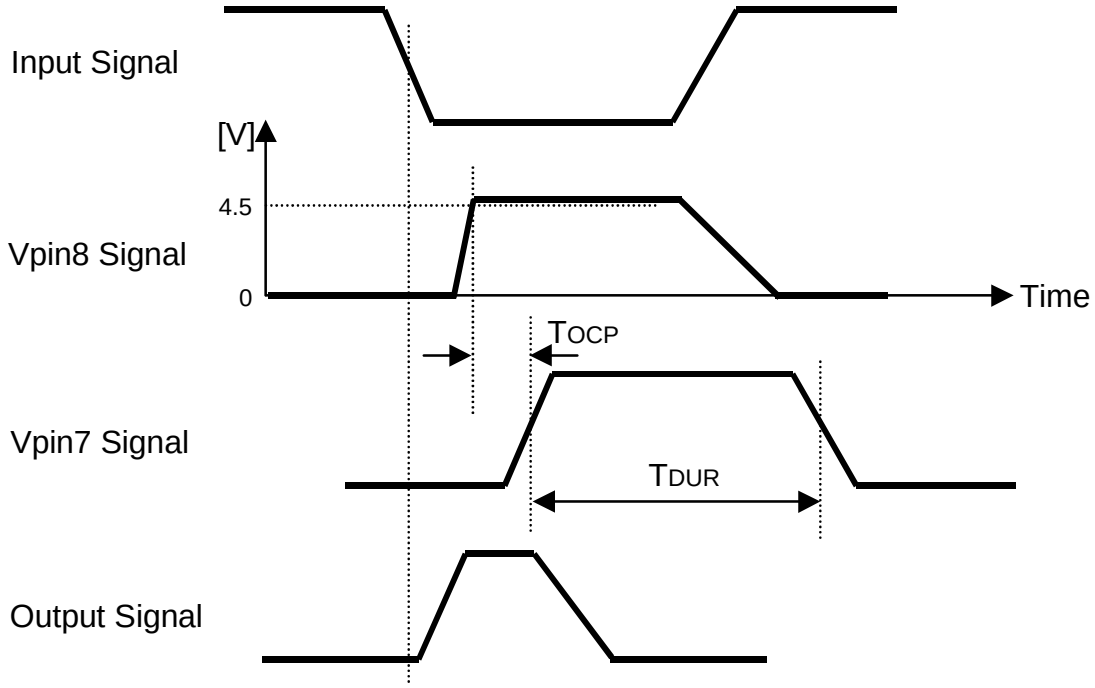


Input and Output Signal

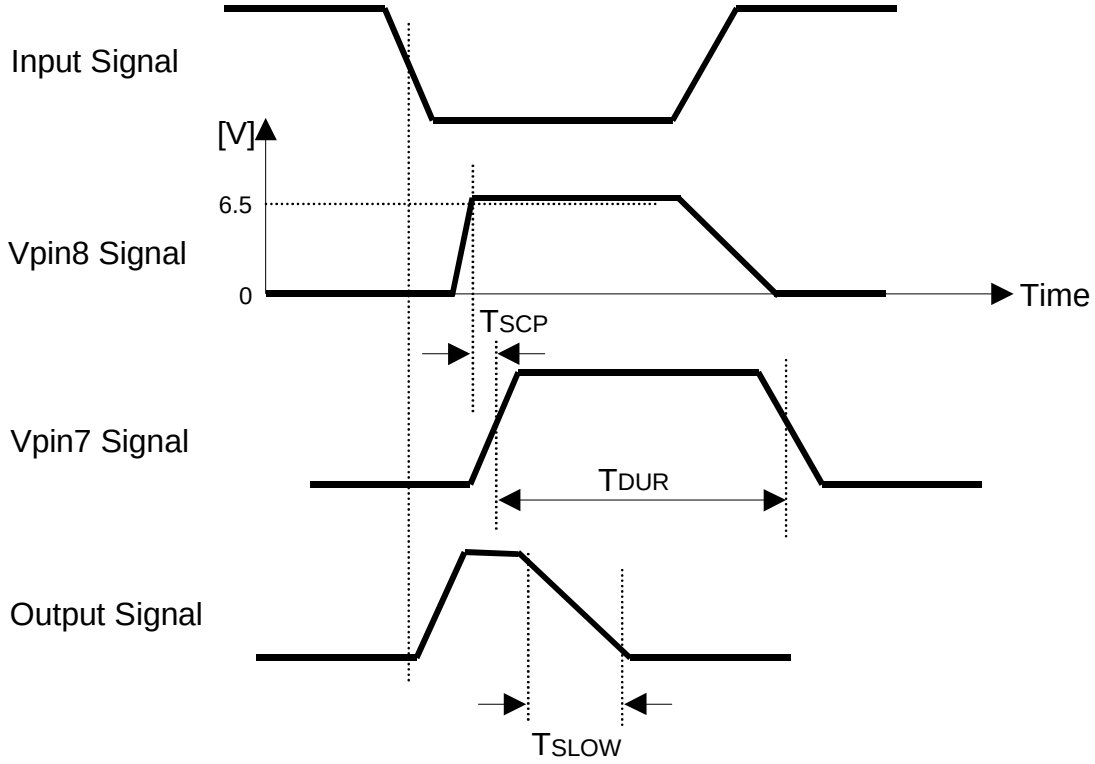


Timing Chart (Continued)

OCP Delay time

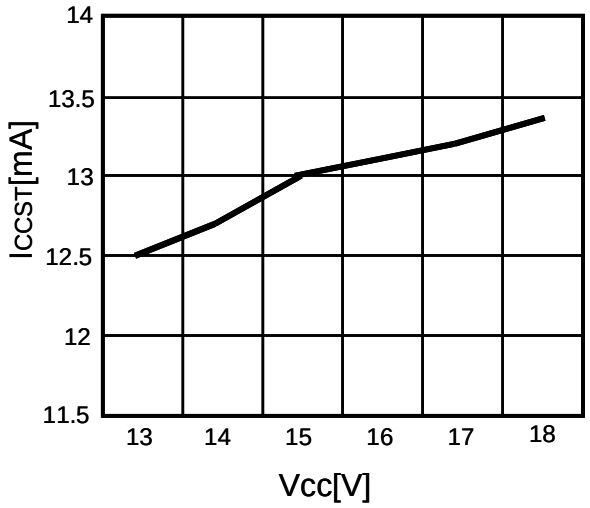


SCP Delay time

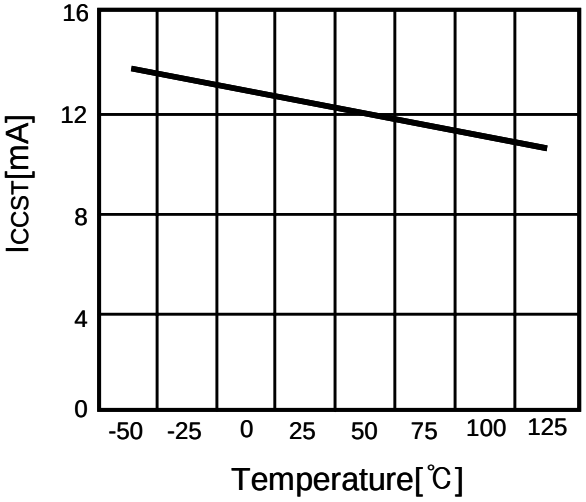


Typical Perfomance Characteristics

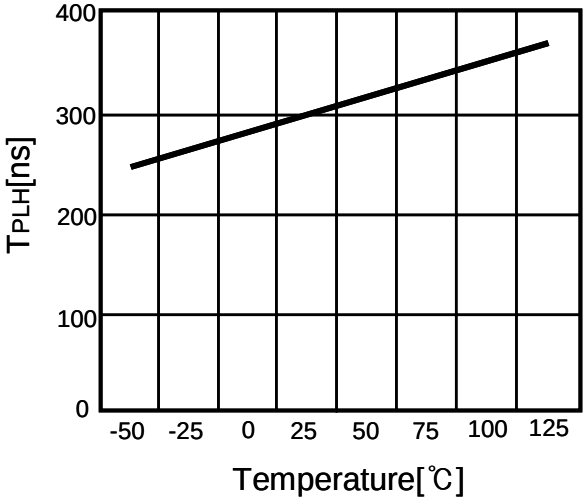
1. Vcc vs. Icc



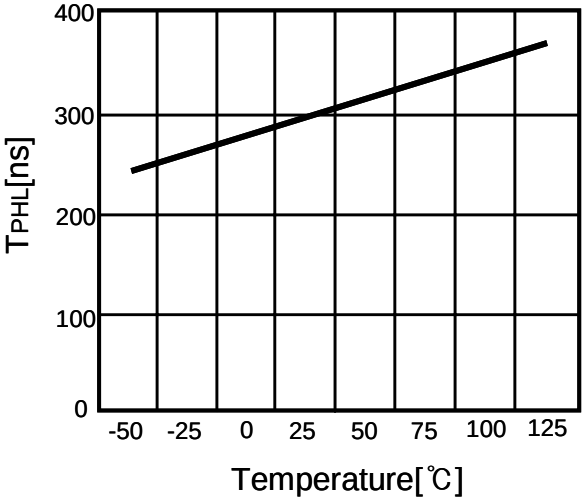
2. Temperature vs. ICCST



3. Temperature vs. TPLH

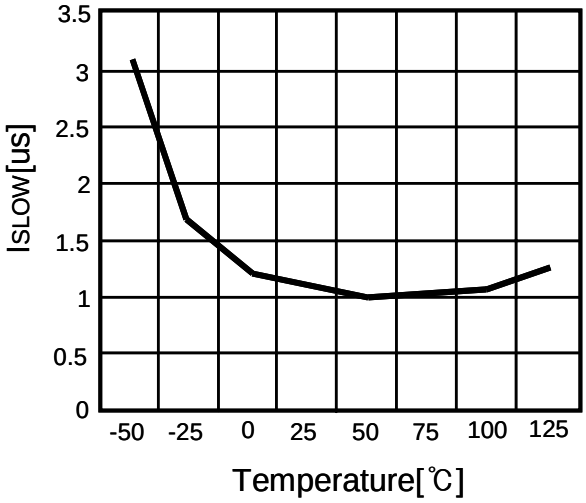


4. Temperature vs. TPHL

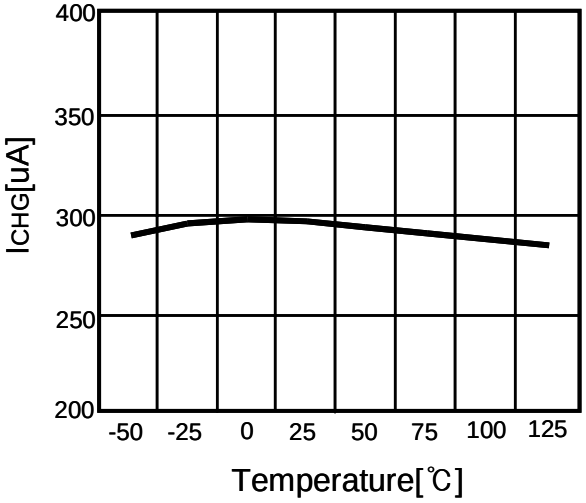


Typical Perfomance Characteristics (Continued)

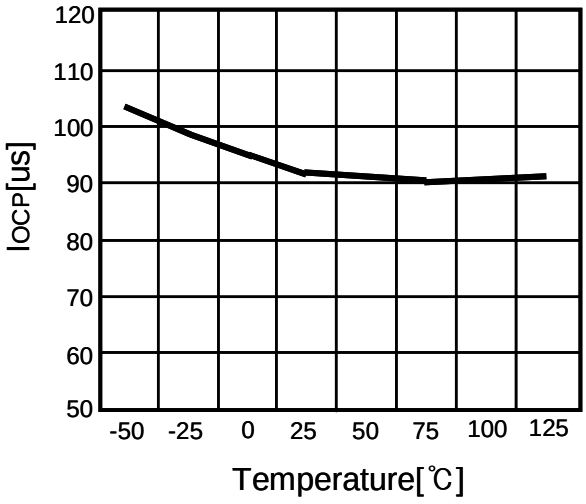
5. Temperature vs. T_{SLOW}



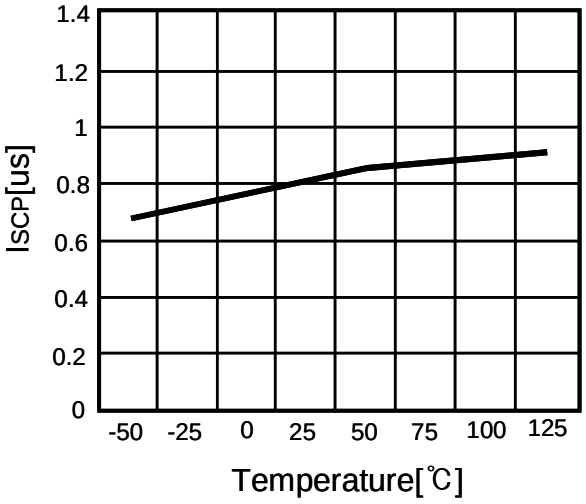
6. Temperature vs. I_{CHG}



7. Temperature vs. T_{OCP}



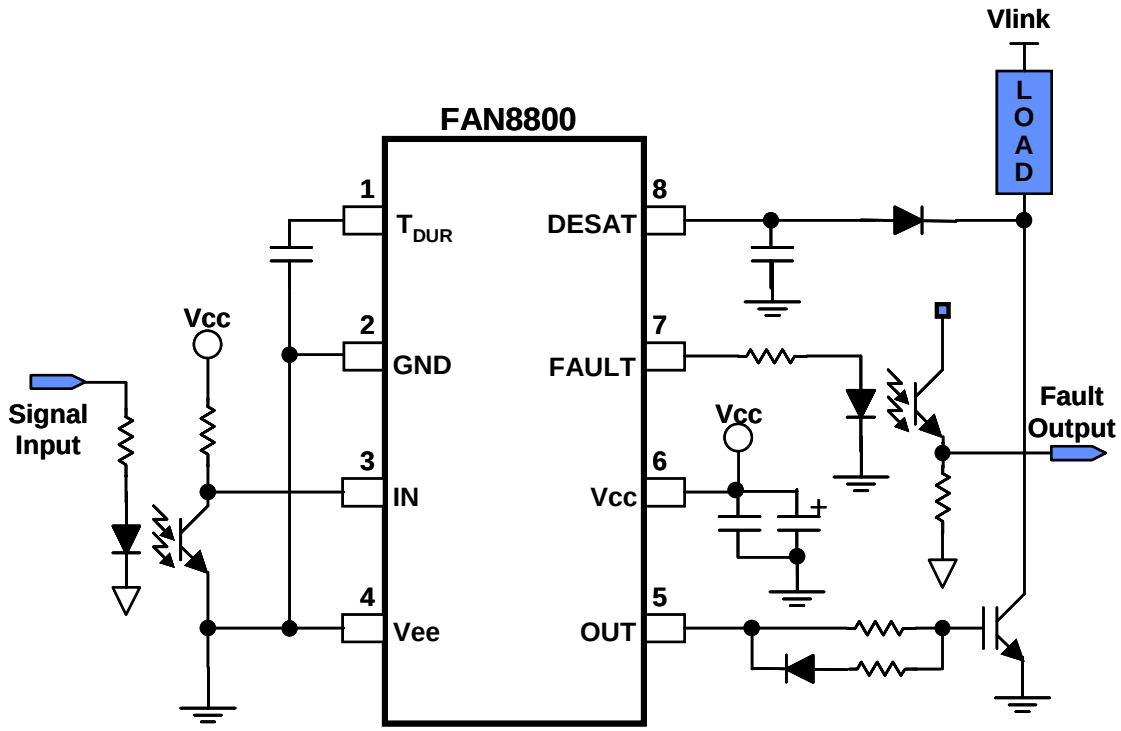
8. Temperature vs. T_{SCP}



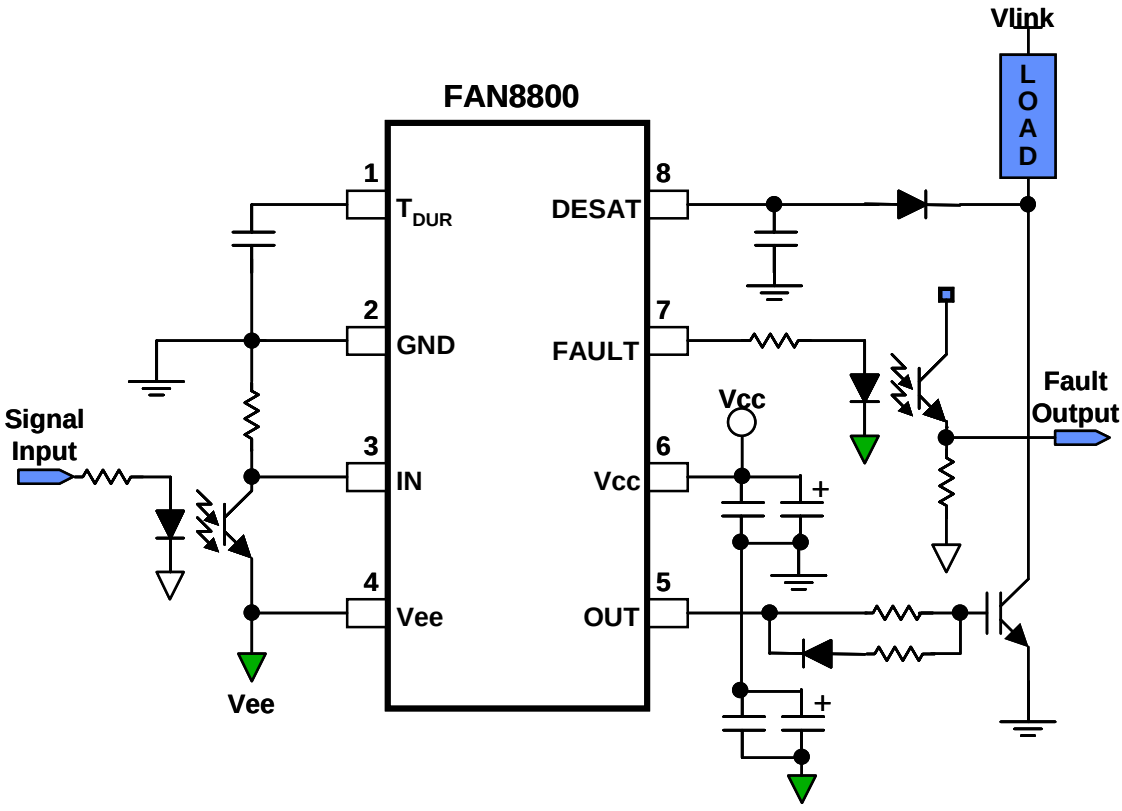
ETC. DRIVE IC

Typical Application Circuits

Single Power Supply Application



Dual Power Supply Application



ETC. DRIVE IC

Ordering Information

Device	Package	Operating Temperature
FAN8800	8-DIP	-40°C ~ +105°C

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