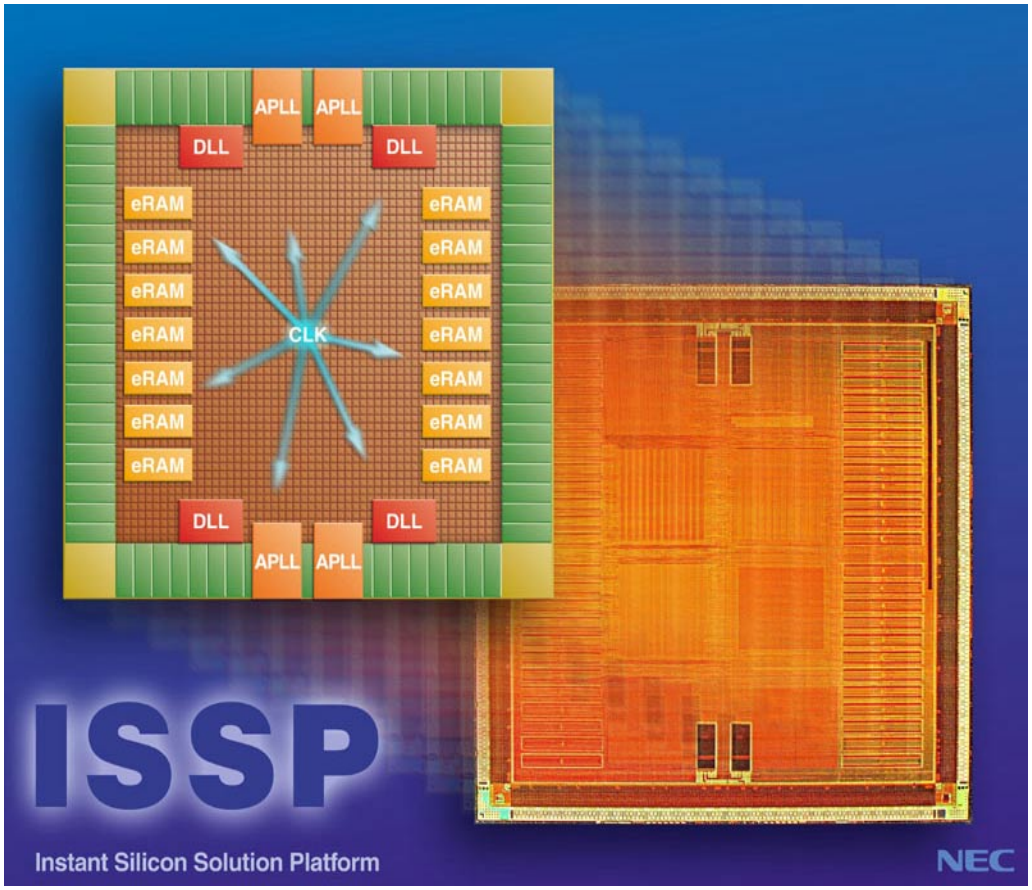
Empowered by Innovation NEC

## New ASIC Solution Platform

# ISSP Series

# (ISSP1-STD Family)



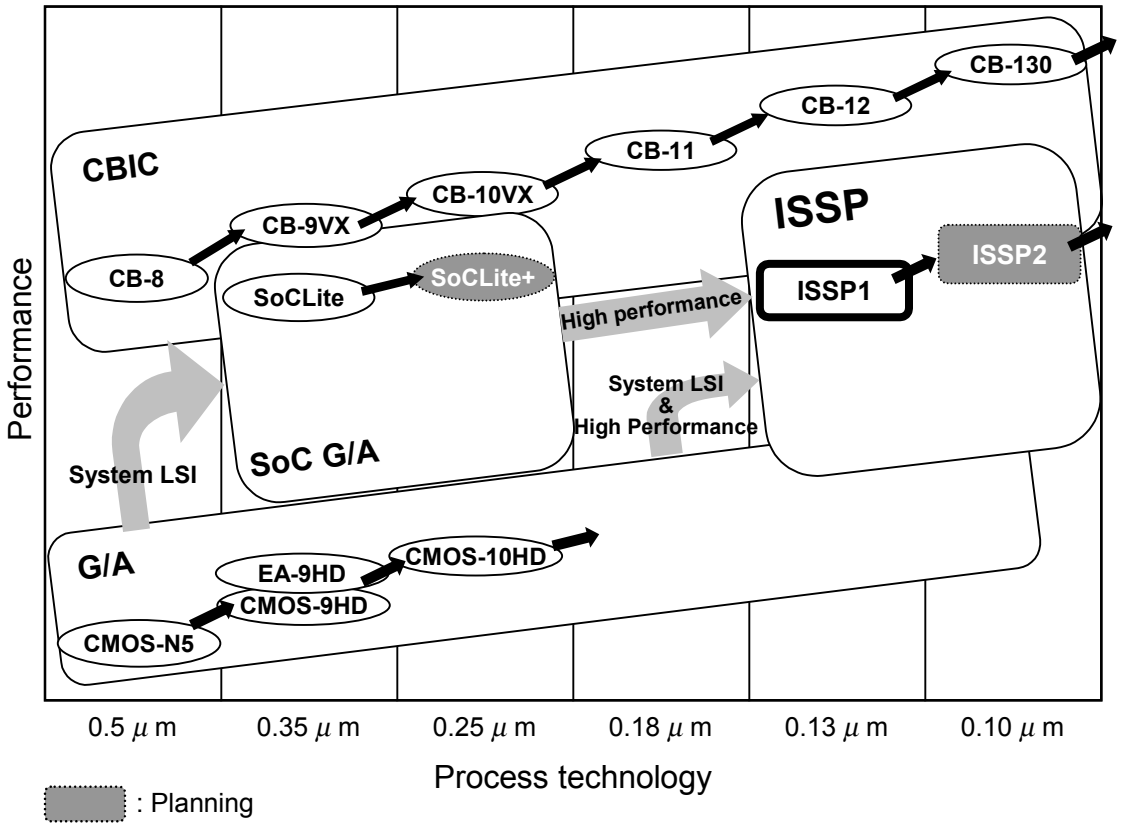

**< Brand-new ASIC Platform >**
**--- Low risk approach for complex System LSI ---**

New Products

# FEATURES (1/2)

Introduced by NEC Electronics, an ISSP represents a new class of ASIC devices based on a cost effective, high-function and easy to design ASIC architecture. ISSP devices are easily customizable using upper metal layers to meet individual design requirements. An ISSP is ideal for mid-volume designers engaged in complex designs with high system clock speeds. However, the platforms are generally very easy to design, consume much lower power than a comparable FPGA based solution and offer up to an order of magnitude lower NRE than cell-based designs. NEC Electronics offers a breadth of ASIC solutions using Cell-Based and Gate Array products. An ISSP complements these approaches by serving the growing number of mid-volume applications which cannot bear the development costs associated with leading-edge cell-based designs but which require higher complexity than a Gate Array or FPGA solution.

**ASIC Roadmap**

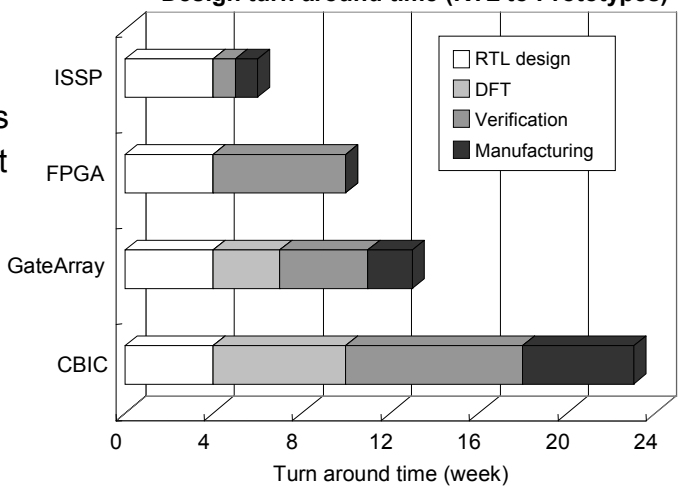



Advantages of ISSP

(1) System LSI with low overall development cost (engineering resources/mask NRE)
(2) New “Built-in” features (DFT, clocks, signal integrity) drastically provide “easy to design” .
(3) Includes many other benefits associated with Gate Array, Cell-Based and even FPGA
(4) Ability to leverage Cell-Based IP – allows quick migration to Cell-Based designs
(5) Small/Middle production volume capabilities with very quick turn around time

# FEATURES (2/2)

**Design turn around time (RTL to Prototypes)**




### Design Time Advantage

Design cycle times for complex ASICs are on the rise due to the need to insert and verify DFT(Design For Test) and to address deep sub-micron design issues such as signal integrity (SI). Even in the FPGA world, it is not unusual to spend weeks to converge on timing especially for higher utilized large gate-count designs exceeding 100 MHz clock speeds.

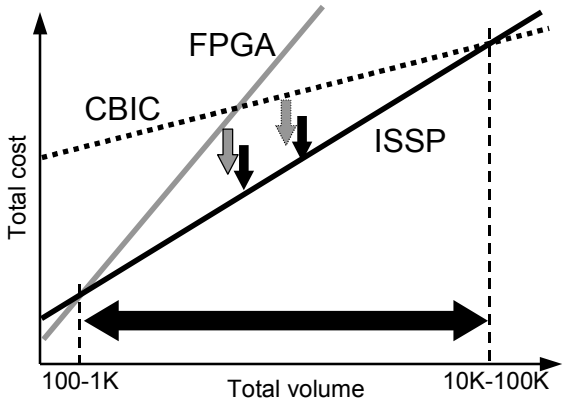
Users designing with ISSPs do not have to worry about a DFT impact to their design cycle because an ISSP comes pre-configured with all testing technologies like SCAN, BSCAN etc. The clock domains are also built into the ISSP, which results in additional design time savings due to predictable timing and lower clock skew. The use of a high performance process technology also enables the designer to achieve high clock speeds.

### The Low Risk Advantage

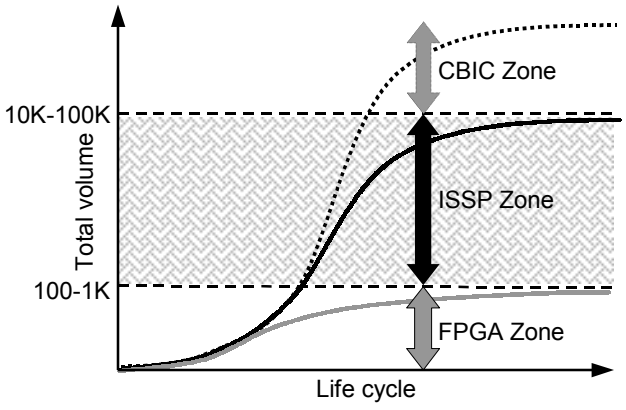
The rising development and mask NRE costs of deep sub-micron ASICs make it more difficult for mid-volume designers to target multiple re-spins of their prototypes. For early stage products, there is also an additional risk involved in predicting the production volumes necessary to amortize these development costs.

By providing a high performance solution, an easy design flow and an NRE typically associated with Gate Arrays, an ISSP allows quick re-spins of prototypes and enables products to reach mid-volume production at very reasonable costs. If the volumes increase, ISSP users can migrate to NEC Electronics's Cell Based products which are built on the same process technology and based on same IP and design flow.

**Total volume vs Total cost**




**Most cost effective device zone**




Total cost = Engineering cost + Mask NRE + Total volume x Unit cost

# PRODUCT OUTLINE (ISSP1-STD Family)

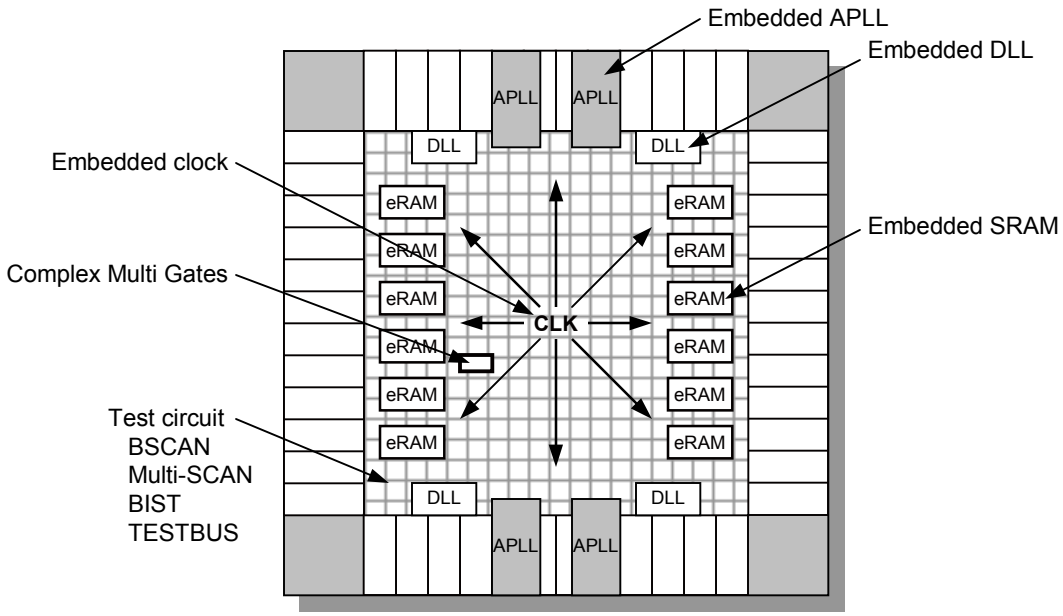
NEC Electronics's first generation of ISSP platforms known as the ISSP1-STD family includes embedded high density SRAM, Analog PLLs (APLL), and Delay-Locked Loops (DLL). ISSP1-STD family is based on NEC Electronics's production-proven UX4 CMOS process technology with 5 metal layer (aluminum) technology. It features advanced 0.13 $\mu$ m (drawn) transistors, which enables up to 300 MHz system clock speeds and a 1.5 V core voltage, which results in low-power dissipation.

This product applies a complex multi gates architecture to the user-defined logic area. The lower 3 metal layers are predefined for the interconnection related to the embedded IP cores, the built-in testing (DFT) circuits, clock domains and power lines. The upper 2 metal layers are used for customization of the users design.

The ISSP1-STD is a versatile platform and is targeted to support several major applications such as high performance broadband communication and networking equipments, computer peripherals, instrumentation and digital consumer products.

In the future NEC Electronics is planning to introduce ISSP platforms with embedded processor cores and high speed interface macros.

**Chip Structure of ISSP1-STD Family**




**Planned ISSP1-STD Family Master Offering**

| Master | Usable gates | Embedded SRAM block (16 K bit) | Embedded SRAM size (bit) | Package (TBGA) |
|---|---|---|---|---|
| $\mu$PD65701 | 227 K | 16 | 262,144 | 352<br>420 |
| $\mu$PD65702 | 530 K | 48 | 786,432 | 352<br>500<br>696 |
| $\mu$PD65703 | 1,109 K | 64 | 1,048,576 | 500<br>576<br>696 |

# Specification for ISSP1-STD Family

| | |
|---|---|
| Process | 0.13 $\mu$ m (drawn) Si gate CMOS, 5 metal layers |
| Maximum usable gates | 1 M gates (Usable) |
| Packages **Note** | 352 / 420 / 500 / 576 / 696 TBGA |
| Supply voltage | Internal : 1.5V<br>Interface : 2.5V / 3.3V, other high speed interfaces |
| Power dissipation | 0.014 $\mu$ W/MHz/gate (@Operating ratio: 0.3) |
| Maximum frequency | 300 MHz |
| Interface | 3.3V / 2.5V LVTTL<br>3.3V PCI, PCI-X<br>LVDS, HSTL, SSTL, PECL, others |
| Embedded cores | SRAM : 1/2 port compile type synchronous (Max: 1M bit)<br>APLL : High / Middle speed type<br>DLL : for High speed DRAM interface |
| Soft cores | SRAM : Distributed compiled type synchronous SRAM<br>UART, Ethernet™ MAC, Memory interface, others |
| Embedded clocks | Main clock : 2<br>Local clock : 8 |
| Embedded testing | SCAN, BSCAN, BIST, TESTBUS |



**Note** The number of usable signal pins depend on each package.

# MEMO

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