QL5030 - QuickPCI™ ESP
33 MHz/32-bit PCI Target with Embedded Programmable Logic and Dual Port SRAM

Advance Data *Updated: 1-Apr-99*

DEVICE HIGHLIGHTS

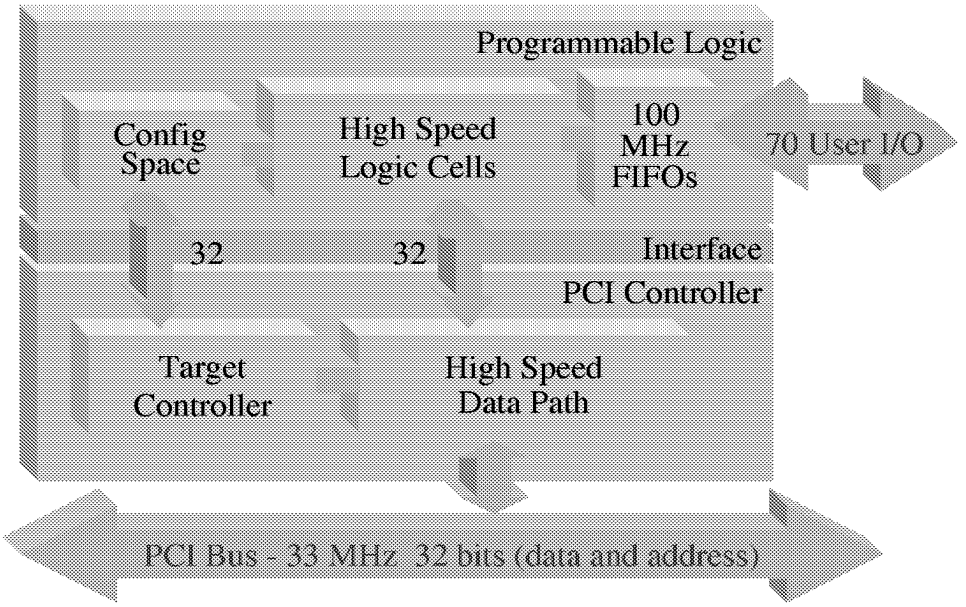
High Performance PCI Controller
- 32-bit / 33 MHz PCI Target PCI
- Zero-wait state PCI Target provides 132 MB/s transfer rates
- Programmable back-end interface to optional local processor
- Independent PCI bus (33 MHz) and local bus (up to 160 MHz) clocks
- Fully customizable PCI Configuration Space
- Configurable FIFOs with depths up to 128
- Reference design with driver code (Win 95/98/NT4.0) available

Expanded PCI Functionality
- Unlimited Burst Transfers Supported
- Support for Configuration Space from 0x40 to 0x3FF
- Multi-Function, Expanded Capabilities, & Expansion ROM capable
- Power management, Compact PCI, hot-swap/hot-plug compatible

High Speed Programmable Logic and Embedded SRAM
- 250 MHz 16-bit counters, 275 MHz Datapaths, 160 MHz FIFOs
- All back-end interface and glue-logic can be implemented on chip

User I/O	Gates	Logic Cells	Flip-Flops	RAM Bits
70 (144 TQFP)	5K	120	184	11,520

FIGURE 1: QL5030 DIAGRAM



ARCHITECTURE OVERVIEW

The QL5030 device in the QuickLogic QuickPCI ESP (Embedded Standard Product) family provides a complete and customizable PCI interface solution married with 5,000 gates of programmable logic. This device eliminates any need for the designer to worry about PCI bus compliance, yet allows for the maximum 32-bit PCI bus bandwidth (132 MB/s).

The programmable logic portion of the device contains 120 QuickLogic Logic Cells, and 10 QuickLogic Dual-Port RAM Blocks. These configurable RAM blocks can be configured in many width/depth combinations. They can also be combined with logic cells to form FIFOs, or be initialized via Serial EEPROM on power-up and used as ROMs. See the RAM section of this data sheet for more information.

The QL5030 device meets PCI 2.1 electrical and timing specifications and has been fully hardware-tested. This device also supports the Win'98 and PC'98 standards. The QL5030 device features 3.3-volt operation with multi-volt compatible I/Os. Thus it can easily operate in 3-volt only systems, as well as mixed 3.3 volt/5 volt systems.

A wide range of additional features complements the QL5030 device. The FPGA portion of the device is 5 volt and 3-volt PCI-compliant and can perform high-speed logic functions such as 160 MHz FIFOs. I/O pins provide individually controlled output enables, dedicated input/feedback registers, and full JTAG capability for boundary scan and test. In addition, the QL5030 device provides the benefits of non-volatility, high design security, immediate functionality on power-up, and a single chip solution.

APPLICATIONS

The QL5030 device supports maximum 32-bit PCI transfer rates, so many applications exist which are ideally suited to the device's high performance. High-speed data communications, telecommunications, and computing systems are just a few of the broad range of applications areas that can benefit from the high speed PCI interface and programmable logic.

CONFIGURABLE FIFOS

The RAM modules in the programmable region can be used to create configurable 32-bit FIFOs. Each 32-bit FIFO can be independently assigned to Target address space for read pre-fetch or write posting. Using the 10 QuickLogic RAM modules, the combinations include:

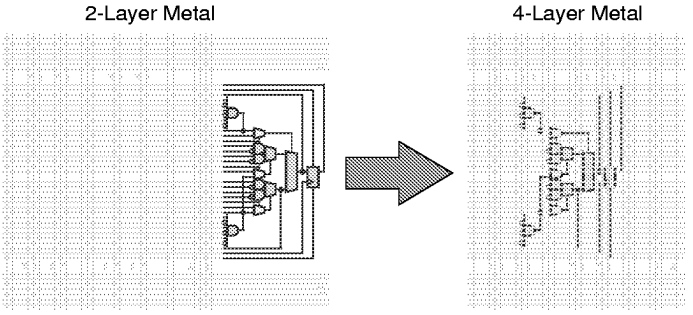
- 5 independent 64-deep FIFO (2 RAMs each), or
- 2 independent 128-deep FIFOs (4 RAMs each), or
- a combination of the above that requires 10 or less QuickLogic RAM Modules

Asynchronous FIFOs (with different read and write clocks) are also supported.

Array Of Logic Cells

The QL5030 device architecture consists of an array of user-configurable logic building blocks, called logic cells, set beneath a grid of metal wiring channels similar to those of a gate array. Through ViaLink elements located at the wire intersections, the output(s) of any cell may be programmed to connect to the input(s) of any other cell. By moving all interconnect resources above the logic cells, die sizes are less than half of two-layer metal technologies, as shown in Figure 2.

Figure 2: Four-Layer Metal Reduces Die Size



The regular and orthogonal interconnect makes the QL5030 programmable architecture similar in structure and performance to a metal-masked gate array. It also ensures that system operating speed is far less sensitive to partitioning and placement decisions, as minor revisions to a logic design can easily be incorporated without re-routing problems, resulting in only small changes in performance.

Adequate wiring resources permit 100% automatic placement and routing of designs using up to 100% of the logic cells and I/O pins. This capability has been demonstrated on designs that also include a high percentage of fixed pin placements.

The complete QL5030 logic cell consists of two 6-input AND gates, four two-input AND gates, six two-to-one multiplexers and one D flip-flop with asynchronous set and reset controls. The cell has a fan-in of 29 (including register control lines) and fits a wide range of functions with up to 16 simultaneous inputs. The D-type flip-flop can also be configured to provide J-K, S-R, or T-type functions. Two independent set and reset inputs can asynchronously control the output condition. In addition, a 2-bit shift register can be implemented in one logic cell with a macro library macro (LSHFT2Q2).

Figure 3 shows some of the possible configurations of the logic cell. The unique features of the logic cell make it possible to perform many small functions or one large function per logic cell, both at high speed.

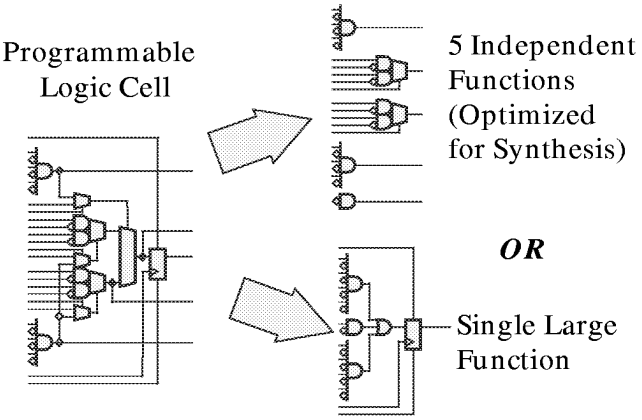


FIGURE 3: EXAMPLE OF LOGIC CELL CONFIGURATIONS

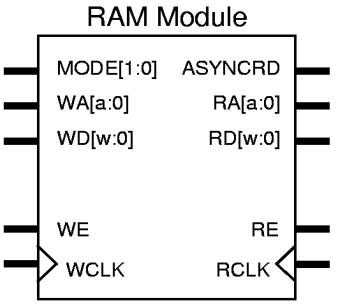
This level of flexibility is especially important for designs synthesized from HDLs such as VHDL or Verilog. Typically, synthesis tools prefer "gate array-like" fine-grained architectures; however, fine-grained FPGA architectures generally yield very poor performance due to the long delays resulting from building functions with multiple levels of gates and slow interconnect elements. The QuickPCI ESP family gives logic synthesis tools the needed degrees of freedom for the high logic utilization benefits of a fine-grained architecture without sacrificing the high performance benefits of a large-grained, high fan-in architecture.

The QL5030 macro library contains more than 400 of the most frequently used logic functions optimized to fit the logic cell architecture. A detailed understanding of the logic cell is therefore not necessary to design successfully with QL5030 devices. CAE tools will automatically map a conventional logic schematic or HDL file into a device and provide excellent performance and utilization.

RAM Module Features

The QL5030 device has ten 1,152-bit RAM modules, for a total of 11,520 RAM bits. Using two "mode" pins, designers can configure each module into 64 (deep) x18 (wide), 128x9, 256x4, or 512x2 blocks. See the figure below. The blocks are also easily cascadable to increase their effective width or depth.

FIGURE 4: RAM MODULE



Mode:	64x18	128x9	256x4	512x2
Address Busses [a:0]	[5:0]	[6:0]	[7:0]	[8:0]
Data Busses [w:0]	[17:0]	[8:0]	[3:0]	[1:0]

The RAM modules are "dual-ported", with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 9 address lines, allowing word lengths of up to 18 bits and address spaces of up to 512 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules. This approach allows up to 512-deep configurations as large as 20 bits wide in the QL5030 device.

A similar technique can be used to create depths greater than 512 words. In this case address signals higher than the eighth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

I/O Features

The QuickPCI ESP family features three distinct types of pins to maximize performance, functionality and flexibility: bi-directional I/O pins, input-only pins, and JTAG pins.

Bi-directional I/O pins can be programmed for input, output, or bi-directional operation. As shown in Figure 5, each bi-directional I/O pin is associated with an I/O cell which features a two-input OR gate, a three-state output buffer, an input buffer, and an input/feedback register. The OR gate allows active high or active low outputs, or can be used for high-speed logical OR functions independently of internal logic cells. The three-state buffer fed by the OR gate allows the I/O pin to act as an input or output. The buffer's output enable can be individually controlled through the logic cell array or any pin, or bank-controlled through a Global network.

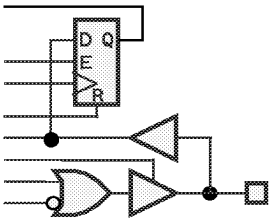


FIGURE 5: I/O CELL

Input-only pins are special low-skew, high-drive-current pins for driving high fan-out nets. The input-only pins can also drive one of two types of special highly-distributed, buffered networks typically used for routing clock or control signals, Array networks or Global networks.

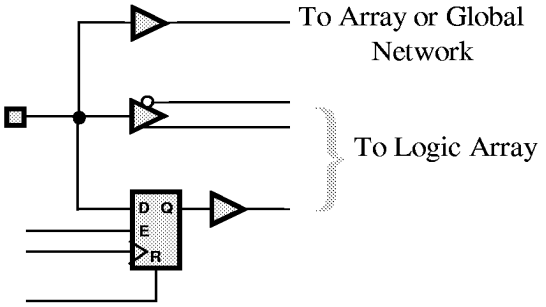


FIGURE 6: INPUT-ONLY CELL WITH ARRAY NETWORK ACCESS

Distributed Array and Global Networks

The QL5030 device includes 6 distributed networks. These distributed networks are highly buffered, well-distributed routing structures designed to provide low-skew signals for high fan-out nets. There are two types of distributed networks: Array networks, and Global networks. The 2 Array networks must be driven from ACLK pins, and may drive to any or all array

logic cell flip-flop clock, set, and reset signals. The 4 Global networks may be driven from GCLK pins, or from any internal node. Global networks route to any or all array logic cell flip-flop controls, input and I/O register controls, I/O cell output enable controls, and to the F1 Logic Cell input.

JTAG Support

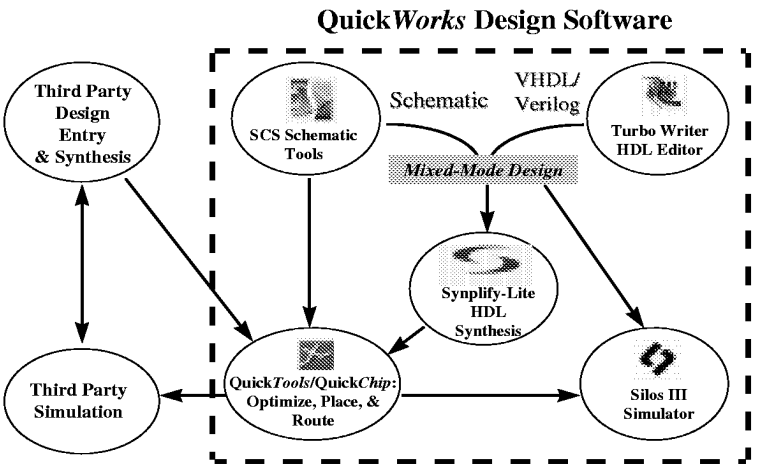
JTAG pins support IEEE standard 1149.1a to provide boundary scan capability for the QL5030 device. Six pins are dedicated to JTAG and programming functions on each QL5030 device, and are unavailable for general design input and output signals. TDI, TDO, TCK, TMS, and TRSTB are JTAG pins. A sixth pin, STM, is used only for programming.

Development Tools

Software support for the QL5030 device is available through the Quick*Works*® development package. This turnkey PC-based Quick*Works* package, shown in Figure 7, provides a complete ESP software solution with design entry, logic synthesis, place and route, and simulation. Quick*Works* includes VHDL, Verilog, schematic, and mixed-mode entry with fast and efficient logic synthesis provided by the integrated Synplicity Synplify Lite™ tool, specially tuned to take advantage of the QL5030 architecture. Quick*Works* also provides functional and timing simulation for guaranteed timing and source-level debugging.

The UNIX-based Quick*Tools*™ and PC-based Quick*Chip*™ packages are a subset of Quick*Works* and provide a solution for designers who use third-party tools for design entry, synthesis, or simulation. Quick*Tools* and Quick*Chip* read EDIF netlists and provide support for all QuickLogic devices. Quick*Tools* and Quick*Chip* also support a wide range of third-party modeling and simulation tools. In addition, the PC-based Quick*Tools* Plus package combines all the features of Quick*Chip* with the SCS schematic capture environment, providing a low-cost design entry and compilation solution.

FIGURE 7: QUICK*WORKS* TOOL SUITE



QL5030 External Device Pins

The QL5030 Device Pins are indicated in the table below. These are pins on the device, some of which connect to the PCI bus, and others that are programmable as user IO.

Type	Description
IN	Input. A standard input-only signal
OUT	Totem pole output. A standard active output driver
T/S	Tri-state. A bi-directional, tri-state input/output pin
S/T/S	Sustained Tri-state. An active low tri-state signal driven by one PCI agent at a time. It must be driven high for at least one clock before being disabled (set to Hi-Z). A pull-up needs to be provided by the PCI system central resource to sustain the inactive state once the active driver has released the signal.
O/D	Open Drain. Allows multiple devices to share this pin as a wired-or.

Signal names which end in a '#' are ACTIVE LOW. These signals may use the suffix "N" in software since the '#' is not a legal character for Verilog or VHDL synthesis.

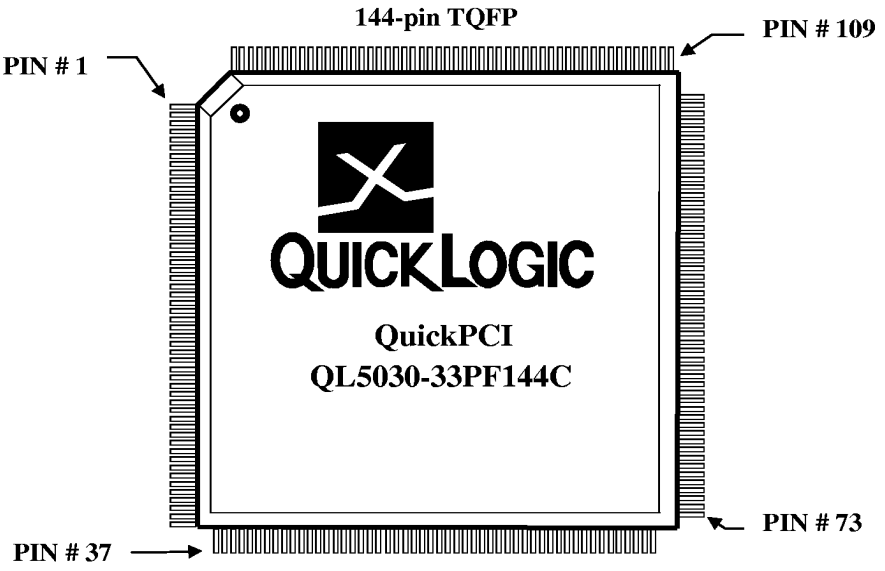
Pin/Bus Name	Type	Function
VCC	IN	Supply pin. Tie to 3.3V supply.
VCCIO	IN	Supply pin for I/O. Set to 3.3V for 3.3V I/O, 5V for 5.0V compliant I/O
GND	IN	Ground pin. Tie to GND on the PCB.
I/O	T/S	Programmable Input/Output/Tri-State/Bi-directional Pin.
GCLK/I	IN	Programmable Global Network or Input-only pin. Tie to VCC or GND if unused.
ACLK/I	IN	Programmable Array Network or Input-only pin. Tie to VCC or GND if unused.
TDI/RSI*	IN	JTAG Data In/Ram Init. Serial Data In. Tie to VCC if unused. Connect to Serial EPROM data for RAM init.
TDO/RCO*	OUT	JTAG Data Out/Ram Init Clock. Leave unconnected if unused. Connect to Serial EPROM clock for RAM init.
TCK	IN	JTAG Clock. Tie to GND if unused.
TMS	IN	JTAG Test Mode Select. Tie to VCC if unused.
TRSTB#/RRO*	IN	JTAG Reset/RAM Init. Reset Out. Tie to GND if unused. Connect to Serial EPROM reset for RAM init.
STM	IN	QuickLogic Reserved pin. Tie to GND on the PCB.

* See QuickNote 65 on the QuickLogic web site for information on RAM initialization.

Pin/Bus Name	Type	Function
AD[31:0]	**T/S**	PCI Address and Data: 32 bit multiplexed address/data bus.
C/BE#[3:0]	**T/S**	PCI Bus Command and Byte Enables: Multiplexed bus which contains byte enables for AD[31:0] or the Bus Command during the address phase of a PCI transaction.
PAR	**T/S**	PCI Parity: Even Parity across AD[31:0] and C/BE#[3:0] busses. Driven one clock after address or data phases. Master drives PAR on address cycles and PCI writes. The Target drives PAR on PCI reads.
FRAME#	**S/T/S**	PCI Cycle Frame: Driven active by current PCI Master during a PCI transaction. Driven low to indicate the address cycle, driven high at the end of the transaction.
DEVSEL#	**S/T/S**	PCI Device Select. Driven by a Target that has decoded a valid base address.
CLK	**IN**	PCI System Clock Input.
RST#	**IN**	PCI System Reset Input
PERR#	**S/T/S**	PCI Data Parity Error. Driven active by the initiator or target two clock cycles after a data parity error is detected on the AD and C/BE# busses.
SERR#	**O/D**	PCI System Error: Driven active when an address cycle parity error, data parity error during a special cycle, or other catastrophic error is detected.
IDSEL	**IN**	PCI Initialization Device Select. Use to select a specific PCI Agent during System Initialization.
IRDY#	**S/T/S**	PCI Initiator Ready. Indicates the Initiator's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDY# and TRDY# are active.
TRDY#	**S/T/S**	PCI Target Ready. Indicates the Target's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDY# and TRDY# are active.
STOP#	**S/T/S**	PCI Stop. Used by a PCI Target to end a burst transaction.
INTA#	**O/D**	Interrupt A. Asynchronous Active-Low Interrupt Request.

QL5030 –144 TQFP PINOUT TABLE

PF144	Function	PF144	Function	PF144	Function	PF144	Function
1	I/O	37	AD[21]	73	AD[4]	109	**TCK**
2	I/O	38	**TDI/RSI**	74	AD[3]	110	**STM**
3	I/O	39	AD[20]	75	AD[2]	111	I/O
4	I/O	40	AD[19]	76	AD[1]	112	I/O
5	I/O	41	AD[18]	77	AD[0]	113	I/O
6	I/O	42	**VCC**	78	I/O	114	**VCC**
7	**VCC**	43	AD[17]	79	**VCC**	115	I/O
8	I/O	44	AD[16]	80	I/O	116	I/O
9	I/O	45	CBEN[2]	81	I/O	117	I/O
10	I/O	46	FRAMEN	82	I/O	118	I/O
11	I/O	47	IRDYN	83	I/O	119	I/O
12	I/O	48	TRDYN	84	I/O	120	I/O
13	I/O	49	DEVSELN	85	I/O	121	I/O
14	I/O	50	**GND**	86	I/O	122	**GND**
15	**GND**	51	STOPN	87	**GND**	123	I/O
16	I/O	52	PERRN	88	I/O	124	I/O
17	GCLK/I	53	SERRN	89	GCLK/I	125	I/O
18	ACLK/I	54	**GND**	90	ACLK/I	126	**GND**
19	**VCC**	55	PAR	91	**VCC**	127	I/O
20	RSTN	56	CBEN[1]	92	GCLK/I	128	I/O
21	CLK	57	AD[15]	93	GCLK/I	129	I/O
22	**VCC**	58	**VCCIO**	94	**VCC**	130	**VCCIO**
23	INTAN	59	AD[14]	95	I/O	131	I/O
24	AD[31]	60	AD[13]	96	I/O	132	I/O
25	AD[30]	61	AD[12]	97	I/O	133	I/O
26	AD[29]	62	AD[11]	98	I/O	134	I/O
27	AD[28]	63	AD[10]	99	I/O	135	I/O
28	AD[27]	64	AD[9]	100	I/O	136	I/O
29	AD[26]	65	AD[8]	101	I/O	137	I/O
30	**GND**	66	**GND**	102	**GND**	138	**GND**
31	AD[25]	67	CBEN[0]	103	I/O	139	I/O
32	AD[24]	68	AD[7]	104	I/O	140	I/O
33	CBEN[3]	69	AD[6]	105	I/O	141	I/O
34	IDSEL	70	AD[5]	106	I/O	142	I/O
35	AD[23]	71	**TRSTB/RRO**	107	I/O	143	**TDO/RCO**
36	AD[22]	72	**TMS**	108	I/O	144	I/O



TARGET CONFIGURATION & ADDRESS/ COMMAND DECODE

Target Configuration and Address/Command Decoding are done in the programmable logic region of the device. Since these functions are not timing critical, leaving these elements in the programmable region allows the greatest degree of flexibility to the designer. A reference Configuration Space and Address/Command Decode block is included to minimize design complications.

The configuration space is totally customizable in the programmable region of the device. The Configuration Space and Address/Command Decode function blocks include:

- From 1 to 6 32-bit Base Address Registers (BARs) may be used. These can be defined as memory or IO, with configurable address size.
- Expansion ROM, Extended Configuration Space, and Multi-function devices may be defined.
- The designer may control all configuration space default values.
- Any number of address decodes can be performed.
- The designer may modify the list of supported PCI commands that are decoded as Target read and Target Writes. Special functions may be defined for Memory Read Line/Multiple, and Memory Write and Invalidate PCI commands.

CONFIGURABLE FIFO WIDTH AND DEPTH

FIFOs may be created with the Ram/FIFO wizard in the QuickWorks tools. The figure below shows the graphical interface used to create these FIFOs. FIFOs may be designed up to 128 deep. With 10 RAM modules available in the QL5030, that allows for up to 5 FIFOs at 64 deep (36 wide), or 2 FIFOs at 128 deep (36 wide).

INTERNAL INTERFACE SIGNAL DESCRIPTIONS

Signals used to connect to the PCI interface in the QL5030 are described below. The direction of the signal indicates if it is an input provided by the local interface (I) or an output provided by the PCI interface (O).

TARGET CONTROLLER INTERFACE		
Usr_RdData[31:0]	I	Target Read data, to be sent to the PCI bus.
Usr_Select	I	Indicates that the current transaction should be claimed due to a valid address/command decode.
Usr_Stop	I	Abort/disconnect the current PCI transaction on the next PCI clock.
Usr_Interrupt	I	Generates a PCI interrupt while set high.
Usr_Rdy	I	Asserted when the user is ready to transmit or receive data. Can be used to delay the assertion of TRDY on the PCI bus.
Usr_RdDecode	I	PCI read transaction decoded (e.g. I/O read, memory read, memory read line, or memory read multiple).
Usr_WrDecode	I	PCI write transaction decoded (e.g. I/O write or memory write).
Cfg_RdData[31:0]	I	Read data from PCI configuration space. Generated from the Reference Config Space block.
Cfg_CmdReg6	I	Bit 6 of the PCI Config Space Command Register. Generated from the Reference Config Space block.
Cfg_CmdReg8	I	Bit 8 of the PCI Config Space Command Register. Generated from the Reference Config Space block.
Usr_Data_Valid	O	Valid data on Usr_Addr_WrData[31:0] on Target writes. During read transactions, indicates data on Usr_RdData[31:0] has been received.
Cfg_Write	O	When asserted, valid Target Configuration Write data is present on the Usr_Addr_WrData[3:0] bus.
Usr_Addr_WrData[31:0]	O	PCI address (while Usr_Adr_Valid is active), or write data from PCI bus (while Usr_WrData_Valid).
Usr_CBE[3:0]	O	PCI command (while Usr_Adr_Valid is high) and byte enables (while Usr_Adr_Valid is low)
Usr_Adr_Valid	O	Active when a PCI address is available on Usr_Addr_WrData[31:0] (at the beginning of a new PCI transaction).
Usr_Adr_Inc	O	Active when the address counter should be incremented for the next read or write in a Target burst transaction.
Usr_Last_Cycle_D1	O	Last data transfer is occurring on the PCI bus (signals the end of a transaction).
Usr_TRDYN	O	Copy of the Target generated TRDYN signal for the current PCI clock cycle. (Active low)
Usr_STOPN	O	Copy of the Target generated STOPN signal for the current PCI clock cycle. (Active low)
Usr_Devsel	O	Copy of the Target generated DEVSEL signal for the current PCI clock cycle. (Active high)
Cfg_PERR_Det	O	Parity error detected. When this signal is active, bit 15 in the Status Register in the PCI configuration space must be set.
Cfg_SERR_Sig	O	System error signaled. When this signal is active, bit 14 in the Status Register in the PCI configuration space must be set.

INTERNAL PCI INTERFACE		
PCI_IRDYN_D1	O	IRDYN from PCI bus, registered.
PCI_FRAMEN_D1	O	FRAMEN from PCI bus, registered.
PCI_DEVSELN_D1	O	DEVSELN from PCI bus, registered.
PCI_TRDYN_D1	O	TRDYN from PCI bus, registered.
PCI_STOPN_D1	O	STOPN from PCI bus, registered.
PCI_IDSELN_D1	O	IDSELN from PCI bus, registered.
PCI_clock	O	PCI clock.
PCI_reset	O	PCI reset.

The symbol used to connect to the PCI interface of the QL5030 is shown below. This symbol is used in schematic or mixed schematic/HDL design flows in the QuickWorks software.