

2SA1784/2SC4644

PNP Epitaxial Planar Silicon Transistor
NPN Triple Diffused Planar Silicon Transistor

High Voltage Driver Applications

Features

- Adoption of MBIT process
- High breakdown voltage ($V_{CE0} \geq 400V$)
- Excellent linearity of h_{FE}

() : 2SA1784

Absolute Maximum Ratings at $T_a = 25^\circ C$

			unit
Collector to Base Voltage	V_{CBO}	(-)400	V
Collector to Emitter Voltage	V_{CEO}	(-)400	V
Emitter to Base Voltage	V_{EBO}	(-)5	V
Collector Current	I_C	(-)200	mA
Collector Current(Pulse)	I_{CP}	(-)400	mA
Collector Dissipation	P_C	1	W
Junction Temperature	T_j	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$

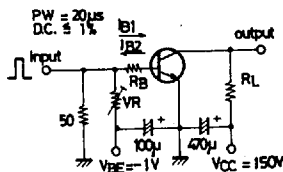
Electrical Characteristics at $T_a = 25^\circ C$

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	$V_{CB} = (-)300V, I_E = 0$			(-)0.1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = (-)4V, I_C = 0$			(-)0.1	μA
DC Current Gain	h_{FE}	$V_{CE} = (-)10V, I_C = (-)50mA$	60*		200*	
Gain-Bandwidth Product	f_T	$V_{CE} = (-)30V, I_C = (-)10mA$		70		MHz
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C = (-)50mA, I_B = (-)5mA$		(- 0.8)	0.6	V
B-E Saturation Voltage	$V_{BE(sat)}$	$I_C = (-)50mA, I_B = (-)5mA$			(-)1.0	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C = (-)10\mu A, I_E = 0$	(-)400			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C = (-)1mA, R_{BE} = \infty$	(-)400			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	$I_E = (-)10\mu A, I_C = 0$	(-)5			V
Output Capacitance	C_{ob}	$V_{CB} = (-)30V, f = 1MHz$		(5)4		pF
Reverse Transfer Capacitance	C_{re}	$V_{CB} = (-)30V, f = 1MHz$		(4)3		pF
Turn-ON Time	t_{on}	See specified Test Circuit.	0.25			μs
Turn-OFF Time	t_{off}	See specified Test Circuit.	5.0			μs

*: The 2SA1784/2SC4644 are classified by 50mA h_{FE} as follows:

60 D 120	100 E 200
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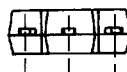
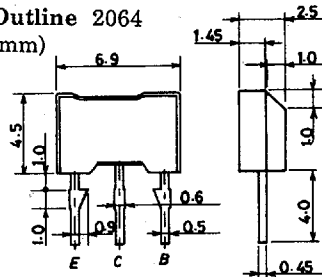
Switching Time Test Circuit



$10I_{B1} = -10I_{B2} = I_C = 50mA$
 $R_L = 3k\Omega, R_B = 200\Omega, \text{ at } I_C = 50mA$
 (For PNP, the polarity is reversed.)

Unit(Resistance : Ω , Capacitance : F)

Case Outline 2064
(unit : mm)



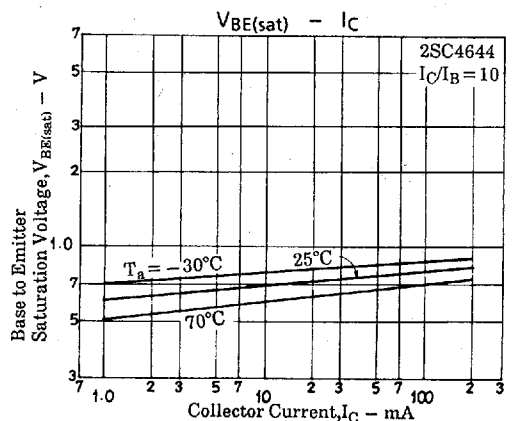
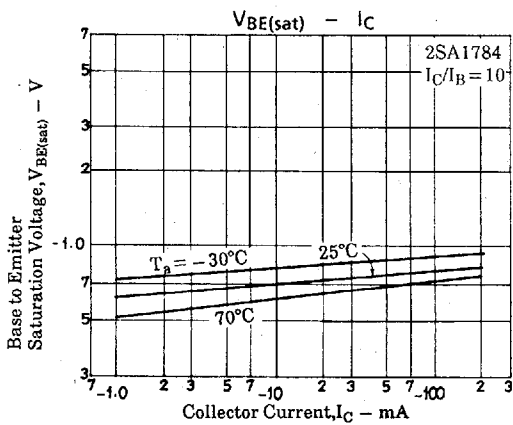
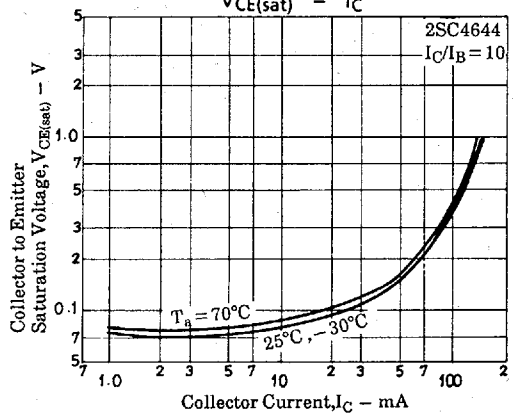
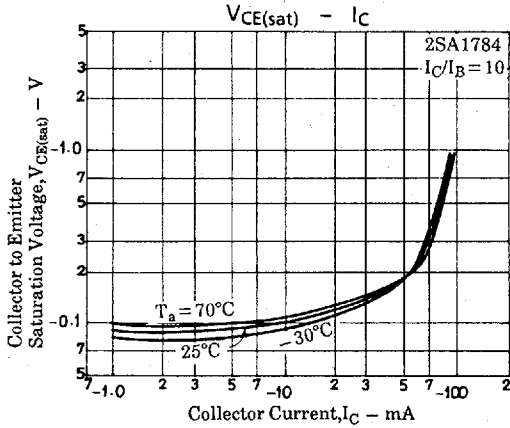
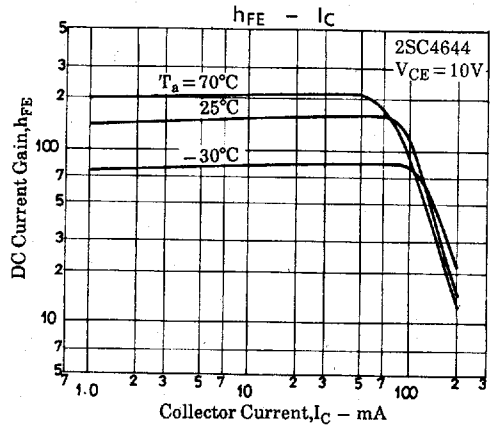
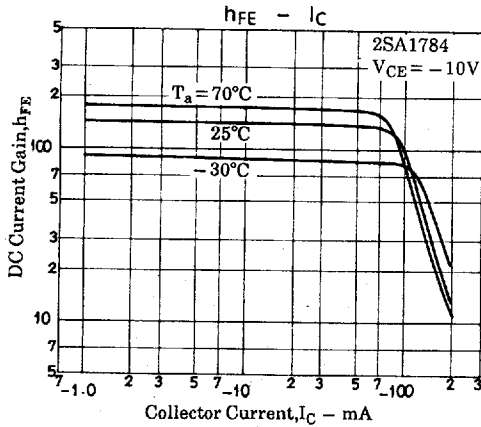
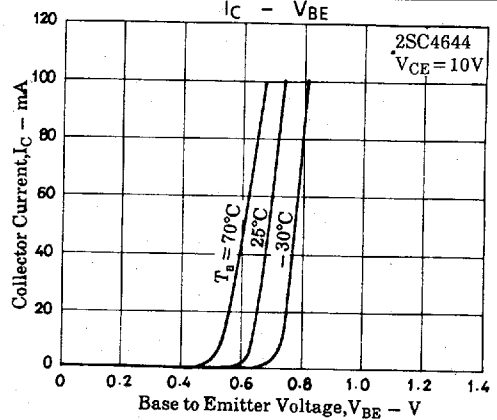
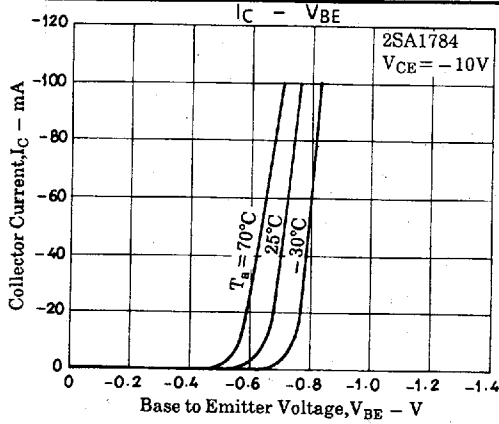
E: Emitter
 C: Collector
 B: Base

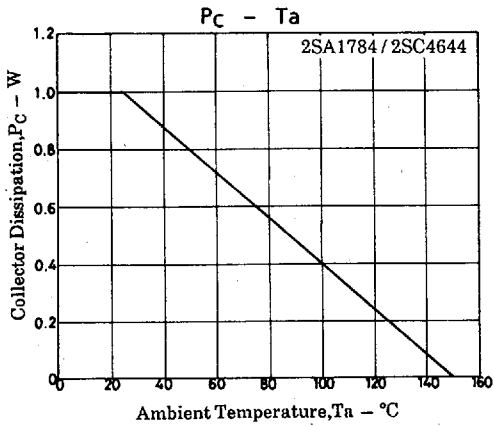
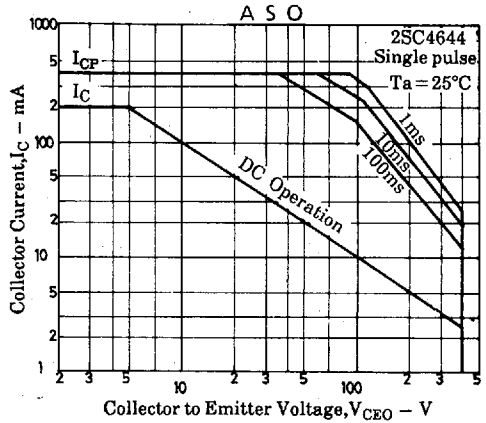
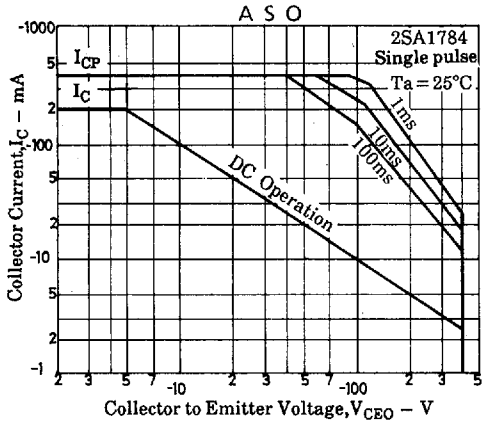
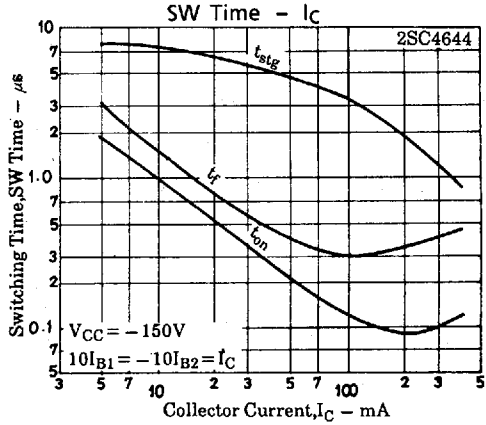
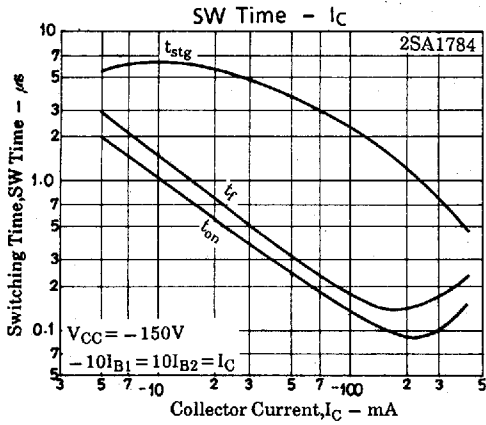
SANYO: NMP

Specifications and information herein are subject to change without notice.

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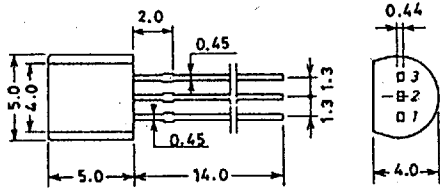




CASE OUTLINES OF LEAD FORMED SMALL SIGNAL TRANSISTORS

- All of Sanyo lead formed small signal transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

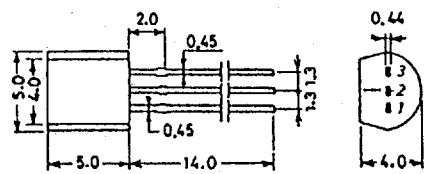
Case Outline 2003A/2003B (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Emitter
2 : Collector
3 : Base

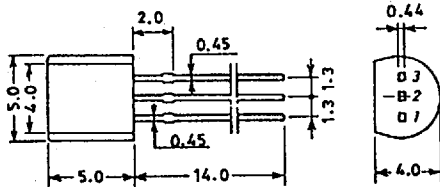
Case Outline 2019A/2019B (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Source
2 : Gate
3 : Drain

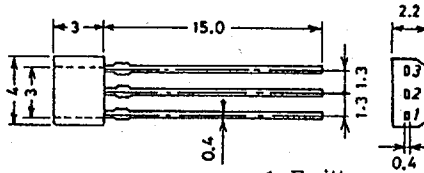
Case Outline 2004A (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Base
2 : Emitter
3 : Collector

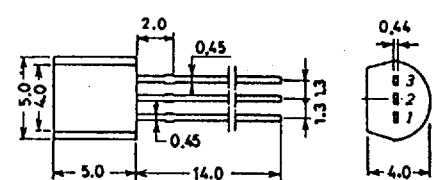
Case Outline 2033 (unit : mm)



1 : Emitter
2 : Collector
3 : Base

SANYO : SPA

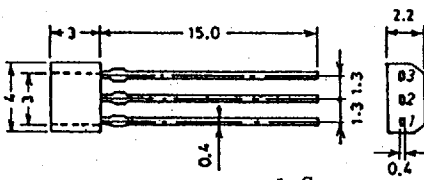
Case Outline 2005A (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Drain
2 : Source
3 : Gate

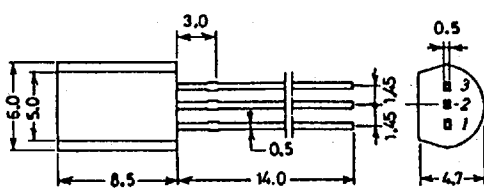
Case Outline 2034/2034A (unit : mm)



1 : Source
2 : Gate
3 : Drain

SANYO : SPA

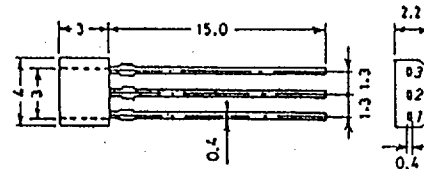
Case Outline 2006A (unit : mm)



EIAJ : SC-51
SANYO : MP

1 : Emitter
2 : Collector
3 : Base

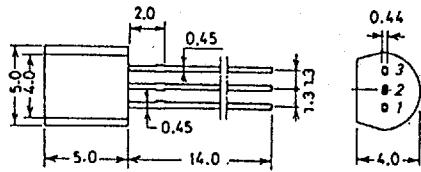
Case Outline 2040 (unit : mm)



1 : Drain
2 : Source
3 : Gate

SANYO : SPA

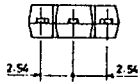
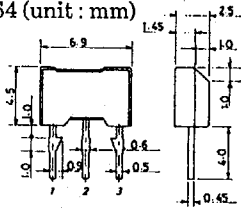
Case Outline 2061 (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1: Emitter
2: Base
3: Collector

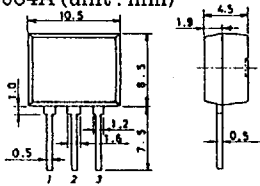
Case Outline 2064 (unit : mm)



1: Emitter
2: Collector
3: Base

SANYO : NMP

Case Outline 2084A (unit : mm)



1: Emitter
2: Collector
3: Base

SANYO : FLP