ACE24LC02/04/08/16
Two-wire Serial EEPROM

Description

The ACE24LC02/04/08/16 provides low operation voltage of 2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Features

- Low Operation Voltage: Vcc=1.7V to 3.6V
- 5V tolerant I/O
- Internally Organized: 256x8(2K), 512x8(4K), 1024x8(8K) or 2048x8(16K)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1MHz (3.6V,2.7V,2.5V) and 400 kHz (1.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-byte Page(2K), 16-byte Page (4K,8K,16K) Write Modes
- Partial Page Writes are Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years

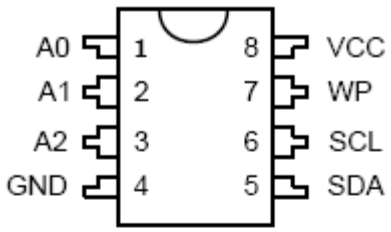
Absolute Maximum Ratings

Operating Temperature		-55℃ to +125℃
Storage Temperature		-65℃ to +150℃
Voltage on Any Pin with Respect to Ground		-1.0V to +7.0V
Maximum Operating Voltage	ACE24LC02/04/08/16	6.25V
DC Output Current		5.0 mA

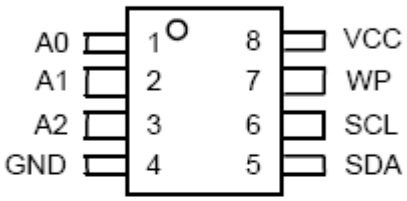
*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

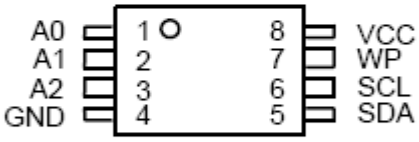
DIP8



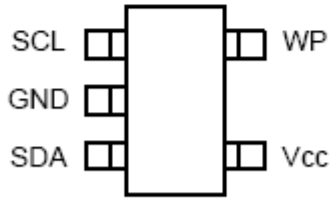
SOP8



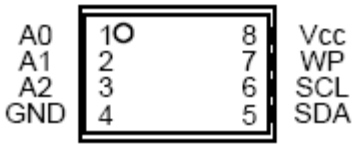
TSSOP8



SOT23-5



TDFN8



Pin Configurations

Pin Name	Function
A0~A2	Device Address Inputs
SDA	Serial Data Input / Output
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
GND	Ground

Block Diagram

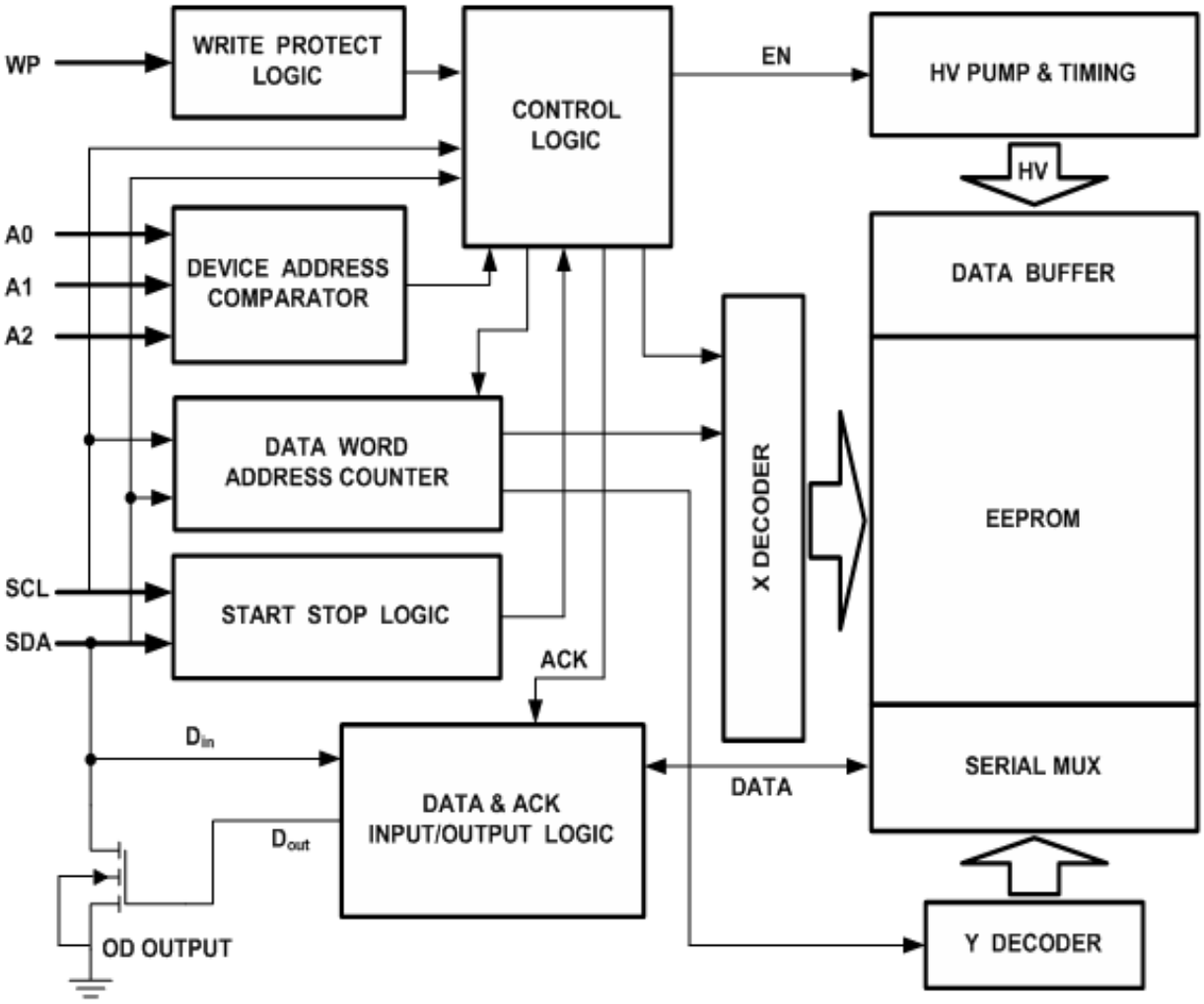


Figure 1

Ordering information

ACE24LC02/04/08/16 XX + X H

- H : Halogen-free
- X : U : Tube / T : Tape and Reel
- + : Pb - free
- XX : DP : DIP-8 / FM : SOP-8 / TM : TSSOP-8 / BN : SOT-23-5 / DM : TDFN-8

Serial Clock (SCL):

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA):

The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device/Page Addresses (A2, A1, A0):

The A2, A1 and A0 pins are device address inputs that are hard wired for the ACE24LC02, As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The ACE24LC04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pins are no connects.

The ACE24LC08 only uses A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The ACE24LC16 does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

Write Protect (WP):

The ACE24LC02/04/08/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is conceded to Vcc the write protection feature is enabled.

Write Protect Description

WP Pin Status	Part of the Array Protected			
	ACE24LC02	ACE24LC04	ACE24LC08	ACE24LC16
WP=V_{CC}	Full (2K) Array	Full (4K) Array	Full (8K) Array	Full (16K) Array
WP=GND	Normal Read / Write Operations			

Memory Organization

ACE24LC02, 2K SERIAL EEPROM:

Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

ACE24LC04, 4K SERIAL EEPROM:

Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

ACE24LC08, 8K SERIAL EEPROM:

Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

ACE24LC16, 16K SERIAL EEPROM:

Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

Pin Capacitance

Applicable over recommended operating range from: T_A = 25℃, f = 1.0 MHz, V_{CC} = +1.7V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$[1]	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}[1]	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +3.6V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V, Read at 100K		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V, Write at 100K		2.0	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V, V_{IN} = V_{CC}/ V_{SS}			1.0	μA
I_{SB2}	Standby Current	V_{CC} = 3.6V, V_{IN} = V_{CC}/ V_{SS}			3.0	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/V_{SS}		0.10	3.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}/ V_{SS}		0.05	3.0	μA
V_{IL}[1]	Input Low Level		-0.6		V_{CC}x0.3	V
V_{IH}[1]	Input High Level		V_{CC}x0.7		5.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V, I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +3.6V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7-volt		2.5-volt		3.6-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000		1000	kHz
T_{LOW}	Clock Pulse Width Low	1.3		0.4		0.4		μs
T_{HIGH}	Clock Pulse Width High	0.6		0.4		0.4		μs
T_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	0.05	0.55	μs
T_{BUF}[1]	Time the bus must be free before a new transmission can Start	1.2		0.5		0.5		μs
$T_{HD.STA}$	Start Hold Time	0.6		0.25		0.25		μs
$T_{SU.STA}$	Start Setup Time	0.6		0.25		0.25		μs
$T_{HD.DAT}$	Data In Hold Time	0		0		0		μs
$T_{SU.DAT}$	Data In Setup Time	100		100		100		ns
T_R	Inputs Rise Time		0.3		0.3		0.3	μs
T_F	Inputs Fall Time		300		100		100	ns
$T_{SU.STO}$	Stop Setup Time	0.6		0.25		0.25		μs
T_{DH}	Data Out Hold Time	50		50		50		ns
T_{WR}	Write Cycle Time		5		5		5	ms
Endurance[1]	3.3V, 25℃, Page Mode	1,000,000						Write Cycles

Notes:1. This parameter is characterized and not 100% tested.

2.AC measurement conditions:

RL (connects to Vcc): 1.3kΩ

Input pulse voltages: 0.3 Vcc to 0.7 Vcc

Input rise and fall times: ≦50 ns

Input and output timing reference voltages: 0.5Vcc

Device Operation

Clock and Data Transitions:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

Stop Condition:

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

Acknowledge:

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word. The happens during the ninth clock cycle. Following receipt each word from the EEPROM, the microcontroller should send a zero to EEPROM and continue to output the next data word or send a stop condition to finish the read cycle.

Standby Mode :

The ACE24LC02/04/08/16 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Device Reset :

After an interruption in protocol power loss or system reset, any two-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high and then.
3. Create a start condition.

Bus Timing

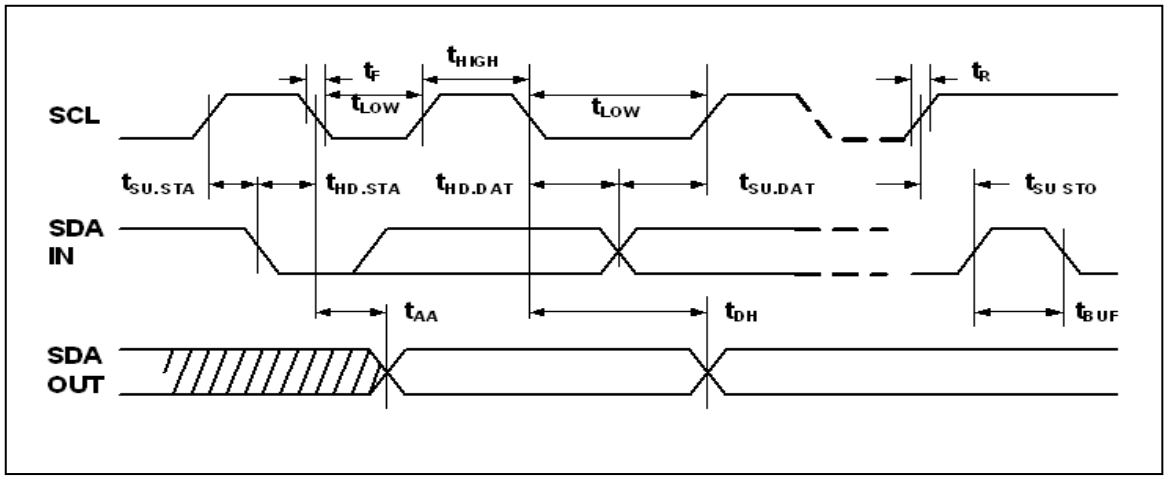


Figure 2 · SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

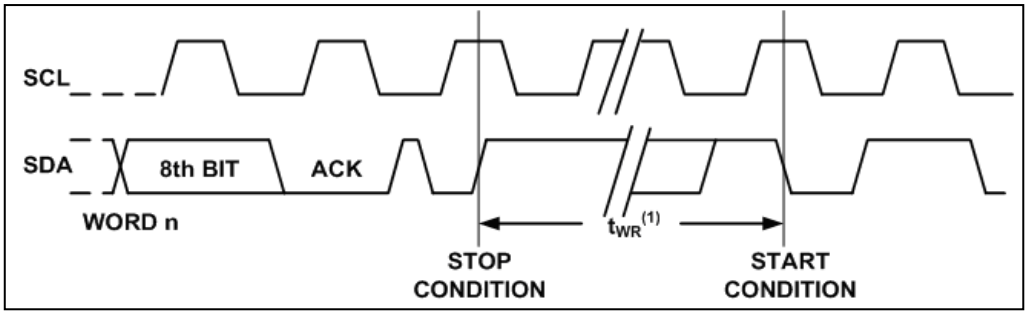


Figure 3. SCL: Serial Clock, SDA: Serial Data I/O

Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

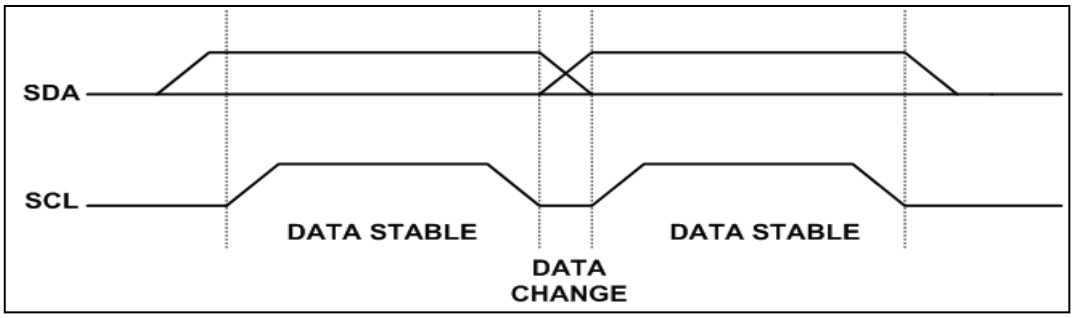


Figure 4 · Data Validity

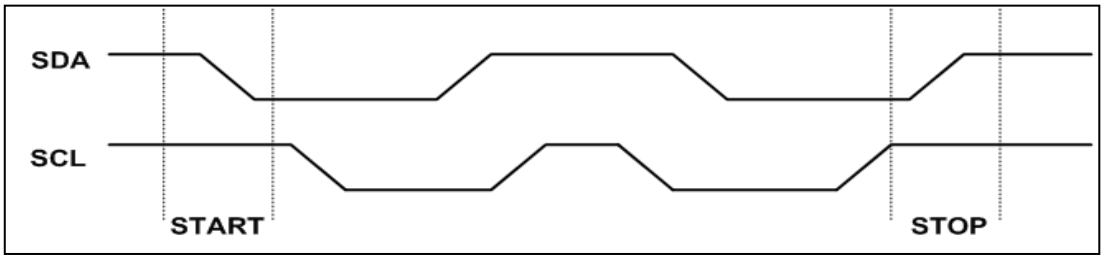


Figure 5 · Start and Stop Definition

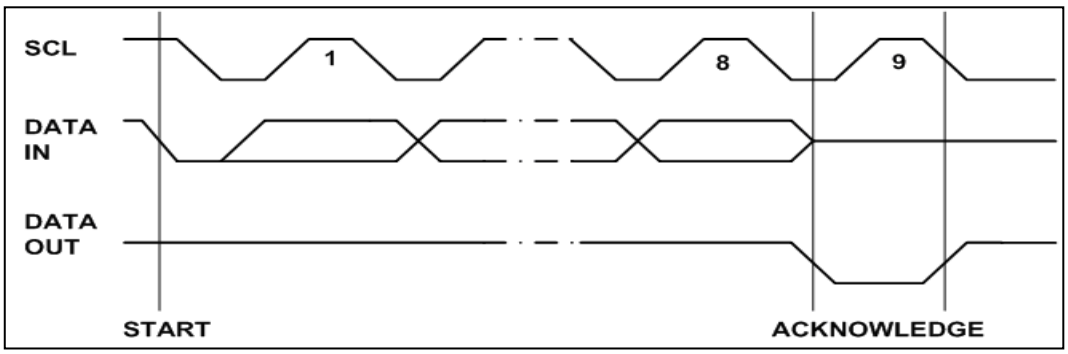


Figure 6 · Output Acknowledge

Device Addressing

The 2K, 4K, 8K and 16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 7).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins (The A2, A1 and A0 device address bits are “0” for the 2K EEPROM of STO-23-5 package)

The 4K EEPROM only uses the A2 and A1 device addressing. The third bit is a memory page address bit. The A2, A1 bit must compare to its corresponding hard-wired input pin. The A0 pin is no connecting.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connecting.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

Byte Write:

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 8).

Page Write:

The 2K EEPROM is capable of an 8-byte page write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 9).

The data word address lower three (2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

Acknowledge Polling:

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

Current Address Read:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 10).

Random Read:

A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 11).

Sequential Read:

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit (2K,8K,16K) is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 12).

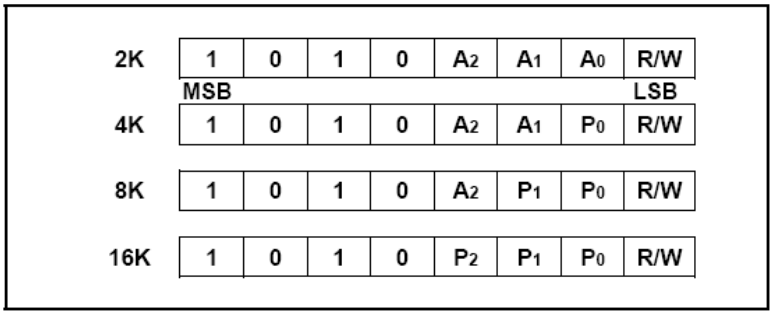


Figure 7 · Device Address

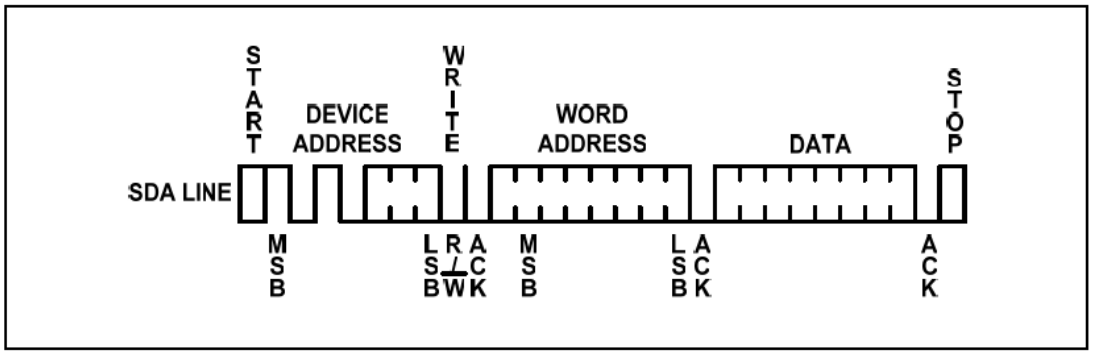


Figure 8 · Byte Write

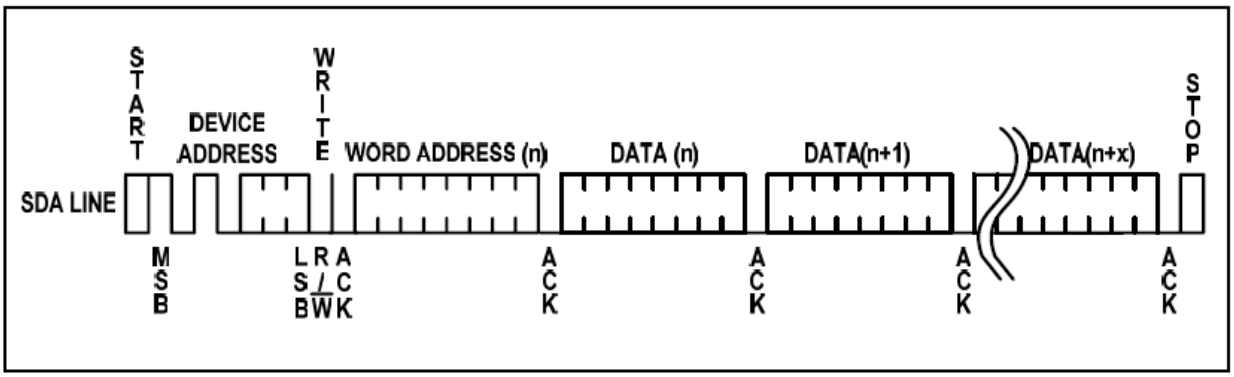


Figure 9 · Page Write

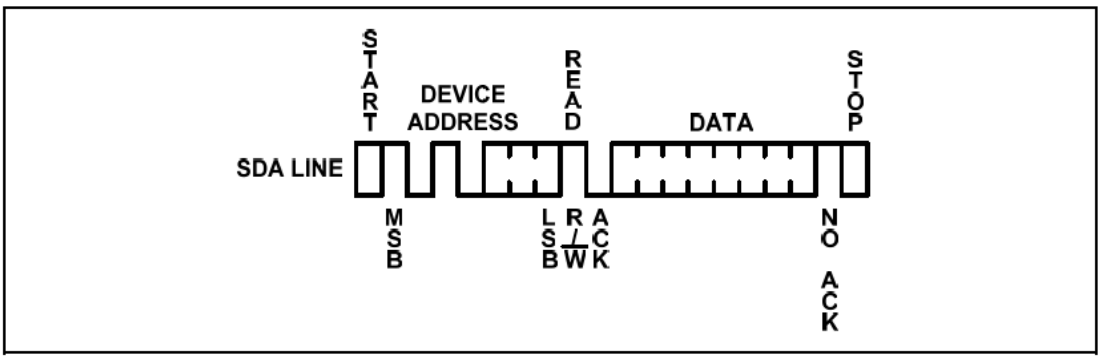


Figure 10 · Current Address Read

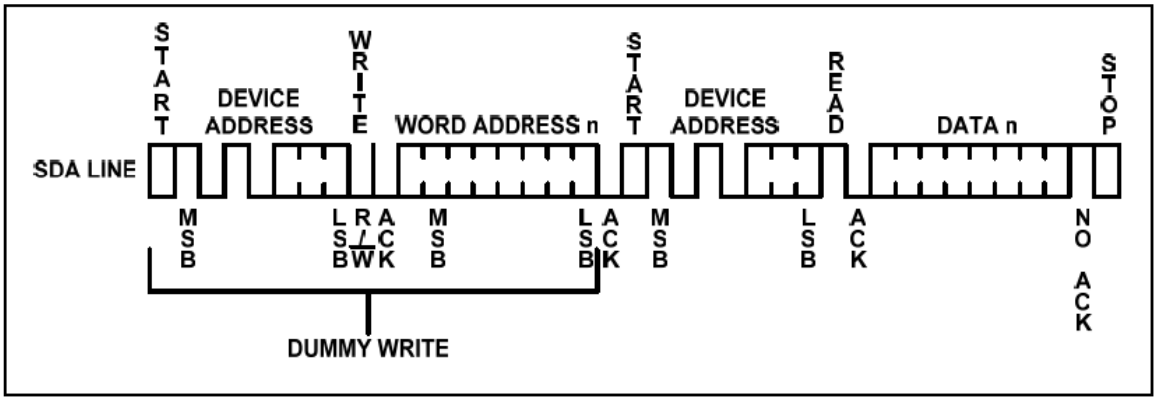


Figure 11 · Random Read

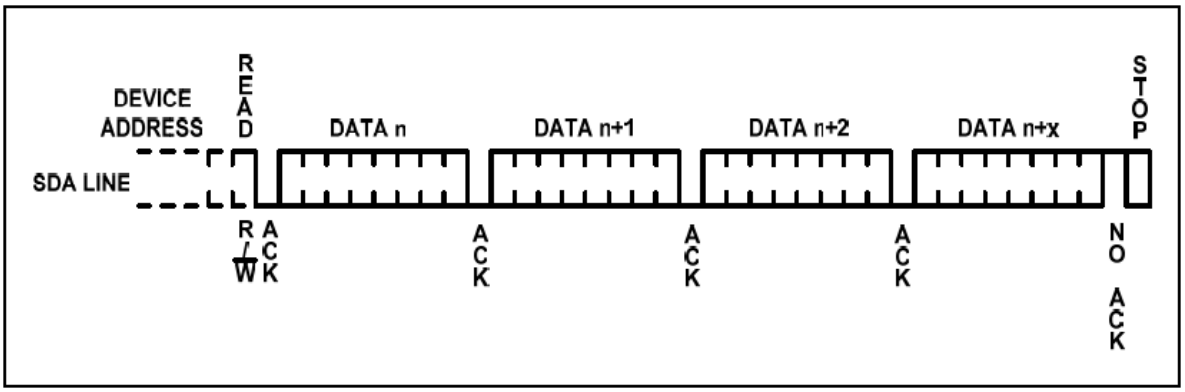
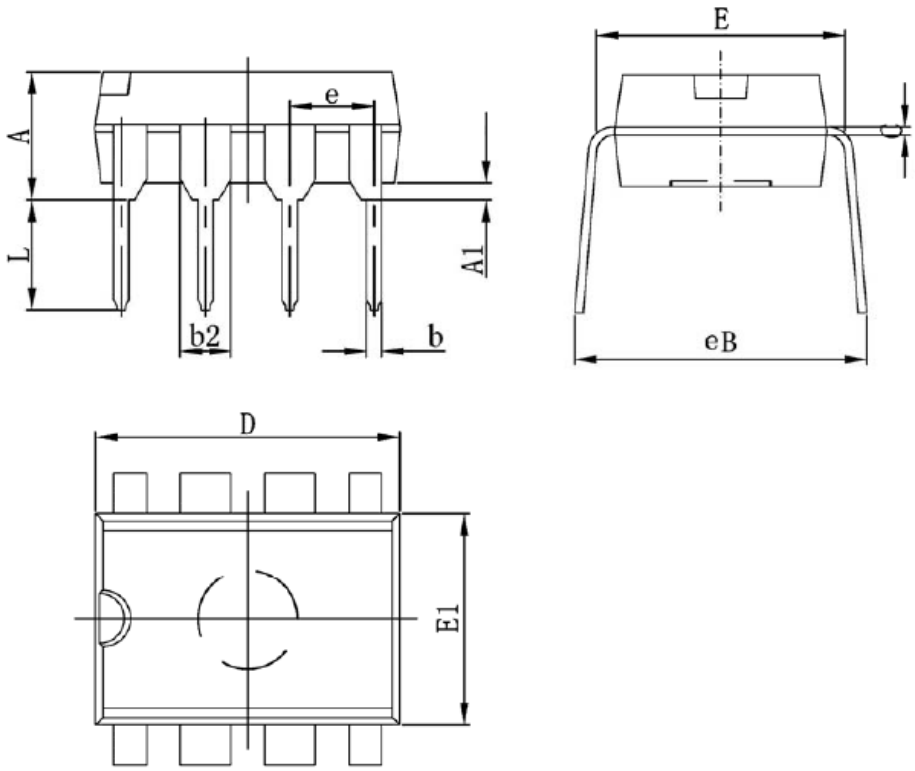


Figure 12 · Sequential Read

Packaging information

DIP-8

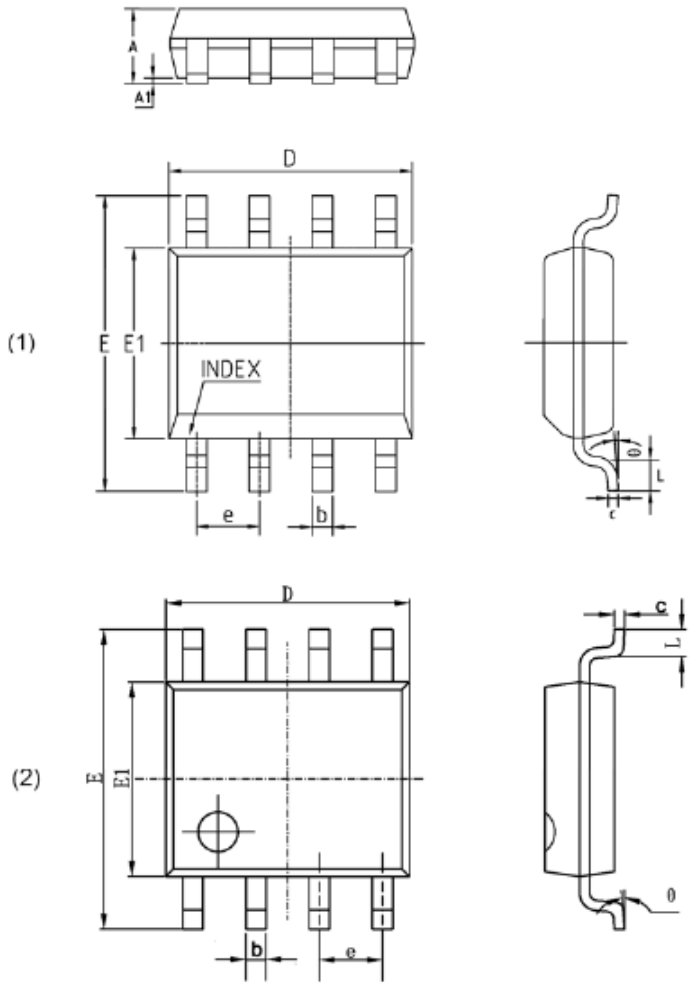


Symbol	MIN	MAX
A	3.710	4.310
A1	0.510	
b	0.380	0.570
b2	1.524(BSC)	
C	0.204	0.360
D	9.000	9.400
E1	6.200	6.600
E	7.320	7.920
e	2.540(BSC)	
L	3.000	3.600
eB	8.400	9.000

NOTE:
1. Dimensions are in Millimeters.

Packaging information

SOP-8

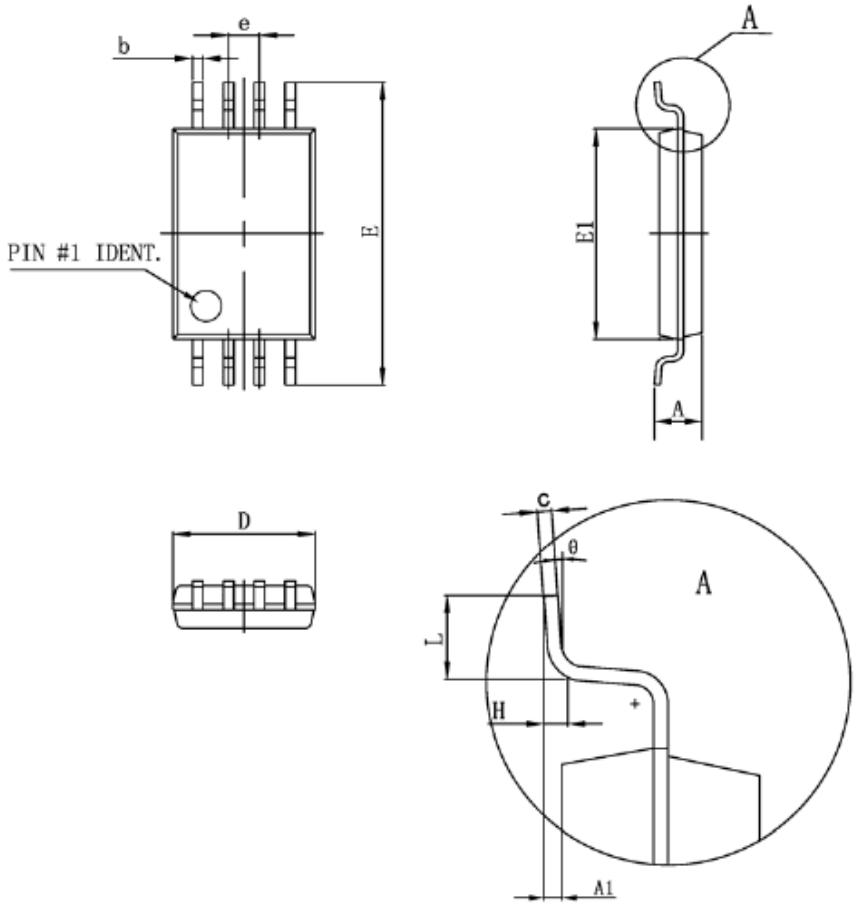


Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.250
D	4.700	5.150
E1	3.800	4.000
E	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

NOTE:
1. Dimensions are in Millimeters.

Packaging information

TSSOP-8

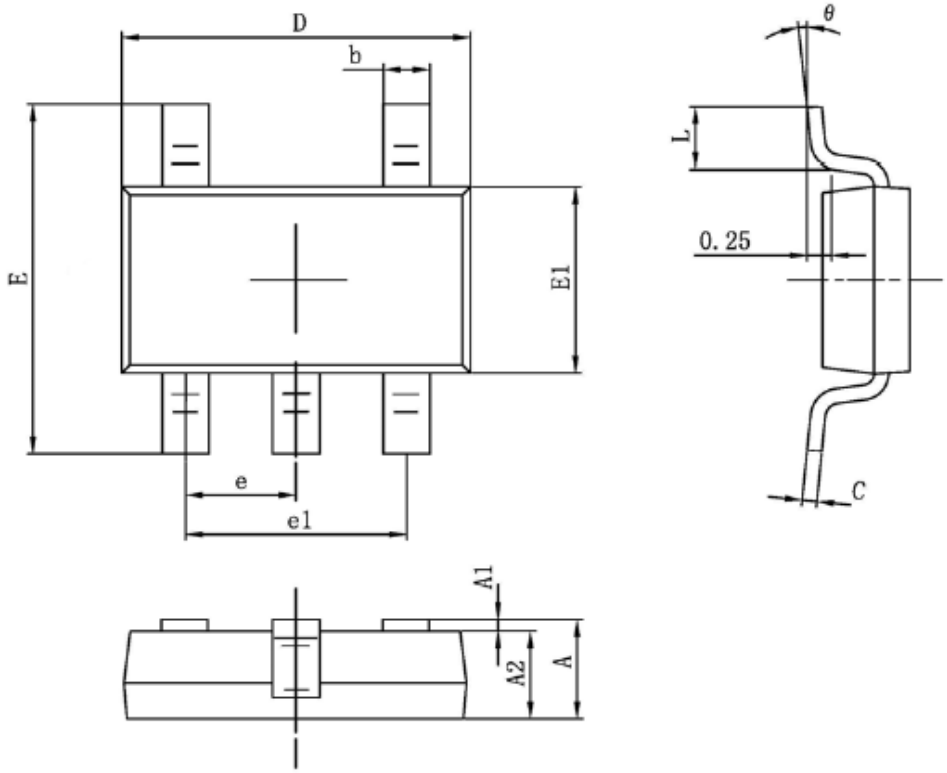


Symbol	MIN	MAX
D	2.830	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
H	0 250 (TYP)	
θ	0°	8°

NOTE:
1. Dimensions are in Millimeters.

Packaging information

SOT-23-5

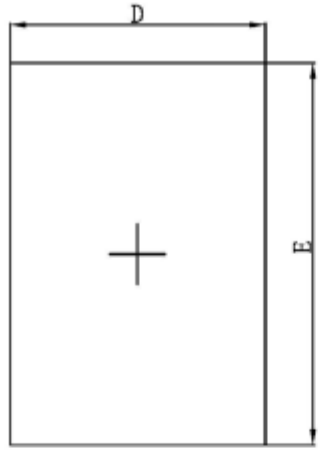


Symbol	MIN	MAX
A	0.700	0.900
A1	0.000	0.100
A2	0.700	0.800
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E1	1.600	1.700
E	2.650	2.950
e	0.950(BSC)	
e1	1.900(BSC)	
L	0.300	0.600
θ	0°	8°

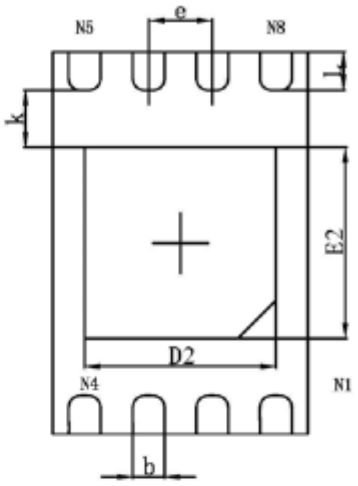
NOTE:
1. Dimensions are in Millimeters.

Packaging information

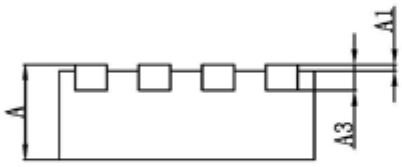
TDFN-8



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
A3	0.203(REF)	
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.600
k	0.200(MIN)	
b	0.200	0.300
e	0.500(TYP)	
L	0.200	0.400

NOTE:
1. Dimensions are in Millimeters.

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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