TORISAN

ENGINEERING SPECIFICATIONS

LIQUID CRYSTAL DOT MATRIX DISPLAY MODULE

10.4 inch VGA, Dual Scan Color STN

LM-EH53-22NAK

(640×R·G·B×480 dots)

(With cold fluorescent backlight)

Nonglare type

(TENTATIVE)

	Oct.	26, 1995
Rev.1	Jan.	25, 1996
Rev.2	Feb.	8, 1996
Rev.3	Jul.	4, 1996

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This specifications may be changed without any notice in order to improve performance or quality.

HISTORY OF CHANGES

DATE	REVISION NO.	PAGE	DESCRIPTIONS

NOTE

■ MECHANICAL CHARACTERISTICS

Item	Specification	Unit
Package dimensions	243(W)×179.4(H)×7±0.5(D)	mm
Structure	640(W)×R·G·B(W)×480(H)	dot
Dot size	0.09(W)×0.31(H)	mm
Dot pitch	0.11(W)×0.33(H)	mm
Effective area	216.2(W)×163.4(H)	mm
Weight	Approx. 390	g

■ ELECTRICAL ABSOLUTE MAXIMUM RATINGS

Item	Symbol	MIN.	MAX.	Unit	Remark
Power supply for logic	$V_{DD}-V_{SS}$	0	6.0	V	Ta=25℃
Input voltage	V_I	0	V_{DD}	V	Ta=25℃

■ ELECTRICAL CHARACTERISTICS

Ta=25℃

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Power supply for Logic	$V_{DD}-V_{SS}$			3.0	—	5.5	V
Contrast adjust voltage (1/240 duty)	$V_{COM}-V_{SS}$	Note1	Ta= 5℃	0.8	—	—	V
			Ta=25℃	—	2.1	—	V
			Ta=40℃	—	—	2.8	V
Input signal voltage	V_{IH}	High level		0.7 V_{DD}	—	V_{DD}	V
	V_{IL}	Low Level		0	—	0.3 V_{DD}	V
Supply current(Logic)	I_{DD}	V_{DD}=5.0V Note 2		—	50	250	mA
		V_{DD}=3.3V Note 2		—	70	380	mA

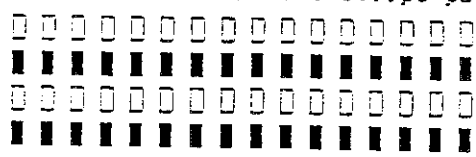
Note 1) The viewing angle ϕ at which the optimum contrast is obtained can be set by adjusting $V_{COM}-V_{SS}$. Refer to *1 for the difinition of ϕ.

Note 2) Under the following conditions :

① Max.value : $V_{COM}-V_{SS}$ = 0.8 V

Typ.value : $V_{COM}-V_{SS}$ = 2.1 V

② Max.value : Black/White stripe pattern



Typ.value : Display data UD0-UD7.LD0-LD7="High"(White)

③ Frame frequency = 74 Hz

■ ENVIRONMENTAL CONDITIONS

Item	Storage		Operating		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-20℃	60℃	5℃	40℃	Note 1
Humidity	Note 2		Note 2		No condensation
Vibration		2.0 G		—	10~55 Hz, X/Y/Z Except for resonant frequency
Shock		50 G		—	XYZ 11 ms

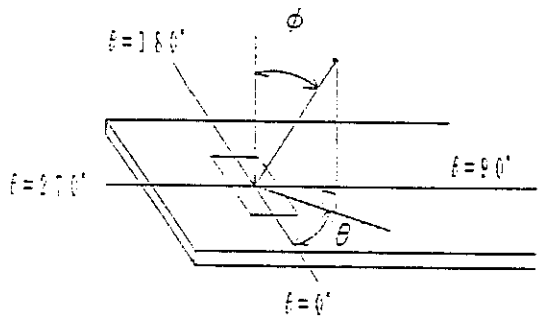
Note 1) Care should be taken so that the LCD unit may not be subjected to the temperature out of this specification.

Note 2) Ta≦40℃ : 85% RH MAX.
Ta>40℃ : Absolute humidity shall be less than that in 85%RH/40℃.

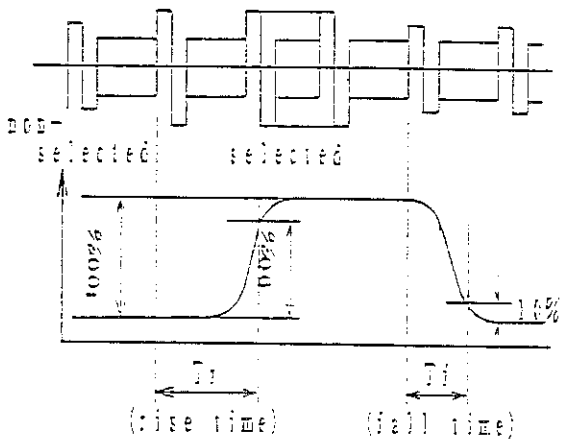
■ OPTICAL CHARACTERISTICS (1)

V_{DD}-V_{SS}=3.3V, V_{CON}-V_{SS}=V_{Kmax}, Ta=25℃

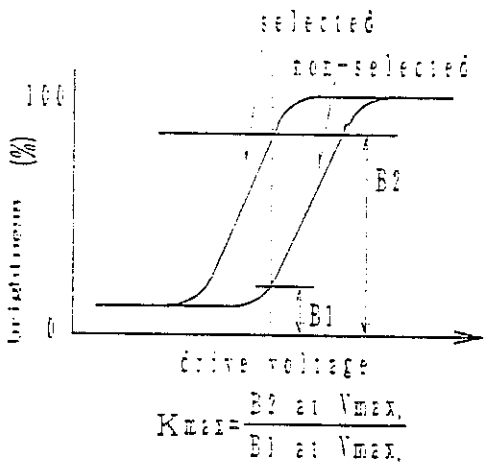
Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range		ϕ	K > 2	θ = 0°	15	—	—	deg.	* 1
				θ =90°	30	—	—		
				θ =180°	20	—	—		
				θ =270°	30	—	—		
Contrast ratio		Kmax	ϕ =0°		15	35		—	* 2 * 4
Response time	Rise	tr	ϕ =0°		—	150	—	ms.	* 3
	Fall	tf	ϕ =0°		—	120	—	ms.	



*1 φ and θ

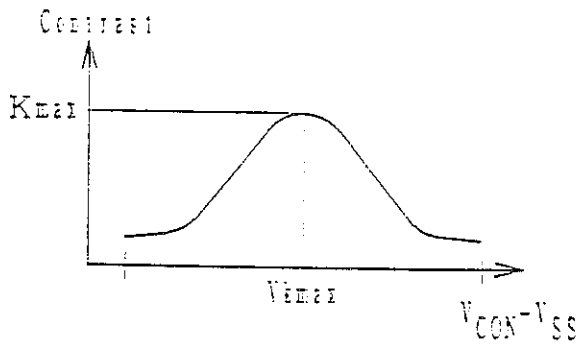


*3 response time



$$Kmax = \frac{B2 \text{ at } Vmax}{B1 \text{ at } Vmax}$$

*2 contrast ratio 'K'



*4 definition of Vkmax.

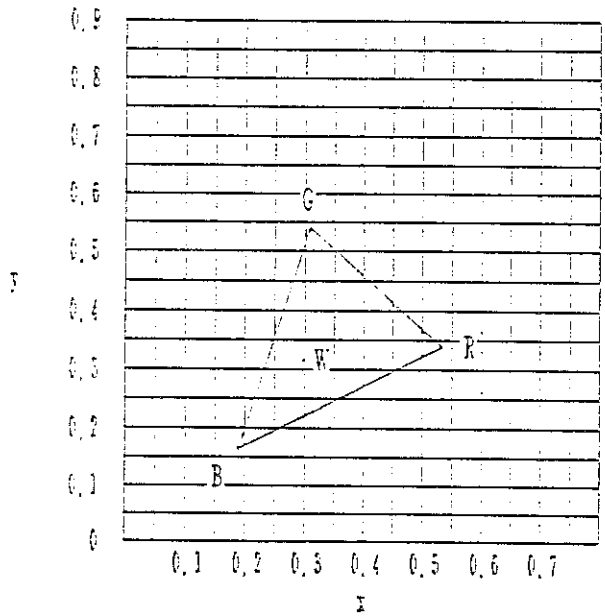
■ OPTICAL CHARACTERISTICS(2)

V_{DD}-V_{SS}=3.3V, V_{COM}-V_{SS}=V_{KMAX}, Ta = 25℃

Item		Symbol	Condition	Typ.	Unit	Note
Color of CIE Coordinate	Red	x	ϕ=0°, θ=0°	0.53	—	*5
		y		0.34		
	Green	x	ϕ=0°, θ=0°	0.31	—	
		y		0.54		
	Blue	x	ϕ=0°, θ=0°	0.19	—	
		y		0.17		
	White	x	ϕ=0°, θ=0°	0.30	—	
		y		0.32		

Tolerance : ± 0.05

*5. Measuring at position 3 on Fig.1
CIE chromaticity diagram



■ OPTICAL CHARACTERISTICS (3)

Surface Brightness of LCD

Item	Min.	Typ.	Max.	Unit
Brightness	50	70	—	cd/m²

Note) The brightness shall be the average of the following 5 point.

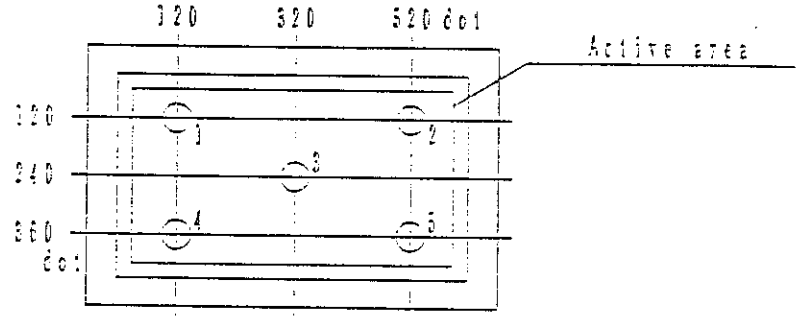


Fig. 1 Measuring points

Measurement equipment : BM-7 (TOPCON Corporation) or CA-1000(MINOLTA)

Measurement condition

① Ambient temperature : 25℃

② LCD : All digits WHITE , V_{DD}= 3.3V, V_{COM}-V_{SS}=V_{RMS},
Frame frequency=74Hz
UD_0 — UD_1=HIGH(WHITE), LD_0 — LD_1=HIGH(WHITE)

③ Measurement after 30 minutes of CFL operating.

④ I_L= 3.5 mArms

■ BACKLIGHT CHARACTERISTICS

CFL RATINGS

Ta=25℃ , Within no conductor closed.

Item		Max. allowable value
Non-load output voltage (V_S)	1200 Vrms Min. (*)	—
Lamp current (I_L)	3 mArms — 5 mArms	5 mArms
Lamp voltage (V_L)(at 3.5 mA)	580 Vrms Typ.	—
Operating life (at 3.5 mA)	10000 hours Min.	—

(*) The Non-load output voltage(VS) of the inverter should be designed to have some margin(reference value:1400Vrms MIN.), because VS may be increased due to the leak current which may be caused by wiring of CFL cables.

■ INTERFACE PIN CONNECTION

Interface		Pin No.	Symbol	Function
LCM	CN1	1	LD4	Display data (Lower)
		2	VSS	GND
		3	LD5	Display data (Lower)
		4	FLM	Scan start-up signal
		5	LD6	Display data (Lower)
		6	CL1	Input data latch signal
		7	LD7	Display data (Lower)
		8	VSS	GND
		9	VSS	GND
		10	CL2	Data input clock
		11	LD0	Display data (Lower)
		12	VCON	Contrast adjust voltage
		13	LD1	Display data (Lower)
		14	VDD	Logic supply voltage
		15	VSS	GND
		16	VDD	Logic supply voltage
		17	LD2	Display data (Lower)
		18	DISP	Display control signal H:ON , L:OFF
		19	LD3	Display data (Lower)
		20	NC	
		21	VSS	GND
		22	UD3	Display data (Upper)
		23	UD4	Display data (Upper)
		24	UD2	Display data (Upper)
		25	UD5	Display data (Upper)
		26	UD1	Display data (Upper)
		27	VSS	GND
		28	UD0	Display data (Upper)
		29	UD6	Display data (Upper)
		30	VSS	GND
		31	UD7	Display data (Upper)

CN1 : DF9B-31P-1V (HIROSE)／Suitable Connector : DF9B-31S-1V (HIROSE)

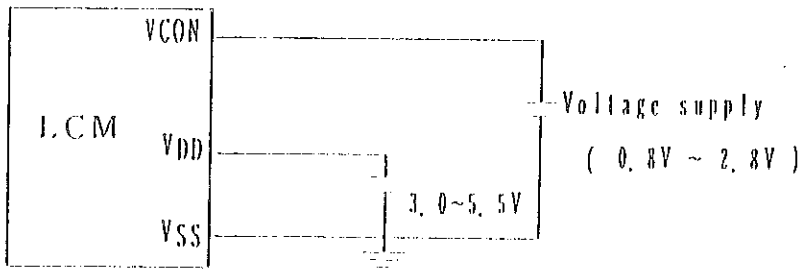
Connector	Pin No.	Symbol	Function
FLCN	1	H.V	Power supply voltage for CFL
	2	N.C	———
	3	GND	CFL GND

FLCN : BHR-03VS-1 (JST)／Suitable Connector : SM02(8.0)B-BHS-1 (JST)

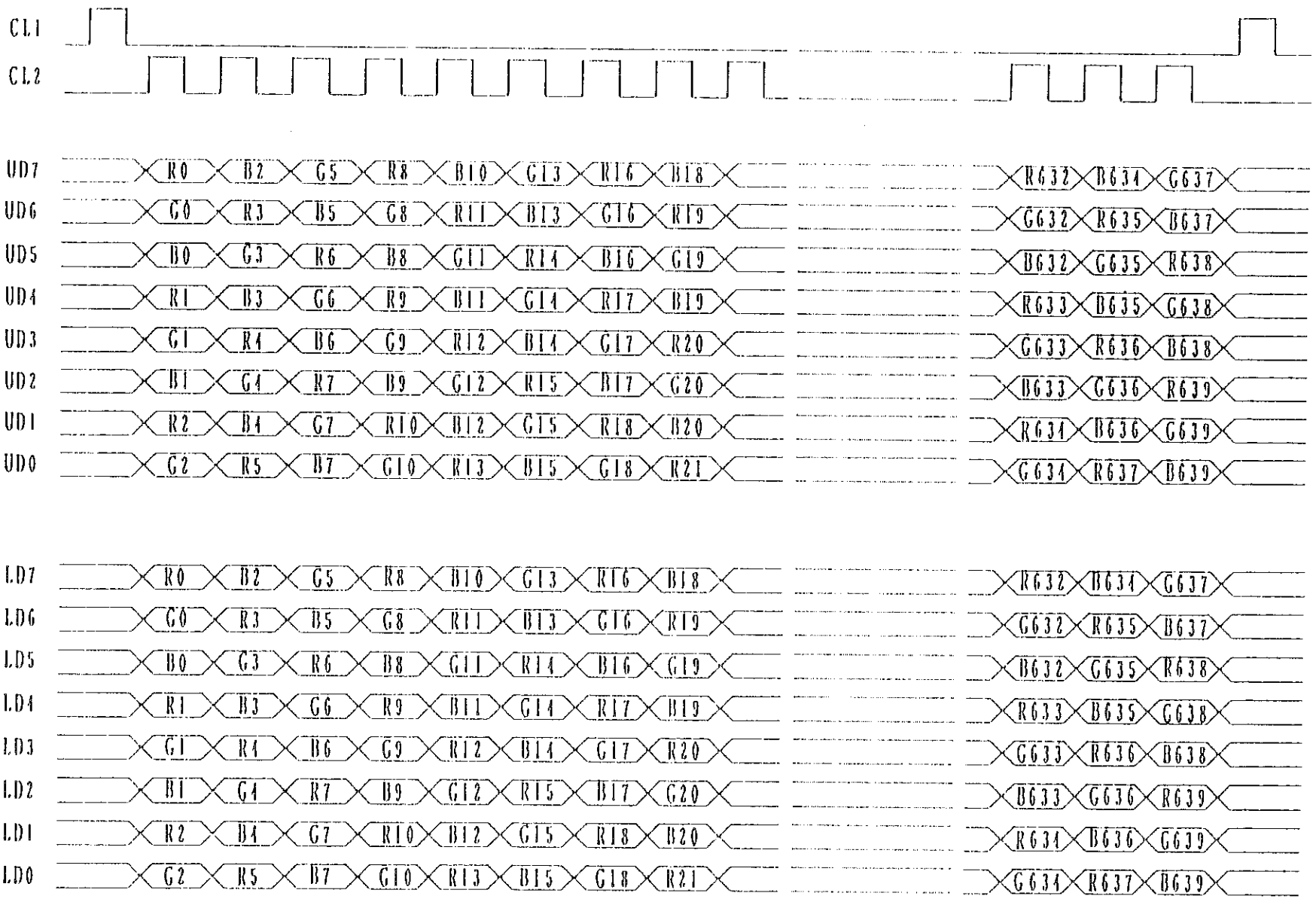
■ DISPLAY VS. DATA CORRESPONDING DIAGRAM

X \ Y	1	2	3	4	5	6	7	8	...	1913	1914	1915	1916	1917	1918	1919	1920
1	R0 UD7	G0 UD6	B0 UD5	R1 UD4	G1 UD3	B1 UD2	R2 UD1	G2 UD0		G637 UD7	B637 UD6	R638 UD5	G638 UD4	B638 UD3	R639 UD2	G639 UD1	B639 UD0
2	R0 UD7	G0 UD6	B0 UD5	R1 UD4	G1 UD3	B1 UD2	R2 UD1	G2 UD0		G637 UD7	B637 UD6	R638 UD5	G638 UD4	B638 UD3	R639 UD2	G639 UD1	B639 UD0
239	R0 UD7	G0 UD6	B0 UD5	R1 UD4	G1 UD3	B1 UD2	R2 UD1	G2 UD0		G637 UD7	B637 UD6	R638 UD5	G638 UD4	B638 UD3	R639 UD2	G639 UD1	B639 UD0
240	R0 UD7	G0 UD6	B0 UD5	R1 UD4	G1 UD3	B1 UD2	R2 UD1	G2 UD0		G637 UD7	B637 UD6	R638 UD5	G638 UD4	B638 UD3	R639 UD2	G639 UD1	B639 UD0
241	R0 LD7	G0 LD6	B0 LD5	R1 LD4	G1 LD3	B1 LD2	R2 LD1	G2 LD0		G637 LD7	B637 LD6	R638 LD5	G638 LD4	B638 LD3	R639 LD2	G639 LD1	B639 LD0
242	R0 LD7	G0 LD6	B0 LD5	R1 LD4	G1 LD3	B1 LD2	R2 LD1	G2 LD0		G637 LD7	B637 LD6	R638 LD5	G638 LD4	B638 LD3	R639 LD2	G639 LD1	B639 LD0
479	R0 LD7	G0 LD6	B0 LD5	R1 LD4	G1 LD3	B1 LD2	R2 LD1	G2 LD0		G637 LD7	B637 LD6	R638 LD5	G638 LD4	B638 LD3	R639 LD2	G639 LD1	B639 LD0
480	R0 LD7	G0 LD6	B0 LD5	R1 LD4	G1 LD3	B1 LD2	R2 LD1	G2 LD0		G637 LD7	B637 LD6	R638 LD5	G638 LD4	B638 LD3	R639 LD2	G639 LD1	B639 LD0

■ POWER SUPPLY



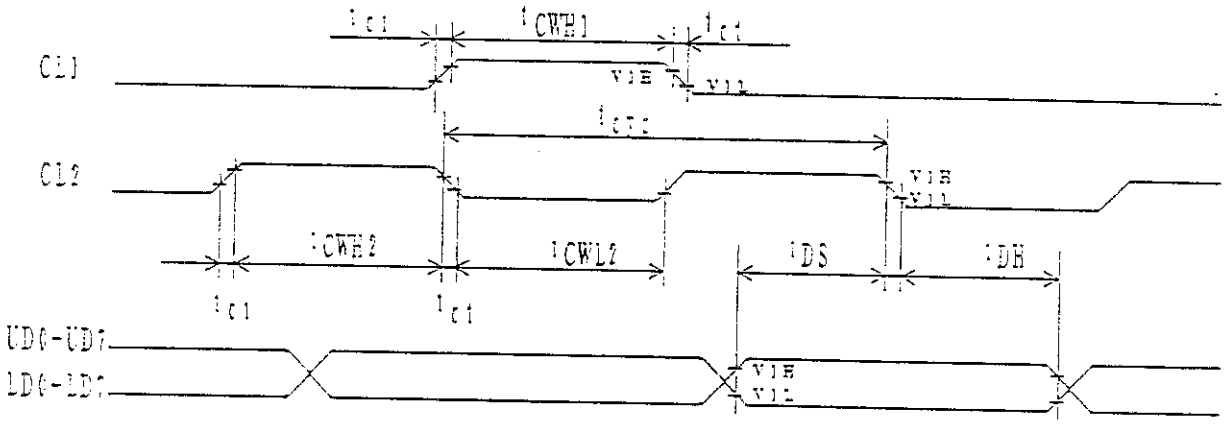
TIMING CHART

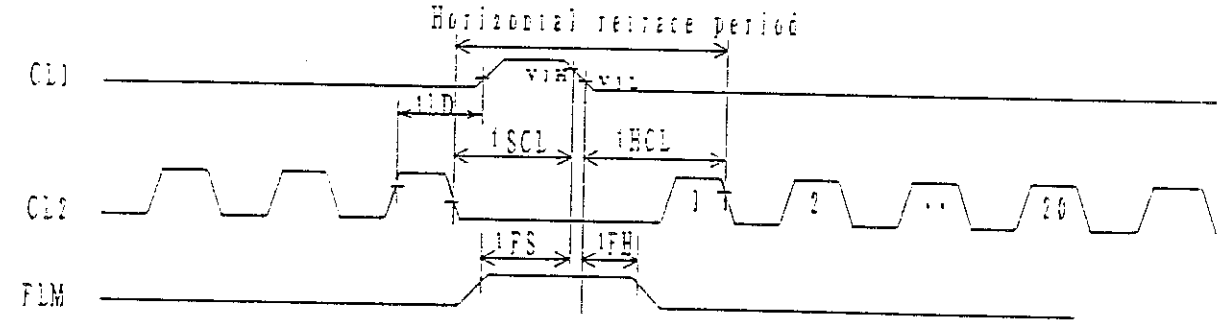


AC ELECTRICAL CHARACTERISTICS

V_{DD}=3-4.5V Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle time	t_{CY2}	76	—	—	ns
CL2 High level width	t_{CWH2}	25	—	—	ns
CL2 Low level width	t_{CWL2}	25	—	—	ns
CL1 High level width	t_{CWH1}	50	—	—	ns
CL2 setup time	t_{SCL}	100	—	—	ns
CL2 hold time	t_{HCL}	100	—	—	ns
CL2 → CL1 rise time	t_{LD}	0	—	—	ns
Clock rise/fall time	t_{C1}	—	—	50	ns
Data setup time	t_{DS}	20	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
FLM setup time	t_{FS}	100	—	—	ns
FLM hold time	t_{FH}	30	—	—	ns
Frame frequency	f_{FLM}	70	74	130	Hz

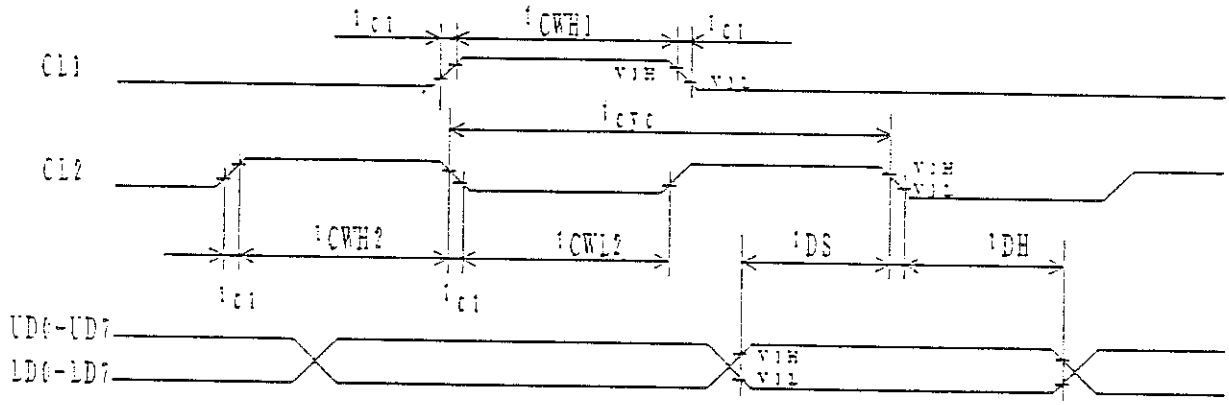


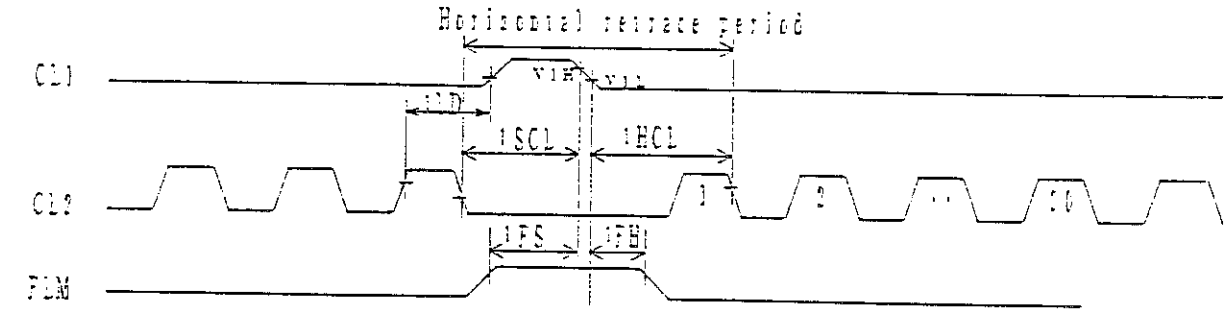


■ AC ELECTRICAL CHARACTERISTICS

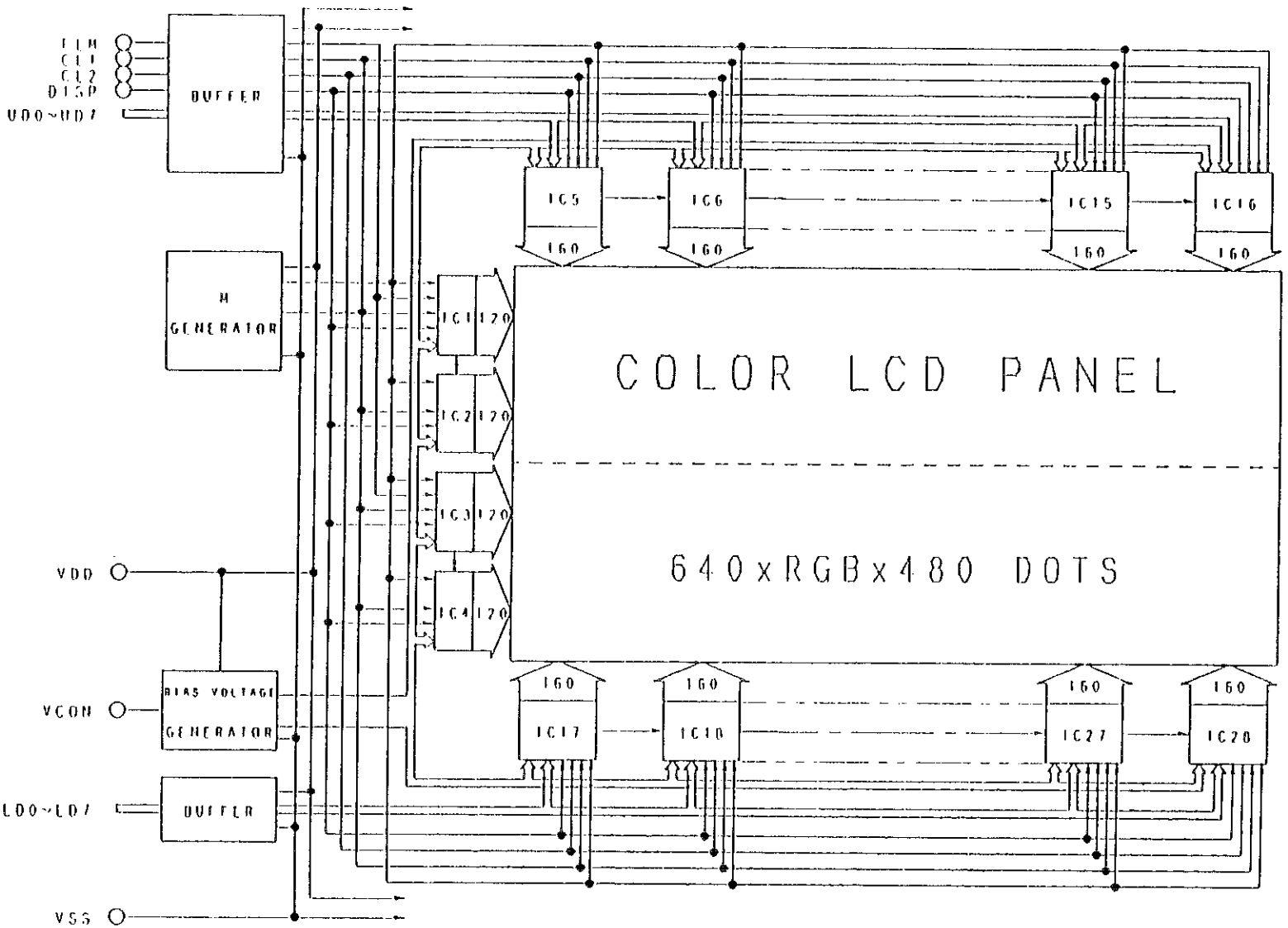
V_{DD}=5V±10% Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle time	t_{CYC}	62	—	—	ns
CL2 High level width	t_{CWH2}	15	—	—	ns
CL2 Low level width	t_{CWL2}	15	—	—	ns
CL1 High level width	t_{CWH1}	50	—	—	ns
CL2 setup time	t_{SCL}	100	—	—	ns
CL2 hold time	t_{HCL}	100	—	—	ns
CL2 → CL1 rise time	t_{LD}	0	—	—	ns
Clock rise/fall time	t_{Ci}	—	—	50	ns
Data setup time	t_{DS}	10	—	—	ns
Data hold time	t_{DH}	10	—	—	ns
FLM setup time	t_{FS}	100	—	—	ns
FLM hold time	t_{FH}	30	—	—	ns
Frame frequency	f_{FLM}	70	74	130	Hz

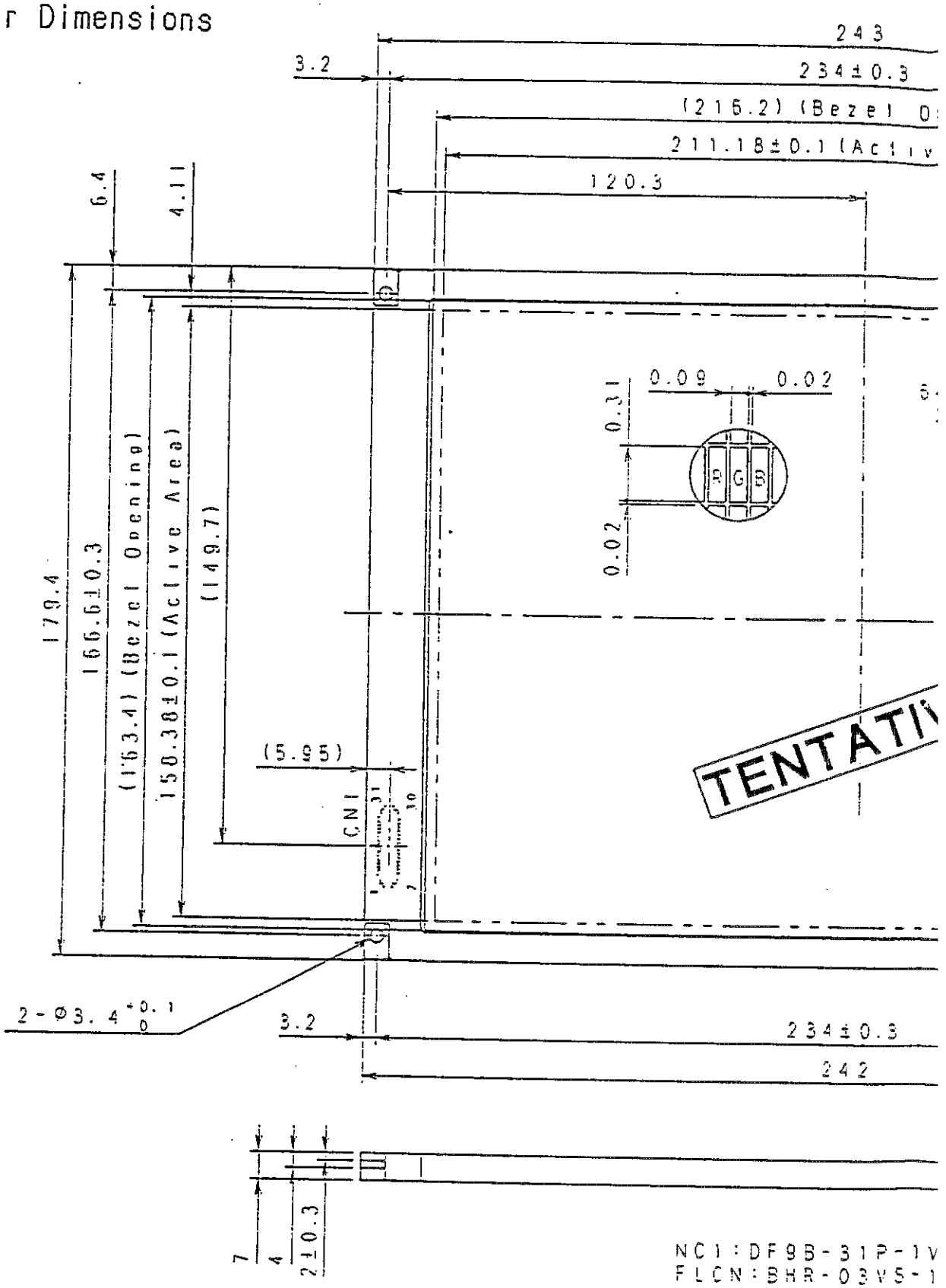




■ BLOCK DIAGRAM

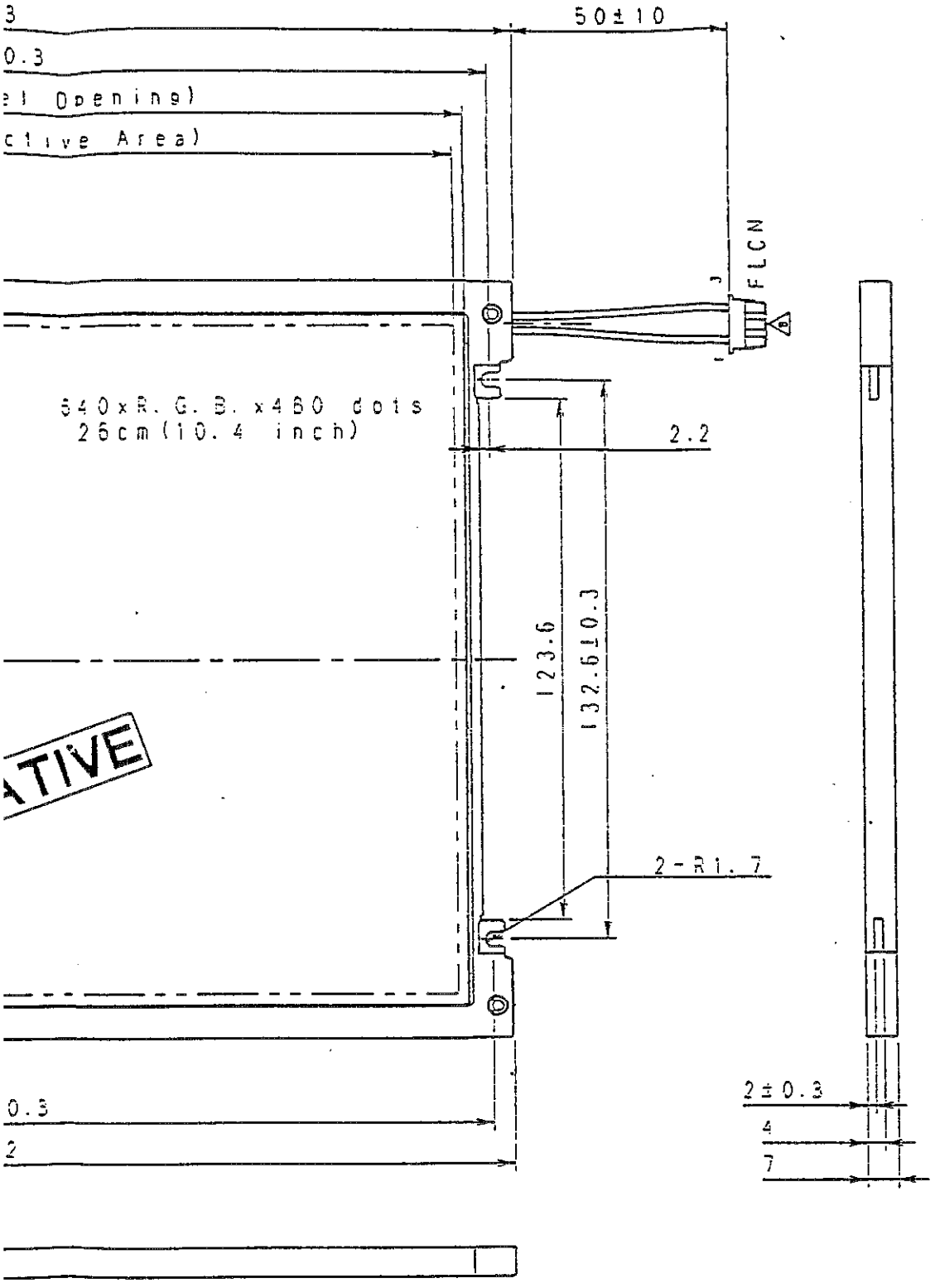


Outer Dimensions



NC1 : DF9B-31P-1V
FLCN : BHR-03VS-1

NOTE : ALL DIMENSION
UNLESS OTHERW



1P-1V(HIROSE)
BVS-1(JST)

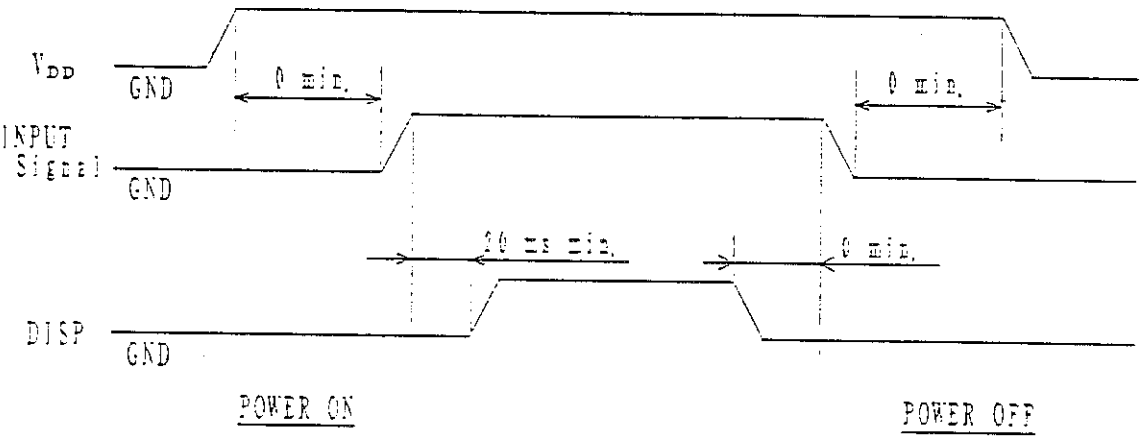
FLCN PIN-1:HIGH
PIN-3:GND

NSIONAL TOLERANCE ±0.5
THERWISE SPECIFIED

Unit:mm

■ Power Supply Sequence

Do not apply DC voltage to the LCD panel because that induces the electro-chemical reaction and reduces its life time. Please follow the power supply ON/OFF sequence to prevent DC driving of LCD or latch-up of CMOS LSI, as shown below.



Note 1. DISP rise and fall time should be 100 ns max.

Fig.2 Power ON/OFF sequence

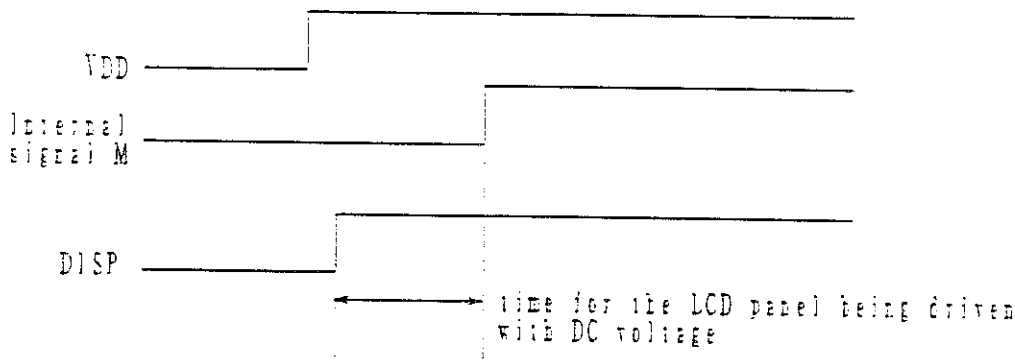


Fig.3 Time for the LCD panel being driven with DC voltage

At power on, if "DISP" signal is "H" level before LCD panel AC driving signal(M) is generated, the LCD panel is driven with DC voltage in the meantime. (Refer to Fig.3.)

■ Example to prevent LCD DC apply by using DISP

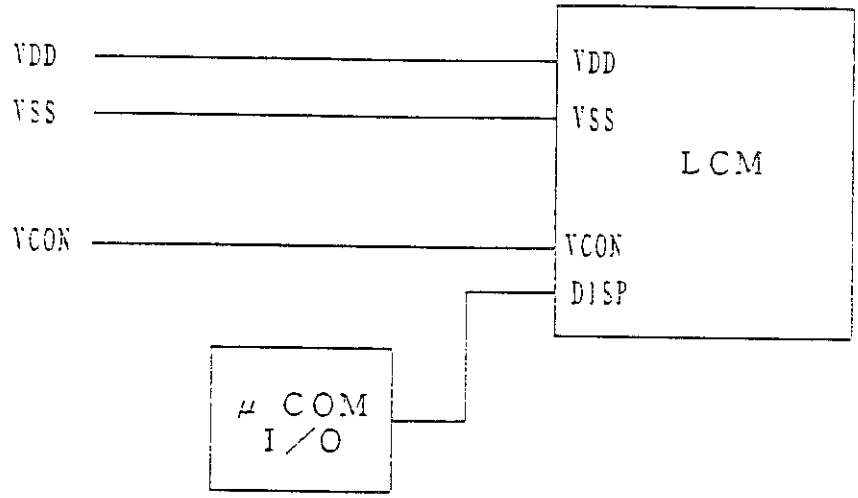


Fig.4 Example to prevent LCD DC apply by using DISP

Connect I/O port of micro-computer in the main system with DISP and control it. Until initialization of LC control LSI is finished after power ON, signal(M) isn't generated, so that DC voltage is applied to the LCD panel. (Refer to Fig.3.) During this time, switch I/O port(DISP) to 'L' and force apply voltage to the LCD panel into 0V. After initialization of LC control LSI, switch I/O port(DISP) to 'H', so that the LCD panel is returned to the normal driving voltage. (Refer to Fig.5.)

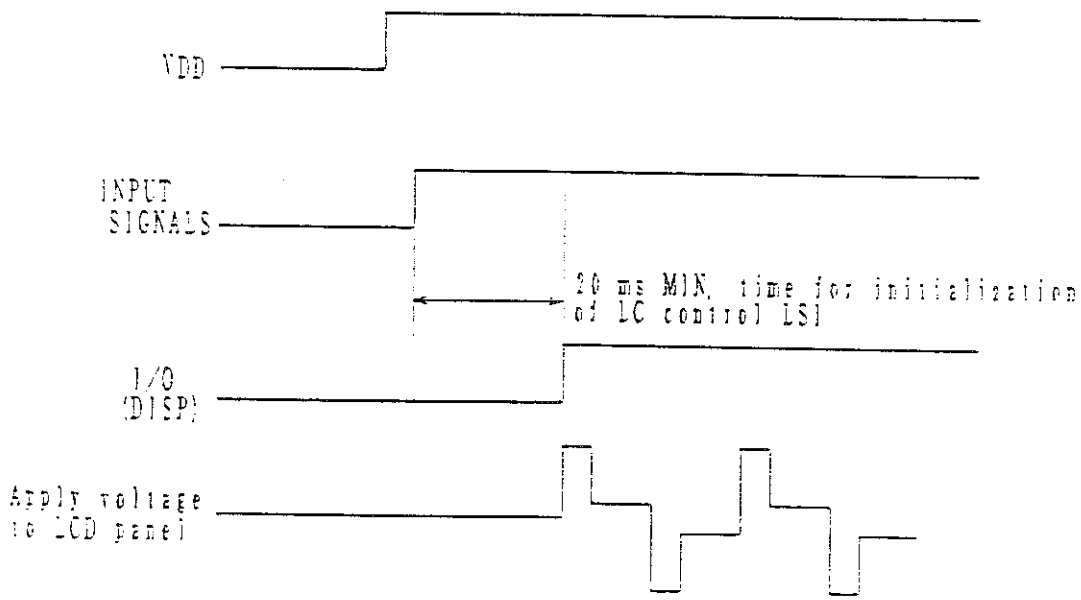


Fig.5 Timing chart without DC apply to the LCD panel (2)

■ PRECAUTION FOR USING

1. Handling

(1) Do not touch, press or rub the display panel with a hard, stiff tool or the like (e.g. tweezers) since the polarizers on the surface are easily scratched.

(2) Do not use organic solvents to clean the display panel as these solvents may adversely affect the polarizer. To clean the display panel dampen a bit of absorbent cotton with petroleum benzine and gently wipe the panel, or stick contaminations by using a scotch tape.

(3) Do not touch terminals of electrodes of P.W.B. or LSI leads.

(4) Avoid using or storing the LCM under high temperature and high humidity conditions. At the storing, it is recommended that the device is packaged in a conductive polyethylene bag and placed under the condition where the temperature is relatively lower (10 to 30℃), and the direct sunlight or fluorescent lamp must be cut off.

(5) The casing for the module shall be designed taking account of the rise in temperature because of the heat from the backlight so that good quality of images can be provided on the screen.

(6) Do not suck in, drink or hands off the liquid crystal when it is flown out of the display element due to it's damage.
Wipe the liquid crystal off and wash up with soap or alcohol immediately when hands, clothes, etc. are stuck.

(7) Wash the liquid crystal with pure water for more than 15 minutes and have medical treatment by the doctor when it gets in the eyes.

(8) Follow to the ordinances or the regulations set by the self-governing body in disposing of CFLs.

2. Operation

(1) Do not connect or disconnect the LCM from the main system while power is being supplied.

(2) Use the module within specified temperature; lower temperature causes the retardation of blinking speed of the display; higher temperature makes overall display discolor. When the temperature gets to be within normal limits, the display will operate normally.

(3) Adjust the operating voltage for driving (V_{COM}) so that the display shows optimum contrast.

(4) When supplying an M signal from the external unit to a graphic display of LCM, set the duty to 50% ± 1%. If the duty deviates too greatly from the value, a DC voltage will be applied to the liquid crystal, which could induce an electrochemical reaction and reduce the life of the LCM.

(5) At the operating control voltage for driving (Vcon) varies, the brightness of the display varies likewise.
When Vcon is supplied from the VR, which is composed between VDD and VSS, the variation of the power supply effect to the display, in the case of the stability of the power supply VDD being worse.

3. Workmanship

(1) Never disassemble the module. After disassembling, in case that the module is assembled again and shows a disordered operation, the responsibility of the failure will not lie with vendor.

(2) Care should be taken as not to be charged static electricity, as the circuit of the module contains a CMOS LSI. The workman's body should be grounded with an earth-band. The material which prevents static electricity should be selected for a working clothes.

4. Precautions for handling of CFL cable

(1) Suspended capacity
Take enough precaution with wiring of the CFL cable when incorporating the module in PC unit, and suspended capacity caused by the external mold.

(2) High-frequency noise
Confirm with PC unit and, if necessary, measures should be taken.