73S8009R
Low Cost Versatile Smart Card Interface

Simplifying System Integration™

DATA SHEET

DS_8009R_056

October 2009

ISO/IEC 7816-3

EMVCo

DESCRIPTION

The 73S8009R is a very low-cost level shifter, single smart card (ICC) interface IC. The device includes a level shifter interface between a 3.3 V (typical) logic circuitry (host microcontroller) and an ISO-7816 / EMV smart card. The 73S8009R is designed to provide full electrical compliance with ISO-7816-3 EMV4.1 (EMV2000) and GSM11-11 specifications.

In normal operating mode, for maximum designer flexibility, the host microcontroller is responsible for card activation and deactivation. The 73S8009R incorporates an ISO-7816-3 deactivation sequencer that controls the card signals in case of fault detection and card removal. Card presence and faults are reported to the host through an interrupt output. When the 73S8009R is ready to support a card with the selected voltage, a RDY signal informs the host it can initiate the card activation sequence.

The 73S8009R supports 5V, 3V and 1.8V cards. Selection is done through 2 dedicated digital inputs. Level-shifters drive the card signals with the selected card voltage coming from an internal Low Drop-Out (LDO) voltage regulator. The LDO regulator is powered by a dedicated power supply input, VPC. Digital circuitry is separately powered by a digital power supply, VDD.

Emergency card deactivation is initiated upon card extraction or any fault generated by the protection circuitry. The fault can be a card over-current, a VDD (digital power), a VPC (regulator power), a VCC (card power output) or an over-heating fault.

A chip select digital input drives internal latches that allow the host controller to control multiple 73S8009R ICs in parallel. A power down digital input also allows the host microcontroller to place the IC in a very low-power mode making the 73S8009R particularly suitable for low-power and battery-powered applications.

Auxiliary I/O lines are also available (SO28 package only) and make the 73S8009R suitable for all kind of cards, including synchronous (memory) cards.

APPLICATIONS

- Set-Top-Box Conditional Access and Pay-per-View
- SIM card readers in DECT and GSM phones, GPRS, WIFI and VOIP devices
- Point of Sales & Transaction Terminals
- General purpose smart card readers

ADVANTAGES

- Lowest cost smart card interface IC on the market
  - → Ideal to replace discrete designs in POS terminals and Set-Top-Boxes
- Traditional step-up converter is replaced by an LDO regulator
  - → Greatly reduced power dissipation
  - → Fewer external components are required
  - → Better noise performance
  - → Very low power dissipation
- Small format (4x4x0.8 mm) QFN20 package option

FEATURES

- Card Interface:
  - Complies with ISO-7816-3, EMV 4.0 and GSM 11-11 specifications
  - An LDO voltage regulator provides 1.8V / 3V / 5V to the card from an external power supply input
  - Provides at least 90 mA to the card
  - ISO-7816-3 card emergency deactivation sequencer
  - Protection includes 3 voltage supervisors that detect voltage drops on V_{CC} (card), V_{DD} (digital) and V_{PC} (regulator) power supplies
  - Over-current detection, 150 mA max.
  - 2 card detection inputs, 1 for each user polarity
  - Auxiliary I/O lines for C4 / C8 contact signals
  - Card CLK clock frequency up to 20 MHz

- System Controller Interface
  - Five signal images of the card signals (RSTIN, CLKIN, IOUC, AUX1UC, AUX2UC)
  - Two inputs select card voltage ($\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC3}}$)
  - Two Interrupt outputs ($\overline{\text{OFF}}$, RDY) inform the system controller of card presence / faults and the interface status
  - Chip select input (CS)
  - Power down input (PWRDN)
- Regulator Power Supply (V_{PC}):
  - Class A-B-C readers: 5V, 3V and 1.8V cards: 4.75 V to 6.0 V
- Digital Interface (V_{DD}): 2.7 V to 3.6 V
- 6 kV ESD protection on the card interface
- SO28 or QFN20 package

FUNCTIONAL DIAGRAM

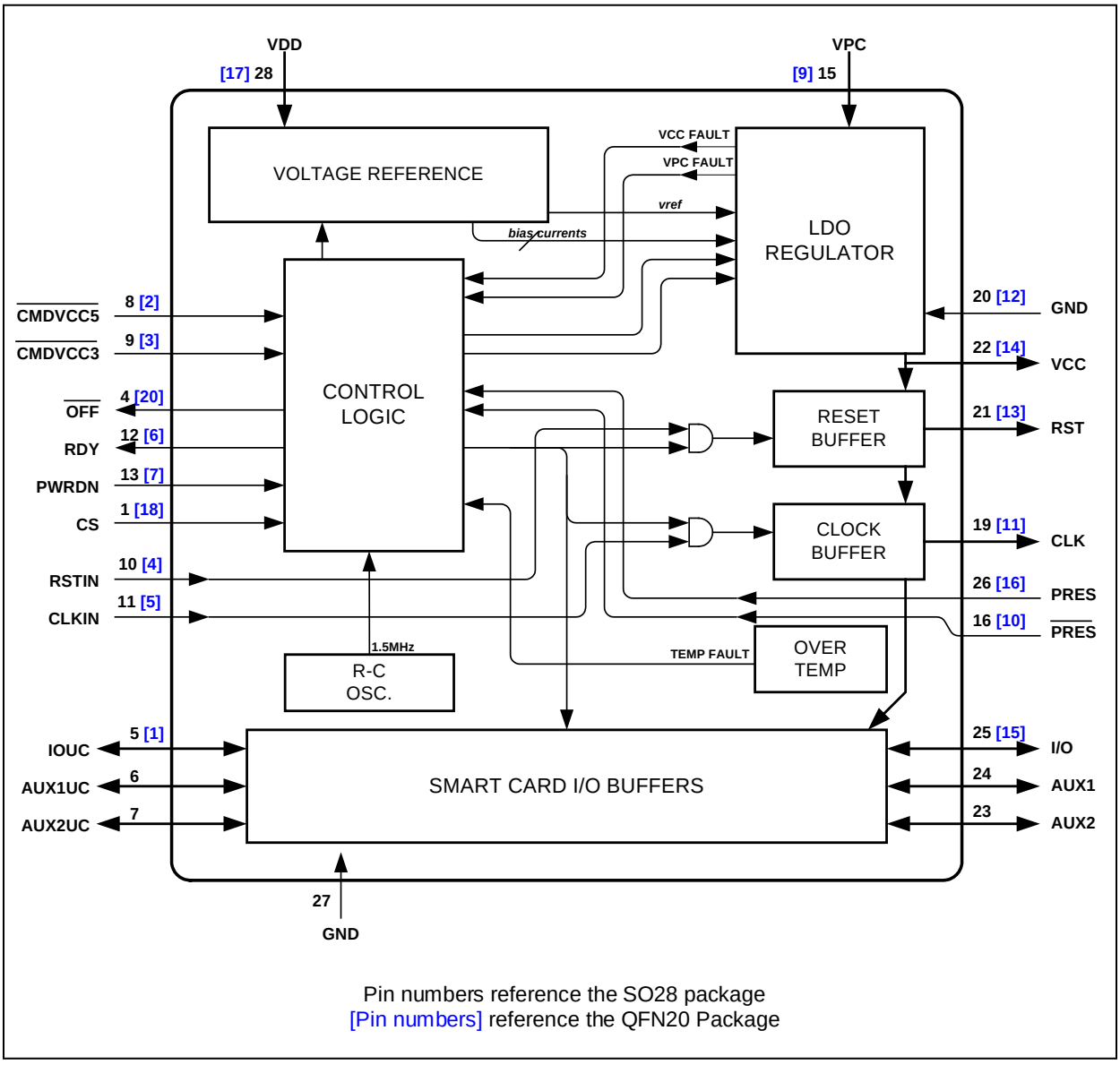

Figure 1: 73S8009R Block Diagram

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1 Pinout

The 73S8009R is supplied as a 20-pin QFN package and as a 28-pin SO package.

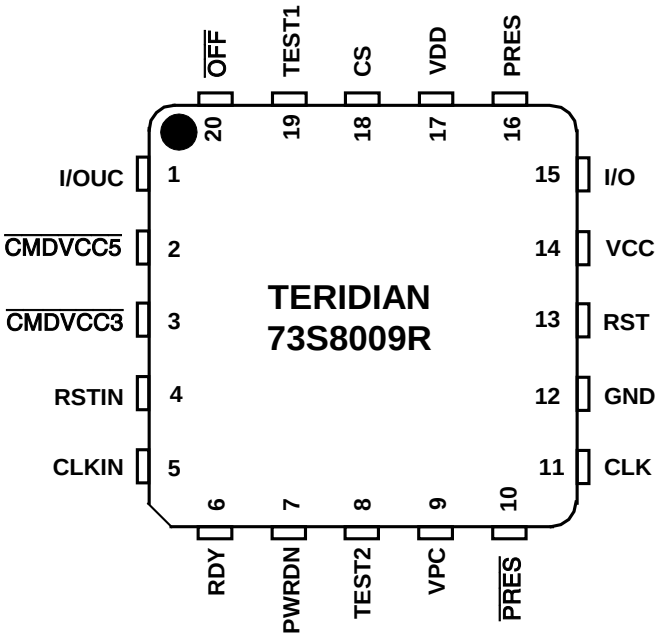

Figure 2: 73S8009R 20-Pin QFN Pinout

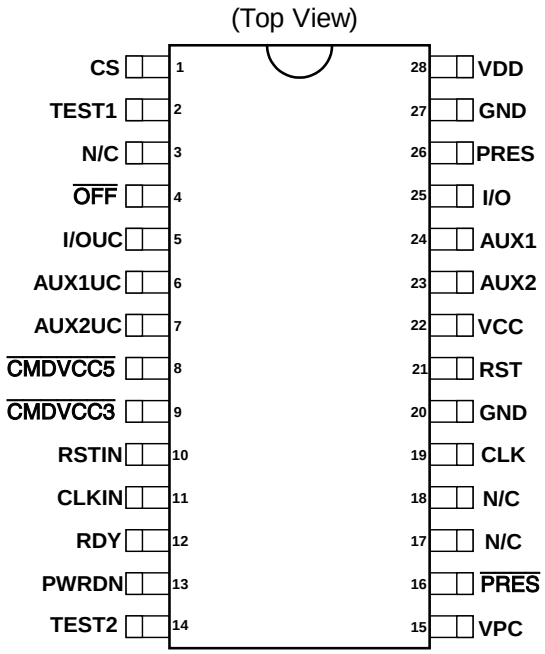

Figure 3: 73S8009R 28-Pin SO Pinout

Table 1 describes the pin functions for the device.

Table 1: 73S8009R Pin Definitions

Pin Name	Pin (SO28)	Pin (QFN20)	Type	Description
Card Interface				
I/O	25	15	IO	Card I/O: Data signal to/from card. Includes a pull-up resistor to V_{CC}.
AUX1	24	NA	IO	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to V_{CC}.
AUX2	23	NA	IO	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to V_{CC}.
RST	21	13	O	Card reset: provides reset signal to card.
CLK	19	11	O	Card clock: provides clock signal to card. The rate of this clock is determined by the external clock frequency provided on pin CLKIN.
PRES	26	16	I	Card Presence switch: active high indicates card is present. Should be tied to GND when not used, but includes a high-impedance pull-down current source.
$\overline{\text{PRES}}$	16	10	I	Card Presence switch: active low indicates card is present. Should be tied to VDD when not used, but includes a high-impedance pull-up current source.
VCC	22	14	PSO	Card power supply – logically controlled by the sequencer, output of LDO regulator. Requires an external filter capacitor to GND.
GND	20	NA	GND	Card ground.
Miscellaneous Inputs and Outputs				
CLKIN	11	5	I	Clock source for the card clock.
TEST1	2	19	–	This pin must be tied to GND in typical applications.
TEST2	14	8	–	This pin must be tied to GND in typical applications.
NC	3,17,18	NA	–	Non-connected pin.
Power Supply and Ground				
VDD	28	17		System interface supply voltage and supply voltage for internal circuitry.
VPC	15	9		LDO regulator power supply source.
GND	27	12	GND	Ground.
Microcontroller Interface				
CS	1	18	I	When CS = 1, the control and signal pins are configured normally. When CS is set low, $\overline{\text{CMDVCC5}}$, RSTIN, and $\overline{\text{CMDVCC3}}$ are latched, IOUC, AUX1UC, and AUX2UC are set to high-impedance pull-up mode and do not pass data to or from the smart card. Signals RDY and $\overline{\text{OFF}}$ are disabled to prevent a low output and the internal pull-up resistors are disconnected.
$\overline{\text{OFF}}$	4	20	O	Interrupt signal to the processor. Active low, multi-function indicating fault conditions and card presence. Open drain output configuration. It includes an internal 20 kΩ pull-up to VDD. The pull-up is disabled in PWRDN and CS=0 modes.

Pin Name	Pin (SO28)	Pin (QFN20)	Type	Description
I/OUC	5	1	I/O	System controller data I/O to/from the card. Includes a pull-up resistor to V_{DD}.
AUX1UC	6	NA	I/O	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to V_{DD}.
AUX2UC	7	NA	I/O	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to V_{DD}.
$\overline{CMDVCC5}$ $\overline{CMDVCC3}$	8 9	2 3	I I	Logic low on one or both of these pins will cause the LDO to ramp the Vcc supply to the smart card and smart card interface to the value described in the following table: $\overline{CMDVCC5}$ / $\overline{CMDVCC3}$ / V_{CC} Output Voltage 0 / 0 / 1.8 V 0 / 1 / 5.0 V 1 / 0 / 3.0 V 1 / 1 / LDO off Refer to for additional information on the $\overline{CMDVCC5}$ and $\overline{CMDVCC3}$ operation.
RSTIN	10	4	I	Reset Input. This signal is the reset command to the card.
RDY	12	6	O	Signal to controller indicating the 73S8009R is ready because V_{CC} is above the required value after $\overline{CMDVCC5}$ and/or $\overline{CMDVCC3}$ is asserted low. A 20 KΩ pull-up resistor to V_{DD} is provided internally. The pull-up is disabled in PWRDN and CS=0 modes.
PWRDN	13	7	I	PWRDN=1 puts the circuit into low-power mode with all analog functions disabled. The circuit will recover from the PWRDN state in the same manner as recovery from a POR event, taking approximately 1 ms. PWRDN assertion when either $\overline{CMDVCC5}$ or $\overline{CMDVCC3}$ is low has no effect and is ignored. There is no pull-up or pull-down provided on this pin.

2 Electrical Specifications

This section provides the following:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Smart Card Interface Requirements
- Digital Signals Characteristics
- DC Characteristics
- Voltage / Temperature Fault Detection Circuits

2.1 Absolute Maximum Ratings

Table 2 lists the maximum operating conditions for the 73S8009R. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability.

Table 2: Absolute Maximum Device Ratings

Parameter	Rating
Supply voltage V_{DD}	-0.5 to 4.0 VDC
Supply voltage V_{PC}	-0.5 to 6.5 VDC
Input voltage for digital inputs	-0.3 to (V_{DD} +0.5) VDC
Storage temperature	-60 °C to +150 °C
Pin voltage (except card interface)	-0.3 to (V_{DD} + 0.5) VDC
Pin voltage (card interface)	-0.3 to (V_{CC} + 0.5) VDC
ESD tolerance – Card interface pins	+/- 6 kV
ESD tolerance – Other pins	+/- 2 kV

Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground. Smart card pins are protected against shorts between any combination of smart card pins.

2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 3.

Table 3: Recommended Operating Conditions

Parameter	Rating
Supply voltage V_{DD}	2.7 to 3.6 VDC
Supply voltage V_{PC} for Class A-B-C Reader	4.75 to 6.0 VDC
Ambient operating temperature	-40 °C to +85 °C

2.3 Smart Card Interface Requirements

Table 4 lists the 73S8009R Smart Card interface requirements.

Table 4: DC Smart Card Interface Requirements

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Card Power Supply (V_{CC}) Regulator General Conditions: -40 °C < T < 85 °C, 4.75 V < V_{PC} < 6.0 V, 2.7 V < V_{DD} < 6.0 V						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1	–	0.1	V
		Inactive mode I_{CC} = 1 mA	-0.1	–	0.4	
		Active mode; I_{CC} < 65 mA; 5 V	4.65	–	5.25	
		Active mode; I_{CC} < 65mA; 5 V, NDS condition	4.75	–	5.25	
		Active mode; I_{CC} < 65 mA; 3 V	2.85	–	3.15	
		Active mode; I_{CC} < 40 mA; 1.8 V	1.68	–	1.92	
		Active mode; single pulse of 100 mA for 2 µs; 5 V, fixed load = 25 mA	4.6	–	5.25	
		Active mode; single pulse of 100 mA for 2 µs; 3 V, fixed load = 25 mA	2.7	–	3.15	
		Active mode; current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 5 V	4.6	–	5.25	
		Active mode; current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t <400 ns; 3 V	2.7	–	3.15	
		Active mode; current pulses of 20 nAs with peak $\|I_{CC}\|$ < 100 mA, t <400 ns; 1.8 V	1.62	–	1.92	
I_{CCrip}	V_{CC} Ripple	f_{RIPPLE} = 20 kHz – 200 MHz	–	–	350	mV
I_{CCmax}	Card supply output current	Static load current, V_{CC} > 1.65 V	–	–	40	mA
		Static load current, VCC > 4.6 V or 2.7 V as selected	–	–	90	
I_{CCF}	I_{CC} fault current	Class A, B (5 V and 3 V)	100	–	180	mA
		Class C (1.8 V)	60	–	130	
V_{SR}	Vcc slew rate, rise rate on activate	C_F = 1.0 µF	0.06	0.15	0.25	V/µs
V_{SF}	Vcc slew rate, fall rate on de-activate	C_F = 1.0 µF on V_{CC}	0.075	0.15	0.6	V/µs
V_{RDY}	V_{CC} ready voltage, V_{CC} rising (RDY = 1)	5 V operation	4.6	–	–	V
		3 V operation	2.75	–	–	
		1.8 V operation	1.65	–	–	
C_F	External filter capacitor (V_{CC} to GND) C_F should be ceramic with low ESR (< 100 mΩ)	ISO 7816-13 application		1.0		µF
		EMV 4.1 application		3.3		

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC, AUX1UC, AUX2UC.						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} = 0 µA	0.9 * V_{CC}	–	V_{CC}+0.1	V
		I_{OH} = -40 µA	0.75 * V_{CC}	–	V_{CC}+0.1	
V_{OH}	Output level, high (I/OUC, AUX1UC, AUX2UC)	I_{OH} = 0 µA	0.9 * V_{DD}	–	V_{DD}+0.1	V
		I_{OH} = -40 µA	0.75 * V_{DD}	–	V_{DD}+0.1	
V_{OL}	Output level, low (I/O, AUX1, AUX2)	I_{OL} = 1 mA	–	–	0.15 * V_{CC}	V
V_{OL}	Output level, low (I/OUC, AUX1UC, AUX2UC)	I_{OL} = 1 mA	–	–	0.3	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)	–	0.6 * V_{CC}	–	V_{CC}+0.30	V
V_{IH}	Input level, high (I/OUC, AUX1UC, AUX2UC)	–	1.8	–	V_{DD}+0.30	V
V_{IL}	Input level, low (I/O, AUX1, AUX2)	–	-0.15	–	0.2 * V_{CC}	V
V_{IL}	Input level, low (I/OUC, AUX1UC, AUX2UC)	–	-0.3	–	0.8	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0	–	–	0.1	V
		I_{OL} = 1 mA	–	–	0.3	
I_{LEAK}	Input leakage	V_{IH} = V_{CC}	–	–	10	µA
I_{IL}	Input current, low (I/O, AUX1, AUX2)	V_{IL} = 0	–	–	0.65	mA
I_{IL}	Input current, low (I/OUC, AUX1UC, AUX2UC)	V_{IL} = 0	–	–	0.7	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 Ω	–	–	15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 Ω	–	–	15	mA
t_R, t_F	Output rise time, fall time	For I/O, AUX1, AUX2, C_L = 80 pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, C_L=50 pF, 10% to 90%.	–	–	100	ns
t_{IR}, t_{IF}	Input rise, fall times		–	–	1	µs
R_{PU}	Internal pull-up resistor	Output stable for >200 ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate		–	–	1	MHz
T_{FDIO}	Delay, I/O to I/OUC, AUX1 to AUX1UC, AUX2 to AUX2UC, I/OUC to I/O, AUX1UC to AUX1, AUX2UC to AUX2 (respectively falling edge to falling edge and rising edge to rising edge)	Edge from master to slave measured at 50% point	60	100	200	ns
T_{RDIO}			–	25	90	
C_{IN}	Input capacitance		–	–	10	pF

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} = -200 µA	0.9 * V_{CC}	–	V_{CC}	V
V_{OL}	Output level, low	I_{OL} = 200 µA	0	–	0.15*V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0	–	–	0.1	V
		I_{OL} = 1 mA	–	–	0.3	V
I_{RST_LIM}	Output current limit, RST	–	–	–	30	mA
I_{CLK_LIM}	Output current limit, CLK	–	–	–	70	mA
CLK_{SR3V}	CLK slew rate	V_{CC} = 3 V	0.3	–	–	V/ns
CLK_{SR5V}	CLK slew rate	V_{CC} = 5 V	0.5	–	–	V/ns
t_R, t_F	Output rise time, fall time	C_L = 35 pF for CLK, 10% to 90%	–	–	8	ns
		C_L = 200 pF for RST, 10% to 90%	–	–	100	
δ	Duty cycle for CLK	C_L =35 pF, F_{CLK} ≤ 20 MHz	45	–	55	%

2.4 Digital Signals Characteristics

Table 5 lists the 73S8009R digital signals characteristics.

Table 5: Digital Signals Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Digital I/O except for OSC I/O						
V_{IL}	Input low voltage	–	-0.3	–	0.8	V
V_{IH}	Input high voltage	–	1.8	–	V_{DD}+0.3	V
V_{OL}	Output low voltage	I_{OL} = 2 mA	–	–	0.45	V
V_{OH}	Output high voltage	I_{OH} = -1 mA	V_{DD}-0.45	–	–	V
R_{OUT}	Pull-up resistor; $\overline{OFF}$, RDY	–	–	20	–	kΩ
$\|I_{IL1}\|$	Input leakage current	GND < V_{IN} < V_{DD}		–	5	µA

2.5 DC Characteristics

Table 6 lists the DC characteristics.

Table 6: DC Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
I_{DD}	Supply current	Normal operation	–	700	1500	µA
		Power down	–	–	5	
I_{PC}	Supply current	V_{CC} on, I_{CC} = 0 , I/O, AUX1, AUX2 = high, CLK not toggling	–	450	650	µA
		Power down	–	–	5	
I_{PCOFF}	V_{PC} supply current when V_{CC} = 0	$\overline{CMDVCC}$ is high	–	345	550	µA

2.6 Voltage / Temperature Fault Detection Circuits

Table 7 lists the voltage / temperature fault detection circuits.

Table 7: Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{PCF}	V_{PC} fault (V_{PC} Voltage Supervisor threshold)	$V_{PC} < V_{CC}$, a transient event	–	$V_{CC} > V_{PC}$ + 0.3	–	V
V_{CCF}	RDY = 0 (V_{CC} fault, V_{CC} Voltage Supervisor threshold)	V_{CC} = 5 V	–	–	4.6	V
		V_{CC} = 3 V	–	–	2.7	
		V_{CC} = 1.8 V	–	–	1.65	
T_F	Die over temperature fault	–	115	–	145	°C
I_{CCF}	Card over current fault	–	110	–	150	mA

3 Applications Information

This section provides general usage information for the design and implementation of the 73S8009R.

3.1 Example 73S8009R Schematics

Figure 4 shows a typical application schematic for the implementation of the 73S8009R. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information.

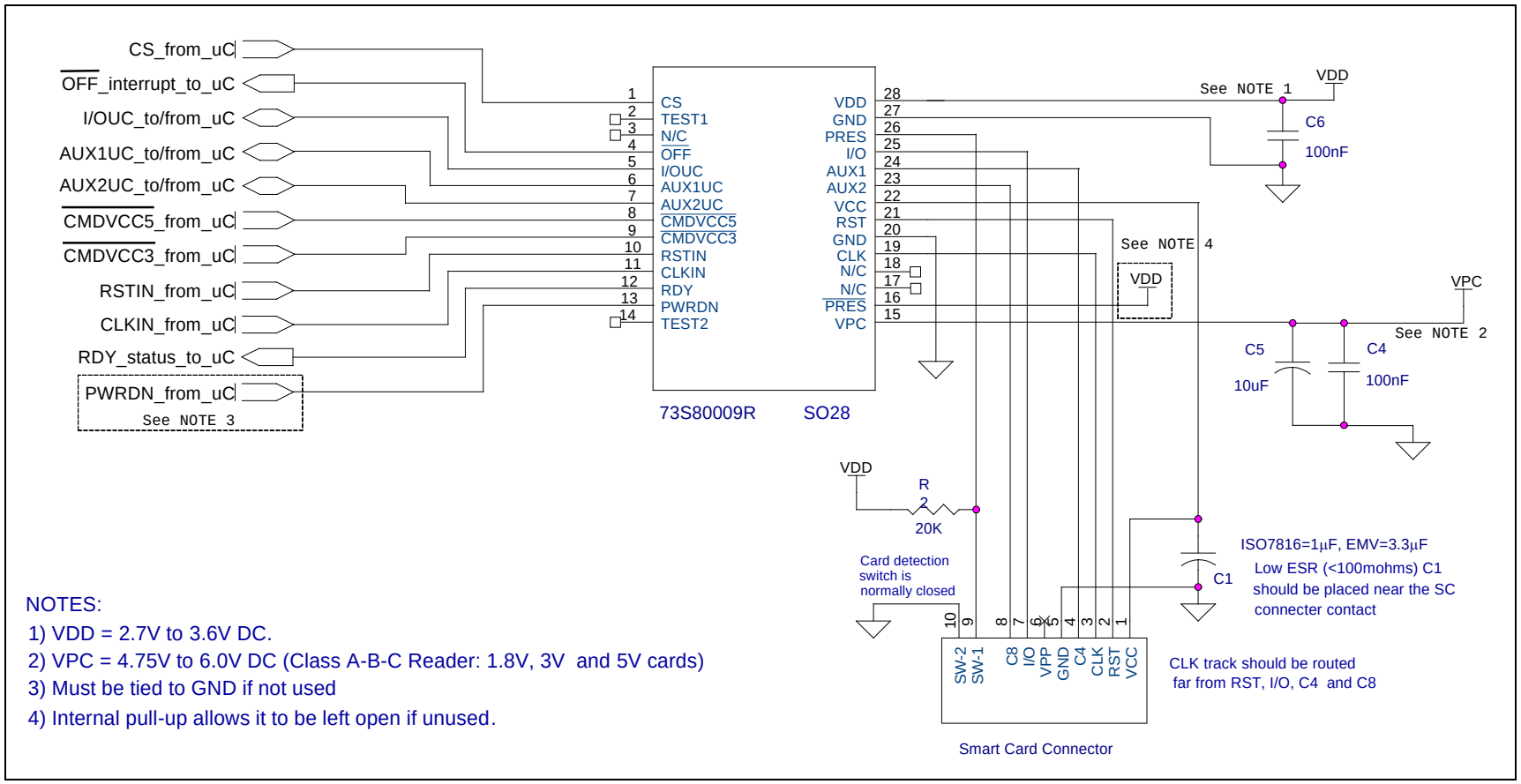

Figure 4: Typical 73S8009R Application Schematic

3.2 System Controller Interface

Four separate digital inputs allow direct control of the card interface from the host as follows:

- Pin CS: Enables the system controller interface.
- Pin $\overline{\text{CMDVCC3}}$ and/or $\overline{\text{CMDVCC5}}$: When low, starts an activation sequence.
- Pin RSTIN: Controls the card Reset signal (when enabled by the sequencer).

Other functions are controlled as follows:

- PWRDN places the 73S8009R in a low power mode and shuts down all functions.
- The card clock is completely controlled by CLKIN.
- Vcc output voltage valid is indicated on the RDY pin.
- Interrupt output to the host: As long as the card is not activated, the $\overline{\text{OFF}}$ pin informs the host about the card presence only (low = no card in the reader).

  When $\overline{\text{CMDVCC}}$ is set low (Card activation sequence requested from the host), a low level on $\overline{\text{OFF}}$ means a fault has been detected (e.g. card removal during card session, or voltage fault, or thermal / over-current fault). This condition automatically initiates a deactivation sequence.

3.3 Power Supply and Voltage Supervision

The Teridian 73S8009R smart card interface IC incorporates a LDO voltage regulator. The voltage output is controlled by the digital input sequence on $\overline{\text{CMDVCC3}}$ and $\overline{\text{CMDVCC5}}$. This regulator is able to provide either 1.8 V, 3 V or 5 V card voltages from the power supply applied on the VPC pin.

Digital circuitry is powered by the power supply applied on the VDD pin. V_{DD} also defines the voltage range to interface with the system controller.

Three voltage supervisors constantly check the presence of the voltages V_{DD}, V_{PC} and V_{CC}. A card deactivation sequence is forced upon a fault detected by any of these voltage supervisors.

The voltage regulator can provide a card current of 65 mA in compliance with EMV 4.1, and of at least 90 mA in compliance with ISO7816-3. The V_{CC} voltage supervisor threshold values are defined from the EMV standard.

3.4 Card Power Supply

The card power supply is internally provided by the LDO regulator. The signals $\overline{\text{CMDVCC3}}$ and $\overline{\text{CMDVCC5}}$ control the turn-on, output voltage value, and turn-off of V_{CC}. When either signal is asserted low, V_{CC} will ramp to the selected value or if both signals are asserted low (within 400 ns of each other), V_{CC} will ramp to 1.8 volts. These signals are edge triggered. If $\overline{\text{CMDVCC5}}$ is asserted low (to command V_{CC} to be 5 V) and at a much later time (greater than 2 µs, typically), $\overline{\text{CMDVCC3}}$ is asserted low, it will be ignored (and vice versa).

At the assertion (low) of either or both $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$ signals, V_{CC} will rise to the requested value. When V_{CC} rises to an acceptable value, and stays above that value for approximately 20 µs, RDY will be set high. Approximately 510 µs after the fall of $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$ the circuit will check the see if V_{CC} is at or above the required minimum value (indicated by RDY=1) and if not, will begin an emergency deactivation sequence. During the 510 µs time, over-temperature, card removal, or de-assertion of $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$ shall also initiate an emergency deactivation sequence.

Choice of the V_{CC} capacitor:

Depending on the application, the requirements in terms of both the V_{CC} minimum voltage and the transient currents that the interface must be able to provide to the card are different. An external capacitor must be connected between the VCC pin and the card ground in order to guarantee stability of the LDO regulator, and to handle the transient requirements. The type and value of this capacitor can be optimized to meet the desired specification. Table 8 shows the recommended capacitors for each V_{PC} power supply configuration and applicable specification.

Table 8: Choice of VCC Pin Capacitor

Specification Requirements			System Requirements		
Specification	**Min V_{CC} Voltage allowed during transient current**	**Max Transient Current Charge**	**Min V_{PC} Power Supply required**	**Capacitor Type**	**Capacitor Value**
EMV 4.1	4.6 V	30 nA·s	4.75 V	X5R/X7R with ESR<100 mΩ	3.3 µF
ISO-7816-3 & GSM11.11	4.5 V	20 nA·s	4.75 V		1 µF

3.5 Over-temperature Monitor

A built-in detector monitors die temperature. When an over-temperature condition occurs, a card deactivation sequence is initiated, and an error or fault condition is reported to the system controller via the $\overline{OFF}$ interrupt.

3.6 Activation and Deactivation Sequence

The host controller is fully responsible for the activation sequencing of the smart card signals CLK, RST, I/O, AUX1 and AUX2. All of these signals are held low when the card is in the deactivated state. Upon card activation (the fall of $\overline{CMDVCC3}$/$\overline{CMDVCC5}$, all the signals will remain low until RDY goes high. The host should set the signals RSTIN, I/OUC, CLKIN, AUX1UC and AUX2UC low prior to activating the card and allow RDY to go high before transitioning any of these signals. In order to initiate activation, the card must be present and there can be no over-temperature fault and no V_{DD} fault.

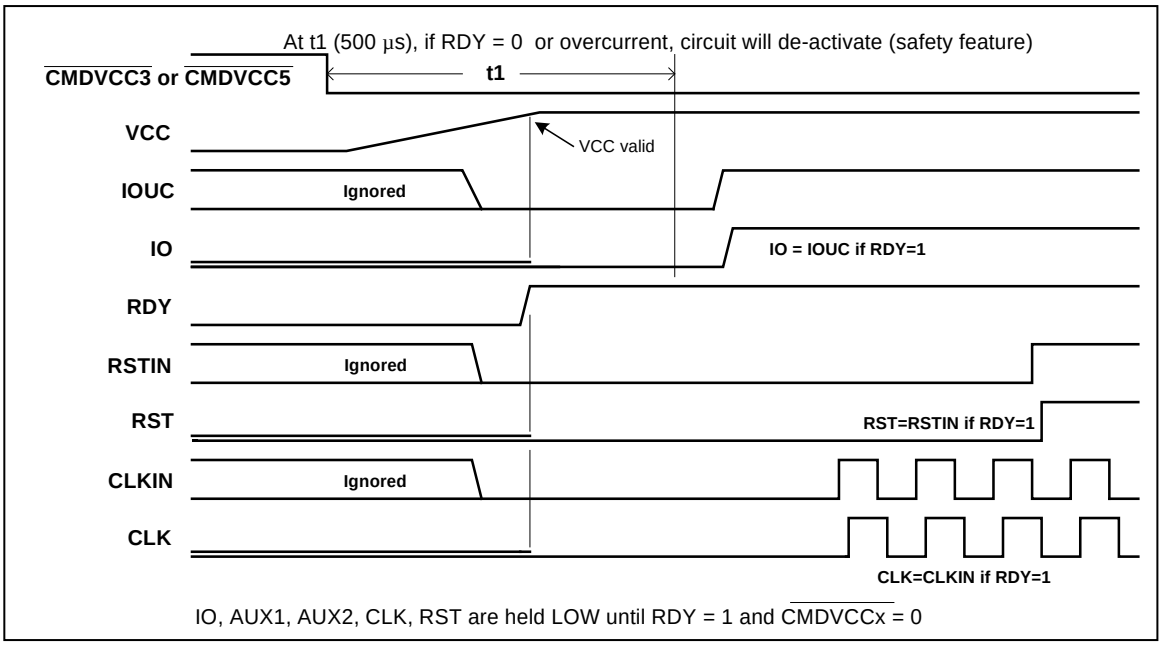

Figure 5: Activation Sequence

Deactivation is initiated either by the system controller setting $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$ high, or automatically in the event of hardware faults. Hardware faults are over-current, over-temperature and card extraction during the session. The host can manage the I/O signals, CLKIN, RSTIN, and $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$ to create other de-activation sequences for non-emergency situations.

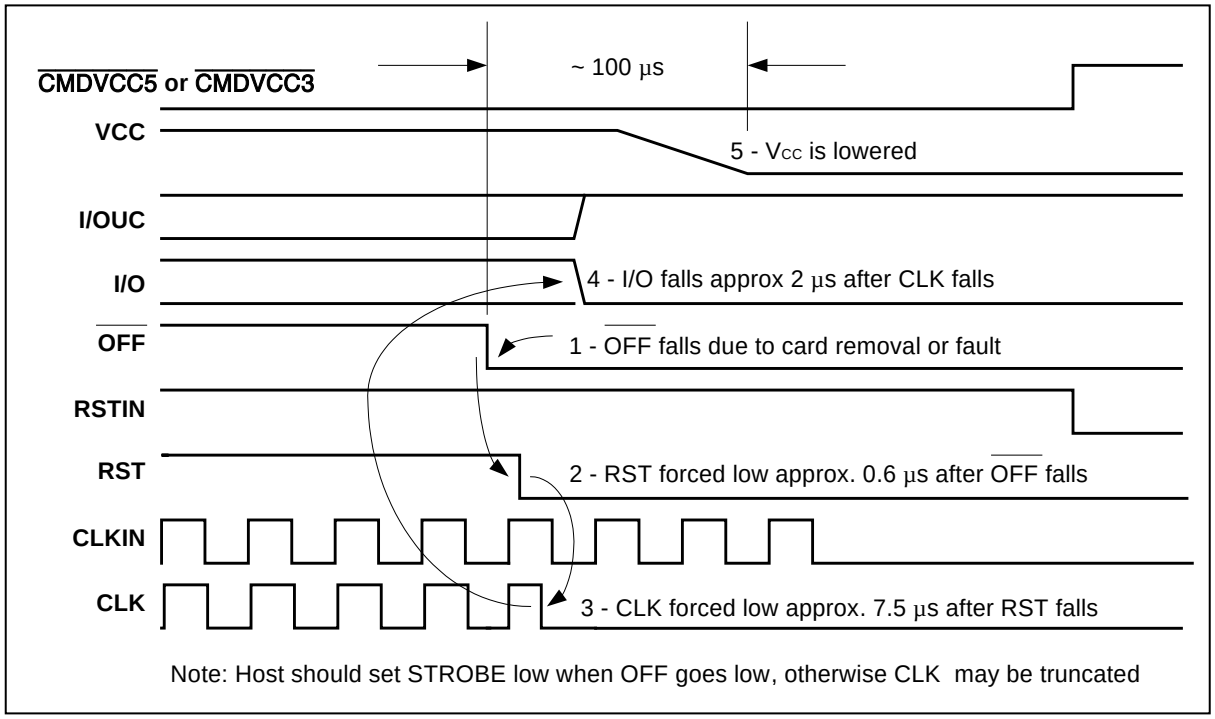

Figure 6: Deactivation Sequence

3.7 $\overline{\text{OFF}}$ and Fault Detection

The system controller can monitor the $\overline{\text{OFF}}$ signal to:

- Query regarding the card presence outside of a card session
- Detect faults during card sessions.

Outside a Card Session

In this condition, $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$) is always high, $\overline{\text{OFF}}$ is low if the card is not present and high if the card is present. Because it is outside a card session, any fault detection will not act upon the $\overline{\text{OFF}}$ signal. No deactivation is required during this time.

During a Card Session

In this condition, $\overline{\text{CMDVCC3}}$/$\overline{\text{CMDVCC5}}$ is always low and $\overline{\text{OFF}}$ falls low if the card is extracted or if any fault is detected. At the same time that $\overline{\text{OFF}}$ is set low, the sequencer automatically starts the deactivation process and the host should stop all transition on the signal lines.

Figure 7 shows the timing diagram for the signals $\overline{\text{CMDVCC3}}$, $\overline{\text{CMDVCC5}}$, PRES and $\overline{\text{OFF}}$ during a card session and outside the card session.

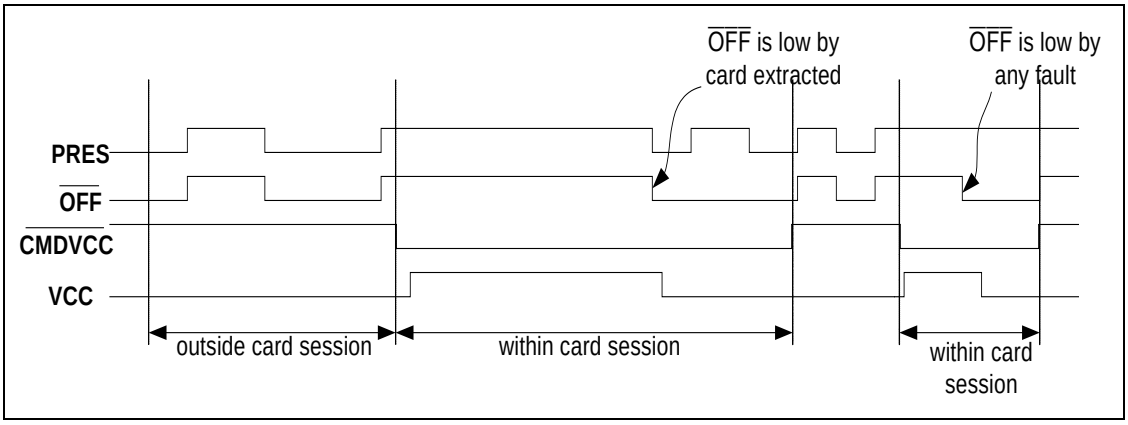

Figure 7: OFF Activity Outside and Inside a Card Session

3.8 Power-down Operation

A power-down function is provided that disables all analog functions. The power-down state is only allowed in the de-activated condition. The host invokes the power-down state when it is desirable to save power.

The signals PRES and PRES are functional in the power-down state so that a card insertion asserts OFF high. If there is no card present (OFF = low) in power-down mode, the pull-up resistor is disabled so that no current is drawn from VDD. If a card is inserted, the pull-up resistor is enabled and OFF goes high.

Upon receiving the OFF indication, the host must then de-assert power down (PWRDN) and wait until the circuit is ready. When PWRDN is de-asserted, OFF goes low to indicate that the circuit is not ready (it is going through the power-on recovery time). When the circuit is ready, OFF will go high if the card is present. Figure 8 illustrates the behavior of the circuit for PWRDN events.

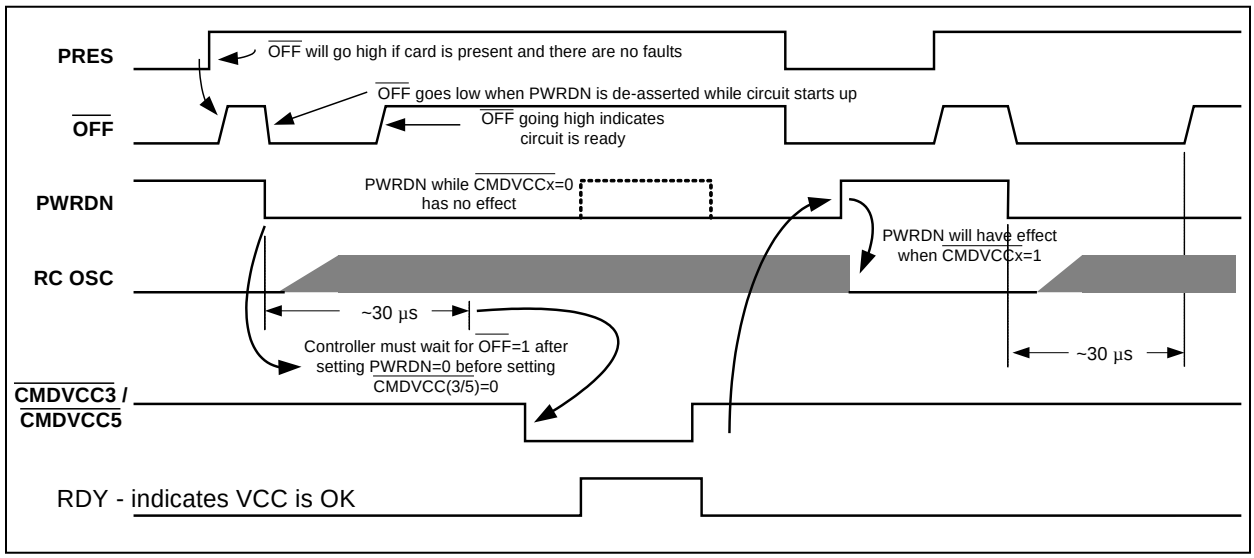

Figure 8: Power-down Operation

3.9 Chip Select

The CS pin is provided to allow multiple circuits to operate in parallel, driven from the same host control bus. When CS is high, the pins RSTIN, $\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC3}}$ and CLKIN control the chip as described. The pins IOUC, AUX1UC, and AUX2UC operate to transfer data to the smart card via IO, AUX1, and AUX2 when the smart card is activated. IO, AUX1, and AUX2 have 11 KΩ pull-up resistors while $\overline{\text{OFF}}$ and RDY have 20 KΩ pull-up resistors.

When CS goes low, the states of the pins RSTIN, $\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC3}}$, and CLKIN are latched and held internally. The pull-up for pins IOUC, AUX1UC, and AUX2UC become a very weak pull-up of approximately 3 microamperes. No transfer of data is possible between IOUC, AUX1UC, AUX2UC and the smart-card signals IO, AUX1, and AUX2. The signals $\overline{\text{OFF}}$ and RDY are set to high impedance and the internal 20 KΩ pull-up resistors are disconnected. PWRDN is not latched when CS is low.

The operation of the fault sensing circuits and card sense inputs (in regards to de-activation) are not affected by CS.

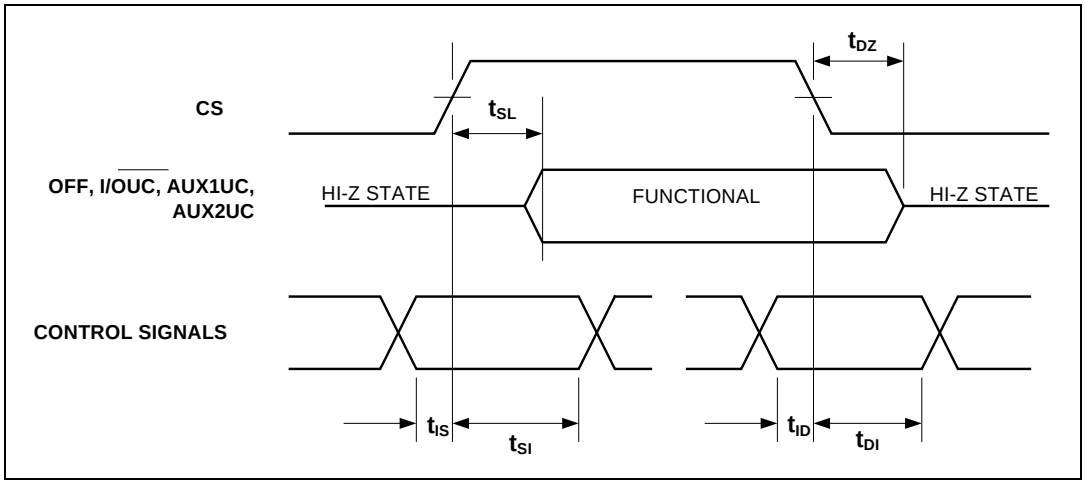

Figure 9: CS Timing Definitions

3.10 I/O Circuitry and Timing

The states of the I/O, AUX1, and AUX2 pins are low after power-on-reset and they are high when the activation sequencer enables the I/O reception state. See Section 3.6 Activation and Deactivation Sequence for more details on when the I/O reception is enabled. The states of the I/OUC, AUX1UC, and AUX2UC are high after power on reset.

Within a card session and when the I/O reception state is turned on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected, both I/O lines return to their neutral state.

Figure 10 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output. The delay between the I/O signals is shown in Figure 11.

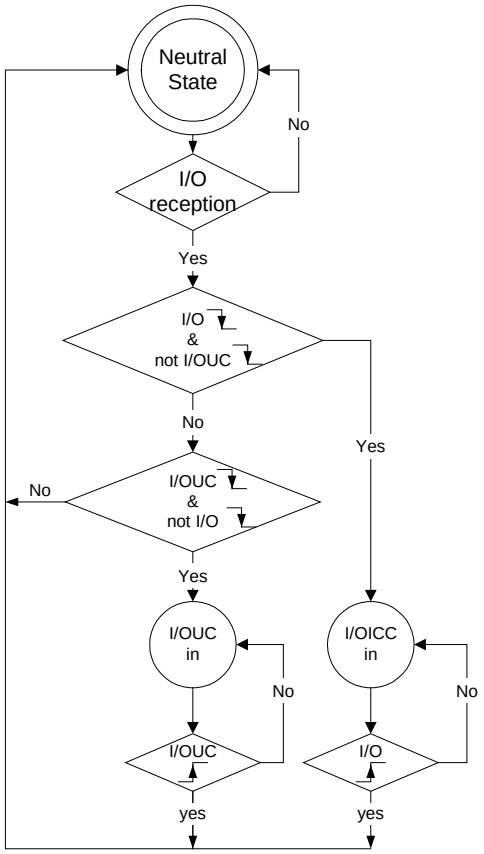

Figure 10: I/O and I/OUC State Diagram

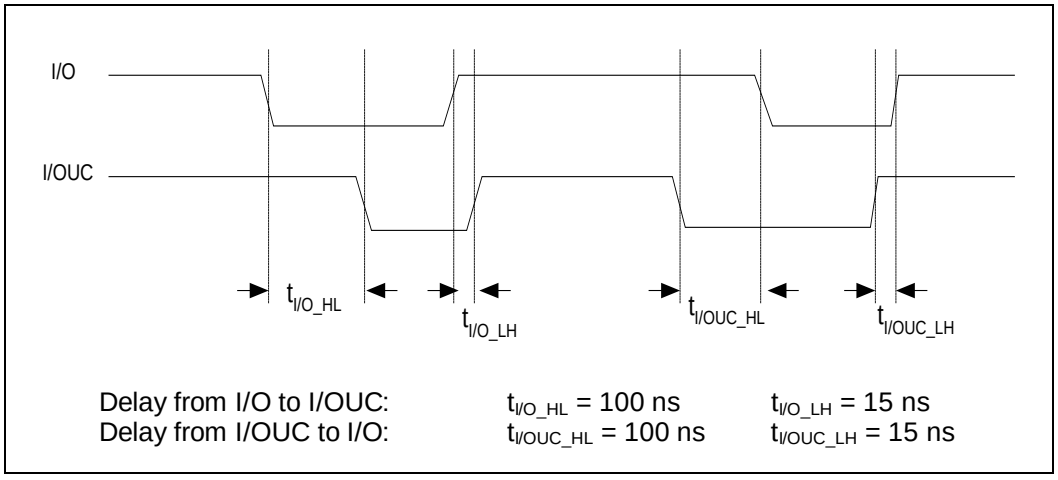

Figure 11: I/O to I/OUC Delay Timing Diagram

4 Mechanical Drawings

4.1 20-pin QFN

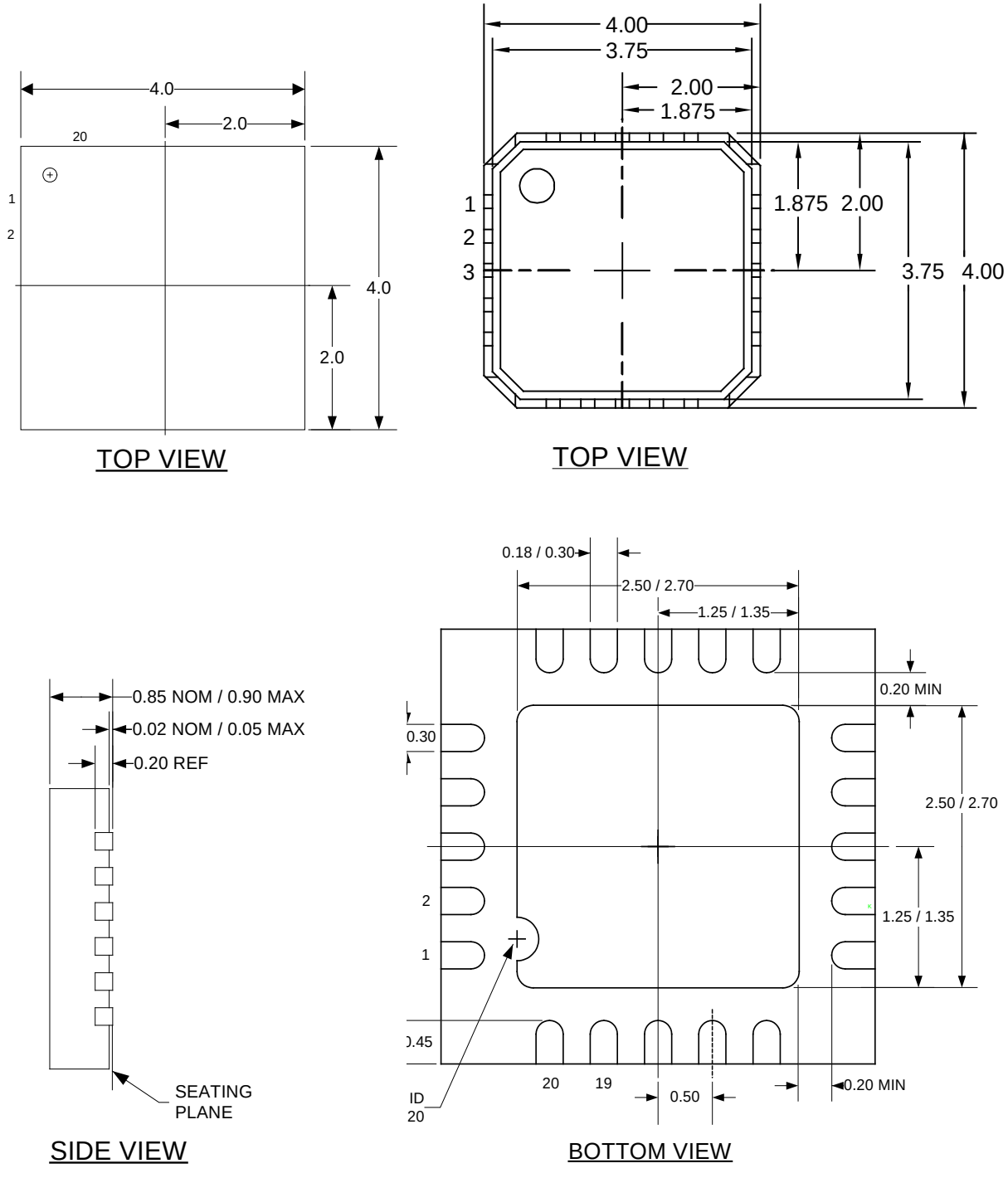

Figure 12: 20-pin QFN Package Dimensions

4.2 28-Pin SO

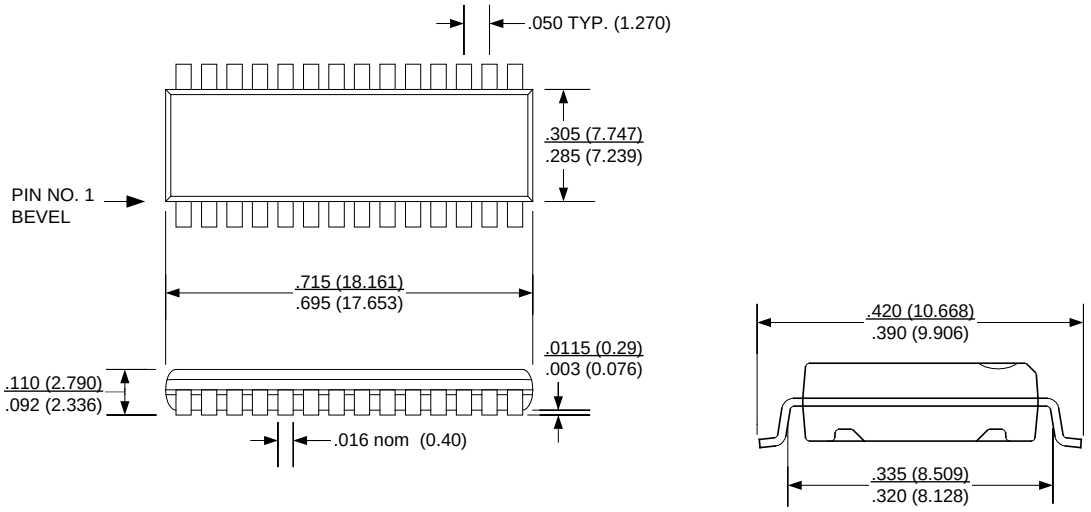

Figure 13: 28-Pin SO Package Dimensions

5 Ordering Information

Table 9 lists the order numbers and packaging marks used to identify 73S8009R products.

Table 9: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S8009R–SOL, 28-pin Lead-Free SO	73S8009R -IL/F	73S8009R -IL
73S8009R–SOL, 28-pin Lead-Free SO Tape / Reel	73S8009R -ILR/F	73S8009R -IL
73S8009R–QFN, 20-pin Lead-Free QFN	73S8009R -IM/F	8009R
73S8009R–QFN, 20-pin Lead-Free QFN Tape / Reel	73S8009R -IMR/F	8009R

6 Related Documentation

The following 73S8009R documents are available from Teridian Semiconductor Corporation:

73S8009R 20QFN Demo Board User Guide
73S8009R 28SO Demo Board User Guide
Migrating from the 73S8024RN to the 73S8009R

7 Contact Information

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For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	8/30/2005	First publication.
1.2	12/11/2007	Updated 28SO package dimensions. Removed leaded options.
1.3	10/22/2009	Formatted to the new Teridian style. Miscellaneous editorial changes.

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