## FEATURES

- 1 GHz Specified Performance
- 22 dB Gain
- Very Low Distortion
- Excellent $75 \Omega$ Input and Output Match
- Stable with High VSWR Load Conditions
- Monolithic Design for Consistent Performance Part-to-Part
- Low DC Power Consumption
- Surface Mount Package Compatible with Automatic Assembly
- Low Cost Alternative to Hybrids
- Meets Cenelec Standards
- Materials set consistent with RoHS Directives.


## APPLICATIONS

- CATV Line Amplifiers, System Amplifiers, Distribution Nodes


## PRODUCT DESCRIPTION

The ACA2402 is a highly linear, monolithic GaAs RF amplifier that has been developed as an alternative to standard CATV hybrid amplifiers. Offered in a convenient surface mount package, the MMIC consists of two pairs of parallel amplifiers that are optimized for exceptionally low distortion and noise figure. A

hybrid equivalent that provides flat gain response and excellent input and output return loss over the 40 to 1000 MHz CATV downstream band is formed when one ACA2402 is cascaded between two appropriate transmission line baluns.


Figure 1: Hybrid Application Diagram


Figure 2: Pin Out

Table 1: Pin Description

| PIN | NAME | DESCRIPTION | PIN | NAME | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | GND | Ground | 16 | GND | Ground |
| 2 | 2 AIN | Amplifier 2A Input | 15 | 1Aout | Amplifier 1A Output |
| 3 | GND | Ground | 14 | Bias 1A | Bias for 1A Amplifier |
| 4 | 1AIN | Amplifier 1A Input | 13 | 2Aout | Amplifier 2A Output and Supply |
| 5 | 1BIN | Amplifier 1B Input | 12 | 2Bout | Amplifier 2B Output and Supply |
| 6 | 1SET | Current Adjust | 11 | Bias 1B | Bias for 1B Amplifier |
| 7 | 2 BIN | Amplifier 2B Input | 10 | 1Bout | Amplifier 1B Output |
| 8 | GND | Ground | 9 | GND | Ground |

Table 2: Absolute Mimimum and Maximum Ratings

| PARAMETER | MIN | MAX | UNIT |
| :--- | :---: | :---: | :---: |
| Supply (pins 12, 13) | 0 | +28 | VDC |
| RF Power at Inputs (pins 4, 5) | - | +75 | dBmV |
| Storage Temperature | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |
| Soldering Temperature | - | +260 | ${ }^{\circ} \mathrm{C}$ |
| Soldering Time | - | 5.0 | Sec |

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.
Notes:

1. Pins $2,4,5$ and 7 should be $A C$-coupled. No external DC bias should be applied.
2. Pin 6 should be AC-grounded and/or pulled to ground through a resistor for current control. No external DC bias should be applied.
3. Pins 11 and 14 are bias feeds for input amplifiers 1A and 1B. No external DC bias should be applied.
4. Pins 10 and 15 receive DC bias directly from pins 11 and 14. No other external bias should be applied.

Table 3: Operating Ranges

| PARAMETER | MIN | TYP | MAX | UNIT |
| :--- | :---: | :---: | :---: | :---: |
| Supply: Vdd (pins 12, 13) | - | +24 | - | VDC |
| RF Frequency | 40 | - | 1000 | MHz |
| Case Temperature | -40 | - | +110 | ${ }^{\circ} \mathrm{C}$ |

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: AC and DC Electrical Specifications
( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{VDD}=+24 \mathrm{VDC}$ )

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gain @ $1000 \mathrm{MHz}{ }^{(1)}$ | 21.1 | 21.6 | 22.1 | dB |  |
| Cable Equivalent Slope ${ }^{(1)}$ | - | 0 | - | dB |  |
| Gain Flatness ${ }^{(1)}$ @ 1000 MHz | - | $\pm 0.2$ | - | dB |  |
| Noise Figure ${ }^{(1)}$ | - | 3.5 | 4.5 | dB |  |
| CTB ${ }^{(1)}$ <br> 77 Channels ${ }^{(2)}$ <br> 77 Channels plus QAM to $1 \mathrm{GHz}^{(6)}$ <br> 110 Channels ${ }^{(3)}$ <br> 110 Channels plus QAM to $1 \mathrm{GHz}{ }^{(7)}$ <br> 128 Channels ${ }^{(4)}$ | - | $\begin{gathered} -76 \\ - \\ -73 \\ - \\ -70 \end{gathered}$ | $\begin{aligned} & -74 \\ & -74 \\ & -71 \\ & -71 \end{aligned}$ | dBc |  |
| $\begin{aligned} & \text { CSO }{ }^{(1)} \\ & 77 \text { Channels }^{(2)} \\ & 77 \text { Channels plus QAM to } 1 \mathrm{GHz}{ }^{(6)} \\ & 110 \text { Channels } \\ & 110 \text { Channels plus QAM to } 1 \mathrm{GHz}^{(7)} \\ & 128 \text { Channels }{ }^{(4)} \end{aligned}$ |  | $\begin{gathered} -72 \\ - \\ -72 \\ - \\ -69 \end{gathered}$ | $\begin{aligned} & -70 \\ & -70 \\ & -70 \\ & -68 \end{aligned}$ | dBc |  |
| XMOD ${ }^{(1)}$ <br> 77 Channels ${ }^{\text {(2) }}$ <br> 77 Channels plus QAM to $1 \mathrm{GHz}^{(6)}$ <br> 110 Channels ${ }^{(3)}$ <br> 110 Channels plus QAM to $1 \mathrm{GHz}^{(7)}$ <br> 128 Channels ${ }^{(4)}$ |  | $\begin{gathered} -65 \\ - \\ -65 \\ - \\ -62 \end{gathered}$ | $\begin{aligned} & -63 \\ & -63 \\ & -63 \\ & -63 \end{aligned}$ | dBc |  |
| Return Loss (Input/Output) ${ }^{(1)}$ | 18 | 22 | - | dB | $75 \Omega$ system |
| Supply Current ${ }^{(5)}$ | 240 | 250 | 260 | mA |  |
| Thermal Resistance | - | - | 3.8 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |

## Notes:

(1) Measured with baluns on the input and output of the device.
(2) Parts measured with 77 channels flat output, +42 dBmV per channel.
(3) Parts measured with 110 channels flat output, +40 dBmV per channel.
(4) Parts measured with 128 channels flat output, +40 dBmV per channel.
(5) The supply current may be reduced by decreasing the value of R3 (see Figure 17)
(6) 47.5 dBmV output, 9.5 dB tilt @ 1 GHz
(7) 45.5 dBmV output, 9.5 dB tilt @ 1 GHz
8. All specifications as measured on Evaluation Board (see Figures 16 \& 17).

## PERFORMANCE DATA

Figure 3: Noise Figure vs Frequency


Figure 4: Gain (S21) vs. Frequency


Figure 5: Input and Output Return Loss (S11 and S22) vs. Frequency


Figure 6: Isolation (S12) vs. Frequency


Figure 7: CTB vs. Output Power at Worst-case Channel/Frequency (128 total channels, 110 analog channels, flat output)


Figure 8: CSO vs. Output Power at Worst-case Channel/Frequency (128 total channels, 110 analog channels, flat output)


Figure 9: XMOD vs. Output Power at Worst-case Channel/Frequency (128 total channels, 110 analog channels, flat output)


Figure 10: CTB vs. Frequency (110 channels, $\mathbf{+ 4 0} \mathbf{d B m V}$ power, flat output)


Figure 11: CSO vs. Frequency (110 channels, $\mathbf{+ 4 0} \mathbf{~ d B m V}$ power, flat output)


Figure 12: XMOD vs. Frequency (110 channels, $\mathbf{+ 4 0} \mathbf{~ d B m V}$ power, flat output)




Figure 14: CSO vs. Frequency ( 77 channels, $\mathbf{+ 4 2} \mathbf{~ d B m V}$ power, flat output)


Figure 15: XMOD vs. Frequency ( 77 channels, $\mathbf{+ 4 2 \mathrm { dBmV } \text { power, flat output) } { } ^ { \text { d } } \text { ( }}$


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## APPLICATION INFORMATION



Figure 16: Evaluation Board Layout
Notes:

1. Via holes should be 35 mils $(0.89 \mathrm{~mm})$ in diameter, and plated to 1 mil ( 0.025 mm ) thickness. They need not be solderfilled.
2. WARNING: Due to the power dissipation of this device, the printed circuit board should be mounted/attached to a heat sink.
3. More assembly details, such as via hole diameters, via spacing, solder paste application, and soldering recommendations are provided in the application note entitled, "Thermal Management of ANADIGICS' Surface Mounted Amplifiers".


Figure 17: Evaluation Board Schematic

Table 5: Evaluation Board Parts List

| REF | DESCRIPTION | QTY | VENDOR | VENDOR P/N |
| :--- | :--- | :---: | :--- | :--- |
| C1, C2, C3, C6, <br> C7, C10, C14 | $0.01 \mu$ F CHIP CAP | 7 | MURATA | GRM39X7R103K50V |
| C4, C5, C8, C9 | 470 pF CHIP CAP | 4 | MURATA | GRM39X7R471K50V |
| C12, C13 | 1.0 pF CHIP CAP | 2 | MURATA | GRM36COG1R0C50 |
| C15 | $47 \mu$ F ELECT. CAP | 1 | DIGI-KEY CORP | P5275-ND |
| R1, R2, C11 | NOT USED |  |  |  |
| R3 | 18 k R RESISTOR | 1 | DIGI-KEY CORP | P18KGCT-ND |
| TVS | TVS 24 VOLT 600 <br> WATT | 1 | DIGI-KEY CORP | SMBJ24ACCCT-ND |
| L1, L2, L3, L4 ${ }^{(3)}$ | 680 nH INDUCTOR | 4 | COILCRAFT | $1008 C S-681$ XKBC |
| CONNECTOR ${ }^{(1)}$ | $75 \Omega$ N MALE PANEL <br> MOUNT | 2 | PASTERNACK <br> ENTERPRISES | PE4504 |
| T1, T2 ${ }^{(2)}$ |  |  |  |  |
| (BALUN) | Ferrite Core | 2 | FAIR-RITE | 2843002702 |
|  | Wire | Printed Circuit Board | 1 | STANDARD <br> PRINTED CIRC. INC |
| MWS WIRE IND. | T-2361429-20 |  |  |  |
| INDIUM | $300 \times 160$ MILS | 1 | INDIUM CORP OF <br> AMERICA | $14996 Y$ |

Notes:
(1) $N$ connector center pin should be approximately 80 mils in length.
(2) $T 1, T 2$ balun: 5.5 turns thru, as shown in Figure 18.
(3) 200 mA minimum current rating.


Figure 18: Balun Drawing


Figure 19: S7 Package Outline - 16 Pin Wide Body SOIC with Heat Slug

ORDERING INFORMATION

| ORDER NUMBER | TEMPERATURE <br> RANGE | PACKAGE <br> DESCRIPTION | COMPONENT PACKAGING |
| :---: | :---: | :---: | :---: |
| ACA2402S7TR | -40 to $110^{\circ} \mathrm{C}$ | 16 Pin Wide Body <br> SOIC with Heat Slug | 1,500 piece tape and reel |
| ACA2402RS7P2 | -40 to $110^{\circ} \mathrm{C}$ | RoHS-Compliant <br> 16 Pin Wide Body <br> SOIC with Heat Slug | 1,500 piece tape and reel |
| ACA2402S7P0 | -40 to $110^{\circ} \mathrm{C}$ | 16 Pin Wide Body <br> SOIC with Heat Slug | Plastic tubes (50 pieces per tube) |
| ACA2402RS7P0 | -40 to $110^{\circ} \mathrm{C}$ | RoHS-Compliant <br> 16 Pin Wide Body <br> SOIC with Heat Slug | Plastic tubes (50 pieces per tube) |

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