PWR-NCH401

T-39-90

4-Channel MOSFET Array
400 V – 335 mA (per channel)

POWER INTEGRATIONS, INC.

Product Highlights

4 open-drain N-channel MOSFETs per package
- 200, 300, and 400 V versions
- 335 mA per ouput @ $T_A = 25°C$

Direct logic to high-voltage interface
- Interfaces directly with TTL or 5 V CMOS logic
- No intermediate gate-drive power supply needed

Measures Current without external voltage drops
- Each MOSFET includes a proportional current sense output
- Can be used to tell if current is flowing
- Can be used to tell if too much current is flowing

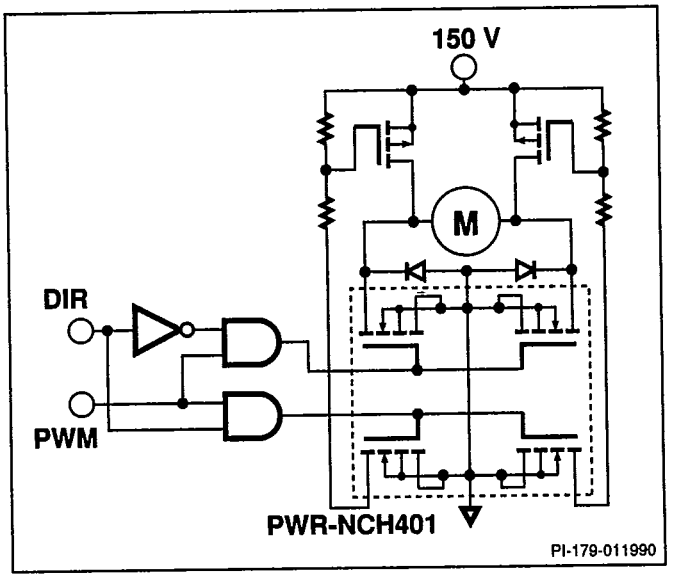

Figure 1. Typical Application

Description

The PWR-NCH401 high-voltage array is designed to provide a cost-effective interface with TTL or 5 V CMOS logic and high-voltage loads such as relays, solenoids, tungsten lamps, printer hammers, and small motors. Each circuit consists of 4 N-channel, enhancement mode MOSFET transistors in a common source configuration with independent open drains. Each MOSFET transistor is rated at up to 400 V, and with its low R_{DS} (ON) of 10 Ω, can handle 335 mA at an ambient temperature of 25°C (675 mA total package capability). The 400 V blocking rating makes the MOSFET transistors usable on 110 VAC mains.

Each of the MOSFETs come provided with an added current sense capability. The SENSE output allows the transistor current to be measured without introducing a sense resistor in series with the load, which causes an additional voltage drop and power dissipaiton within the circuit. The SENSE output varies proportionally with output current in the ratio of about 750:1. The SENSE current can be used to control load current or to flag a microcontroller to either the presence or absence of load current.

The PWR-NCH401 is available in a 300 mil (narrow body) 24-pin plastic DIP package.

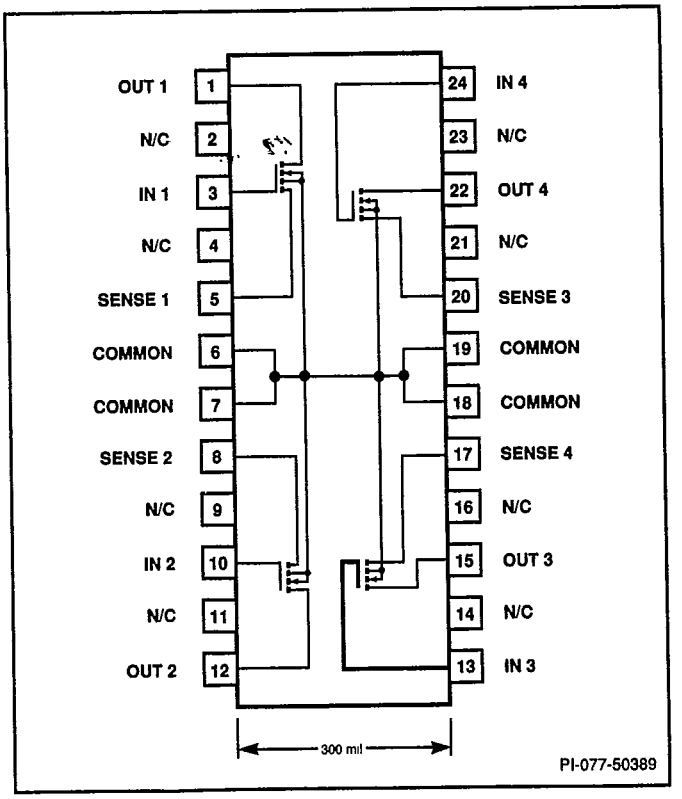

Figure 2. Pin Configuration and Schematic Diagram

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Application Guidelines

The use of the Power Integrations PWR-NCH401 MOSFET array is analogous to the use of any N-channel, enhancement mode MOSFET. Like all semiconductors, the performance of the device is sensitive to junction temperature. Therefore, ratings for power dissipation and maximum current should be calculated based on the ambient temperature of the particular application.

The PWR-NCH401 threshold voltage has been designed to meet TTL and 5 V CMOS logic levels, unlike most discrete MOSFETs which require a gate voltage of 10 V for full enhancement.

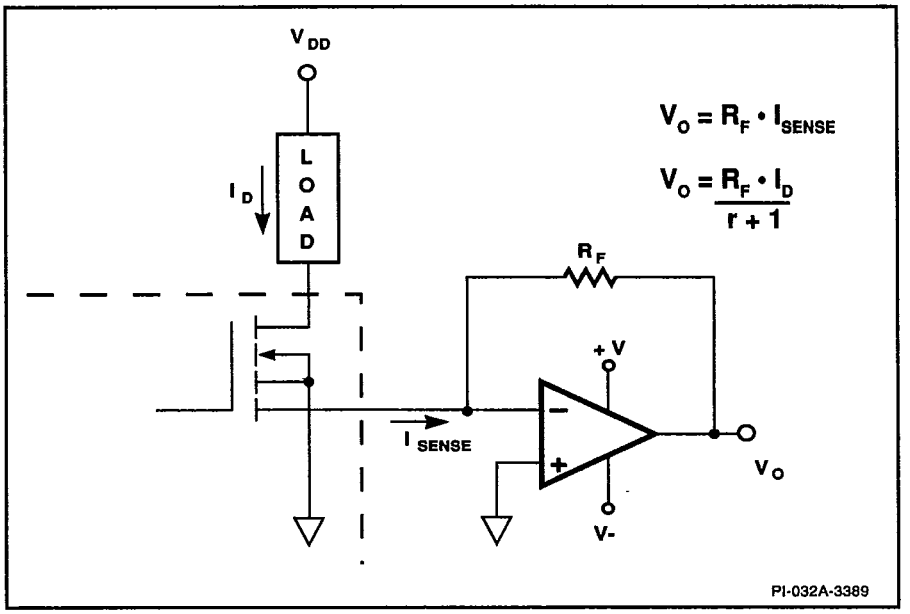

Figure 3. Virtual ground current sensing circuit

Current Sense

The proportional current sensing capability of the MOSFETs gives this device extreme versatility. The current from the SENSE output is approximately 1/750 of the output current. The circuit that yields the best performance in terms of accuracy and noise immunity is shown in Figure 3. The three major disadvantages of this circuit are:

1. Dual supplies are required.
2. The output voltage is inverted.
3. Output response is limited by the slew rate of the op amp.

The resistor sensing circuit shown in Figure 4 eliminates the first two disadvantages at the expense of reduced accuracy.

The op amp amplifies the voltage developed across R_S. The op amp should be selected from those designed to operate with a single supply, e.g. LM324, LM358, etc.

The selection of R_S is not a trivial matter. In order not to degrade the current sense ratio (r) at high currents, voltage

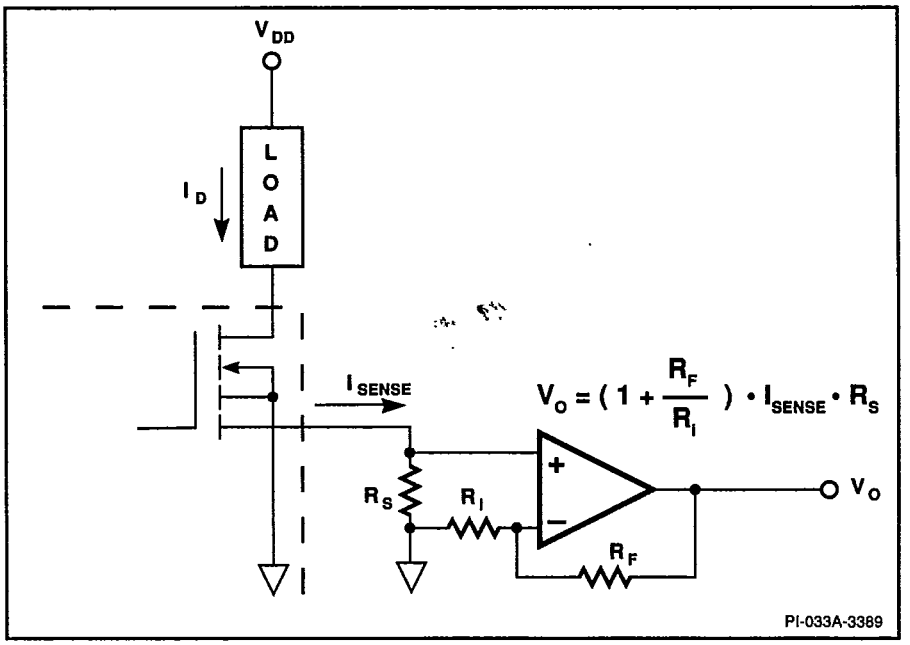

Figure 4. Resistor sensing circuit

developed across R_S should be less than r times 100 mV.
Thus:

$$R_S(max) < \frac{(0.1\ V)\ r}{I_D(max)}$$

The lower bound for R_S will be determined by the offset voltage of the op amp and the lowest voltage that can be amplified without being impacted by signal noise. However, while proportional control using I_{SENSE} appears formidable, the current mirror can easily be used to warn of current overloads, or for the detection of the presence or absence of load current.

NOTE: If the SENSE pins are not used, they should **always** be shorted to COMMON. **Do not** leave them floating. The source of the SENSE device could float toward the MOSFET drain voltage, exceeding the gate-to-source rating of the device.

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Schematic Diagram and Pin Configuration

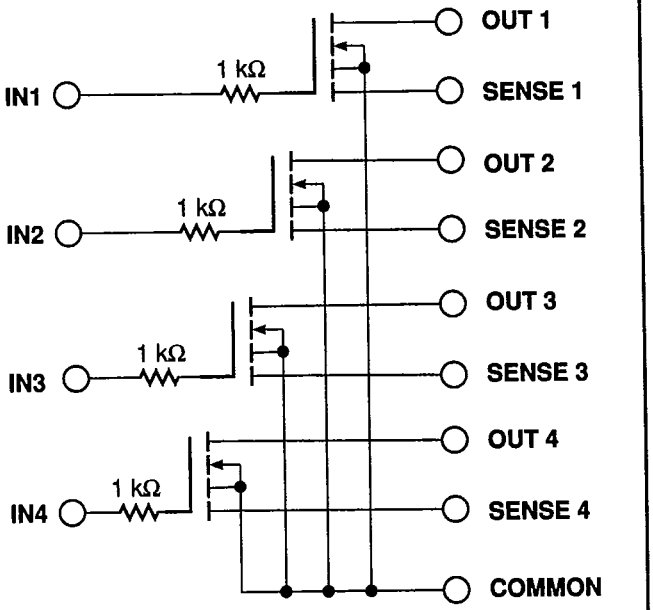


Figure 5. Schematic diagram

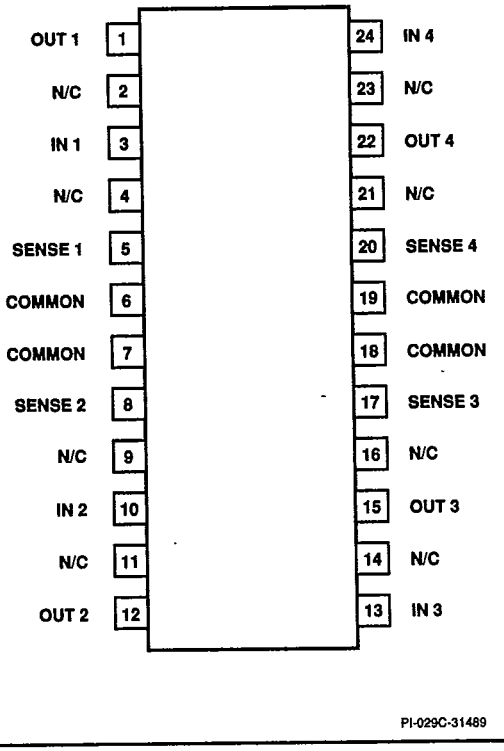


Figure 6. Pin configuration

Absolute Maximum Ratings[1]

Drain (OUT)Voltage
- -1 Suffix ..... 200 V
- -2 Suffix ..... 300 V
- -3 Suffix ..... 400 V

Gate (IN) Voltage ..... -7 V to 7 V

Drain (OUT) Current
- Continuous (per transistor - T_A = 25°C)[2]. ..... 335 mA
- (per transistor - T_A = 70°C)[2]. ..... 270 mA
- (per package - T_A = 25°C) ..... 675 mA
- (per package - T_A = 70°C) ..... 525 mA
- Peak (per transistor) [2,3]. ..... 430 mA
- (per package)[3]. ..... 1.7 A

Storage Temperature ..... -65 to 125°C
Ambient Temperature ..... 0 to 70°C
Junction Temperature ..... 150°C
Lead temperature [4]. ..... 260°C
Power Dissipation (T_A =25°C) ..... 1.7 W
(T_A =70°C) ..... 1.1 W
Thermal Impedance, (θ_{JA}) ..... 73.5°C/W

1. Unless noted, all voltages referenced to COMMON
2. One transistor conducting at any time.
3. 300 µs pulse, < 2% duty cycle.
4. 1/16" from case for 5 seconds

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{SENSE} = 0 V, T_A = 0 to 70°C		Limits MIN	Limits TYP	Limits MAX	Units
OFF-STATE CHARACTERISTICS[1]							
Breakdown Voltage	BV_{DSS}	I_{OUT} = 100 µA, V_{IN}= 0 V	-1 Suffix	200			V
			-2 Suffix	300			
			-3 Suffix	400			
Drain Source Leakage Current	I_{DSS}	V_{OUT} = 80% of BV_{DSS}, V_{IN} = 0 V	T_j =25°C			10	µA
			T_j = 150°C			25	
Gate Body Leakage Current	I_{GSS}	V_{IN} = 5 V, V_{OUT} = 0 V				500	nA
ON-STATE CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{IN} = V_{OUT}, I_{OUT} =1 mA		0.5		1.5	V
On-State Resistance	$R_{DS}(ON)$	V_{IN} = 5 V, I_{OUT} = 100 mA	T_j = 25°C		7	10	Ω
			T_j = 150°C		14	16	
$\Delta R_{DS}(ON)$ over Temperature	$\Delta R_{DS}(ON)$	I_{OUT} =100 mA, V_{IN} = 5 V				0.6	%/°C
SENSE Current	I_{SENSE}	R_{SENSE} = 150 Ω (See Figure 8), I_{OUT} =100 mA		105		165	µA
Trans-conductance	g_{fs}	I_{OUT} =100 mA, V_{OUT} = 25 V			3.0		S
DYNAMIC CHARACTERISTICS							
Total Gate Charge	Q_G	V_{DD} = 25 V, V_{IN} = 0 V, f = 1 MHz			900		pC
Output Capacitance	C_{OSS}	V_{DD} = 25 V, f = 1 MHz			24		pF
Turn-on DelayTime	$t_{d(on)}$	See Figure 8			30	45	ns
Fall Time	t_f	See Figure 8			100	150	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 8			170	220	ns
Rise Time	t_r	See Figure 8			160	210	ns

NOTES:
1. All gates(IN X) and drains (OUT X) not under test connected to COM

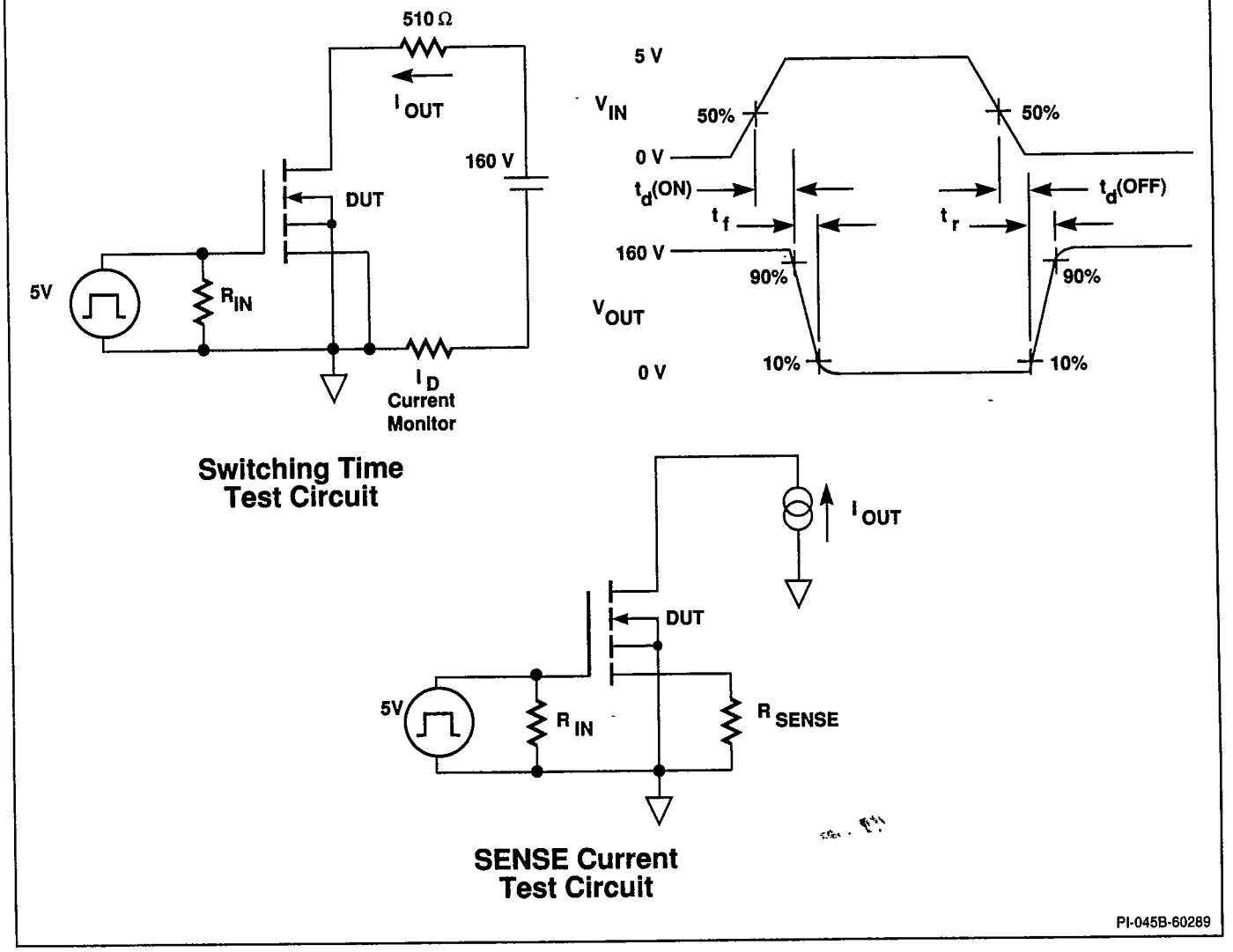
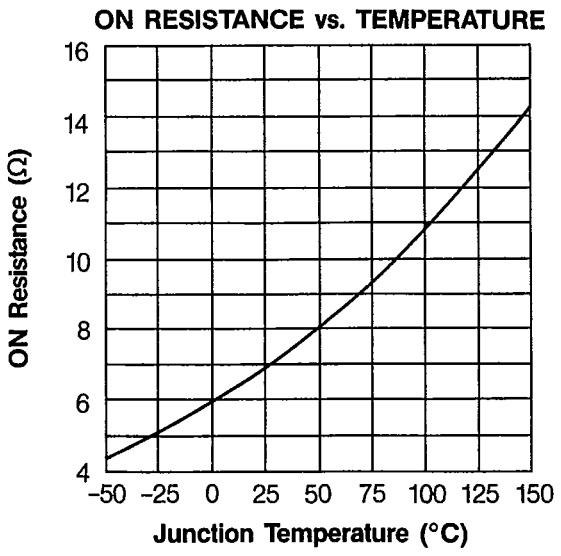
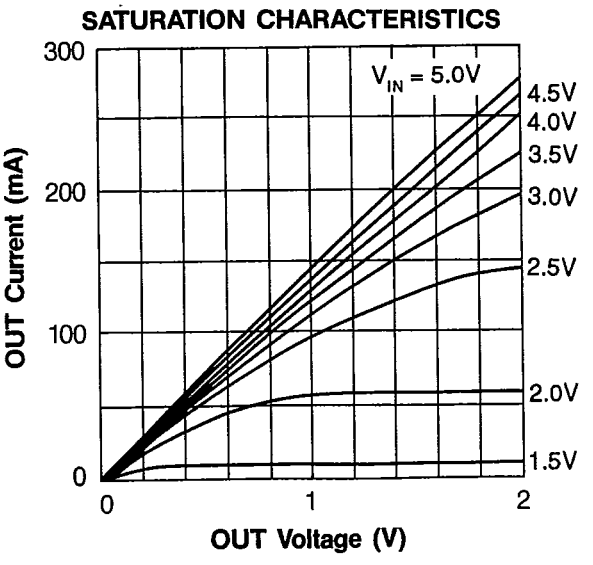
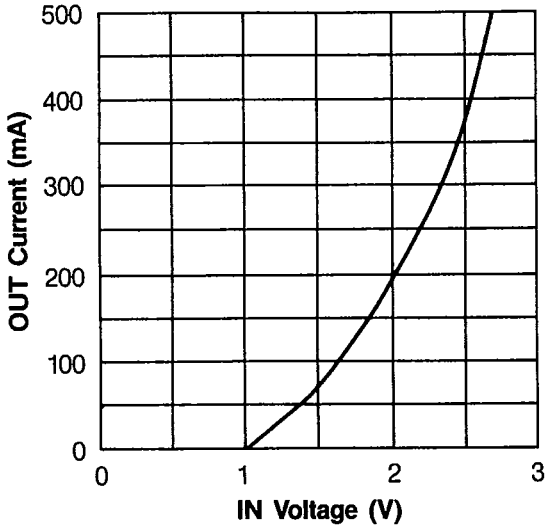


Figure 8. Test circuits

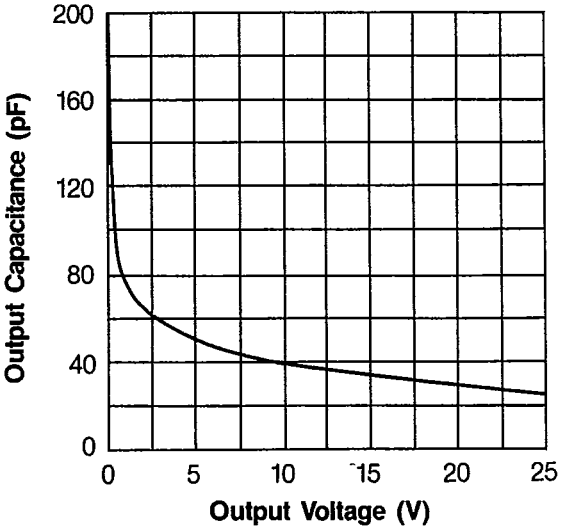




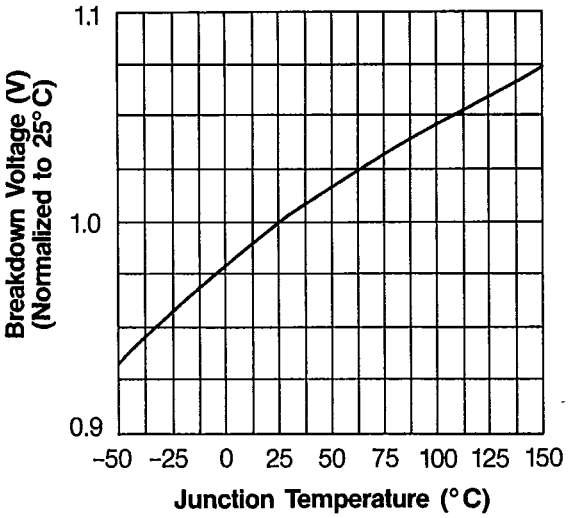
TRANSFER CHARACTERISTICS



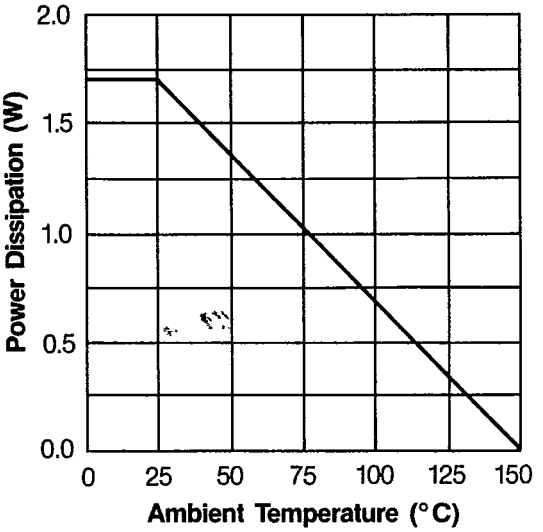
OUTPUT CAPACITANCE (Coss)



BVDSS vs. JUNCTION TEMPERATURE



PACKAGE POWER DERATING

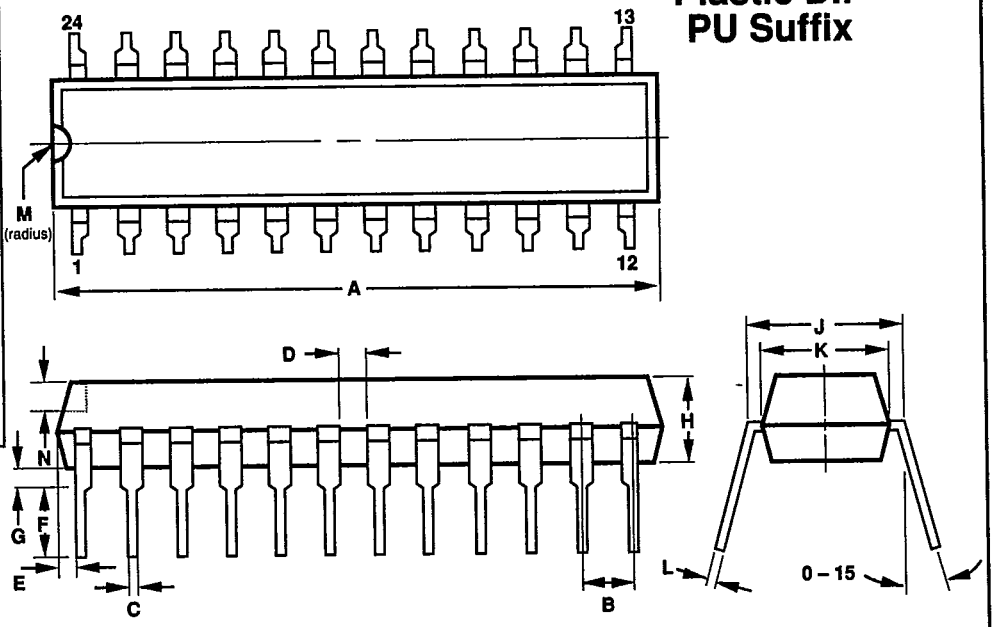


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE RANGE	BREAKDOWN VOLTAGE
PWR-NCH401PUC1	24-PIN PDIP	0 TO 70° C	200 V
PWR-NCH401PUC2	24-PIN PDIP	0 TO 70° C	300 V
PWR-NCH401PUC3	24-PIN PDIP	0 TO 70° C	400 V

DIM	inches	mm
A	1.270 MAX	32.26 MAX
B	.090-.110	2.286-2.794
C	.015-.021	.381-.533
D	.040 TYP	1.016 TYP
E	.010-.040	.254-1.016
F	.125 MIN	3.175 MIN
G	.020 MIN	.508 MIN
H	.125-.135	3.175-3.429
J	.300-.320	7.620-8.128
K	.245-.255	6.223-6.477
L	.009-.015	.229-.381
M	.030-.110	.762-2.794
N	.020 TYP	.508 TYP

24-Pin Narrow-body Plastic DIP PU Suffix



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