EPSON

SLA9000F Series

●High speed, high integration gate array.
●Number of gates mounted: 2.7K to 44K gates.

■ DESCRIPTION

The SLA9000F series is a SOG type CMOS gate which has realized high speed, high integration and high driving capability. This series is offered with 2,784 to 44,070 gates to ensure an optimum application for any mid size high speed systems.
This series is designed to operate on both 5 V and 3 V systems to correspond to increasing low-voltage oriented applications. Simplified level shifter cell is available on this series. And, the μA order low noise output cell of the series has made it suitable for small size, handy equipments and many other applications.

■ FEATURES

- Super-high density (adopting 1.0μm silicon gate CMOS with 2-metal layer)
- High-speed operation (operation delay of internal gate = 0.3ns at 5.0V, 2-input Power NAND standard)
- Simplified level shifter cells available
- Output drivability (I_{OL} = 100μ, 2, 6, 12, 24 mA when 5.0V, I_{OL} = 100μ, 2, 4, 8, 12mA when 3.3V)
- On-chip RAM available
- Low noise output cells available

■ PRODUCT LINEUP

Master		SLA902F	SLA904F	SLA907F	SLA909F	SLA913F	SLA919F	SLA927F	SLA944F
Total BCs (Raw Gates)		2,784	4,392	7,872	9,540	13,144	19,350	27,234	44,070
Usable Bcs		1,809	2,854	4,723	5,724	7,229	10,642	13,617	22,035
Number of PADs		80	100	128	144	160	184	208	256
Propagation Delay	Internal Gates	tpd = 0.30ns (standard at 5.0V), tpd = 0.43ns (standard at 3.3V)							
	Input Buffers	tpd = 0.91ns (standard at 5.0V), tpd = 1.08ns (standard at 3.3V)							
	Output Buffers	tpd = 3.5ns (standard at 5.0V), tpd = 4.2ns (standard at 3.3V) CL = 50pF							
I/O Level		TTL, CMOS							
Input Mode		TTL, CMOS, Pull-up/Pull-down, Schmitt, 3.0/3.3/5.0V Level interface							
Output Mode		Normal, Open drain, 3-state, Bi-directional, 3.0/3.3/5.0V Level interface							

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SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

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http://www.epson.co.jp