Power Management Switch ICs for PCs and Digital Consumer Products

Load Switch ICs for Potable Equipment

BD6520F,BD6522F

No.11029EBT12

●Description

The power switch for expansion module is a power management switch having one circuit of N-channel Power MOS FET. The switch realizes 50mΩ(Typ.) ON resistance. The switch turns on smoothly by the built-in charge pump, therefore, it is possible to reduce inrush current at switch on. And soft start control by external capacitor is available.
Further, it has a discharge circuit that discharges electric charge from capacitive load at switch off, Under voltage lockout circuit, and a thermal shutdown circuit.

●Features

1) Low on resistance (50mΩ, Typ.) N-MOS switch built in
2) Maximum output current: 2A
3) Discharge circuit built in
4) Soft start control circuit built in
5) Under voltage lockout (UVLO) circuit built in
6) Thermal shutdown (Output off latching)
7) Reverse current flow blocking at switch off (only BD6522F)

●Applications

Notebook PC, PC peripheral device, etc.

●Lineup

Parameter	BD6520F	BD6522F
Supply Voltage	3 to 5.5V	3 to 5.5V
Switch current	2A	2A
On Resistance	50mΩ	50mΩ
OUT Rise Time	2000μs	1000μs
OUT Fall Time	3μs	4μs
Package	SOP8	SOP8
Reverse current flow blocking at switch off	-	○

●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.3 to 6.0	V
CTRL Input Voltage	V_{CTRL}	-0.3 to 6.0	V
Switch Output Voltage	V_{OUT}	-0.3 to V_{DD} + 0.3 (BD6520F)	V
		-0.3 to 6.0 (BD6522F)	V
Storage temperature	T_{STG}	-55 to 150	℃
Power dissipation	Pd	560*1	mW

*1 This value decreases 4.48mW/℃ above Ta=25℃
* Resistance radiation design is not doing.
* Operation is not guaranteed.

●Operation conditions

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	3.0 to 5.5	V
Switch current	I_{OUT}	0 to 2	A
Operating Temperature	T_{OPR}	-25 to 85	℃

●Electrical characteristics

◎BD6520F(Unless otherwise specified, Ta = 25℃, V_{DD} = 5V)

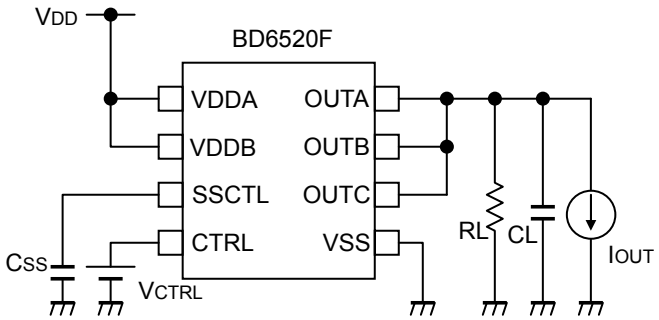
Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
On Resistance	$R_{ON}1$	-	50	70	mΩ	V_{DD} = 5V, V_{CTRL} = 5V
	$R_{ON}2$	-	60	85	mΩ	V_{DD} = 3V, V_{CTRL} = 3V
Operating Current	I_{DD}	-	110	220	μA	V_{CTRL} = 5V, OUT = OPEN
	I_{DDST}	-	-	2	μA	V_{CTRL} = 0V, OUT = OPEN
Control Input voltage	$V_{CTRL}L$	-	-	0.7	V	V_{CTRL} L = Low Level
	$V_{CTRL}H$	2.5	-	-	V	V_{CTRL} H = High Level
Control Input current	I_{CTRL}	-1	0	1	μA	V_{CTRL} = L, H
Turn On Delay	Trd	200	1000	2000	us	RL = 10Ω,SSCTL = OPEN CTRL = L→H → OUT=50%
Turn On Rise Time	Tr	500	2000	7500	us	RL = 10Ω,SSCTL = OPEN CTRL = 10% → 90%
Turn Off Delay	Tfd	-	3	20	us	RL = 10Ω,SSCTL = OPEN CTRL = H→L → OUT=50%
Turn Off Fall Time	Tf	-	1	20	us	RL = 10Ω,SSCTL = OPEN CTRL = 90% → 10%
Discharge Resistance	R_{SWDC}	-	350	600	Ω	V_{DD} = 5V, V_{CTRL} = 0V, V_{OUT} = 5V
UVLO Threshold Voltage	$V_{UVLO}H$	2.3	2.5	2.7	V	V_{DD} increasing
	$V_{UVLO}L$	2.1	2.3	2.5	V	V_{DD} decreasing
UVLO Hysteresis Voltage	V_{HYS}	100	200	300	mV	V_{HYS} = $V_{UVLO}H$ - $V_{UVLO}L$
Thermal Shutdown Threshold	T_{TS}	-	135	-	℃	V_{CTRL} = 5V
SSCTL Output Voltage	V_{SSCTL}	-	13.5	-	V	V_{CTRL} = 5V

◎BD6522F(Unless otherwise specified, Ta = 25℃, V_{DD} = 5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
On Resistance	$R_{ON}1$	-	50	70	mΩ	V_{DD} = 5V, V_{CTRL} = 5V
	$R_{ON}2$	-	60	85	mΩ	V_{DD} = 3.3V, V_{CTRL} = 3.3V
Operating Current	I_{DD}	-	110	220	μA	V_{CTRL} = 5V, OUT = OPEN
	I_{DDST}	-	-	2	μA	V_{CTRL} = 0V, OUT = OPEN
Control Input Voltage	$V_{CTRL}L$	-	-	0.7	V	V_{CTRL}L = Low Level
	$V_{CTRL}H$	2.5	-	-	V	V_{CTRL}H = High Level
Control Input Current	I_{CTRL}	-1	0	1	μA	V_{CTRL} = L, H
Turn On Time	T_{ON}	-	1000	3500	us	RL = 10Ω,SSCTL = OPEN CTRL = H → OUT =90%
Turn Off Time	T_{OFF}	-	4	20	us	RL = 10Ω,SSCTL = OPEN CTRL = L → OUT = 10%
Discharge Resistance	R_{SWDC}	-	350	600	Ω	V_{DD} = 5V,V_{CTRL} = 0V
UVLO Threshold Voltage	$V_{UVLO}H$	2.3	2.5	2.7	V	V_{DD} increasing
	$V_{UVLO}L$	2.1	2.3	2.5	V	V_{DD} decreasing
UVLO Hysteresis Voltage	V_{HYS}	100	200	300	mV	V_{HYS} = $V_{UVLO}H$ - $V_{UVLO}L$
Thermal Shutdown Threshold	T_{TS}	-	135	-	℃	V_{CTRL} = 5V
SSCTL Output Voltage	V_{SSCTL}	-	13.5	-	V	V_{CTRL} = 5V

●Measurement circuit

◎BD6520F



◎BD6522F

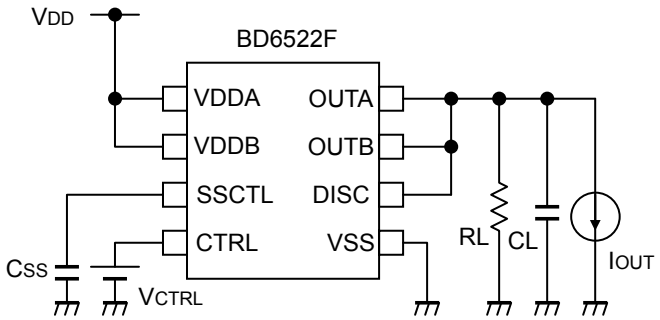
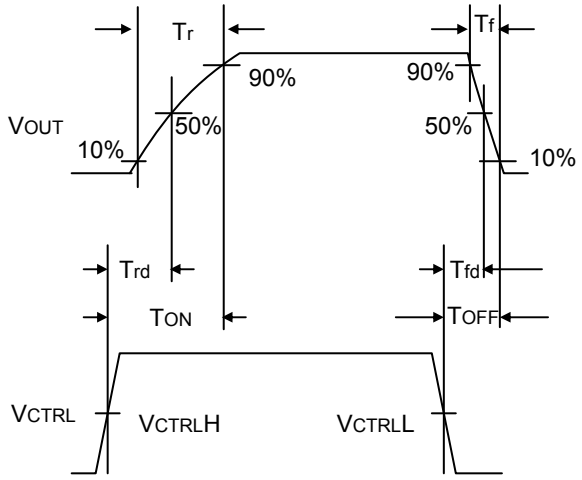


Fig.1 Measurement circuit

●Timing diagram

◎BD6520F



◎BD6522F

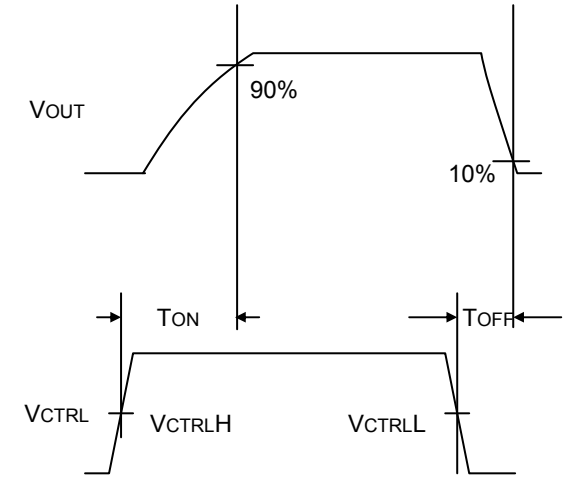


Fig.2 Timing diagram

●Typical characteristics

◎BD6520F

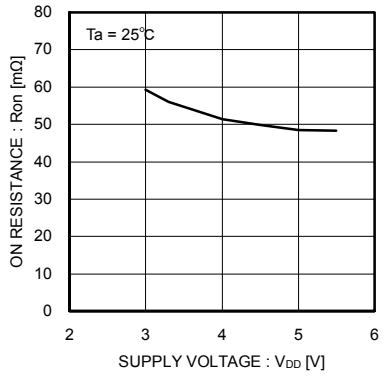


Fig.3 On resistance

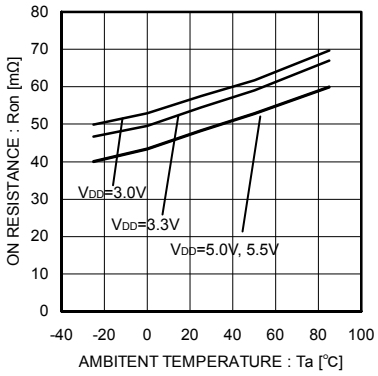


Fig.4 On resistance

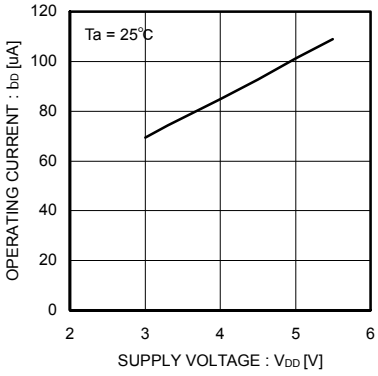


Fig.5 Operating current (CTRL enable)

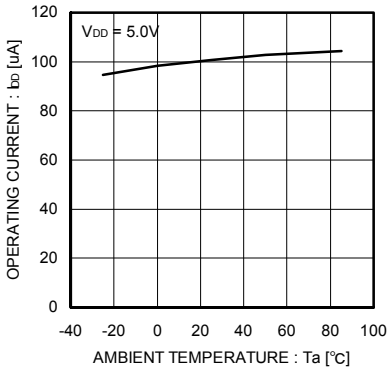


Fig.6 Operating current (CTRL enable)

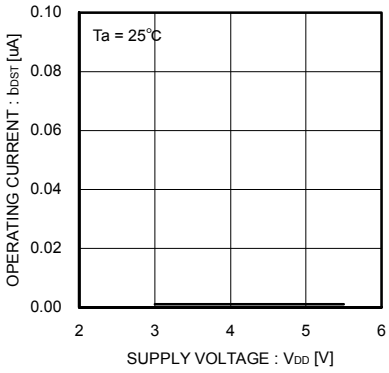


Fig.7 Operating current (CTRL disenable)

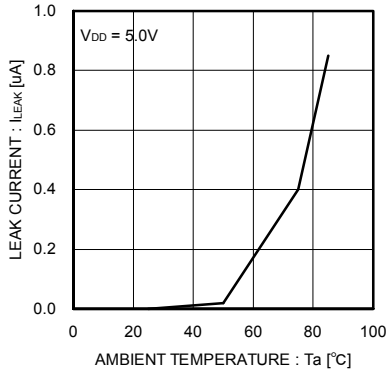


Fig.8 Leak current

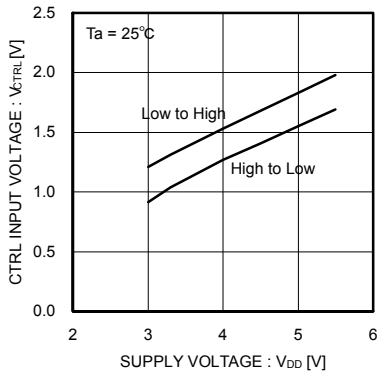


Fig.9 CTRL input voltage

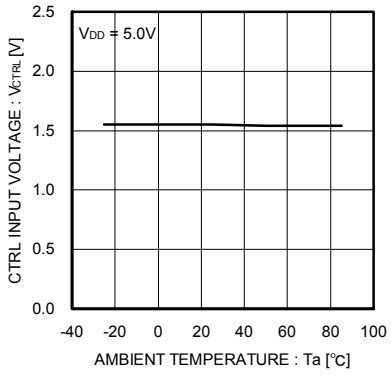


Fig.10 CTRL input voltage H→L

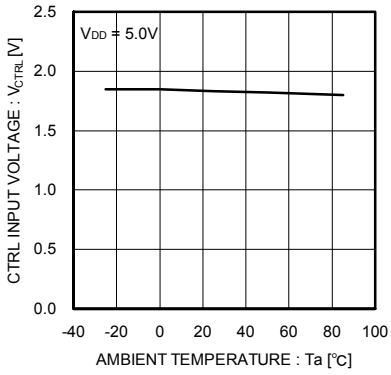


Fig.11 CTRL input voltage L→H

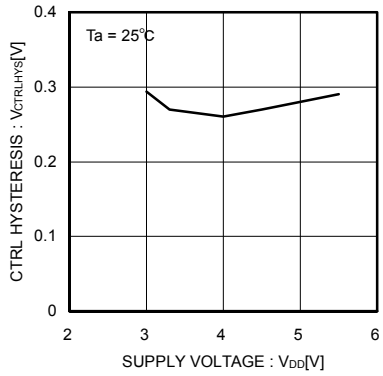


Fig.12 CTRL hysteresis voltage

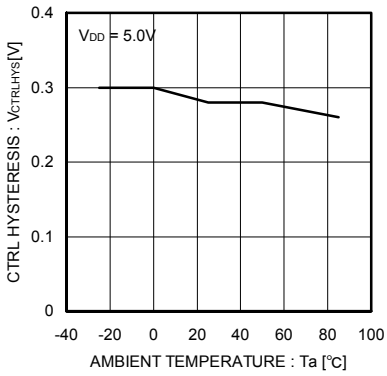


Fig.13 CTRL hysteresis voltage

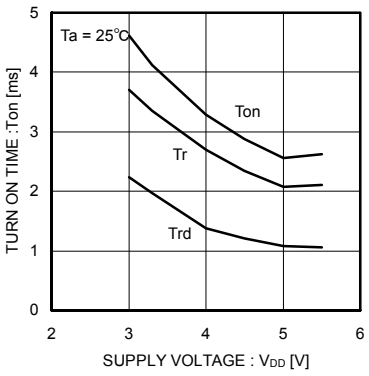


Fig.14 Turn On Rise time

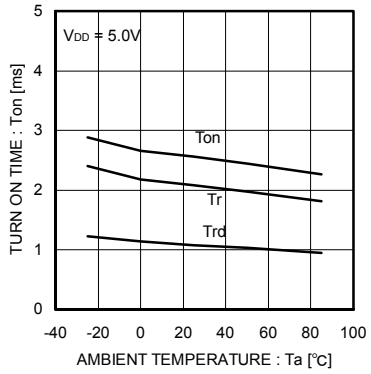


Fig.15 Turn On Rise time

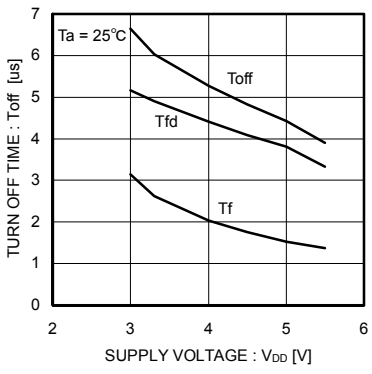


Fig.16 Turn Off Fall time

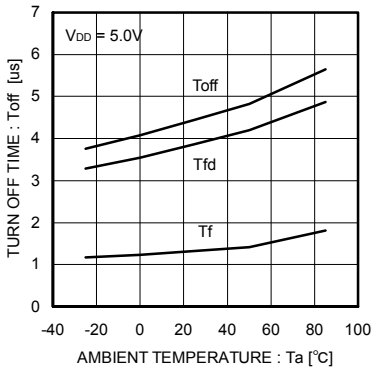


Fig.17 Turn Off Fall time

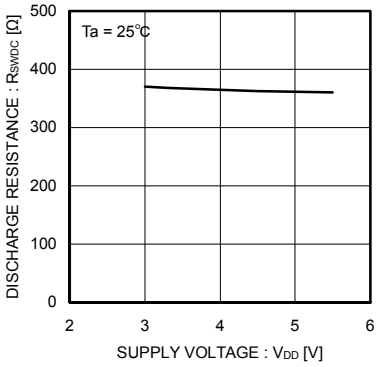


Fig.18 Switch discharge resistance

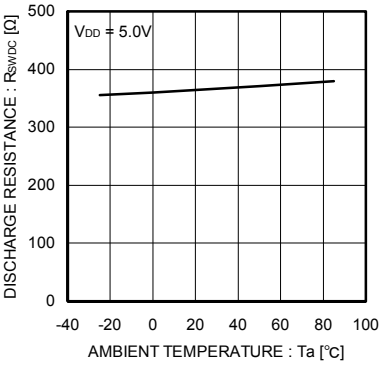


Fig.19 Switch discharge resistance

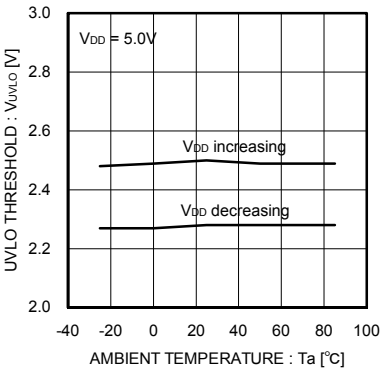


Fig.20 UVLO threshold voltage

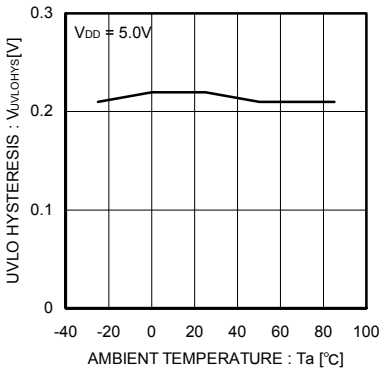


Fig.21 UVLO hysteresis voltage

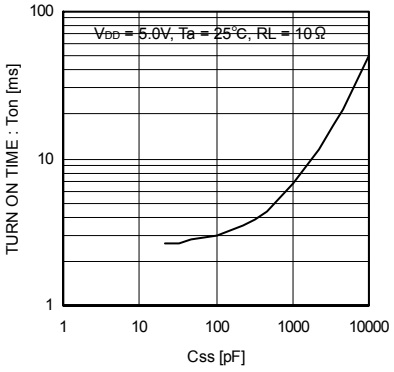


Fig.22 Turn On Rise time (vs. Css)

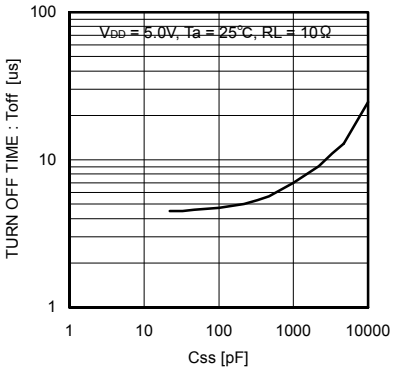


Fig.23 Turn Off Fall time (vs. Css)

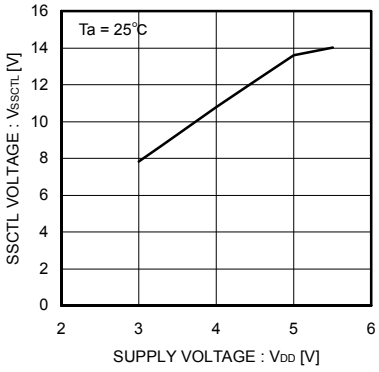


Fig.24 SSCTL output voltage

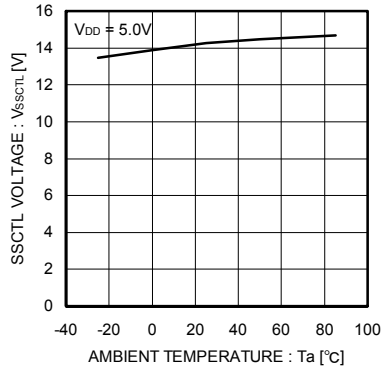


Fig.25 SSCTL output voltage

◎BD6522F

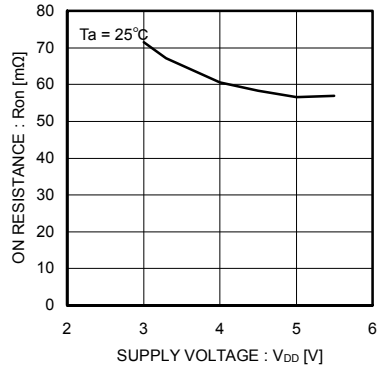


Fig.26 ON resistance

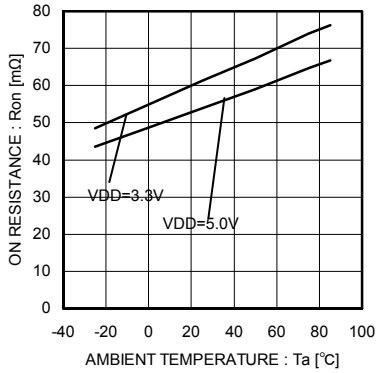


Fig.27 ON resistance

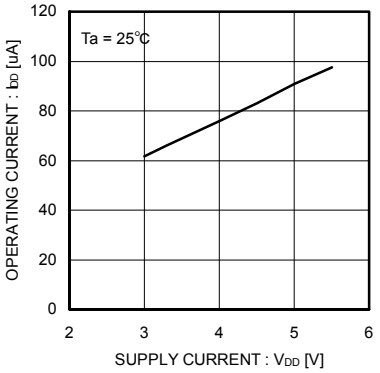


Fig.28 Operating current (CTRL enable)

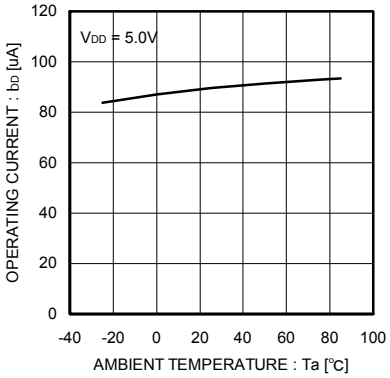


Fig.29 Operating current (CTRL enable)

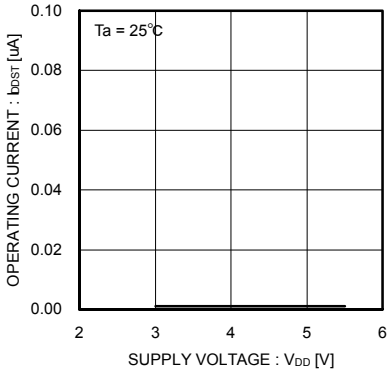


Fig.30 Operating current (CTRL disenable)

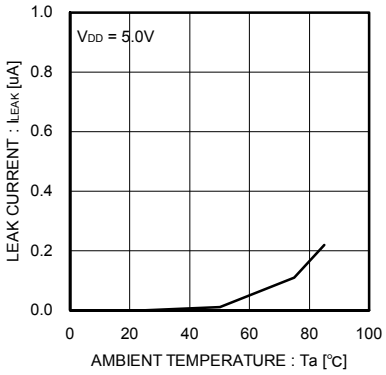


Fig.31 Leak current

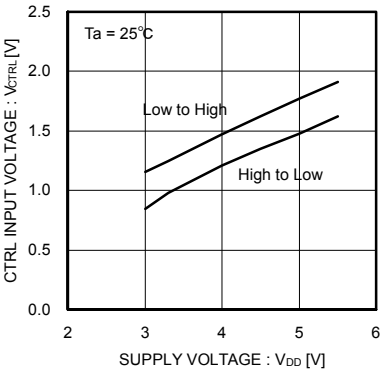


Fig.32 CTRL input voltage

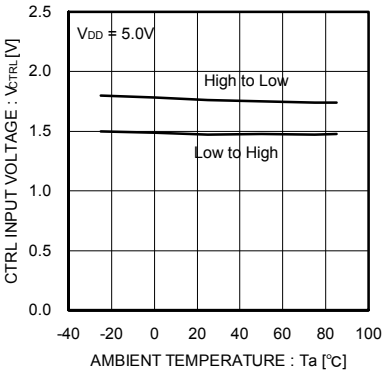


Fig.33 CTRL input voltage

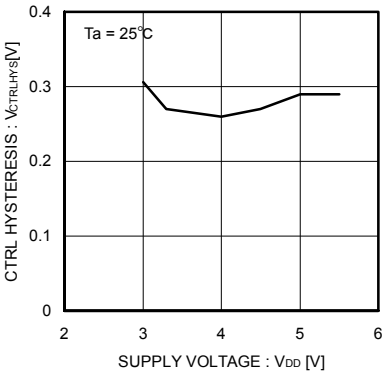


Fig.34 CTRL hysteresis voltage

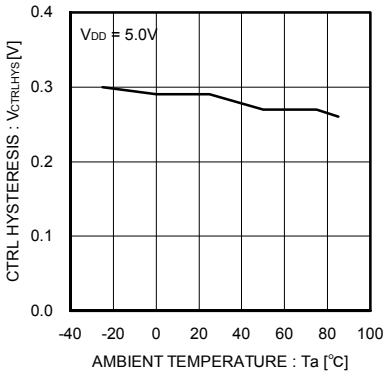


Fig.35 CTRL hysteresis voltage

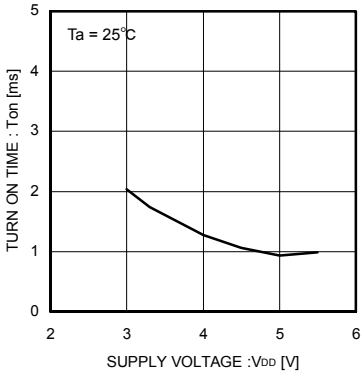


Fig.36 Turn On time

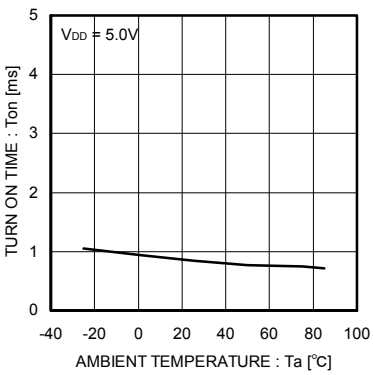


Fig.37 Turn On time

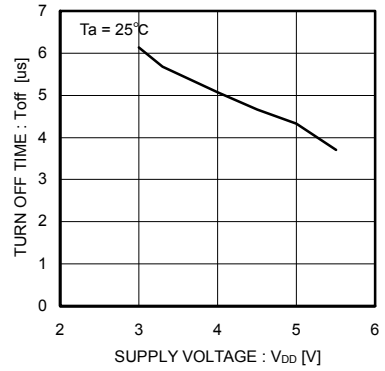


Fig.38 Turn Off time

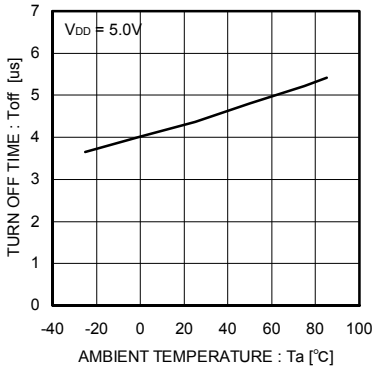


Fig.39 Turn Off time

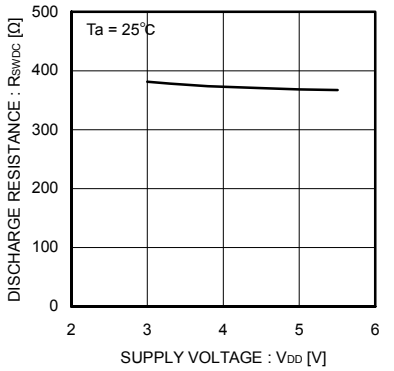


Fig.40 Switch discharge resistance

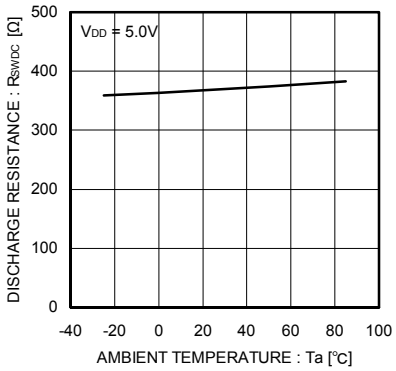


Fig.41 Switch discharge resistance

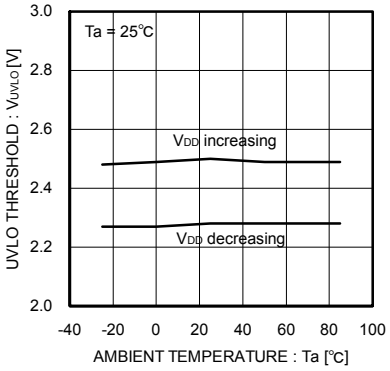


Fig.42 UVLO threshold voltage

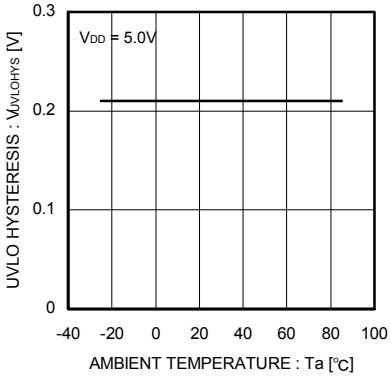


Fig.43 UVLO hysteresis voltage

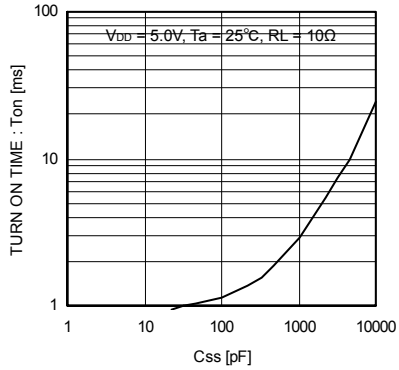


Fig.44 Turn On time (vs. Css)

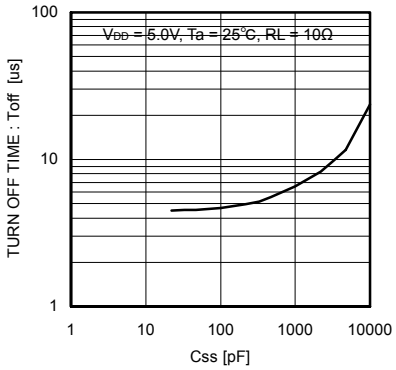


Fig.45 Turn Off time (vs. Css)

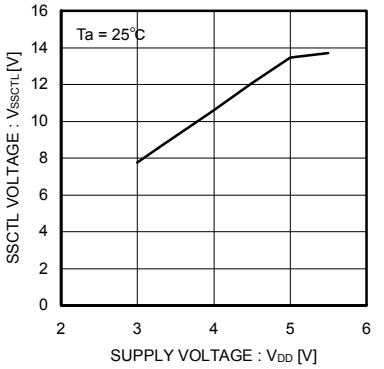


Fig.46 SSCTL output voltage

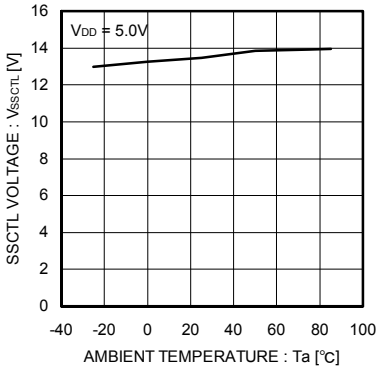


Fig.47 SSCTL output voltage

●**Waveform data**

V_{DD} = 5V, CL = 47μF, RL = 47Ω, unless otherwise specified.

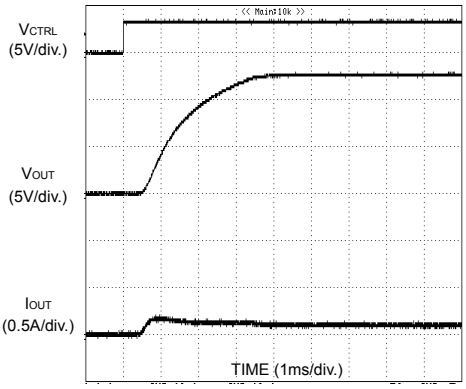


Fig.48 Turn On Rise Time
(BD6520F)

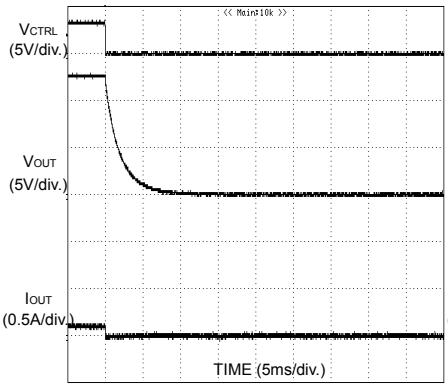


Fig.49 Turn Off Fall Time
(BD6520F)

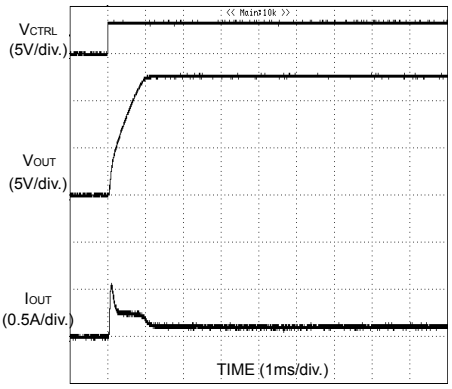


Fig.50 Turn On Rise Time
(BD6522F)

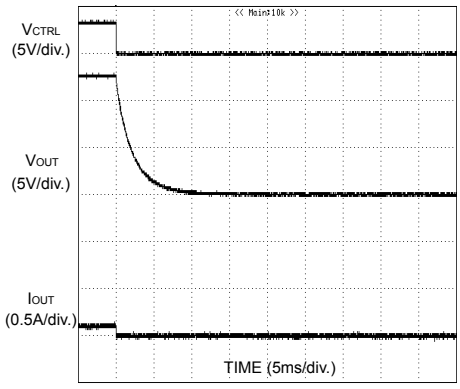


Fig.51 Turn Off Fall Time
(BD6522F)

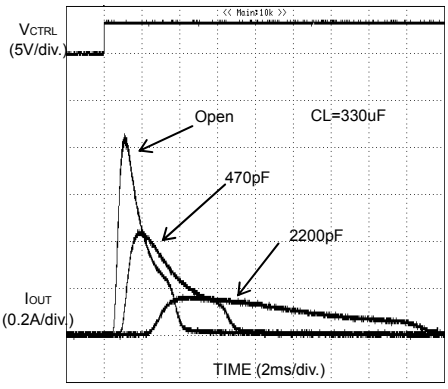


Fig.52 Inrush current vs. Css
(BD6520F)

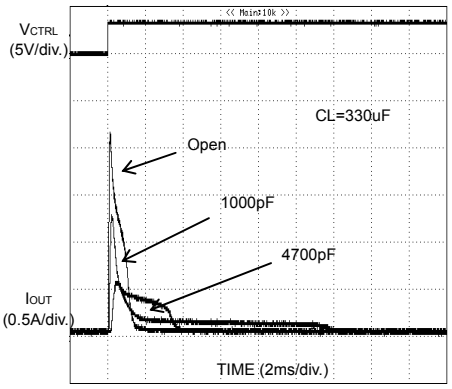


Fig.53 Inrush current vs. Css
(BD6522F)

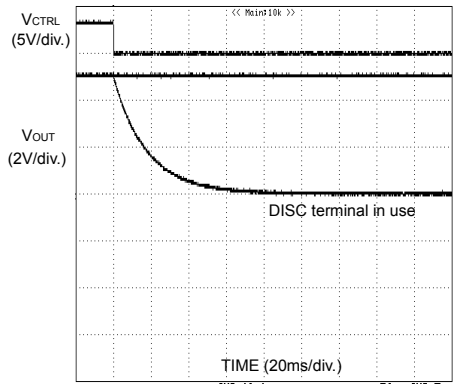


Fig.54 Discharge: CL = 47uF, RL = Open
(BD6522F)

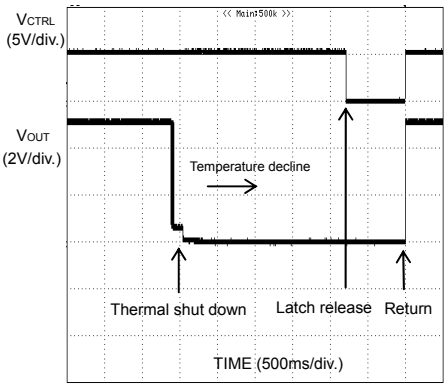


Fig.55 Thermal shutdown

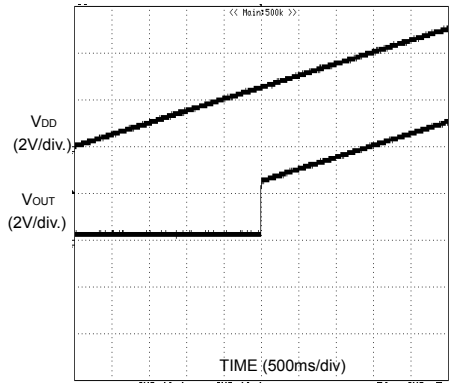


Fig.56 UVLO (at VDD increase)

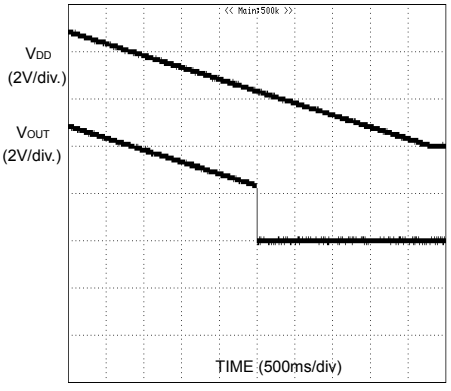


Fig.57 UVLO (at VDD decrease)

●**Block diagram, pin configuration, pin description**
(BD6520F)

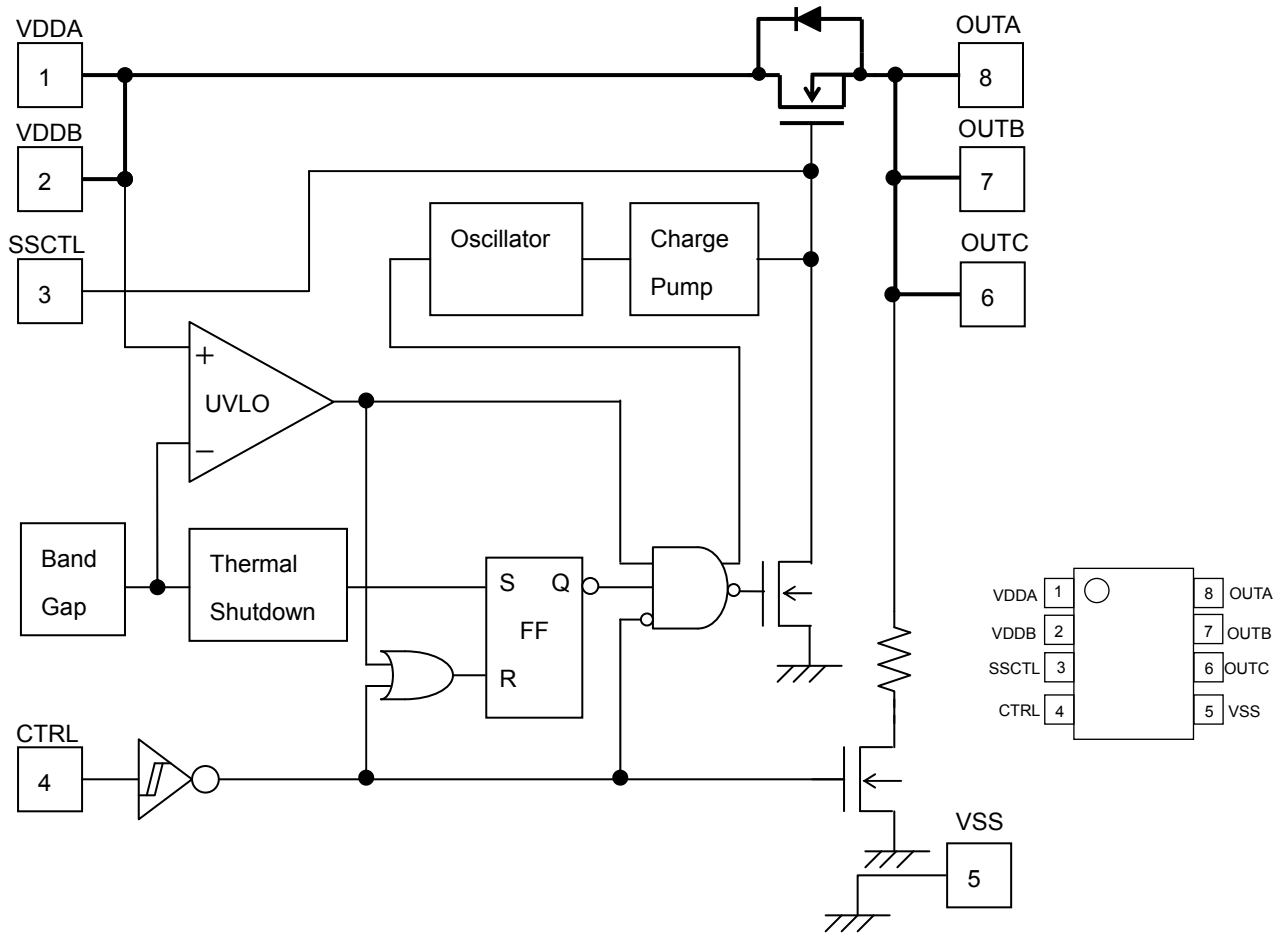


Fig.58 Block diagram(BD6520F)

Pin No.	Symbol	Pin Function
1,2	VDDA, VDDB	Switch input pin At use, connect each pin outside.
3	SSCTL	Soft start setting pin Add external capacitor, it is possible to delay switch On, Off time.
4	CTRL	Control input pin Switch On at High level, switch Off at Low level.
5	VSS	Ground
6,7,8	OUTA, OUTB, OUTC	Switch output pin At use, connect each pin outside.

(BD6522F)

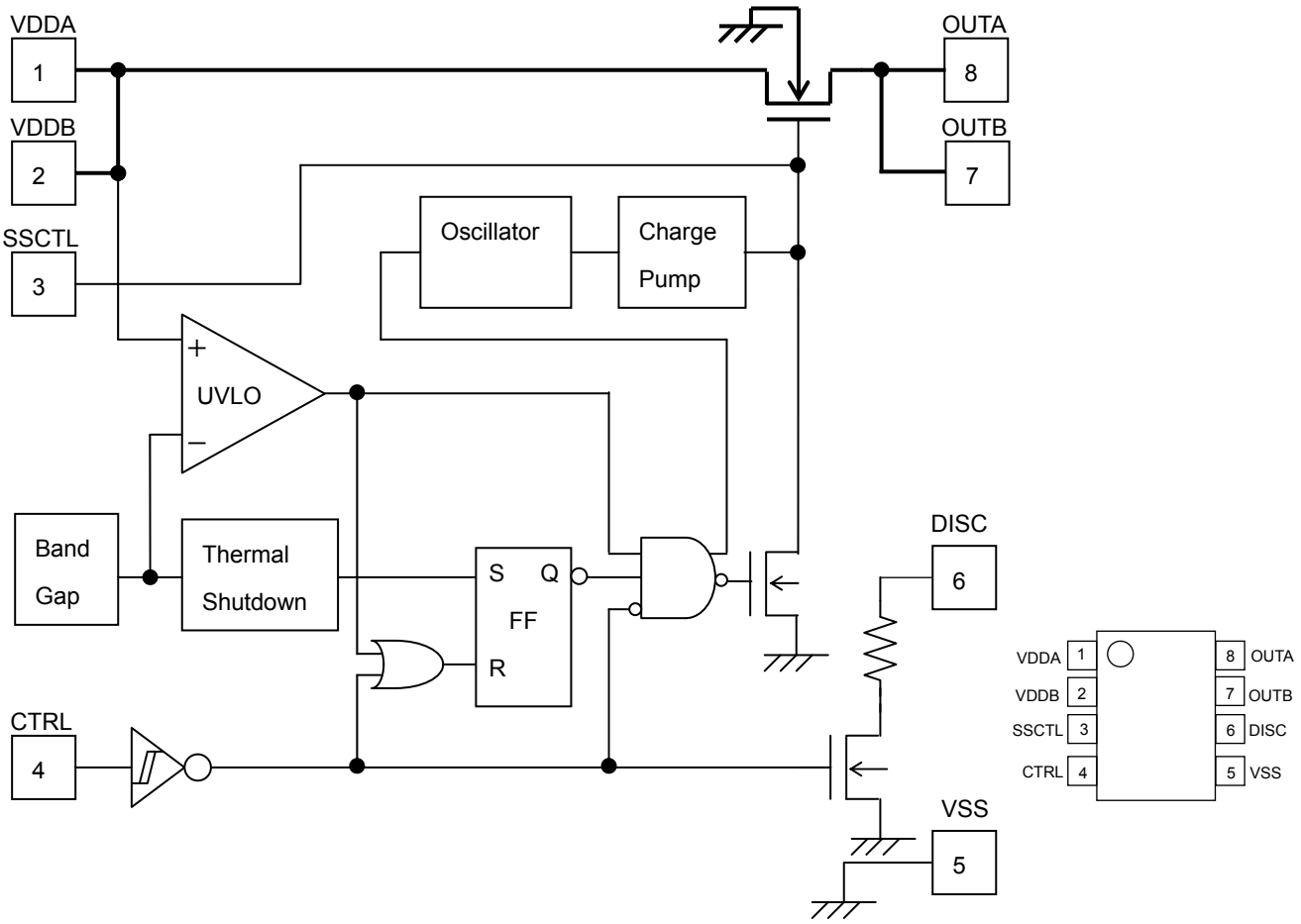


Fig.59 Block diagram(BD6522F)

Pin No.	Symbol	Pin Function
1,2	VDDA, VDDB	Switch input pin At use, connect each pin outside.
3	SSCTL	Soft start setting pin Add external capacitor, it is possible to delay switch On, Off time.
4	CTRL	Control input pin Switch On at High level, switch Off at Low level.
5	VSS	Ground
6	DISC	Discharge pin
7,8	OUTA, OUTB	Switch output pin At use, connect each pin outside.

●I/O circuit

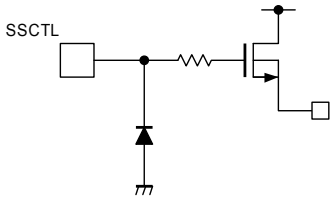
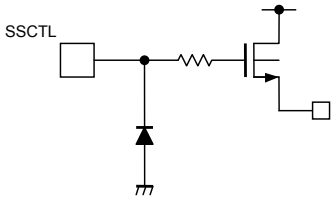
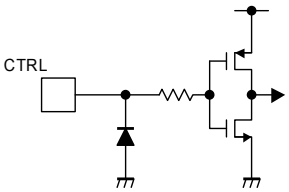
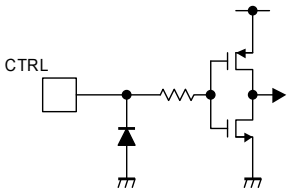
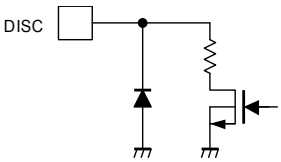
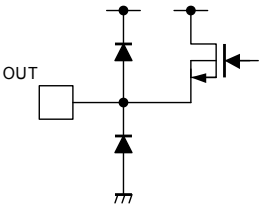
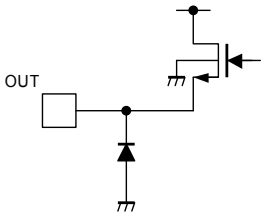
Symbol	Pin No.	Equivalent circuit BD6520F	Equivalent circuit BD6522F
SSCTL	3		
CTRL	4		
DISC	6 (BD6522F)		
OUT	6 (BD6520F), 7, 8		

Fig.60 I/O circuit

●Functional description

1. Switch operation

VDD pin and OUT pin are connected to the drain and the source of switch MOSFET respectively. And the VDD is used also as power source input to internal control circuit.

When CTRL input is set to High level and the switch is turned on, VDD and OUT is connected by a 50mΩ switch. In a normal condition, current flows from VDD to OUT. If voltage of OUT is higher than VDD, current flows from OUT to VDD, since the switch is bidirectional.

In BD6520F, there is a parasitic diode between the drain and the source of switch MOSFET. Therefore, even when the switch is off, if the voltage of OUT is higher than that of VDD, current flows from OUT to VDD. In BD6522F, there is not this parasitic diode, it is possible to prevent current from flowing reversely from OUT to VDD.

2. Thermal shutdown

Thermal shut down circuit turns off the switch when the junction temperature exceeds 135℃(Typ.).

The switch off status of the thermal shut down is latched. Therefore, even when the junction temperature goes down, switch off is maintained. To release the latch, it is necessary to input a signal to switch off to CTRL terminal or make UVLO status. When the switch on signal is input or UVLO is released, the switch output is recovered.

The thermal shut down circuit works when CTRL signal is active.

3. Low voltage malfunction prevention circuit (UVLO)

The UVLO circuit monitors the voltage of the VDD pin, when the CTRL input is active. UVLO circuit prevents the switch from turning on until the V_{DD} exceeds 2.5V(Typ.). If the V_{DD} drops below 2.3V(Typ.) while the switch turns on, then UVLO shuts off the switch.

4. Soft start control

In BD6520F/BD6522F, soft start is carried out in order to reduce inrush current at switch on. Further, in order to reduce inrush current, soft start control pin (SSCTL) is prepared.

By connecting external capacitor to between SSCTL and GND, it is possible to make smoother the switch rise time. When the switch is enabled, SSCTL outputs voltage of about 13.5V.

SSCTL terminal requires high impedance, so pay attention in packaging it so that there should not be leak current. And when voltage is impressed from the outside to SSCTL terminal, switch on, off cannot be made correctly.

5. Discharge circuit

When the switch between the VDD and the OUT is OFF, the 200Ω(Typ.) discharge switch between OUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged.

In BD6522F, the input of discharge circuit is separately prepared as DISC pin. When to use the discharge circuit, connect OUT pin and DISC pin outside.

●Timing diagram

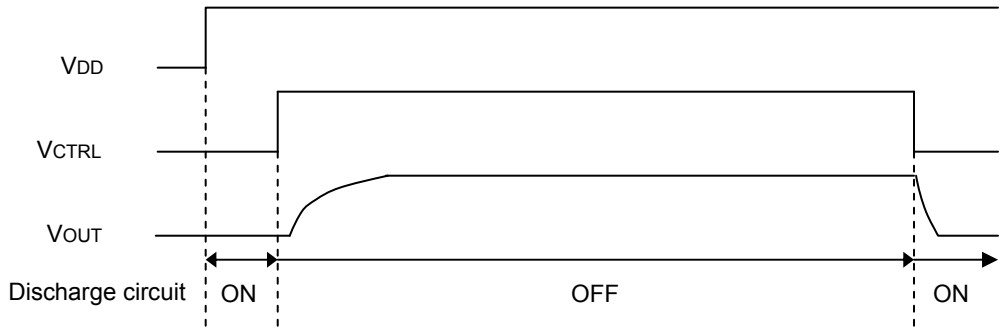


Fig.61 Normal operation

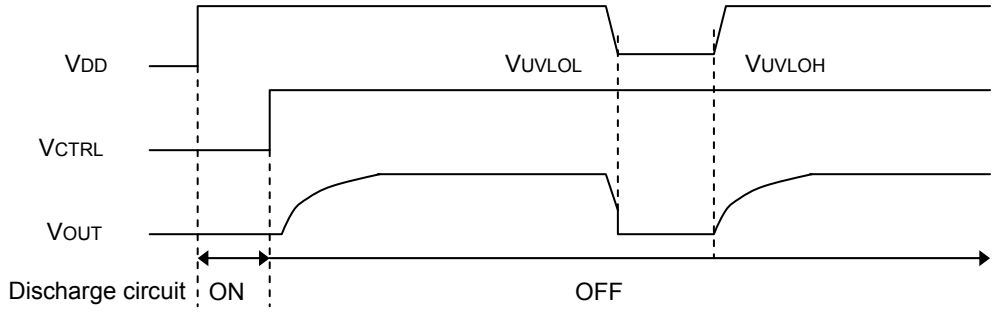


Fig.62 UVLO operation

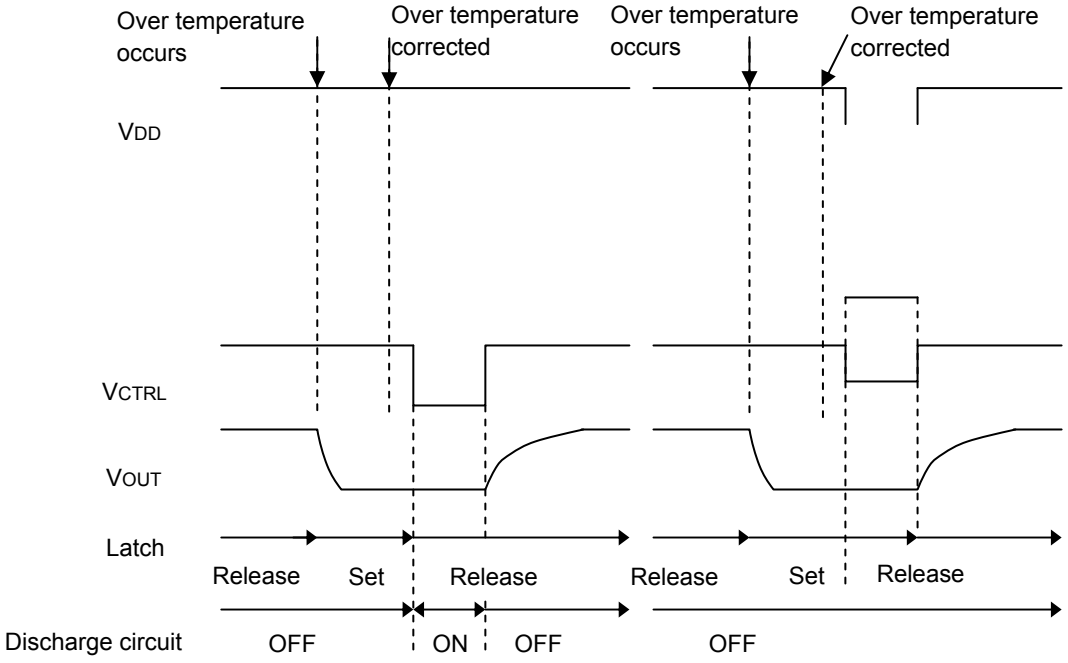


Fig.63 Thermal shutdown operation

●Typical application circuits

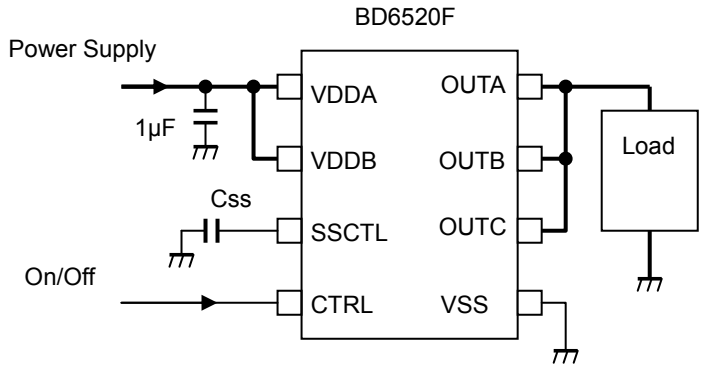


Fig.64 Power supply switch circuit (BD6520F)

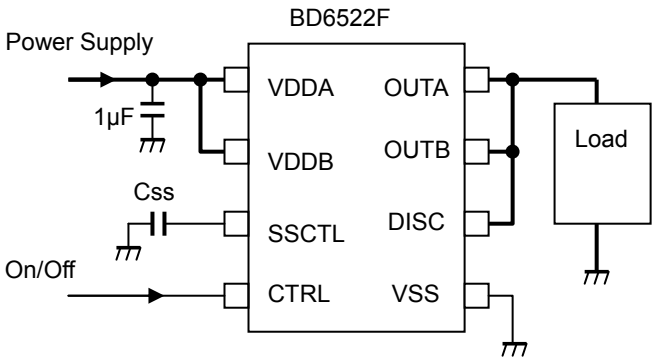


Fig.65 Power supply switch circuit (BD6522F)

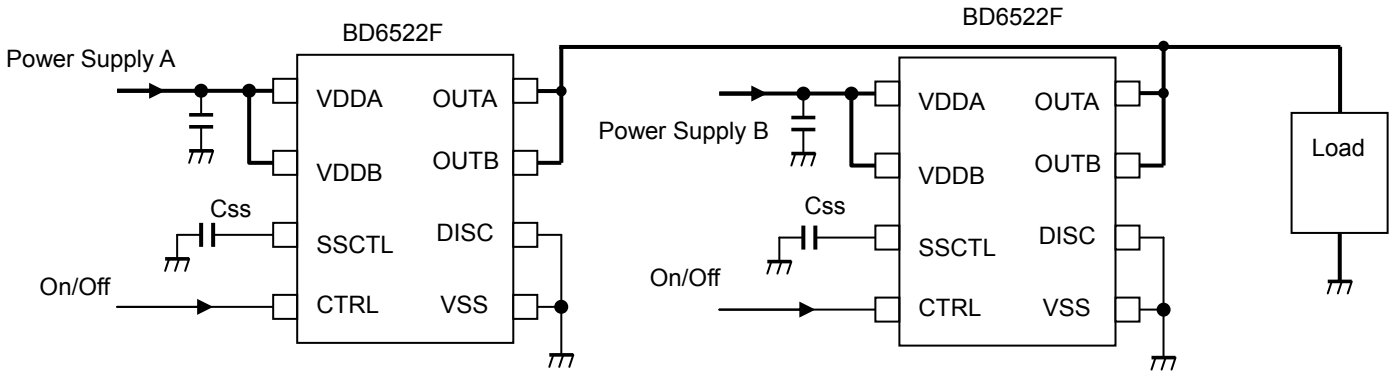


Fig.66 2 power supply changeover switch circuit (BD6522F)

●Thermal derating characteristic

(SOP8)

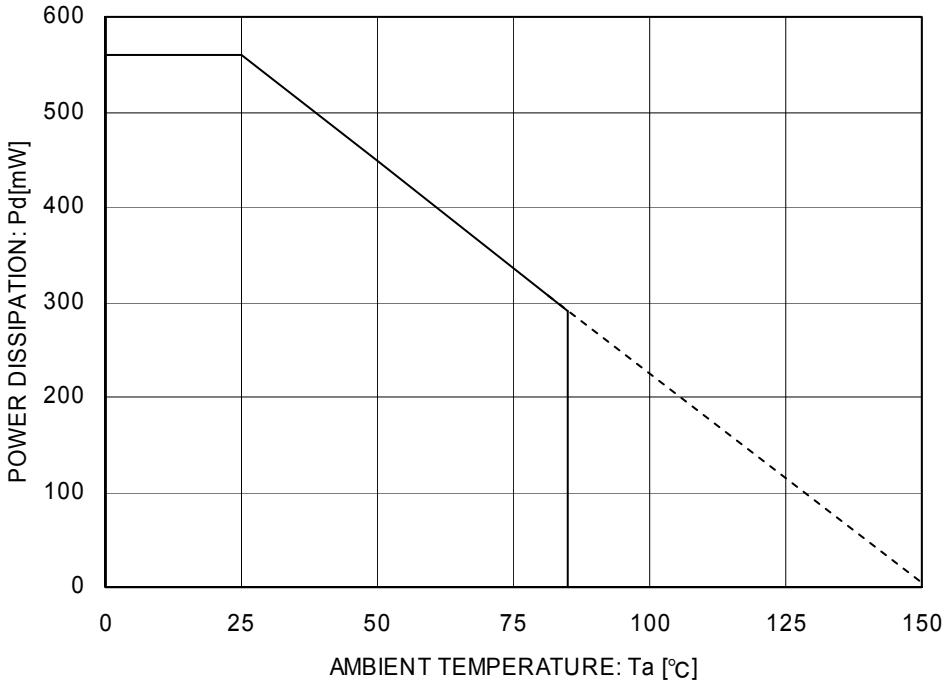


Fig. 67 Power dissipation curve

●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

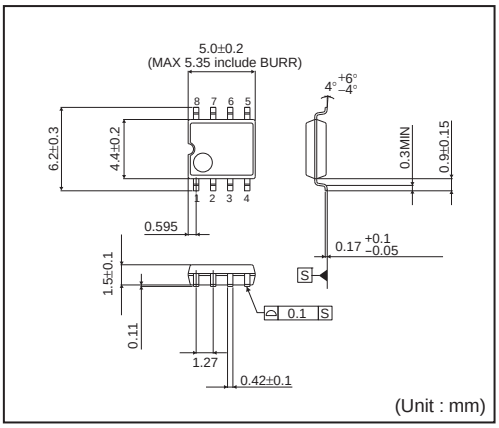
(12) Thermal shutdown circuit (TSD)
When junction temperatures become 135°C (typ.) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design
Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

●Ordering part number

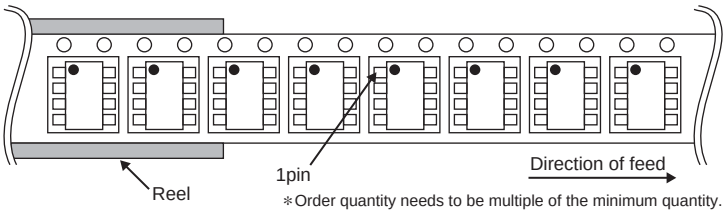
B	D		6	5	2	0		F	-	E	2
Part No.			Part No. 6520 6522					Package F: SOP8		Packaging and forming specification E2: Embossed tape and reel (SOP8)	

SOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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