

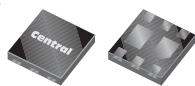
**CTLDM7003T-M563D**  
**SURFACE MOUNT**  
**DUAL, N-CHANNEL**  
**ENHANCEMENT-MODE**  
**SILICON MOSFETS**



[www.centralsemi.com](http://www.centralsemi.com)

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLDM7003T-M563D is a Dual N-channel MOSFET packaged in a space saving 1.6 x 1.6mm TLM™ surface mount package. This device is a TLM™ equivalent of the popular CMLDM7003T, SOT-563 device, featuring enhanced thermal characteristics, a package footprint compatible with standard SOT-563 mounting pad geometries, and a height profile of only 0.4mm.



Top View      Bottom View

**TLM563D CASE**

- Device is *Halogen Free* by design

**APPLICATIONS:**

- Load Power Switches
- DC/DC Converters
- Battery powered devices including Cell Phones, PDAs, Digital Cameras, MP3 Players, etc.

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage	$V_{DS}$	50	V
Drain-Gate Voltage	$V_{DG}$	50	V
Gate-Source Voltage	$V_{GS}$	12	V
Continuous Drain Current	$I_D$	280	mA
Maximum Pulsed Drain Current	$I_{DM}$	1.5	A
Power Dissipation (Note 1)	$P_D$	350	mW
Operating and Storage Junction Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
Thermal Resistance (Note 1)	$\Theta_{JA}$	357	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS PER TRANSISTOR:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=5.0\text{V}, V_{DS}=0$			50	nA
$I_{GSSF}, I_{GSSR}$	$V_{GS}=10\text{V}, V_{DS}=0$			0.5	$\mu\text{A}$
$I_{GSSF}, I_{GSSR}$	$V_{GS}=12\text{V}, V_{DS}=0$			1.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=50\text{V}, V_{GS}=0$			50	nA
$BV_{DSS}$	$V_{GS}=0, I_D=10\mu\text{A}$	50			V
$V_{GS(\text{th})}$	$V_{DS}=10\text{V}, I_D=250\mu\text{A}$	0.75		1.2	V
$V_{SD}$	$V_{GS}=0, I_S=115\text{mA}$			1.4	V
$r_{DS(\text{ON})}$	$V_{GS}=1.8\text{V}, I_D=50\text{mA}$		1.6	2.3	$\Omega$
$r_{DS(\text{ON})}$	$V_{GS}=2.5\text{V}, I_D=50\text{mA}$		1.3	1.9	$\Omega$
$r_{DS(\text{ON})}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		1.1	1.5	$\Omega$
$g_{FS}$	$V_{DS}=10\text{V}, I_D=200\text{mA}$	200			$\text{mS}$
$C_{rss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			5.0	pF
$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			50	pF
$C_{oss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			25	pF

Notes: (1) Mounted on 2 inch square FR4 PCB with copper mounting pad area of 1.8mm<sup>2</sup>.

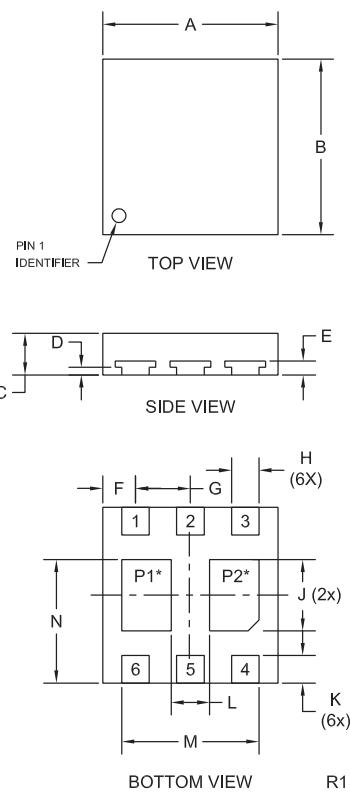
R1 (17-February 2010)

**CTLDLM7003T-M563D**

**SURFACE MOUNT  
DUAL, N-CHANNEL  
ENHANCEMENT-MODE  
SILICON MOSFETS**



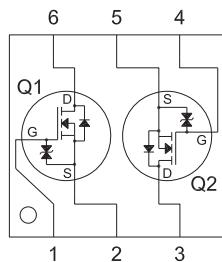
**TLM563D CASE - MECHANICAL OUTLINE**



\*Note:

- Exposed pad P1 common to pin 6.
- Exposed pad P2 common to pin 3.

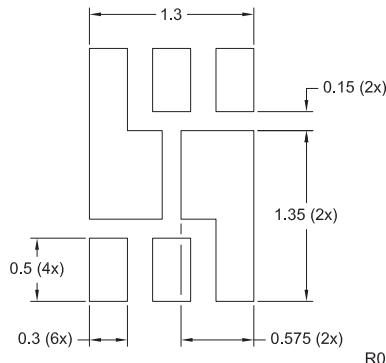
**PIN CONFIGURATION**



SYMBOL	DIMENSIONS		INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX
A	0.062	0.064	1.57	1.63		
B	0.062	0.064	1.57	1.63		
C	0.014	0.017	0.36	0.43		
D	0.002	0.004	0.04	0.10		
E	0.004	0.006	0.10	0.16		
F	0.011	0.013	0.27	0.33		
G	0.019	0.021	0.47	0.53		
H	0.009	0.011	0.22	0.28		
J	0.024	0.027	0.62	0.68		
K	0.009	0.011	0.22	0.28		
L	0.013	0.015	0.32	0.38		
M	0.048	0.050	1.22	1.28		
N	0.043	0.045	1.09	1.16		

TLM563D (REV:R1)

**SUGGESTED MOUNTING PADS**  
(Dimensions in mm)



**LEAD CODE:**

- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

**MARKING CODE: CJA**

R1 (17-February 2010)