# TDA9935

## Dual 14-bit, up to 80 Msample/s, 2 × Interpolating Digital-to-Analog Converter (DAC)

Rev. 01 — 14 December 2004 Objective data sheet

## 1. General description

The TDA9935 is optimized to reduce architecture complexity and overall system cost. Thanks to its direct IF conversion capabilities. It leads dynamic performances in multi-carrier support. With an internal sampling rate up to 160 Msample/s, TDA9935 is an extremely competitive solution for WCDMA, CDMA2000 and GSM/EDGE transmitters, as well as high data rate radio services as WLL, LMDS and BWA.

## 2. Features

- Dual 14-bit resolution
- SFDR = 82 dBc at 2.5 MHz
- Input data rate up to 80 Msample/s
- Two time interpolation filter
- Output data rate up to 160 Msample/s
- Single 3.3 V power supply
- Low noise cap free integrated PLL
- Low power dissipation
- HTQFP80 package
- Operating ambient temperature from –40 °C to +85 °C.

## 3. Applications

- Broadband wireless systems
- Digital radio links
- Cellular base stations
- Instrumentation.

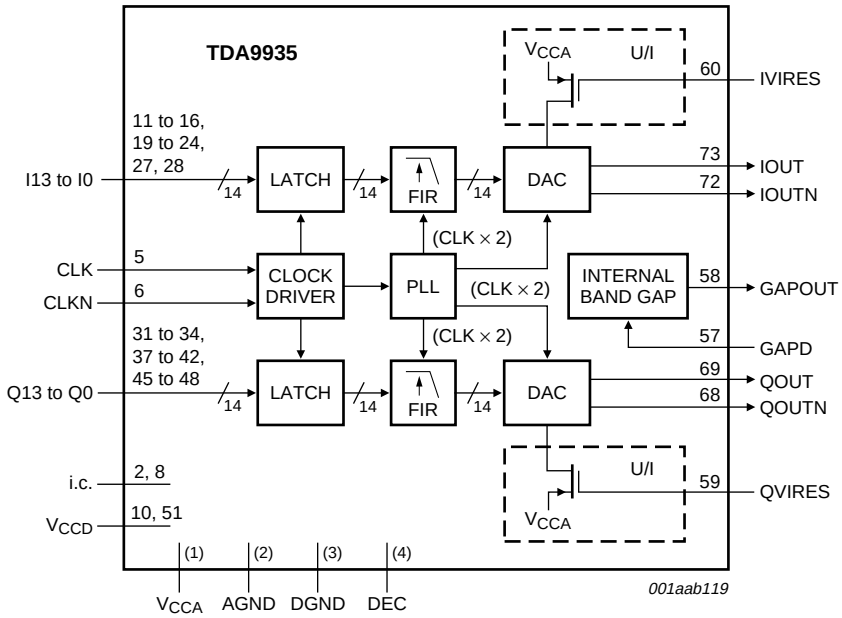
## 4. Ordering information

**Table 1: Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA9935HW | HTQFP80 | plastic thermal enhanced thin quad flat package; 80 leads; body 12 × 12 × 1 mm; exposed die pad | SOT841-1 |

PHILIPS

## 5. Block diagram




(1) Pins 1, 3, 61, 65, 76, 80.

(2) Pins 4, 7, 62, 64, 66, 67, 70, 71, 74, 75, 77, 79.

(3) Pins 9, 17, 25, 29, 30, 35, 44, 49, 50, 52, 53, 54, 55, 56.

(4) Pins 18, 26, 36, 43, 63, 78.

**Fig 1. Block diagram.**

# 6. Pinning information

## 6.1 Pinning

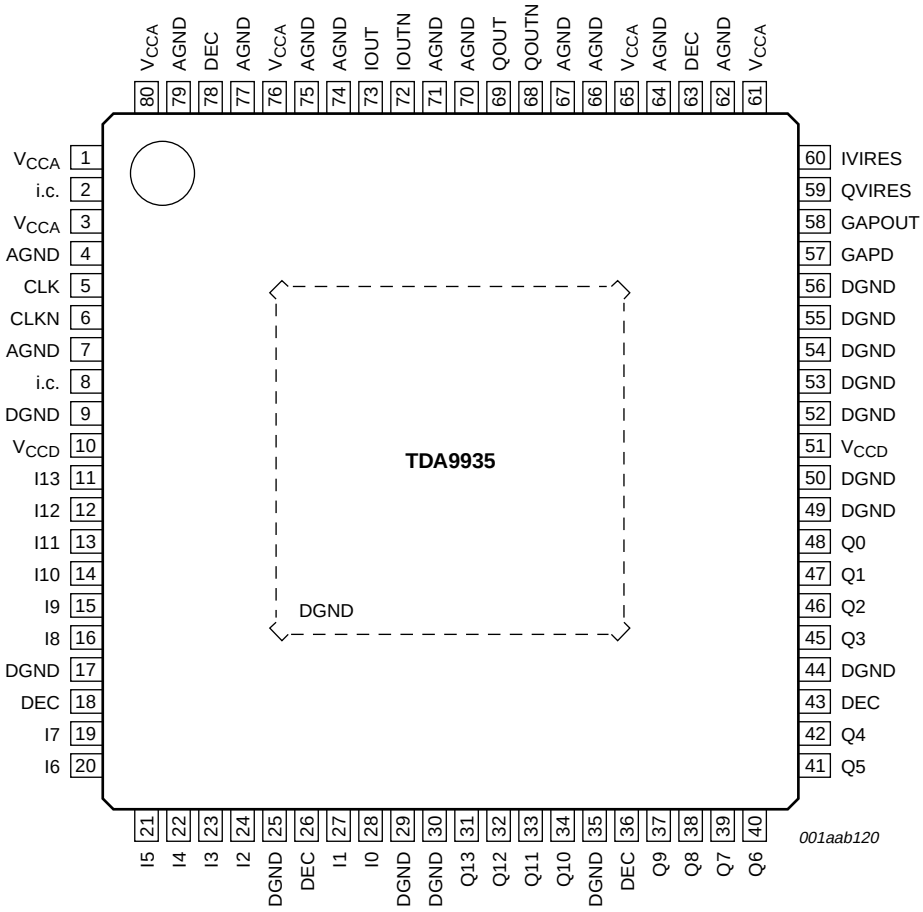



**Fig 2. Pin configuration.**

## 6.2 Pin description

**Table 2: Pin description**

| Symbol | Pin | Type [1] | Description |
|---|---|---|---|
| $V_{CCA}$ | 1 | S | analog supply voltage |
| i.c. | 2 | I/O | internally connected; leave open |
| $V_{CCA}$ | 3 | S | analog supply voltage |
| AGND | 4 | G | analog ground |
| CLK | 5 | I | clock input |
| CLKN | 6 | I | complementary clock input |
| AGND | 7 | G | analog ground |
| i.c. | 8 | O | internally connected; leave open |
| DGND | 9 | G | digital ground |

**Table 2: Pin description** *…continued*

| Symbol | Pin | Type [1] | Description |
|---|---|---|---|
| $V_{CCD}$ | 10 | S | digital supply voltage |
| I13 | 11 | I | I data input bit 13 (MSB) |
| I12 | 12 | I | I data input bit 12 |
| I11 | 13 | I | I data input bit 11 |
| I10 | 14 | I | I data input bit 10 |
| I9 | 15 | I | I data input bit 9 |
| I8 | 16 | I | I data input bit 8 |
| DGND | 17 | G | digital ground |
| DEC | 18 | O | decoupling node |
| I7 | 19 | I | I data input bit 7 |
| I6 | 20 | I | I data input bit 6 |
| I5 | 21 | I | I data input bit 5 |
| I4 | 22 | I | I data input bit 4 |
| I3 | 23 | I | I data input bit 3 |
| I2 | 24 | I | I data input bit 2 |
| DGND | 25 | G | digital ground |
| DEC | 26 | O | decoupling node |
| I1 | 27 | I | I data input bit 1 |
| I0 | 28 | I | I data input bit 0 (LSB) |
| DGND | 29 | G | digital ground |
| DGND | 30 | G | digital ground |
| Q13 | 31 | I | Q data input bit 13 (MSB) |
| Q12 | 32 | I | Q data input bit 12 |
| Q11 | 33 | I | Q data input bit 11 |
| Q10 | 34 | I | Q data input bit 10 |
| DGND | 35 | G | digital ground |
| DEC | 36 | O | decoupling node |
| Q9 | 37 | I | Q data input bit 9 |
| Q8 | 38 | I | Q data input bit 8 |
| Q7 | 39 | I | Q data input bit 7 |
| Q6 | 40 | I | Q data input bit 6 |
| Q5 | 41 | I | Q data input bit 5 |
| Q4 | 42 | I | Q data input bit 4 |
| DEC | 43 | O | decoupling node |
| DGND | 44 | G | digital ground |
| Q3 | 45 | I | Q data input bit 3 |
| Q2 | 46 | I | Q data input bit 2 |
| Q1 | 47 | I | Q data input bit 1 |
| Q0 | 48 | I | Q data input bit 0 |
| DGND | 49 | G | digital ground |
| DGND | 50 | G | digital ground |

**Table 2: Pin description** *…continued*

| Symbol | Pin | Type [1] | Description |
|---|---|---|---|
| $V_{CCD}$ | 51 | S | digital supply voltage |
| DGND | 52 | G | digital ground |
| DGND | 53 | G | digital ground |
| DGND | 54 | G | digital ground |
| DGND | 55 | G | digital ground |
| DGND | 56 | G | digital ground |
| GAPD | 57 | I | internal band gap power disable input |
| GAPOUT | 58 | O | band gap output voltage |
| QVIRES | 59 | I | Q DAC biasing resistor |
| IVIRES | 60 | I | I DAC biasing resistor |
| $V_{CCA}$ | 61 | S | analog supply voltage |
| AGND | 62 | G | analog ground |
| DEC | 63 | O | decoupling node |
| AGND | 64 | G | analog ground |
| $V_{CCA}$ | 65 | S | analog supply voltage |
| AGND | 66 | G | analog ground |
| AGND | 67 | G | analog ground |
| QOUTN | 68 | O | complementary Q DAC output current |
| QOUT | 69 | O | Q DAC output current |
| AGND | 70 | G | analog ground |
| AGND | 71 | G | analog ground |
| IOUTN | 72 | O | complementary I DAC output current |
| IOUT | 73 | O | I DAC output current |
| AGND | 74 | G | analog ground |
| AGND | 75 | G | analog ground |
| $V_{CCA}$ | 76 | S | analog supply voltage |
| AGND | 77 | G | analog ground |
| DEC | 78 | O | decoupling node |
| AGND | 79 | G | analog ground |
| $V_{CCA}$ | 80 | S | analog supply voltage |

[1] Type description:
S: Supply;
G: Ground;
I: Input;
O: Output.

# 7. Functional description

The DAC is a segmented architecture composed of a 7-bit thermometer sub-DAC, and the remaining 7-bit in a binary weighted sub-DAC.

The device produces two complementary current outputs on both channels, respectively pins IOUT/IOUTN and QOUT/QOUTN which need to be connected via a load resistor to the ground.

Figure 3 shows the equivalent analog output circuit of one DAC, which consists of a parallel combination of PMOS current sources and associated switches for each segment.

The cascode source configuration enables to increase the output impedance of the source and set to improve the dynamic performance of the DAC by introducing less distortion.

Figure 4 shows the internal reference configuration. In this case the bias current is given by the output of the internal regulator connected to the inverting input of the internal operational amplifiers, while external resistor $R_I$ and $R_Q$ are connected respectively to pins IVIRES and QVIRES. Thus the output current of the two DACs is typically fixed to 20 mA with an appropriate choice of these resistors. This configuration is optimum for temperature drift compensation because the band gap can be matched with the voltage on the feedback resistances.

The relation between $I_{FSOUT}$ and the $R_I$ ($R_Q$) is:

$$R_I = \frac{2048 \times V_{GAPOUT}}{82 \times I_{FSOUT}}$$

The output current can also be adjusted by imposing an external reference voltage to the inverting input pin GAPOUT and disabling the internal band gap with pin GAPD, sets to HIGH. With lower voltage than 1.2 V the current can be set at lower values than 20 mA. The input references at pins IVIRES and QVIRES may also be driven by separated reference voltages to adjust independently the two DAC currents.

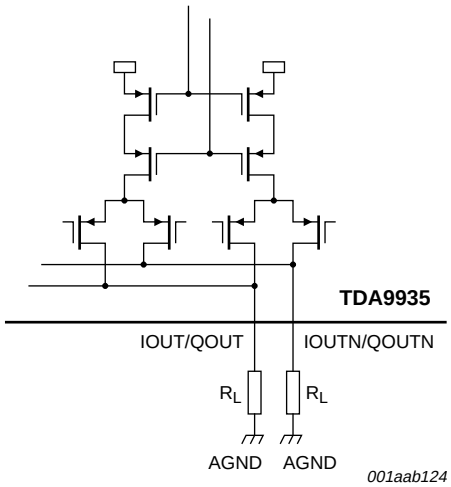



**Fig 3. Equivalent analog output circuit.**

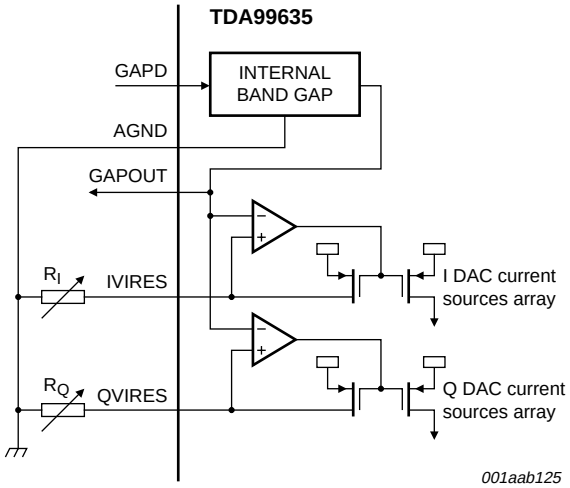



**Fig 4. Internal reference configuration.**

# 8. Limiting values

**Table 3: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCD}$ | digital supply voltage | | [1] | –0.3 | +3.9 | V |
| $V_{CCA}$ | analog supply voltage | | [1] | –0.3 | +3.9 | V |
| $\Delta V_{CCA-CCD}$ | supply voltage difference between the analog and digital supply voltages | | | –150 | +150 | mV |
| $V_I$ | voltage at input pins | pins Qn and In referenced to DGND | | –0.3 | $V_{CCD}$ + 0.3 | V |
| | | pins IVIRES, QVIRES and GAPD referenced to AGND | | –0.3 | $V_{CCA}$ + 0.3 | V |
| | | pins CLK and CLKN referenced to AGND | | –0.3 | $V_{CCA}$ + 0.3 | V |
| $V_O$ | voltage at output pins | pins IOUT, IOUTN, QOUT and QOUTN referenced to AGND | | –0.3 | $V_{CCA}$ + 0.3 | V |
| $T_{stg}$ | storage temperature | | | –55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | | –40 | +85 | °C |
| $T_j$ | junction temperature | | | - | 125 | °C |

[1] All supplies are connected together.

# 9. Thermal characteristics

**Table 4: Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 27.1 | K/W |
| $R_{th(c-a)}$ | thermal resistance from case to ambient | in free air | 11.8 | K/W |

# 10. Characteristics

**Table 5: Characteristics**

*$V_{CCD}$ = $V_{CCA}$ = 3.0 V to 3.6 V; AGND and DGND connected together; $T_{amb}$ = –40 °C to +85 °C; typical values measured at $V_{CCD}$ = $V_{CCA}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCD}$ | digital supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{CCA}$ | analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{CCD}$ | analog supply current | | - | 80 | - | mA |
| $I_{CCA}$ | digital supply current | | - | 50 | - | mA |
| $P_{tot}$ | total power dissipation | $f_{CLK}$ = 80 Msample/s; $f_{IOUT}$ = $f_{QOUT}$ = 2 MHz | - | 430 | - | mW |

**Table 5: Characteristics** *...continued*

*$V_{CCD}$ = $V_{CCA}$ = 3.0 V to 3.6 V; AGND and DGND connected together; $T_{amb}$ = −40 °C to +85 °C; typical values measured at $V_{CCD}$ = $V_{CCA}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Clock inputs (CLK and CLKN)** | | | | | | | |
| $V_{I(CM)}$ | common mode input voltage | | | - | 1.65 | - | V |
| $\Delta V_{CLK}$ | differential input voltage swing | | | - | 0.8 | - | V |
| **Analog outputs (IOUT, IOUTN, QOUT and QOUTN)** | | | | | | | |
| $I_{O(FS)}$ | full-scale output current | differential outputs | | 4 | - | 20 | mA |
| $R_o$ | output resistance | | [1] | - | 150 | - | kΩ |
| $C_o$ | output capacitance | | [1] | - | 3 | - | pF |
| **Digital inputs (I0 to I13, Q0 to Q13 and GAPD)** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | DGND | - | $0.3V_{CCD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{CCD}$ | - | $V_{CCD}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = $0.3V_{CCD}$ | | - | 5 | - | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $0.7V_{CCD}$ | | - | 5 | - | µA |
| **Reference Voltage output (GAPOUT)** | | | | | | | |
| $V_{GAPOUT}$ | output voltage | | | - | 1.25 | - | V |
| $I_{GAPOUT}$ | output current | external voltage | | - | 1 | - | µA |
| $\Delta V_{GAPOUT}$ | output voltage drift | | | - | ±90 | - | ppm/°C |
| **Clock timing inputs (CLK and CLKN)** | | | | | | | |
| $f_{CLK(max)}$ | maximum clock rate | | | 80 | - | - | Msample/s |
| $t_{W(CLKH)}$ | clock HIGH pulse width | | | 5 | - | - | ns |
| $t_{W(CLKL)}$ | clock LOW pulse width | | | 5 | - | - | ns |
| **Timing input (I0 to I13 and Q0 to Q13); see Figure 5** | | | | | | | |
| $t_{h(i)}$ | input hold time | | | 0.5 | - | 3 | ns |
| $t_{su(i)}$ | input setup time | | | −2.5 | - | 0 | ns |
| **Digital filter specification (FIR); see Figure 6, Figure 7 and Table 7** | | | | | | | |
| N | order | | | - | 42 | - | |
| $f_{I(D)}$ | data input rate | | | 80 | - | - | Msample/s |
| $R_{PBW}$ | ripple in pass bandwidth | 0.005 dB attenuation | | - | 0.403 | - | $f_{data}/f_{CLK}$ |
| PBW | pass bandwidth | 3 dB attenuation | | - | 0.48 | - | $f_{data}/f_{CLK}$ |
| SBR | stop band rejection | $f_{data}/f_{CLK}$ = 0.6 to 1 | | - | 73 | - | dB |
| $t_{d(g)}$ | group delay | | | - | $11T_{CLK}$ | - | ns |
| **Analog signal processing** | | | | | | | |
| INL | integral non-linearity | | | - | ±4 | - | LSB |
| DNL | differential non-linearity | | | - | ±2 | - | LSB |
| $I_{n(o)}$ | output noise current | $I_{FSOUT}$ = 20 mA | | - | 120 | - | $\frac{pA}{\sqrt{Hz}}$ |
| $E_{offset(o)}$ | output offset error | relative to full scale | | - | ±0.5 | - | % |
| $E_G$ | gain error (spread from device to device) | | | −3 | - | +3 | %FS |

**Table 5: Characteristics** *...continued*

*$V_{CCD}$ = $V_{CCA}$ = 3.0 V to 3.6 V; AGND and DGND connected together; $T_{amb}$ = −40 °C to +85 °C; typical values measured at $V_{CCD}$ = $V_{CCA}$ = 3.3 V and $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $M_G$ | gain matching | | - | ±0.5 | - | %FS |
| SFDR | spurious free dynamic range | $f_{CLK}$ = 80 Msample/s; BW = Nyquist | | | | |
| | | $f_{OUT}$ = 2.5 MHz at 0 dBFS | - | 82 | - | dBc |
| | | $f_{OUT}$ = 5 MHz at 0 dBFS | - | 77 | - | dBc |
| | | $f_{OUT}$ = 13 MHz at 0 dBFS | - | 70 | - | dBc |
| | | $f_{OUT}$ = 19 MHz at 0 dBFS | - | 68 | - | dBc |
| | | $f_{OUT}$ = 19 MHz at −6 dBFS | - | 65 | - | dBc |
| H2 | second harmonic | $f_{OUT}$ = 5 MHz | - | 77 | - | dBc |
| H3 | third harmonic | $f_{OUT}$ = 5 MHz | - | 86 | - | dBc |
| IMD2 | second order two-tone intermodulation rejection | $f_{CLK}$ = 80 Msample/s; $f_{OUT1}$ = 10 MHz; $f_{OUT2}$ = 12 MHz; BW = Nyquist | - | 65 | - | dBc |
| IMD3 | third order two-tone intermodulation rejection | $f_{CLK}$ = 80 Msample/s | | | | |
| | | $f_{OUT1}$ = 10 MHz; $f_{OUT2}$ = 12 MHz | - | 88 | - | dBc |
| | | $f_{OUT1}$ = 19 MHz; $f_{OUT2}$ = 21 MHz | - | 85 | - | dBc |
| THD | total harmonic distortion | $f_{CLK}$ = 80 Msample/s; BW = Nyquist | | | | |
| | | $f_{OUT}$ = 2.5 MHz | - | 76 | - | dBc |
| | | $f_{OUT}$ = 5 MHz | 68 | 76 | - | dBc |
| NSD | noise spectral density | $f_{CLK}$ = 80 Msample/s | | | | |
| | | $f_{OUT}$ = 2.5 MHz | - | −156 | - | dBm/Hz |
| | | $f_{OUT}$ = 5 MHz | - | −156 | - | dBm/Hz |
| | | $f_{OUT}$ = 19 MHz | - | −153 | - | dBm/Hz |
| S/N | signal-to-noise ratio | $f_{CLK}$ = 80 Msample/s; BW = Nyquist | | | | |
| | | $f_{OUT}$ = 2.5 MHz | - | 78 | - | dBc |
| | | $f_{OUT}$ = 5 MHz | 70 | 78 | - | dBc |
| | | $f_{OUT}$ = 19 MHz | - | 76 | - | dBc |

[1] Guaranteed by design.

**Table 6: Band gap**

| Band gap disable (GAPD) | band gap input/output (GAPOUT) | internal band gap |
|---|---|---|
| 0 | output ($V_{GAPOUT}$ = 1.2 V) | enable |
| 1 | input | disable |

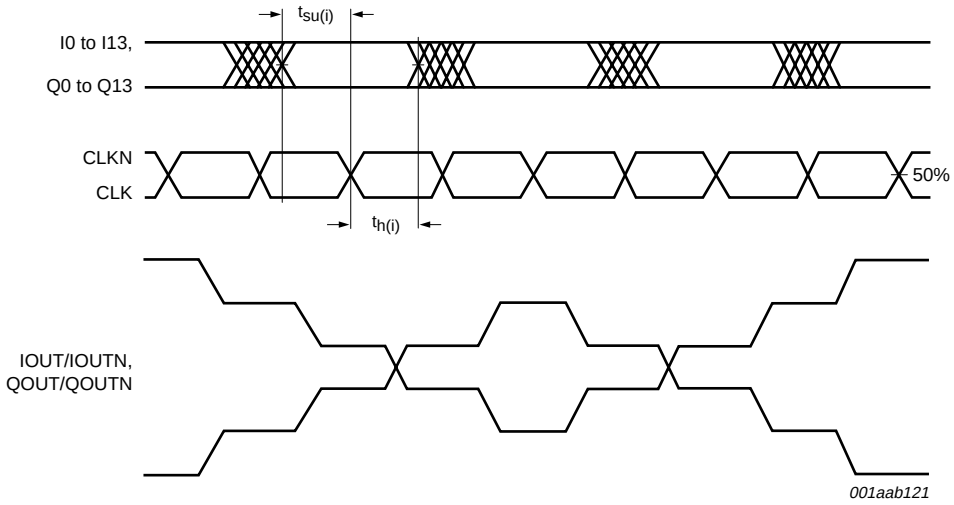



**Fig 5. Input timing diagram.**

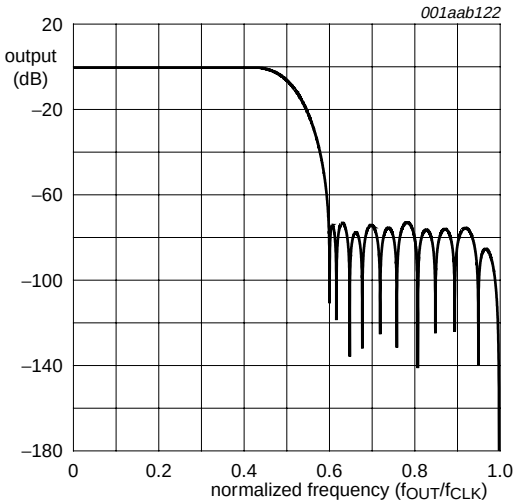



**Fig 6. FIR filter frequency response.**

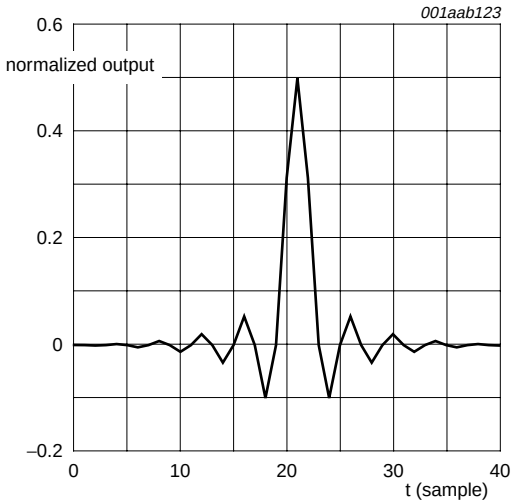



**Fig 7. FIR filter impulse response.**

**Table 7: Interpolation FIR filter coefficient**

| Coefficient | Coefficient | Value |
|---|---|---|
| H(1) | H(43) | 10 |
| H(2) | H(42) | 0 |
| H(3) | H(41) | –31 |
| H(4) | H(40) | 0 |
| H(5) | H(39) | 69 |
| H(6) | H(38) | 0 |
| H(7) | H(37) | –138 |
| H(8) | H(36) | 0 |
| H(9) | H(35) | 248 |

**Table 7: Interpolation FIR filter coefficient** *...continued*

| Coefficient | Coefficient | Value |
|---|---|---|
| H(10) | H(34) | 0 |
| H(11) | H(33) | –419 |
| H(12) | H(32) | 0 |
| H(13) | H(31) | 678 |
| H(14) | H(30) | 0 |
| H(15) | H(29) | –1083 |
| H(16) | H(28) | 0 |
| H(17) | H(27) | 1776 |
| H(18) | H(26) | 0 |
| H(19) | H(25) | –3282 |
| H(20) | H(24) | 0 |
| H(21) | H(23) | 10364 |
| H(22) | - | 16384 |

## 11. Application information

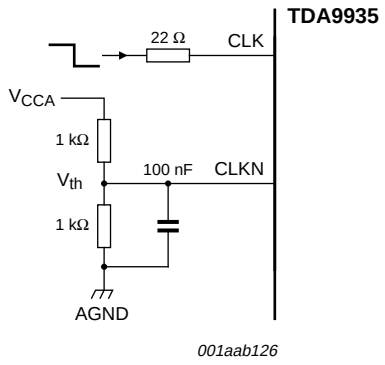



**Fig 8. Single-ended clock schematic.**

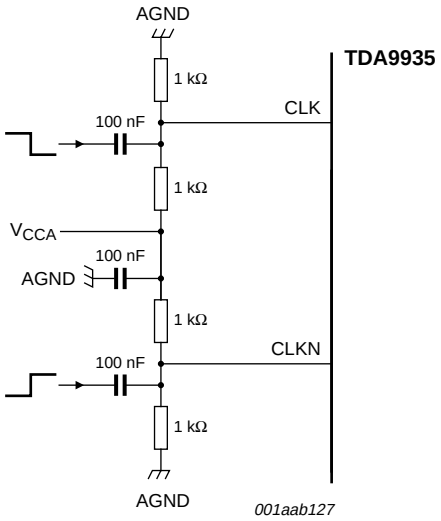
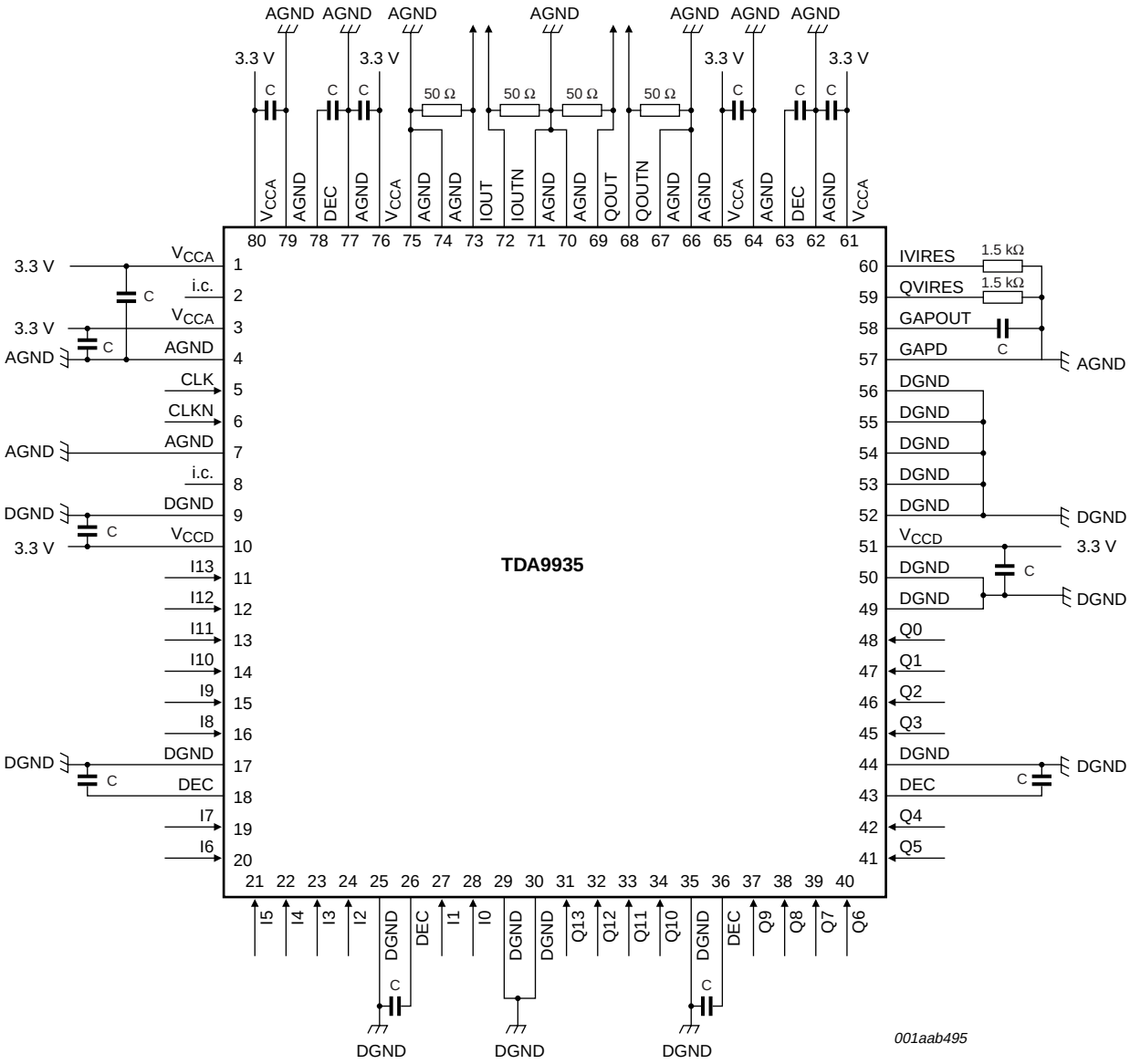



**Fig 9. Differential clock schematic.**



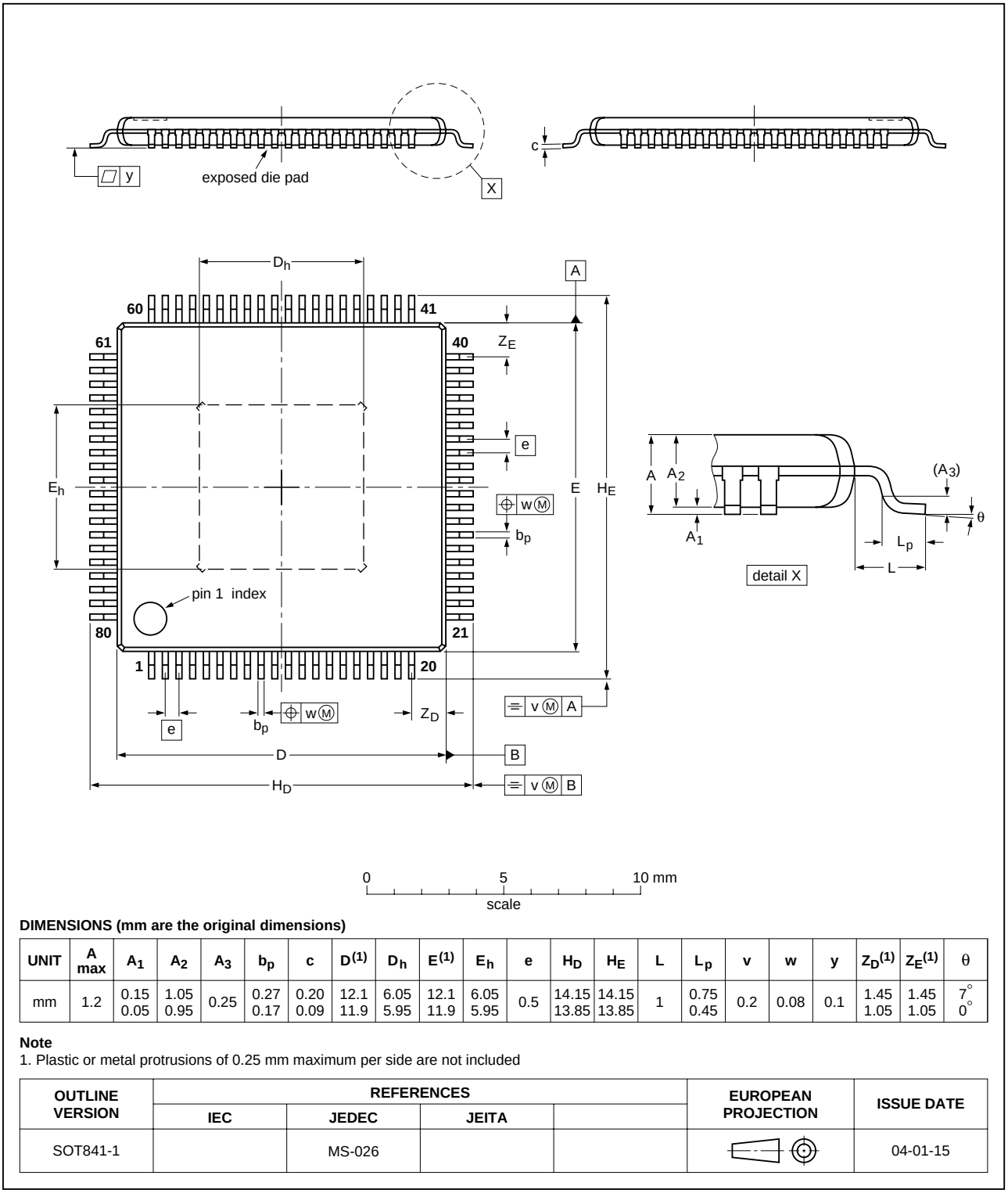

All resistors are 1 % precision resistors

C = 100 nF

**Fig 10. Application diagram.**

## 12. Package outline

**HTQFP80: plastic thermal enhanced thin quad flat package; 80 leads; body 12 x 12 x 1 mm; exposed die pad** **SOT841-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.95 | 0.25 | 0.27<br>0.17 | 0.20<br>0.09 | 12.1<br>11.9 | 6.05<br>5.95 | 12.1<br>11.9 | 6.05<br>5.95 | 0.5 | 14.15<br>13.85 | 14.15<br>13.85 | 1 | 0.75<br>0.45 | 0.2 | 0.08 | 0.1 | 1.45<br>1.05 | 1.45<br>1.05 | 7°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT841-1 | | MS-026 | | | | 04-01-15 |

**Fig 11. Package outline SOT841-1 (HTQFP80).**

# 13. Glossary

## 13.1 Static parameters

**DNL —** Differential Non-Linearity. The difference between the ideal and the measured output value between successive DAC codes.

**INL —** Integral Non-Linearity. The deviation of the transfer function from a best fit straight line (linear regression computation).

## 13.2 Dynamic parameters

**IMD2 —** Two-tone intermodulation rejection; second order. From a dual-tone digital input sinewave (these two frequencies are close together), the intermodulation distortion products IMD2 is the ratio of the RMS value of either tone to the RMS value of the worst 2nd order intermodulation product.

**IMD3 —** Two-tone intermodulation rejection; third order. From a dual-tone digital input sinewave (these two frequencies are close together), the intermodulation distortion products IMD3 is the ratio of the RMS value of either tone to the RMS value of the worst 3th order intermodulation product.

**SFDR —** Spurious Free Dynamic Range. The ratio between the RMS value of the reconstructed output sinewave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

**S/N —** Signal-to-Noise ratio. The ratio of the RMS value of the reconstructed output sinewave to the RMS value of the noise excluding the harmonics and the DC component.

**THD —** Total Harmonic Distortion. The ratio of the RMS value of the harmonics of the output frequency to the RMS value of the output sinewave. Usually, the calculation of THD is done on the first 5 harmonics.

## 14. Revision history

**Table 8: Revision history**

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|---|---|---|---|---|---|
| TDA9935_1 | 20041214 | Objective data | - | 9397 750 13346 | - |

## 15. Data sheet status

| Level | Data sheet status [1] | Product status [2] [3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 16. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

## 19. Contents





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