AN1366
APPLICATION NOTE

HOW TO USE THE ST92163 MICROCONTROLLER RESET

by Microcontroller Division Applications

INTRODUCTION

The ST92163 MCU can be reset in several ways. This application note explains the different reset mechanisms available on the ST92163, so you can make the best use of them when you design your application.

There are 3 available Reset sources that you can either use independently or in conjunction with each other, depending on your application.

Hardware Reset sources:

– An external $\overline{\text{RESET}}$ pin

– An internal Low Voltage Detector, or LVD on some devices

Software Reset source:

– Embedded watchdog activated by software

1 SELECTING WHICH RESET SOURCE TO USE

Operating Voltage Range

Both the external $\overline{\text{RESET}}$ pin and the watchdog Reset can be used over the whole ST92163 voltage range. The LVD function however, requires the MCU supply voltage to remain over 3.8V in its stable phase.

Low Power Modes

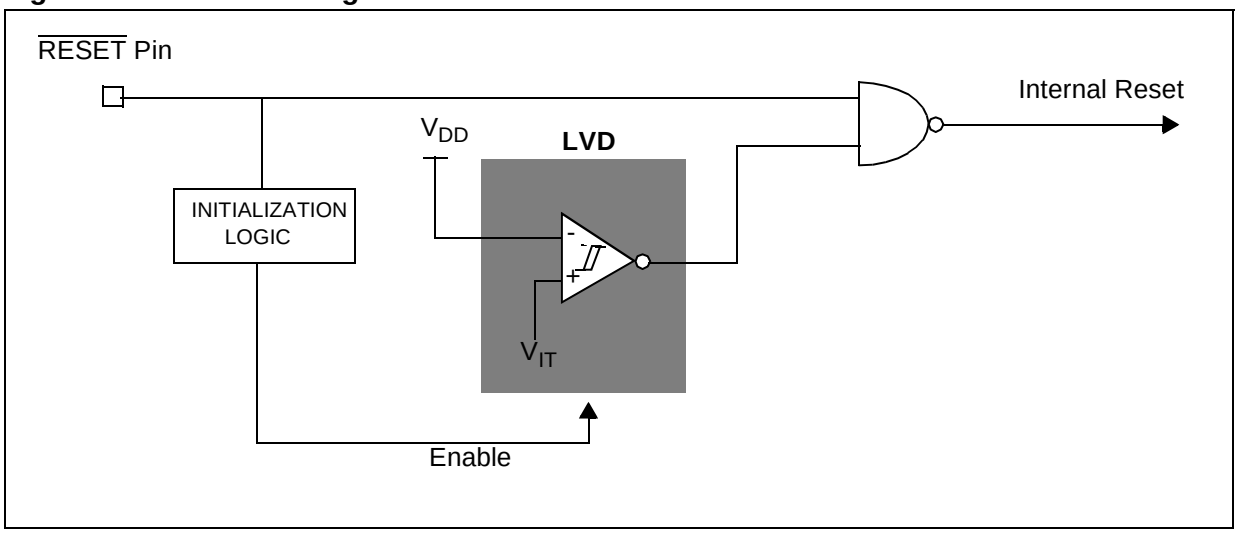
If you intend to use the watchdog to reset the micro, you should note that, once it is activated, the watchdog stays on permanently and cannot be deactivated (other than by a reset). While active, it prevents using any of the ST92163 low power modes (such as STOP mode or USB Suspend Mode).

2 USE OF THE LVD IN THE POWER UP PHASE

The LVD works in conjunction with the external $\overline{\text{RESET}}$ in the power-up phase. An external $\overline{\text{RESET}}$ pulse activates the initialization logic which activates the LVD. Then the LVD ensures the core does not start running before the MCU supply has reached a precise threshold. In other words, the LVD extends the internal Reset signal triggered by the external $\overline{\text{RESET}}$ pin

until the static voltage comparator of the LVD detects that the MCU supply has reached the V_{IT} threshold (see Figure 1).

Figure 1. LVD Block Diagram

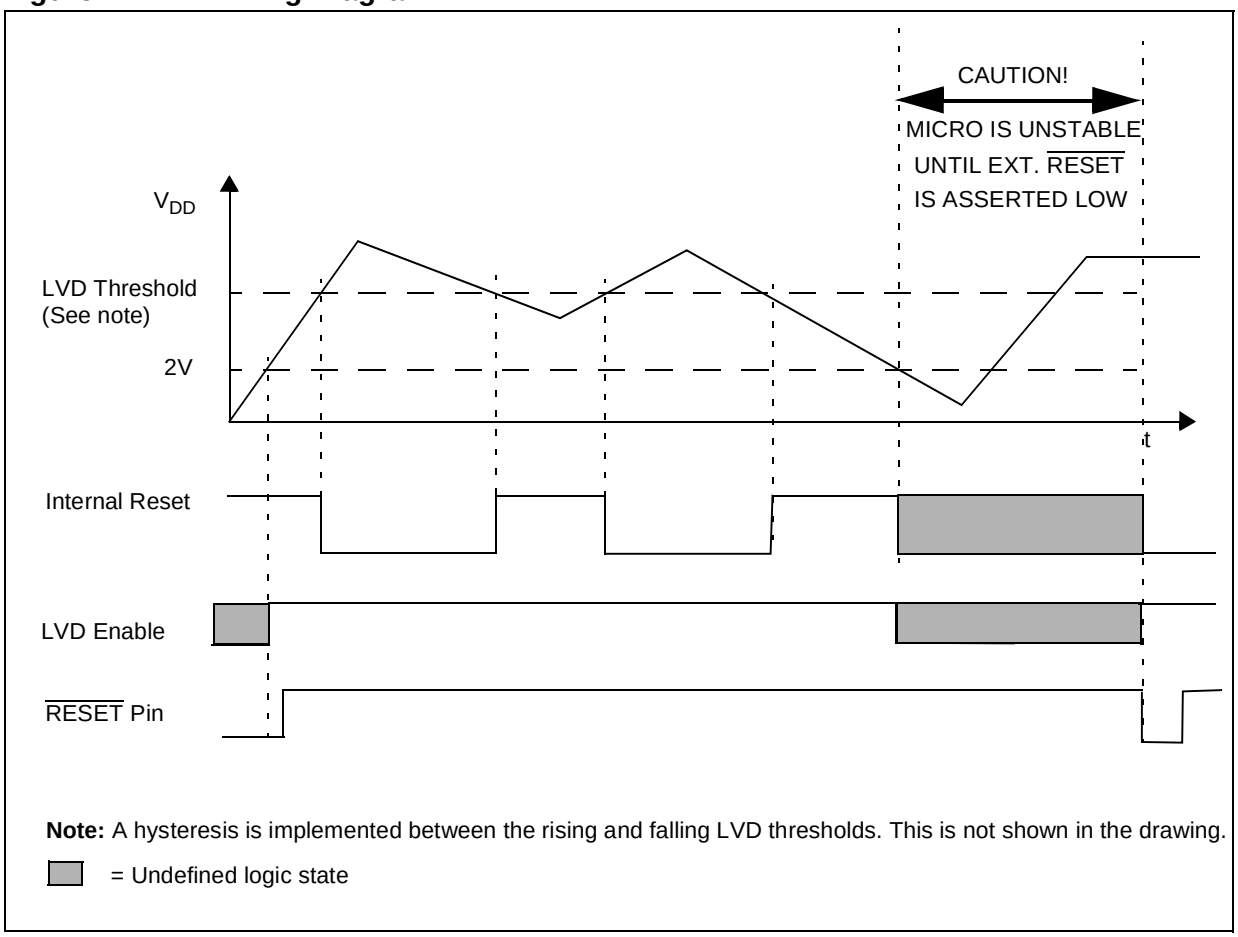


Based on a static voltage comparator, the LVD protects the microcontroller from any changes in the supply voltage, oscillations included, as long as the supply voltage does not fall below 2V. Below this voltage, the internal logic controlling the LVD is not guaranteed anymore (Shaded area in Figure 2). Therefore, it is required to externally keep the $\overline{\text{RESET}}$ pin at a low logic level when the MCU supply voltage is below 2V in order to safely use the LVD.

3 USE OF THE LVD IN THE POWER DOWN PHASE

When the MCU supply voltage drops, the LVD acts as brown-out detection circuit: As soon as the supply goes below a certain threshold, an internal Reset is generated. In the same way as in the power-up phase, the threshold detection is based on a static voltage comparator, and the Reset triggering does not depend on the falling speed.

Figure 2. LVD Timing Diagram



Note: A hysteresis is implemented between the rising and falling LVD thresholds. This is not shown in the drawing.

= Undefined logic state

4 EXTERNAL RESET CIRCUITS

There are several external Reset implementation schemes to choose from based on your application-specific parameters, such as the power supply behaviour. Whatever the solution chosen, the idea is to keep the $\overline{\text{RESET}}$ pin at a low logic level until the supply voltage has reached

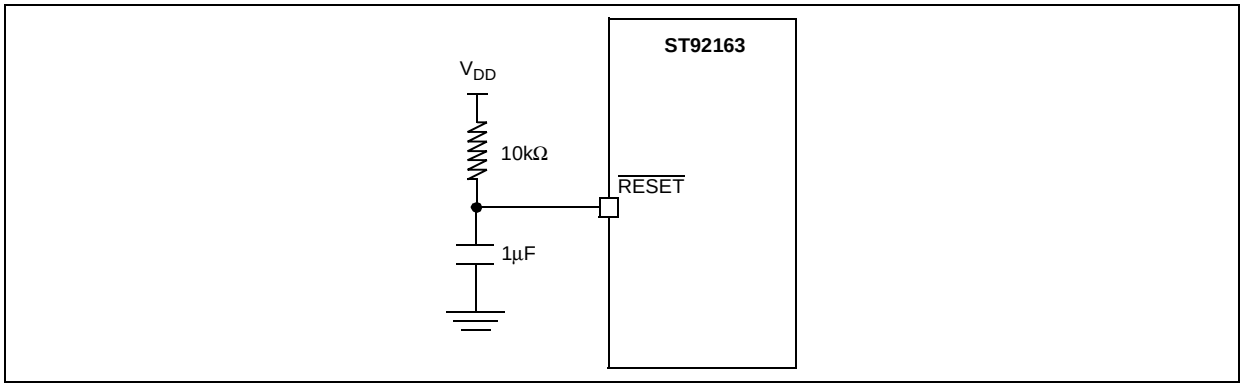
– 2V if the LVD is used, after which point the internal logic is guaranteed

– or 3V if the LVD is not used, in order to guarantee a safe start at 8 MHz. internal frequency.

4.1 DYNAMIC RESET CIRCUIT

This concept is the most cost-effective external Reset solution if the supply waveform is monotonous and the maximum rising time is known

Figure 3. Example of RC Circuit



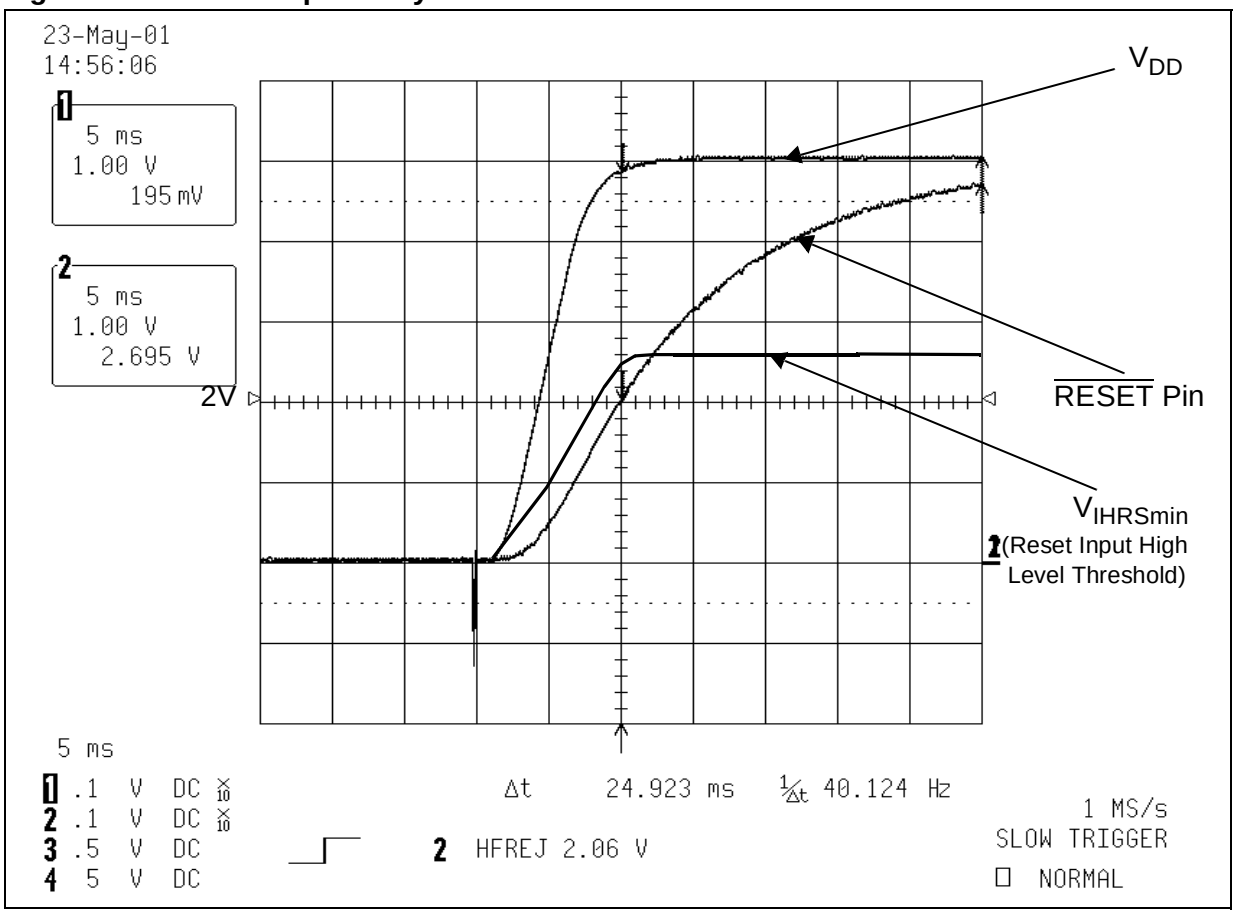
The principle is to let the $\overline{\text{RESET}}$ pin rise with the MCU supply after a delay. A safe design should allow the $\overline{\text{RESET}}$ pin to rise when the MCU supply has reached 2V if the LVD is used, or 3V if the LVD is not used.

The basic solution is to use an RC delay determined by the rise rate of the supply itself: A delay corresponding to 30% of the rise time is generally safe.

Due to statistical dispersion of the R and C values, the delay is not stable: Care must then be taken to ensure that the $\overline{\text{RESET}}$ pin rises while the supply voltage is between 2V if the LVD is used, or 3V if the LVD is not used (Internal logic guaranteed) and the minimum voltage required for the application in its stabilized phase (4.05V in case of a USB application).

See Figure 4.

Figure 4. Good Example of Dynamic Reset Circuit



Note also that this scheme requires a certain delay between a Power-Down and the next Power-Up, because the delay generator has to be reinitialized: In practice, capacitor C needs to be discharged.

This kind of scheme can be used in conjunction with the LVD. The delay holds down the external $\overline{\text{RESET}}$ pin, until the LVD takes over and releases the MCU core when the LVD threshold is reached.

4.2 EXTERNAL MCU POWER SUPPLY MONITOR

This solution is necessary if the power supply oscillates during power on, or if the power rise time is unspecified. There are two reasons for this:

– Firstly, the RC delay will be insufficient if it is too small compared to the total rise time: The $\overline{\text{RESET}}$ pin rises before the MCU supply reaches 2V if the LVD is used, or 3V if the LVD is not used (See Figure 5).

– Secondly, the supply may drop momentarily (oscillate) below the minimum safe level (2V if the LVD is used, or 3V if the LVD is not used), with the $\overline{\text{RESET}}$ pin held high. As a conse-

quence, the internal logic is not guaranteed anymore, and the $\overline{\text{RESET}}$ pin cannot be seen at a Low logic level to ensure a safe restart. See Figure 6.

Note: The second case also applies to applications with short Power-Down/Up cycles.

Figure 5. Bad example of Power On Reset Circuit (delay insufficient)

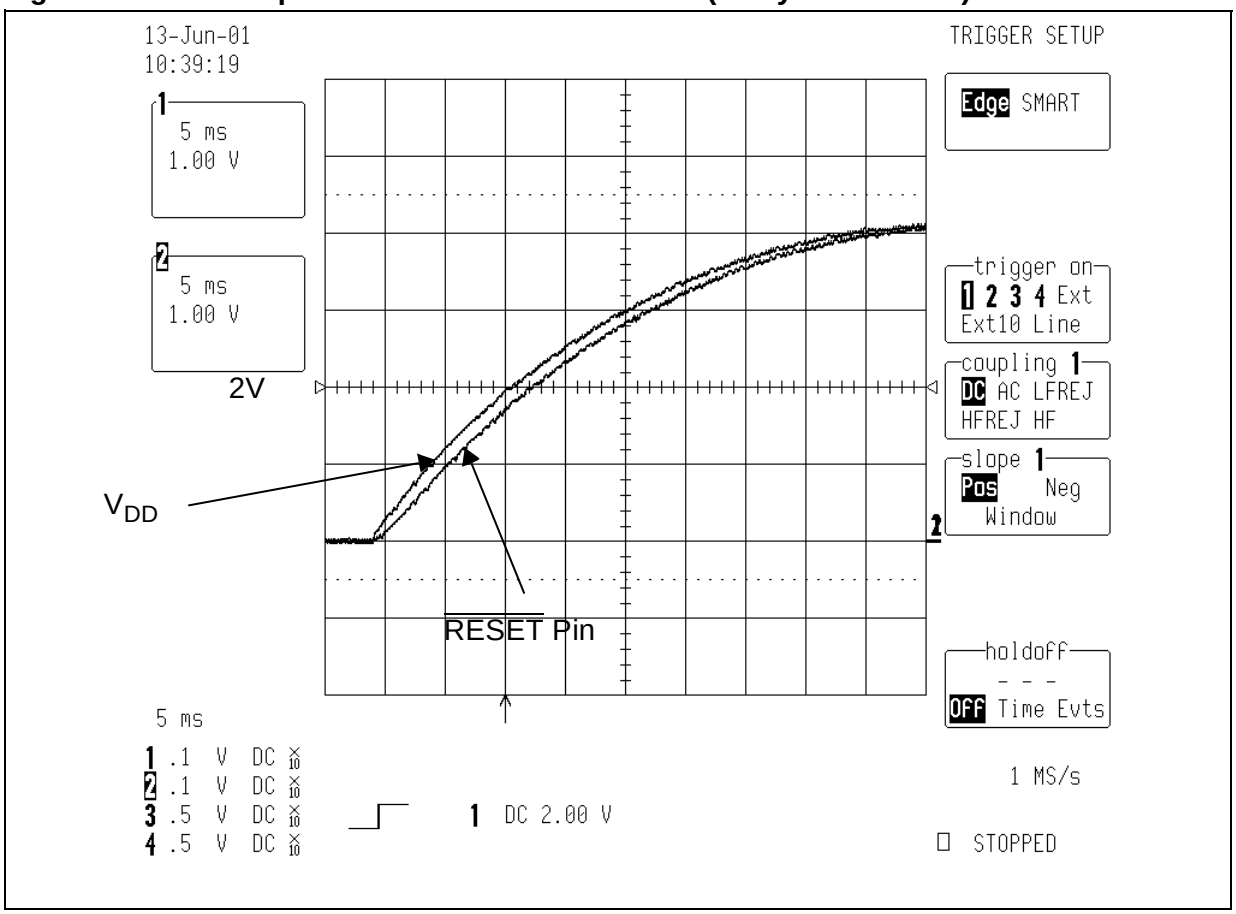
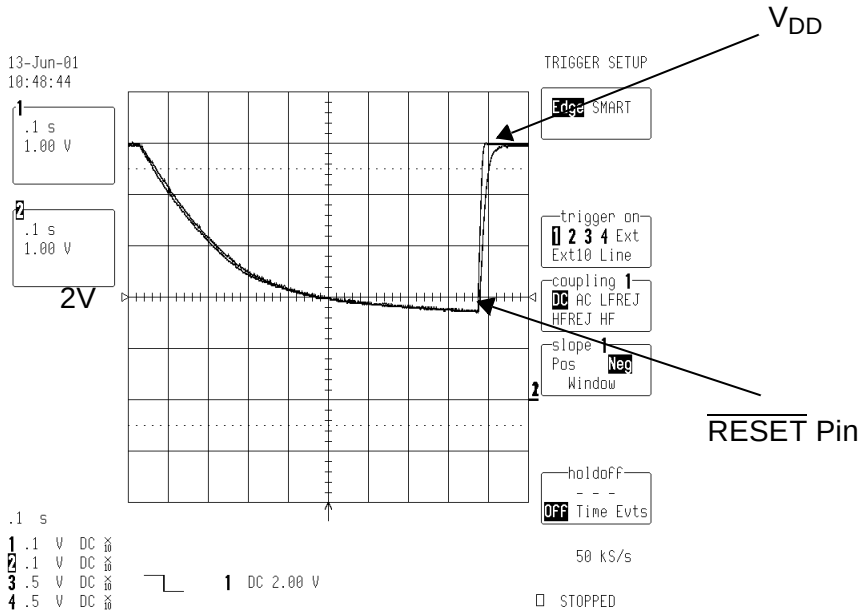


Figure 6. Waveform of Power Brown-Out with RC Circuit (Bad Example)



In this example Reset never goes logic low (under 0.2*V_{DD})

4.3 DEDICATED VOLTAGE MONITOR IC

This solution uses a stand-alone power supply monitor with Reset output. This kind of device is available from STMicroelectronics in the TS83x product family. It includes a precision voltage reference and a static comparator to issue a Reset at a precise threshold independently of how the supply level changes. This solution allows you to get a precise and safe Reset function in cases where the application constraints do not allow the use of the LVD of the ST92163.

4.4 BASIC VOLTAGE MONITOR PLUS LVD

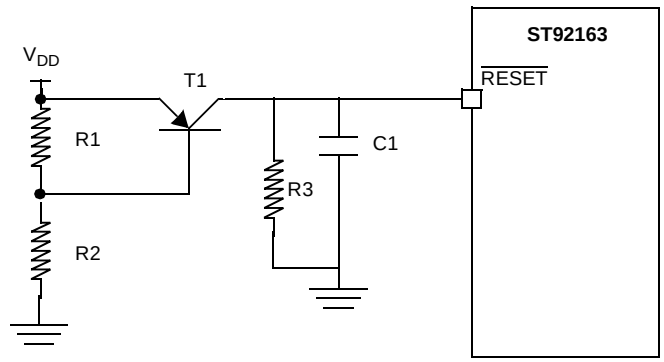
If the LVD is used, it is possible to obtain a more cost-effective solution. A coarse static voltage monitor is sufficient to ensure a Reset between 2V and the LVD threshold. Independently of the variations on the external monitor threshold, the LVD fixes a precise voltage where the internal Reset is released.

An implementation example is given below.

4.4.1 SCHEMATIC

This circuitry is composed of 1 PNP transistor, 3 resistors and 1 capacitor (see Figure 7).

Figure 7. Suggested Power On Reset Circuitry for use with the LVD



R1 = 270 Kohms, +/- 2 %
R2 = 1 Mohms, +/- 2 %
R3 = 1 Mohms, +/- 5 %
C1 = 100 nF, accuracy not important
T1 = BC857, PNP transistor with:
h_{fe} gain approx. 100
V_{eb} = 0.55 v , min = 0.5 v, max = 0.6 v

4.4.2 STATIC BEHAVIOUR

The C1 capacitor is loaded by the T1 Ic current when $V_{DD} > V_{eb} \times (R2 + R1) / R1$ and the $\overline{\text{RESET}}$ pin is put at logical 1.

For this example: V_{DDth} = 2.60 v (min = 2.2 v ; max = 3.4 v)

After reset state, this circuitry is static and consumes about 10 µA max.

4.4.3 DYNAMIC BEHAVIOUR

As soon as $V_{DD} > V_{DDth}$, the capacitor is loaded with the current:

$Ic = hfe \times Ib = hfe \times [((V_{DD} - V_{eb}) / R2) - (V_{eb} / R1)]$.

Ic is about 300 µA (typical, constant if V_{DD} constant).

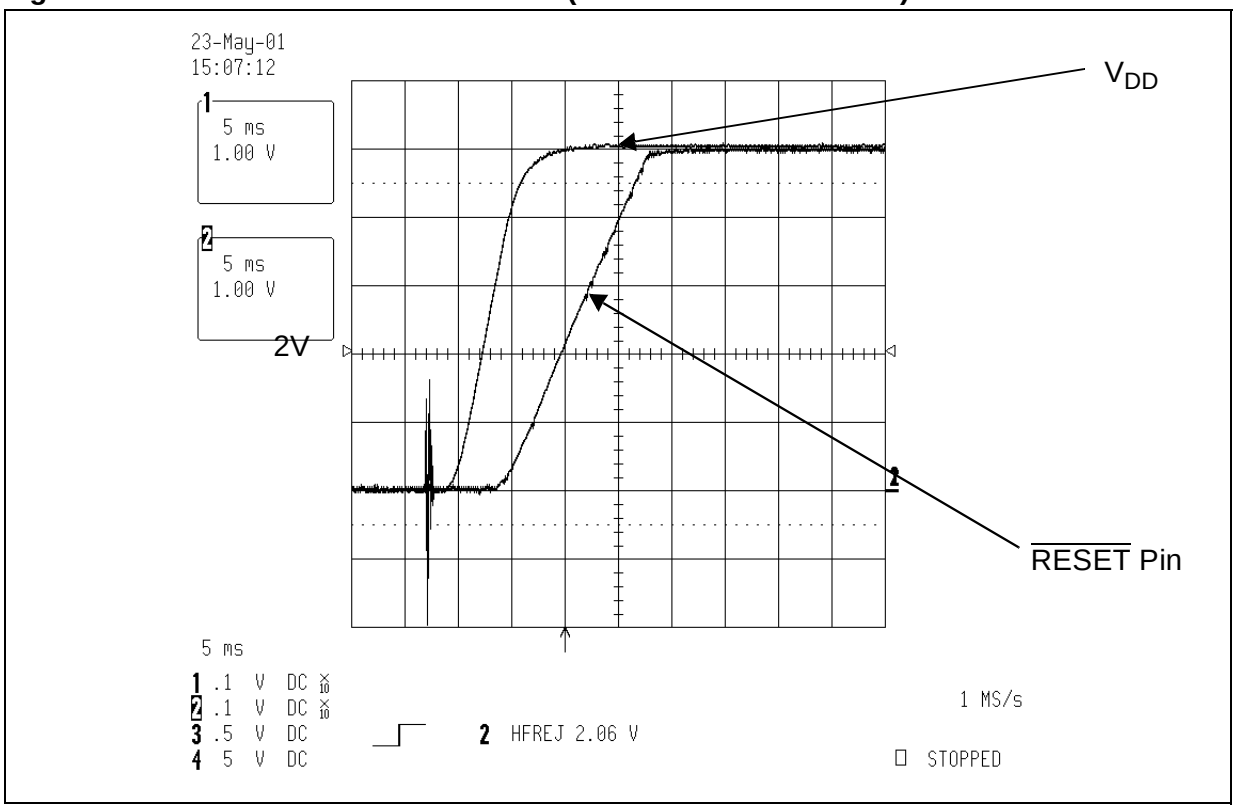
So the time to reach the Reset V_{IH} with V_{DD} = 5 v is:

$t_{reset} = (V_{IH} \times C1) / Ic$.

t_{reset} ~ 1 ms.

See Figure 8.

Figure 8. Waveform of Power ON Reset (with PNP Reset Circuit)

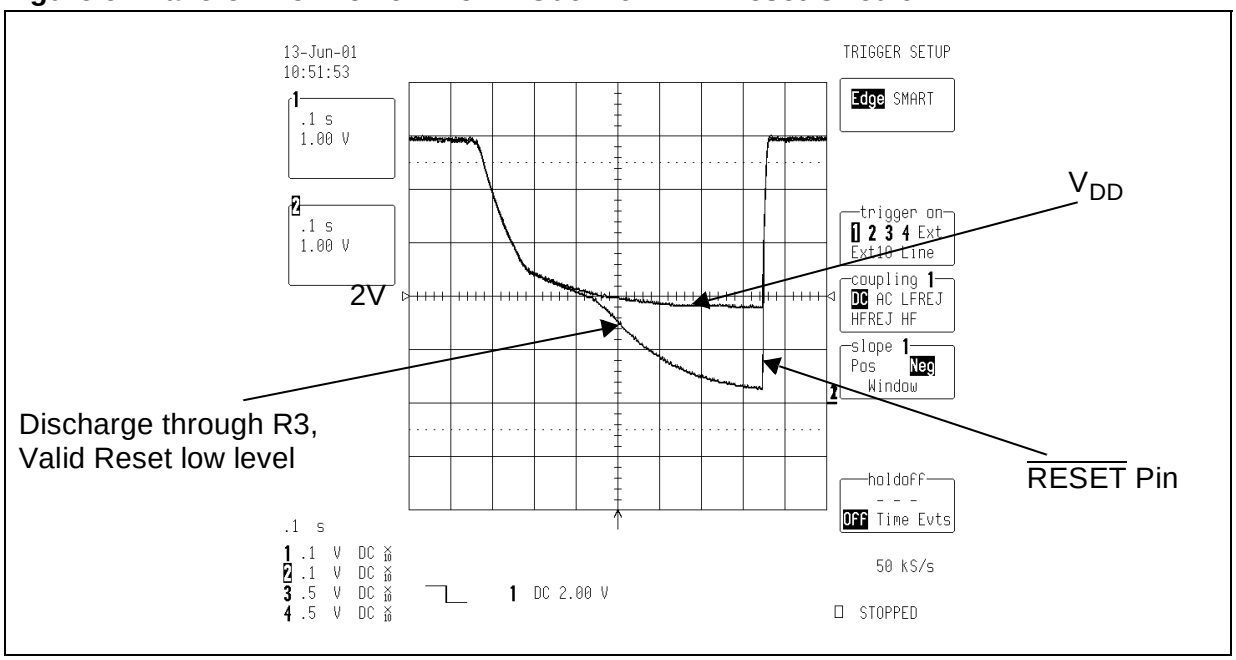


4.4.4 POWER DOWN

The C1 capacitor is discharged through both the internal protection diode of the $\overline{\text{RESET}}$ pin to the V_{DD}, R3 to the ground in order to be 100% discharged. This discharge is guaranteed slow enough by the V_{DD} capacitors and will cause no damage. For this reason, it is necessary to put a 4.7 µF capacitor on V_{DD} to have a maximum current in the diode about 1 mA. R3 allows to have V_{reset} below V_{DD} when V_{DD} is below 2.6V (V_{DDth}) to guarantee a Reset for a slow V_{DD} fall time and a power-up when V_{DD} is not yet at 0V.

See Figure 9.

Figure 9. Waveform of Power Brown-Out with PNP Reset Circuit



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