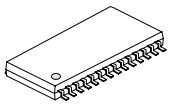
LS3718

CMOS IC

20-BIT SERIAL TO PARALLEL CONVERTER



SOP-28

*Pb-free plating product number: LS3718L

■ DESCRIPTION

The UTC **LS3718** is a 20-bit serial to parallel converter utilizing CMOS Technology. It is incorporates control circuit, shift register, latch and driver into a single ship. It is suitable for MCU interface. The effective interface assignment of MPU is available as the connection between UTC **LS3718** and MPU is required only 4 lines.

The device is designed to operate up to 5MHz. When the serial data input to the DATA terminal and the data is output from parallel output buffer through serial in parallel out shift register and parallel data latches.

The data can through the shift register serial output to the SO terminal. Therefore the **UTC LS3718** can cascade connection to expand the output data number.

The hysteresis input circuit realizes wide noise margin and the high drive-ability output buffer (25mA) can drive LED directly.

■ FEATURES

* 20-Bit serial in parallel out
* Cascade connection
* Operating voltage 5V±10%
* Hysteresis input 0.5V typ
* Output current 25mA
* Operating frequency 5MHz or more

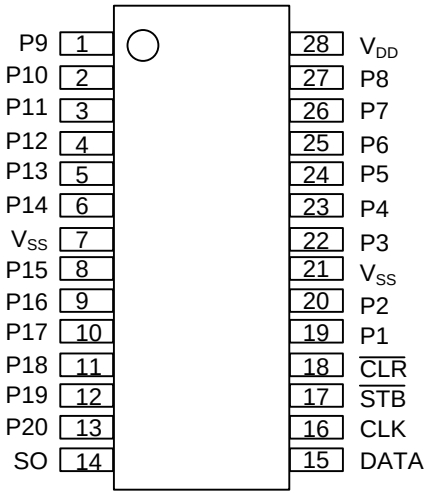
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
LS3718-S28-R	LS3718L-S28-R	SOP-28	Tape Reel
LS3718-S28-T	LS3718L-S28-T	SOP-28	Tube

LS3718L-S28-R
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) R: Tape Reel, T: Tube
(2) S28: SOP-28
(3) L: Lead Free Plating, Blank: Pb/Sn

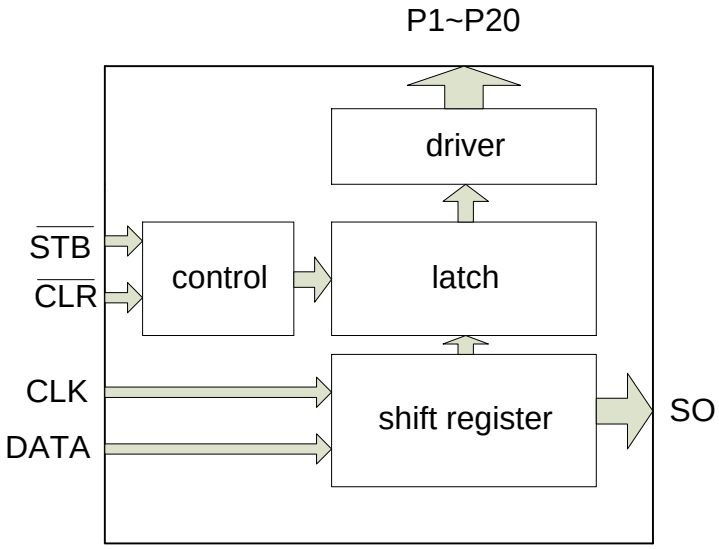
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	I/O	DESCRIPTION
1	P9	O	Parallel Data Output Pin 9
2	P10	O	Parallel Data Output Pin 10
3	P11	O	Parallel Data Output Pin 11
4	P12	O	Parallel Data Output Pin 12
5	P13	O	Parallel Data Output Pin 13
6	P14	O	Parallel Data Output Pin 14
7	V_{SS}		GND
8	P15	O	Parallel Data Output Pin 15
9	P16	O	Parallel Data Output Pin 16
10	P17	O	Parallel Data Output Pin 17
11	P18	O	Parallel Data Output Pin 18
12	P19	O	Parallel Data Output Pin 19
13	P20	O	Parallel Data Output Pin 20
14	SO	O	Serial Data Output Pin
15	DATA	I	Serial Data Input Pin
16	CLK	I	Clock Signal Input Pin
17	$\overline{STB}$	I	Data Strobe, Low Actived
18	$\overline{CLR}$	I	Data Reset, Low Actived
19	P1	O	Parallel Data Output Pin 1
20	P2	O	Parallel Data Output Pin 2
21	V_{SS}		GND
22	P3	O	Parallel Data Output Pin 3
23	P4	O	Parallel Data Output Pin 4
24	P5	O	Parallel Data Output Pin 5
25	P6	O	Parallel Data Output Pin 6
26	P7	O	Parallel Data Output Pin 7
27	P8	O	Parallel Data Output Pin 8
28	V_{DD}		Power Supply

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5~+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Output Current	I_{OUT}	±25	mA
Power Dissipation	P_D	500	mW
Junction Temperature	T_J	+125	℃
Operating Temperature	T_{OPR}	-25 ~ +85	℃
Storage Temperature	T_{STG}	-40 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (V_{DD}=4.5~5.5V, V_{SS}=0V, Ta=25℃)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Operating Voltage		V_{DD}			4.5		5.5	V
Operating Current		I_S	V_{IH}=V_{DD}, V_{IL}=V_{SS}				0.1	mA
Input Leakage Current		$I_{I(LEAK)}$	V_{IN}=0~V_{DD}		-10		10	μA
Input Voltage	High-Level	V_{IH}			0.7V_{DD}		V_{DD}	V
	Low-Level	V_{IL}			V_{SS}		0.3 V_{DD}	
Output Voltage	High-Level	V_{OH}	I_{OH}=-0.4mA	SO Terminal	4.0	4.97	V_{DD}	V
	Low-Level	V_{OL}	I_{OL}=+3.2mA		V_{SS}	0.11	0.4	
Output Voltage	High-Level	V_{OHP}	I_{OH}=-25mA	P1~P20 Terminals (Note)	V_{DD}-1.5	V_{DD}-0.5	V_{DD}	V
			I_{OH}=-15mA		V_{DD}-1.0	V_{DD}-0.3	V_{DD}	
			I_{OH}=-10mA		V_{DD}-0.5	V_{DD}-0.2	V_{DD}	
	Low-Level	V_{OLP}	I_{OL}=+25mA		V_{SS}	0.5	1.5	V
			I_{OL}=+15mA		V_{SS}	0.3	0.8	
			I_{OL}=+10mA		V_{SS}	0.2	0.4	

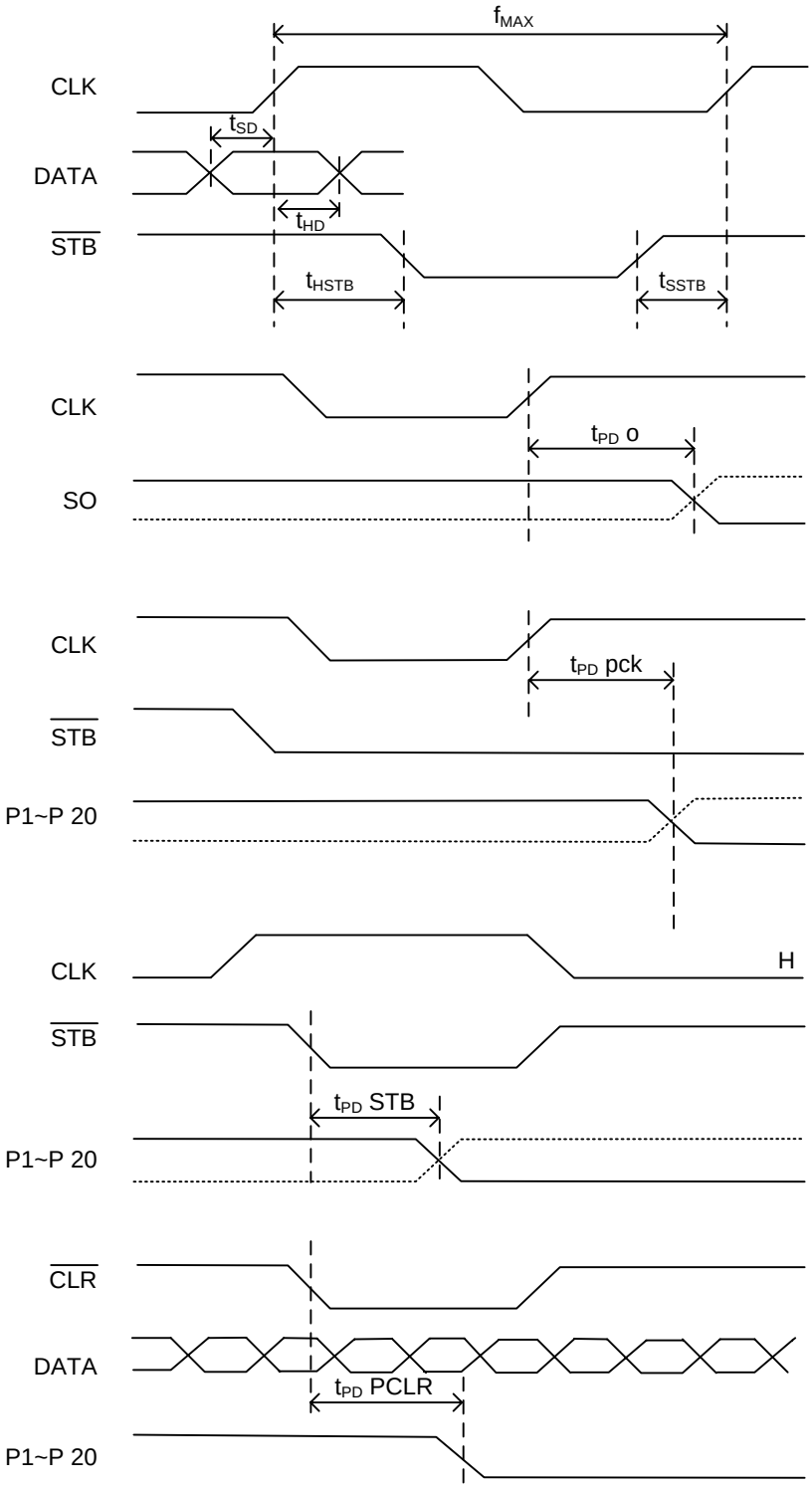
Note: Specified value represent output current per pin. When use, total current consideration and less than power dissipation rating operation should be required.

■ SWITCHING CHARACTERISTICS (V_{DD}=4.5~5.5V, V_{SS}=0V, Ta=-20~75℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data Set-up Time	t_{SD}	DATA-CLK	20			ns
Data Hold Time	t_{HD}	CLK-DATA	20			ns
Set-up Time	t_{SSTB}	$\overline{STB}$-CLK	30			ns
Hold Time	t_{HSTB}	CLK-$\overline{STB}$	30			ns
Output Delay Time	t_{PD} O	CLK-SO			70	ns
	t_{PD} PCK	CLK-P1~P20			100	ns
	t_{PD} PSTB	$\overline{STB}$-P1~P2			80	ns
	t_{PD} PCLR	$\overline{CLR}$-P1~P20			80	ns
Max. Operating Frequency	f_{MAX}		5			MHz

Note: C_{OUT}=50pF

■ SWITCHING CHARACTERISTICS TEST WAVEFORM



■ FUNCTION DESCRIPTION

RESET

When the $\overline{CLR}$ terminal is "L" level, all latches are reset and all of parallel output are "L" level.
Normally, the $\overline{CLR}$ terminal should be "H" level.

DATA TRANSMISSION

When the $\overline{STB}$ terminal is "H" level and input the clock signal to the CLK terminal, the serial data input the DATA terminal and shift in the shift register by synchronizing at rising edge of the clock signal.
When the $\overline{STB}$ terminal is changed to "L" level, the data in the shift register are transferred to the latch.
Even if the $\overline{STB}$ terminal is "L" level, the input clock signal shift the data in the shift register, therefore, the clock signal controlled is needed.

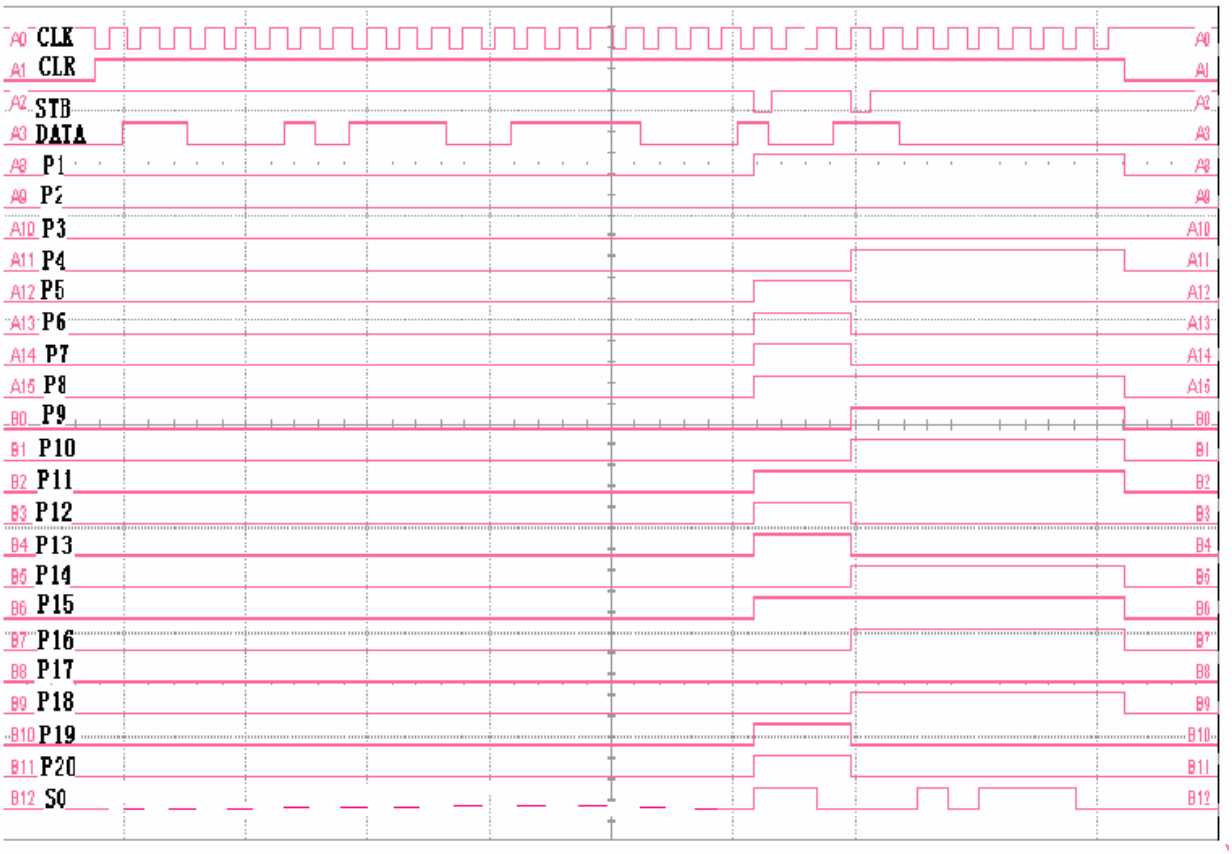
CASCADE CONNECTION

The serial data input from DATA terminal and output from the SO terminal through internal shift register unrelated to the $\overline{CLR}$ and $\overline{STB}$ status.
Furthermore, the 4 input terminals have a hysteresis characteristic by using the schmitt trigger structure to decrease the noise.

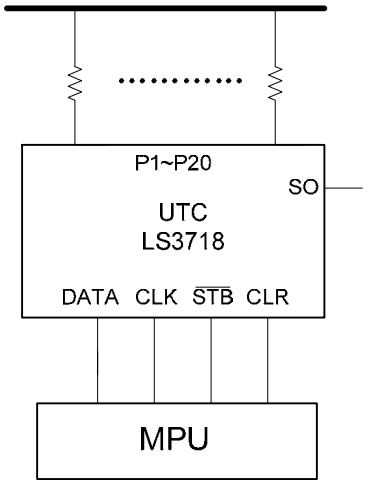
CLK	$\overline{STB}$	$\overline{CLR}$	DESCRIPTION
X	X	L	All latch are reset (the data in the shift register is not change). All of parallel outputs are "L".
⎍	H	H	The serial data input from DATA terminal to the shift register (the data in the latch is not change).
L	L	H	The data in the shift register transfer to the latch. And the data in the latch output from the parallel output.
H			
⎍			The CLK input in the $\overline{STB}$="L" and $\overline{CLR}$="H" state, the data shift in the shift register and latched data also change in accordance with the shift register.

Note: X: Don't care

■ TIMING CHART



■ TYPICAL APPLICATION CIRCUIT



Cascade Connection