R8075 CRC-4 Encoder/Decoder

INTRODUCTION

The Rockwell R8075 CRC-4 Encoder/Decoder is a support device to the R8070/R8070A T-1/CEPT PCM Transceiver and the R8069 Line Interface Unit. Used with the R8070 and the R8069, the R8075 implements transmit and receive functions in accordance with CCITT Recommendation G.704 for PCM30 using CRC-4. Operation of the R8075 is entirely transparent other than error detection/reporting and handling of the Spare Bits. The R8075 can be set in either enable or disable mode, for systems which handle both data encoded with CRC-4 and without CRC-4.

Transmit functions compute the CRC-4 polynomial and insert the proper alignment timing and Spare Bits (SP1, SP2) into the transmit data stream. HDB3 encoding is also handled by the R8075.

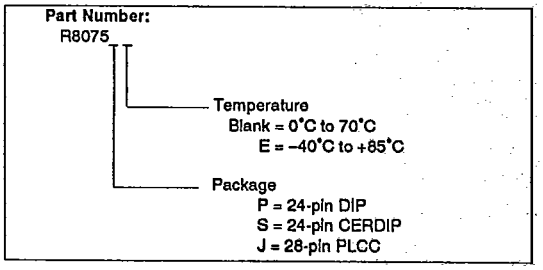
Receive functions are independent error detection of CRC-4 and multiframe alignment, extraction of the spare bits, and HDB3 decoding (including reporting of bipolar violations).

The Bit, Channel and Frame timing signals are available to the system for both the transmit and receive sections. The R8075 can support ISDN applications using the R8070 256N mode and PCM30 signalling modes using the 256S mode.

FEATURES

- CRC-4 transmit and receive as per CCITT Recommendation G.704
- Insertion and extraction of Spare Bits (SP1 and SP2)
- Independent error detection and reporting of CRC-4 and multiframe alignment errors
- CRC-4 enable/disable capability
- Enhanced HDB3 encode/decode section, includes reporting of bipolar violations
- Read/Write access to International Bits in CRC-4 disable mode (through R8070)
- Supports 256N and 256S modes
- Bit, Channel and Frame timing available to system
- Low power CMOS technology
- Operates from single +5V supply
- Package Options
  - 24-pin plastic DIP
  - 24-pin CERDIP
  - 28-pin PLCC

ORDERING INFORMATION



INTERFACE SIGNALS DESCRIPTION

The R8075 interfaces to the R8070 T1/CEPT PCM Transceiver, the R8069 Line Interface Unit, and to the system. The functional interface is shown in Figure 1. Figure 2 shows the signals grouped by interface. The R8075 interface signals are listed by pin number in Figure 3 and shown graphically in Figure 4.

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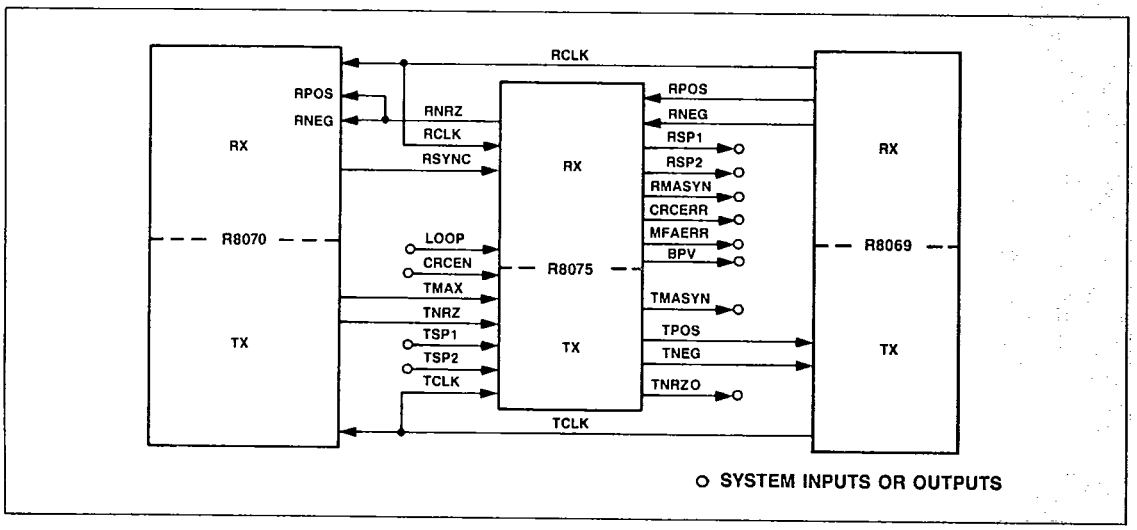

Figure 1. R8075 Functional Interface

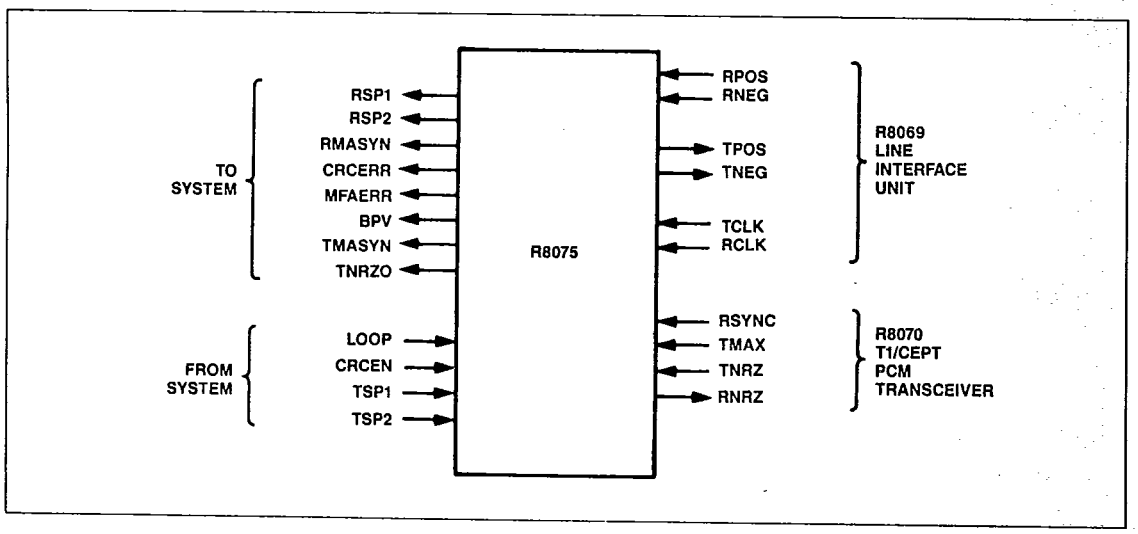

Figure 2. R8075 Interface Signals

Table 1. R8075 Pin Assignments T-75-15

Symbol	24-Pin DIP	28-Pin PLCC	Signal Name	I/O	Source/ Destination
LOOP	1	1	Loopback Mode	I	System
TNEG	2	2	Transmit Unipolar Negative	O	R8069
TPOS	3	3	Transmit Unipolar Positive	O	R8069
N.C.	–	4	No Connect		
TNRZ	4	5	Transmit NRZ Data (IN)	I	R8070
TNRZO	5	6	Transmit NRZ Data (OUT)	O	System
BPV	6	7	Bipolar Violation	O	System
VDD	7	8	+5 VDC Power	–	Power Supply
CRCERR	8	9	CRC-4 Error	O	System
RSP2	9	10	Receive Spare Bit 2	O	System
N.C.	–	11	No Connect		
RSYNC	10	12	Receive Sync	I	R8070
CRCEN	11	13	CRC-4 Enable	I	System
RNRZ	12	14	Receive NRZ Data	O	R8070
RCLK	13	15	Recovered (Receive) Clock	I	R8069
RPOS	14	16	Receive Unipolar Positive	I	R8069
RNEG	15	17	Receive Unipolar Negative	I	R8069
N.C.	–	18	No Connect		
MFAERR	16	19	Multiframe Alignment Error	O	System
TSP1	17	20	Transmit Spare Bit 1	I	System
TSP2	18	21	Transmit Spare Bit 2	I	System
VSS	19	22	Ground	–	Ground
TCLK	20	23	Transmit Clock	I	R8069
TMAX	21	24	Transmit Maximum	I	R8070
N.C.	–	25	No Connect		
RSP1	22	26	Receive Spare Bit 2	O	System
RMASYN	23	27	Receive MF Alignment Sync	O	System
TMASYN	24	28	Transmit MF Alignment Sync	O	System

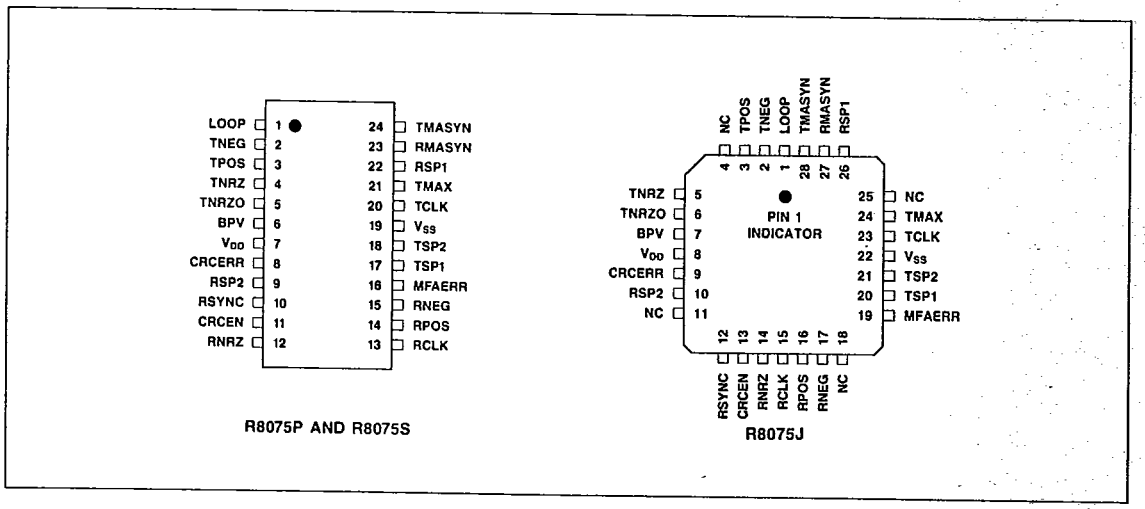

Figure 3. R8075 Pin Assignments

Table 2. R8075 Interface Signal Definitions T-75-15

Mnemonic	DIP Pin No.	PLCC Pin No.	Name/Description
INPUTS FROM R8069 (LINE INTERFACE UNIT)			
RCLK	13	15	**Recovered (Receive) Clock.** From R8069 Output Pin 27. RCLK is the recovered clock output which is locked to the frequency and phase of the incoming data. RPOS and RNEG are clocked out of the R8069 at the falling edge of RCLK in the elastic store bypass mode (CB high). This signal is also input to the R8070 as the receiver clock input, pin 56 of the QUIP (pin 59 of the PLCC).
TCLK	20	23	**Transmit Clock.** From R8069 Output Pin 28. Transmitter clock output which is either the smoothed clock provided through EXCLK (EXternal CLocK Reference, R8069 pin 3) or the smoothed clock extracted from the input data. The receive data is also clocked out on the falling edge of TCLK, except in elastic store bypass mode (CB high). This signal is also input to the R8070 as the transmitter clock input, pin 9 (QUIP) / pin 10 (PLCC).
RPOS RNEG	14 15	16 17	**Receive Unipolar Positive, Negative.** From R8069 Output Pins 16, 17. RPOS and RNEG are the outputs of the received data recovered from RXINP and RXINN AMI line pulses. RPOS and RNEG have TTL levels and are in NRZ format. These are directly connected to the R8075. RPOS and RNEG are clocked out of the R8069 at the falling edge of RCLK (elastic store bypass mode or TCLK in (elastic store enable mode), and clocked into the R8075 at the rising edge of RCLK.
INPUTS FROM R8070 (PCM30 TRANCEIVER)			
RSYNC	10	12	**Receive Sync.** From R8070 Output Pin 37 (QUIP)/Pin 39 (PLCC). While the receiver is synchronized, RSYNC is high during the first bit of each multiframe.
TMAX	21	24	**Transmit Maximum.** From R8070 Output Pin 10 (QUIP)/Pin 11 (PLCC). TMAX is high for one bit time per multiframe coincident with the sampling of the next to last serial bit of a multiframe.
TNRZ	4	5	**Transmit NRZ Data.** From R8070 Output Pin 19 (QUIP)/Pin 20 (PLCC). NRZ (Non-Return-to-Zero) output for transmitted data. This output is unaffected by LOOP or by HDB3 zero-suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
INPUTS FROM THE SYSTEM			
CRCEN	11	13	**CRC-4 Enable.** Control input which enables the R8075 when CRCEN is high. When CRCEN is low, the R8075 is disabled, providing full transparent operation; in this mode, the user has control of the international bits through the TIBITS. The R8075 receiver functions always operate; only the transmit functions are disabled when CRCEN is low.
LOOP	1	1	**Loopback Mode.** Control input placing the R8070 plus R8075 in loopback mode. In this mode, TPOS and TNEG are routed internally to RPOS, RNEG (respectively). This function is identical to the equivalent function of the R8070. It replaces the R8070 loopback function. CRCEN does not affect this function.
TSP1 TSP2	17 18	20 21	**Transmit Spare Bits 1, 2.** Input to R8075 which allows insertion of the spare international bits. When the R8075 is enabled, the user may update the TSP1, TSP2 inputs at the occurrence of TMASYN (R8075 output). These bits are reserved for future international applications, and for now, they should be fixed at 1 on digital paths crossing international borders. If CRCEN is low (R8075 disabled), the user may access the international bit through the IA pin (TIBIT) on the R8070, pin 5 (QUIP and PLCC).
OUTPUTS TO R8069 (LINE INTERFACE UNIT)			
TPOS TNEG	3 2	3 2	**Transmit Unipolar Positive, Unipolar Negative R8069 Input Pins 13,14.** TPOS and TNEG are the "unipolar paired" input for transmitted data. They must have TTL levels and be in NRZ format. These outputs from the R8075 replace those which would ordinarily come from the R8070. They are clocked in at the falling edge of TCLK. The state TPOS, TNEG = 1 is not valid, all other combinations are valid. The R8075 never generates the invalid combination.

Table 2. R8075 Interface Signal Definitions (Cont'd) T-75-15

Mnemonic	DIP Pin No.	PLCC Pin No.	Name/Description
OUTPUTS TO R8070 (PCM30 TRANSCEIVER)			
RNRZ	12	14	**Receive NRZ Data.** R8070 Input Pins 54, 55 (QUIP) / pins 57, 58 (PLCC) This lead is connected to both the RNEG and RPOS pins of the R8070. It must remain stable for 60 ns before and after the rising edge of RCLK. When connected in this manner, the HDB3 encoder and decoder along with the Bipolar Violation Detector in the R8070 are disabled. These functions are supplied by the R8075.
OUTPUTS TO THE SYSTEM			
CRCERR	8	9	**CRC-4 Error.** At the end of every SMF (sub-multiframe, 8 frames each), the current frame CRC result is clocked into a temporary holding register. During the following SMF, the incoming CRC bits on RSER are compared with the contents of the holding register. If a mismatch occurs, the CRC-4 error signal, CRCERR, is generated. This condition can result from a loss of frame alignment or by an incidental data error. This signal is valid after the falling edge of the second RCLK in the SMF and remains valid for the entire SMF, resetting at the end of the SMF.
MFAERR	16	19	**Multiframe Alignment Error.** The Multiframe Alignment Error signal is generated when there is a miss in the CRC-4 alignment bits (sequence of ...001011...). It indicates each instance of multiframe alignment and is valid during each MF. It is reset when the CRC-4 alignment is regained. This signal can be used by the system to improve the frame alarm handling.
TNRZO	5	6	**Transmit NRZ Data.** Serial transmit NRZ data. Derived by the R8075 (from the TNRZ input to the R8075 from the R8070, it is regenerated, aligned with the timebase of the TPOS/TNEG outputs of the R8075.
RMASYN	23	27	**CRC-4 Receive Multiframe Alignment Sync.** Derived signal generated by the R8075 indicating the beginning of the received CRC-4 multiframe. It is a positive pulse of one RCLK in duration.
TMASYN	24	28	**CRC-4 Transmit Multiframe Alignment Sync.** This signal indicates the beginning of the transmitted CRC-4 multiframe. It is a positive pulse of one TCLK period in duration.
BPV	6	7	**Bipolar Violation.** This signal indicates that a Bipolar Violation has occurred. It replaces the equivalent signal RVLL from the R8070, which indicates a Bipolar Violation.
RSP1 RSP2	22 9	26 10	**Receive Spare International Bits.** The receive logic extracts these spare international bits and makes them available to the system at the beginning of each multiframe (RMASYN).
POWER AND GROUND			
V_{DD}	7	8	**Power.** + 5V DC power.
V_{SS}	19	22	**Ground.** Power and signal ground.
NC		4, 11 18, 25	**No Connect.** These are pins on the PLCC which are not to be connected.

FUNCTIONAL DESCRIPTION

The R8075 is used with the R8070 Transceiver and the R8069 Line Interface Unit to provide CRC-4 capability for PCM30 systems. There are two basic sections to the R8075: the Transmit section and the Receive section.

Signals connected to either the R8069 or R8070 are described in the pin definitions (Table 2). For more information, please refer to the functional and interface descriptions of the data sheets for the R8069 and R8070.

TRANSMIT SECTION

The transmit section computes the CRC-4 polynomial, inserts alignment timing signals and spare bits into the transmit data stream, and encodes the bipolar transmit data using HDB3.

The six R8075 transmit section inputs are from the system (TSP1, TSP2, CRCEN), from the R8069 (TCLK), and from the R8070 (TNRZ). The four R8075 transmit section outputs go to the system (TNRZO and TMASYN) and to the R8069 (TPOS and TNEG).

The R8075 transmit section is divided into four blocks:

1. Transmit Logic
2. CRC-4 Encoder
3. HDB3 Encoder
4. Transmit Bit/Frame/Multiframe Control (Transmit Timing Control)

TRANSMIT LOGIC

The Transmit Logic section provides the TNRZO (Transmit NRZ Data) output to the system. This signal has the CRC-4 bits and the Spare Bits inserted at the proper time, as appropriate. There is a 1-bit throughput delay between TNRZ input and TNRZO output.

Data inputs to the Transmit Logic section are the NRZ (Non Return-to-Zero) output for transmitted data from the R8070 (TNRZ) and the Transmit Spare Bits from the system (TSP1, TSP2). When the CRC-4 encoder is enabled (CRCEN = HIGH) the CRC-4 Encoder section provides CRC-4 data to the Transmit Logic section for insertion into the transmitted bit stream. When CRCEN = LOW, CRC-4 is not being implemented, and access to the international bit for each frame is provided through the R8070/70A. In this case, the R8075 passes the international bit transparently.

Control and timing inputs to the Transmit Logic are provided by the Transmit Bit/ Frame/Multiframe Control (Transmit Timing Control) to determine the proper insertion points for the CRC-4 bits if CRCEN is HIGH. The Transmit Timing Control also properly times insertion of the Spare Bits. If CRCEN is LOW, there will be no insertion of CRC-4 bits into the transmitted bit stream, and the Spare Bits are accessed through the R8070 instead of through the R8075. In this condition, the CRC-4 is not implemented.

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The output of the Transmit Logic section to the system is TNRZO, the Transmit NRZ Data which has been CRC-4 encoded and has Spare Bits inserted at the proper time (if CRCEN is HIGH). This is a regenerated signal derived from the TNRZ signal from the R8070, which is unchanged if CRCEN is LOW. This signal, regardless of whether the R8075 is enabled or disabled is used to replace the R8070 TNRZ signal as an output to the system. TNRZO also is an input to the HDB3 Encoder, which generates the Transmit Unipolar Data, TPOS and TNEG. There is a 6-bit throughput delay between TNRZ input and TPOS/TNEG outputs.

CRC-4 ENCODER

This section calculates the CRC-4 polynomial and provides the CRC-4 bits for insertion into the transmitted bit stream. This insertion is performed at the proper time by the Transmit Logic (see above). The CRC-4 Encoder may be disabled for transparent operation without CRC-4 computation by CRCEN set LOW.

The data inputs to the CRC-4 Encoder section is the TNRZ (Non Return-to-Zero) output for transmitted data from the R8070. The R8069 provides TCLK (Transmit Clock) to the CRC-4 Encoder section as a timing input. Control and timing inputs to the CRC-4 Encoder are also provided by the Transmit Bit/Frame/ Multiframe Control (Transmit Timing Control) to determine the proper insertion points for the CRC-4 bits if CRCEN is HIGH. This information is generated using TMAX (from R8070) to derive multiframe timing and CRCEN (from system) to decide whether to compute CRC-4.

The output of the CRC-4 Encoder section goes through a holding register into the Transmit Logic for insertion of the CRC-4 bits (if CRCEN is HIGH) into the Transmit bit stream.

HDB3 ENCODER

This section takes the Transmit NRZ data provided by the Transmit Logic and provides HDB3 encoding. The resulting output is the two unipolar signals TPOS and TNEG which go to the R8069 for transmission onto the PCM-30 line.

Data input to the HDB3 Encoder is the TNRZO output of the Transmit Logic section of the R8075. This signal already has CRC-4 and Spare Bits inserted as appropriate. The TNRZO data is converted to a set of unipolar signals (TPOS, TNEG) using HDB3 encoding for unipolar PCM-30 data. The TCLK input to the HDB3 Encoder comes directly from the R8069.

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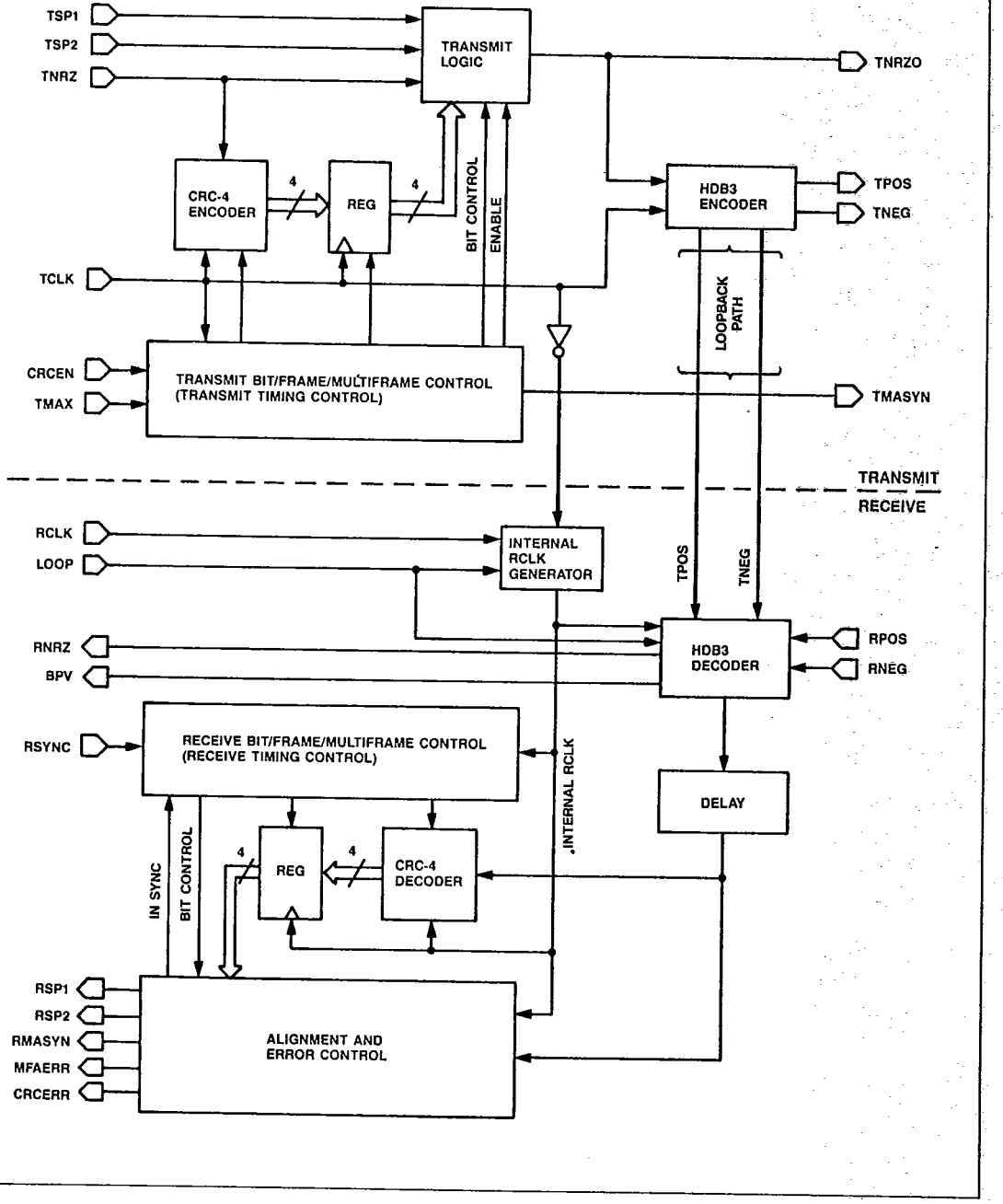

Figure 4. R8075 Functional Block Diagram

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The output of the HDB3 Encoder section is the set of Unipolar Transmit signals, TPOS and TNEG. These signals go directly to the R8069 for transmission onto the PCM-30 line. These signals also are provided to the HDB3 decoder section.

Transmit Bit/Frame/Multiframe Control (Transmit Timing Control)

Transmit timing is provided by this section to properly handle insertion of the CRC-4 bits and the Spare Bits into the outgoing transmit bit stream. This section provides timing and control to the CRC-4 Encoder and Transmit Logic sections. It also provides the Transmit Multiframe Alignment Sync signal to the system, so the system can align properly on multiframe boundaries.

Inputs to this section are TCLK (from R8069), TMAX (from R8070) and CRCEN (from system). If CRCEN is high, the control is provided to the Transmit Logic to implant the CRC-4 and Spare Bits into the transmit bit stream. TCLK is used to derive the bit timing; TMAX is used to derive the frame and multiframe timing.

The CRC-4 bits are inserted in the even frames, in the bit 1 position of these frames. There are four CRC-4 bits in each 8-frame Sub-MultiFrame (SMF). In odd frames, bit 1 of the first six frames of each 16-frame MultiFrame (MF) contains the CRC multiframe alignment signal (001011). Bit 1 of the last two odd frames of the multiframe (frame 13, 15) contain the Spare Bits. Access to the International Bit (bit 1 of each frame) is provided through the R8070 when the R8075 is in CRC-4 disable mode.

Outputs from this section are the timing and controls described above, and the Transmit Multiframe Alignment Sync (TMASYN) signal. TMASYN is an output to the system which indicates the beginning of the transmitted CRC-4 multiframe. It is a positive pulse of one TCLK period in duration.

RECEIVE SECTION

The receive section provides independent error detection/reporting of the CRC-4 and Multiframe Alignment errors, extraction of the Spare Bits, and HDB3 decoding with reporting of bipolar violations. The R8075 receive section also provides RNRZ (Receive NRZ Data) to the R8070, connected to the R8070 RPOS, RNEG inputs. This connection will bypass the HDB3 encoder and decoder sections of the R8070, along with the R8070 bipolar violations detector. These functions are supplied by the Transmit and Receive sections of the R8075.

The four inputs to the R8075 receive section are: RPOS and RNEG (unipolar receive data) from the R8069, RSYNC (receive sync) from the R8070, and LOOP (Loopback Mode) from the system. There is a 6-bit throughput delay between RPOS/RNEG inputs and RNRZ output. Also, the international bit is internally sampled (after a 21-bit delay from RPOS/RNEG inputs) in order to calculate the CRC bits.

The seven outputs from the R8075 receive section are: RNRZ (receive NRZ data) to the R8070, and the R8075 outputs to the system. These are: CRCERR (CRC-4 Error), MFAERR (Multiframe Alignment Error), RMASYN (Receive Multiframe Alignment Sync), BPV (Bipolar Violation), RSP1 and RSP2 (Receive Spare Bits).

The receive section has the following functional blocks:

1. Internal RCLK Regenerator
2. HDB3 Decoder
3. CRC-4 Decoder
4. Alignment and Error Control
5. Receive Bit/Frame/Multiframe Control (Receive Timing Control)

Internal RCLK Generator

This section takes the RLCK and TCLK from the R8069, along with the LOOP control from the system and produces the internal RCLK timing. This RCLK provides master bit timing for the other blocks of the receive section of the R8075.

HDB3 Decoder

This section takes the RPOS and RNEG from the R8069 and generates the RNRZ output to the R8070 and identifies bipolar violations (BPV) for output to the system.

Inputs to this section are the RPOS and RNEG (from R8069), TPOS and TNEG (from R8075 HDB3 encoder block), the LOOP control (from system), and the internal RCLK (from internal RCLK). Using the LOOP and TPOS/TNEG signals, if the loopback mode is enabled (LOOP = HIGH), the TPOS and TNEG signals generated in the R8075 HDB3 encoder are routed to the RPOS/RNEG inputs of the HDB3 decoder. This function is identical to and replaces the equivalent R8070 function.

Outputs from this section are RNRZ (to the R8070) and BPV (to system). The RNRZ is generated according to the HDB3 format, and sent to the R8070 RPOS/RNEG inputs, bypassing the R8070's HDB3 encode and decode functions. According to the HDB3 algorithm, bipolar violations are detected and reported through the BPV (system output). After HDB3 decoding of the receive data, it is also passed to the CRC-4 Decoder and the Alignment/Error Control blocks. Note that tying RPOS and RNEG together will bypass the HDB3 decode section. This function is identical in the R8070 and R8075, bypassing the respective HDB3 decode logic in each device used in this manner.

CRC-4 Decoder

The RNRZ output of the HDB3 decoder section, the internal RCLK, and the RSYNC timing are inputs to the CRC-4 decoder. At the end of every SMF, the current frame CRC-4 result computed by the CRC-4 decoder block is clocked into a temporary holding register. During the following SMF, the incoming CRC-4 bits on RSER are compared with the contents of the holding register. If a mismatch occurs, the CRC-4 error signal (CRCERR) is generated in the Alignment/Error control block. Timing is generated by the receive bit/frame/MF control block.

Alignment/Error Control

This block generates the receive multiframe alignment sync signal output to the system (RMASYN), outputs the Receive Spare Bits (RSP1, RSP2), and generates the error signals MFAERR (Multiframe Alignment Error) and CRCERR (CRC-4 error) output to the system.

Handling of the errors is a system function to be done in accordance with CCITT Standard G70X and Recommendation I.431.

Inputs to the Alignment/Error Control block are the internally generated RCLK, the RNRZ data from the HDB3 decoder block, the contents of the CRC-4 holding register, and timing signals from the Receive Bit/Frame/MF control block.

While the CRCERR and MFAERR are closely related, they are independently generated. CRCERR is generated upon a mismatch between the incoming CRC bits from RSER and the previous SMF's CRC result from the previous SMF, found in the holding register. This can occur due to an incidental data error or by a loss of frame alignment. This signal is valid for the entire SMF, resetting at the end of each SMF. MFAERR is generated when there is a miss in the CRC-4 alignment bits, indicating each instance of multiframe alignment error. It is valid during each MF, and is reset when the CRC-4 alignment is regained. This signal is useful to the system for implementing alarm handling.

Alignment/Error Control (continued)

RMASYN is derived from the RCLK. It is a positive pulse of one RCLK period in length, and indicates the beginning of the received CRC-4 multiframe. This section also extracts the Spare Bits (RSP1 and RSP2), making them available to the system at the beginning of each multiframe (at RMASYN).

Receive Bit/Frame/MF Control (Receive Timing Control)

This section takes RSYNC from the R8070, the internally generated RCLK, and a sync valid signal generated by the Alignment/Error control block to generate timing for the CRC-4 Decoder and the bit timing for the Alignment/Error control blocks. This block generates internal timing. It has no off-chip outputs.

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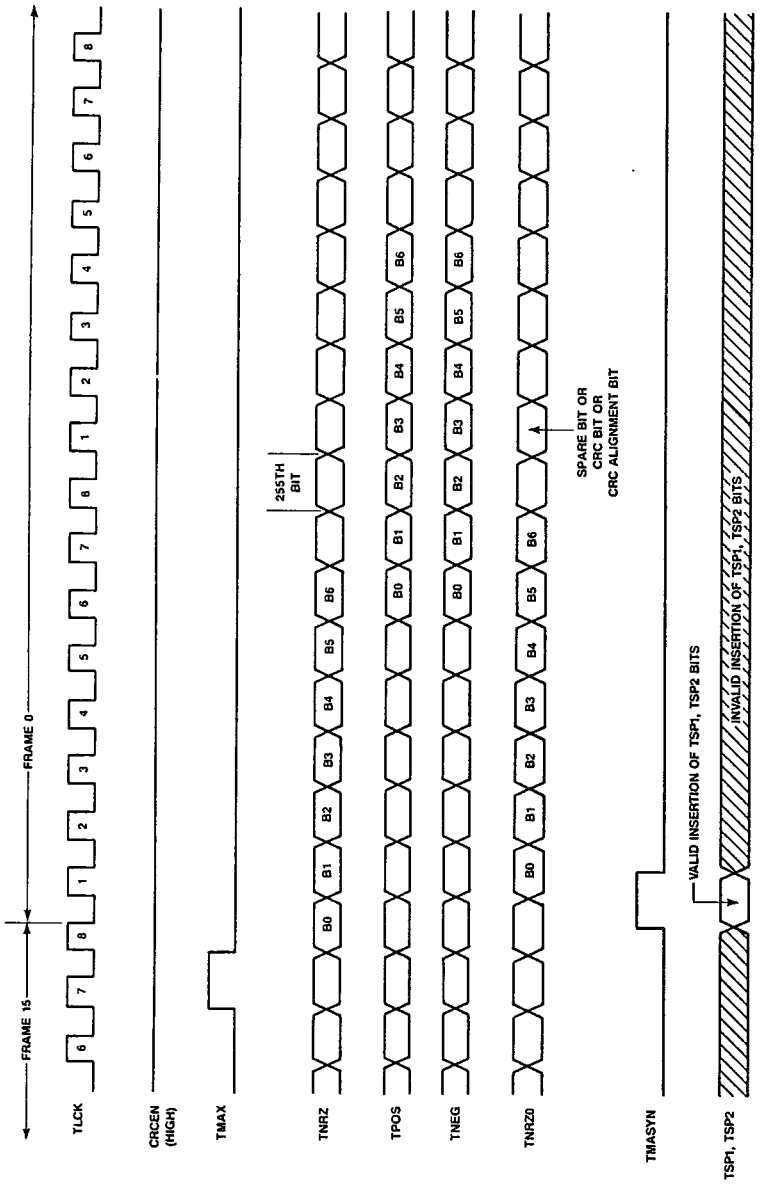

Figure 5. R8075 Transmit Timing

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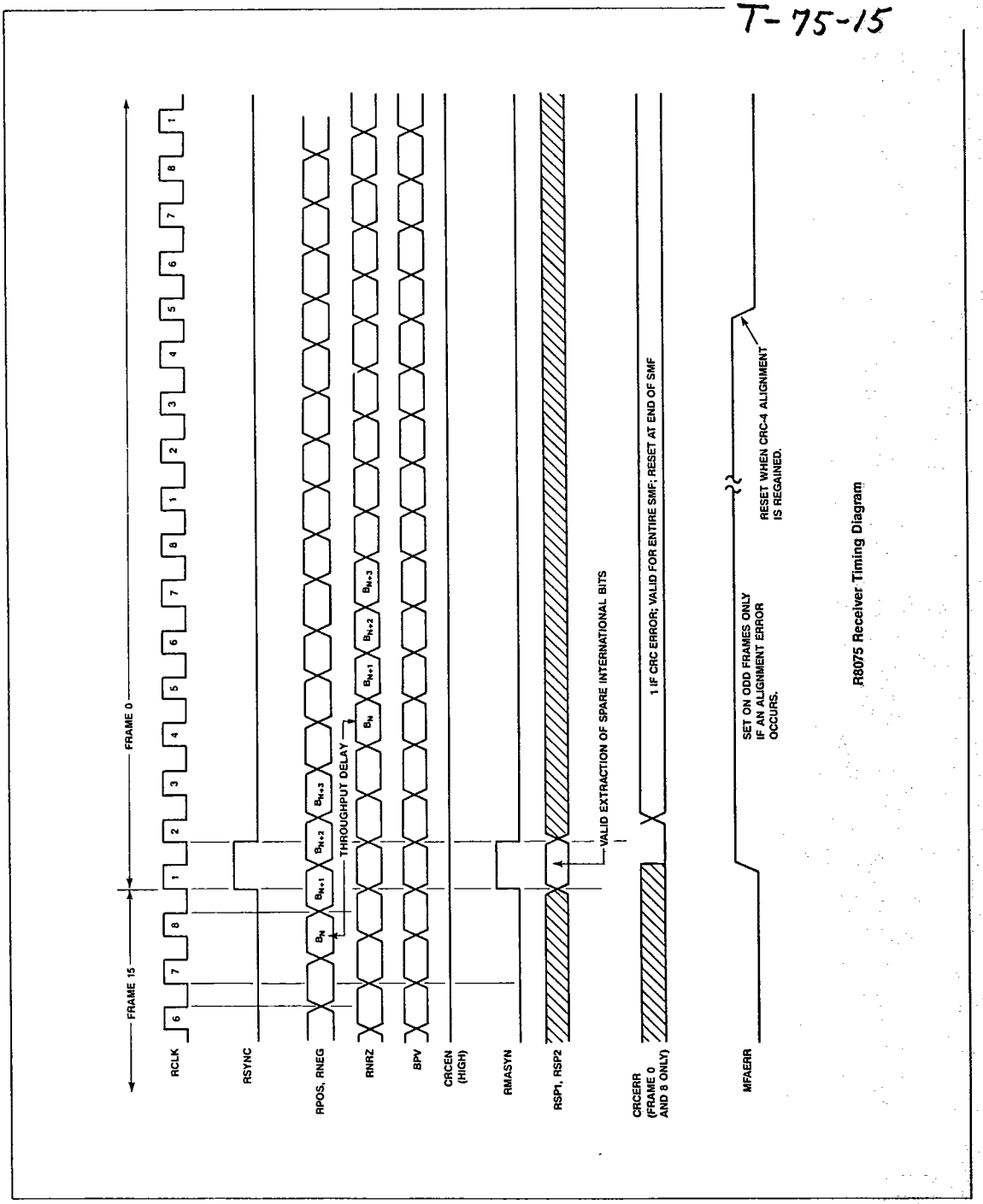

Figure 6. R8075 Receive Timing

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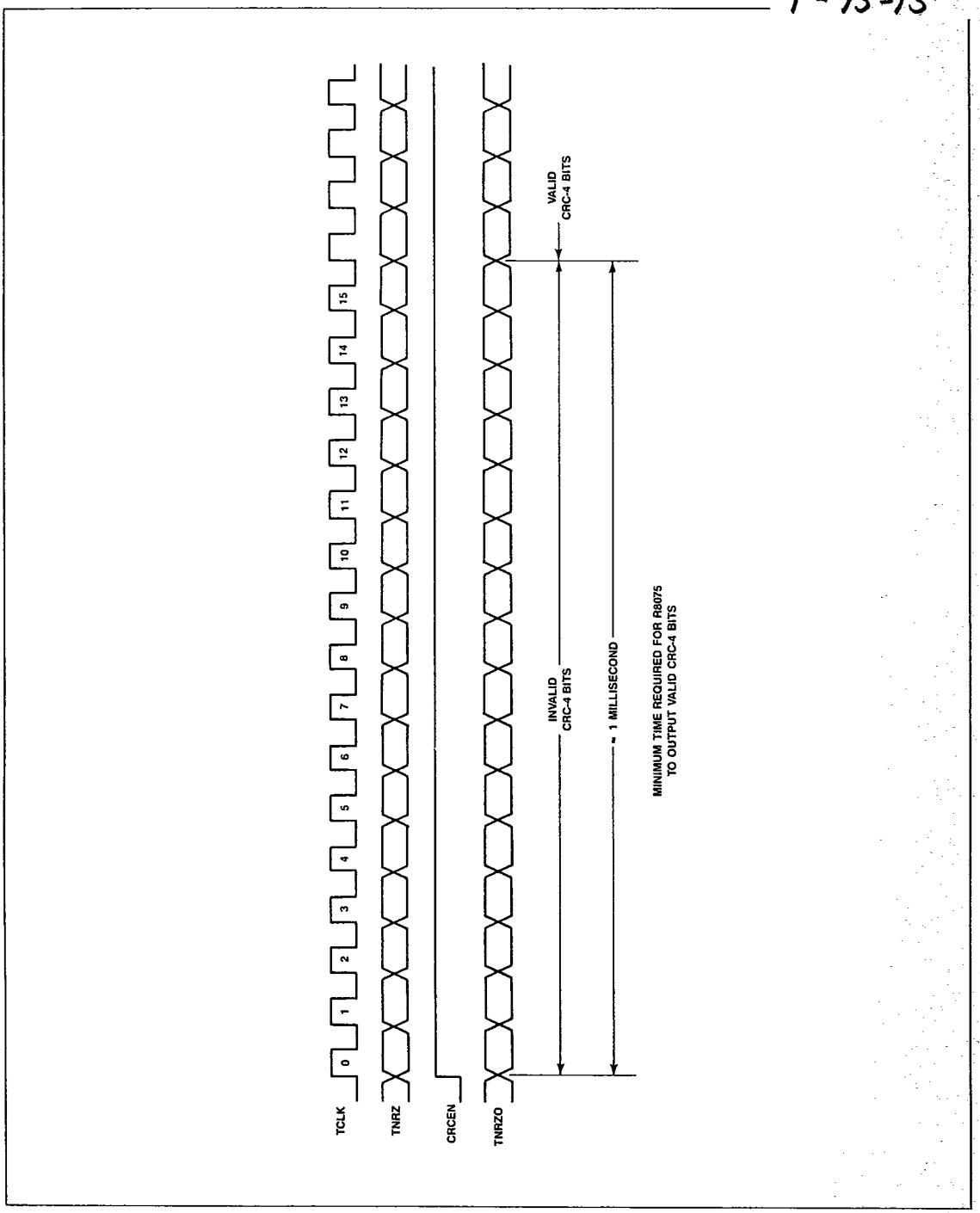

Figure 7. CRC-4 Output Timing

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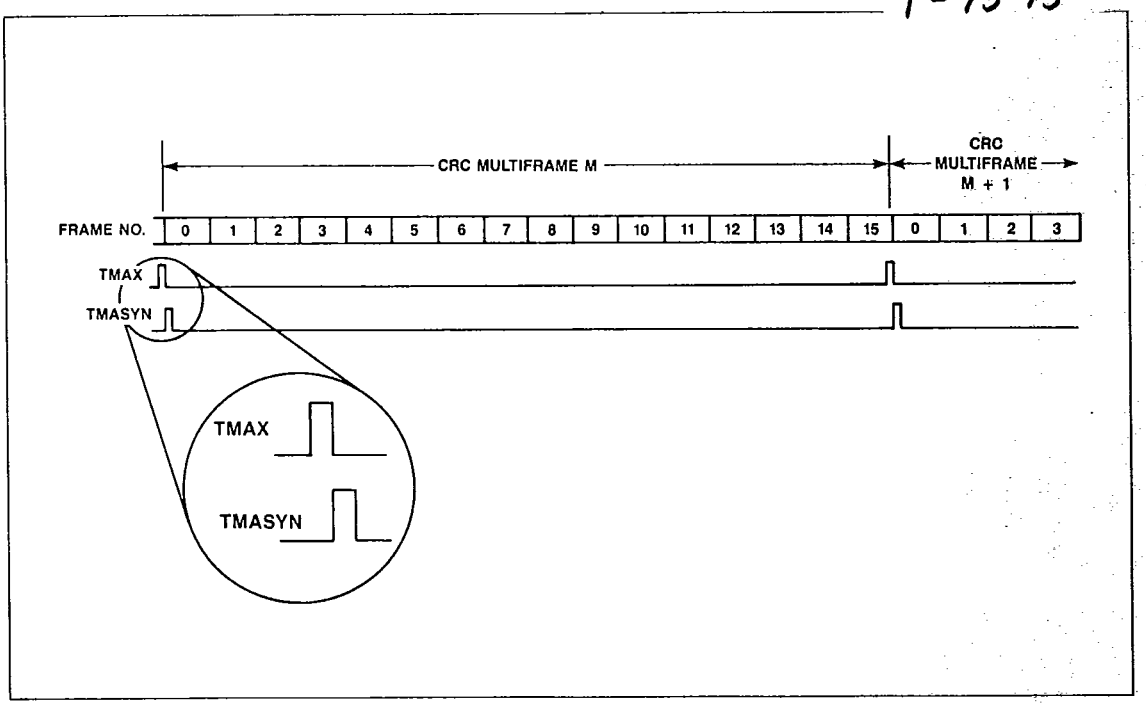

Figure 8. Transmit CRC Multiframe - R8070 Mode 256S

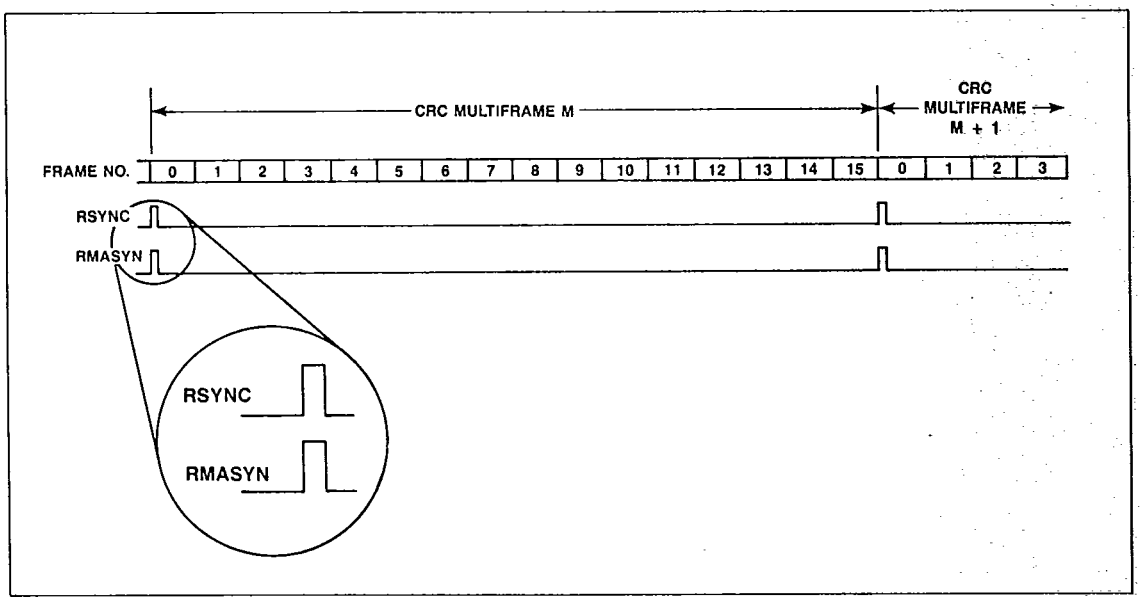

Figure 9. Receive CRC Multiframe - R8070 Mode 256S

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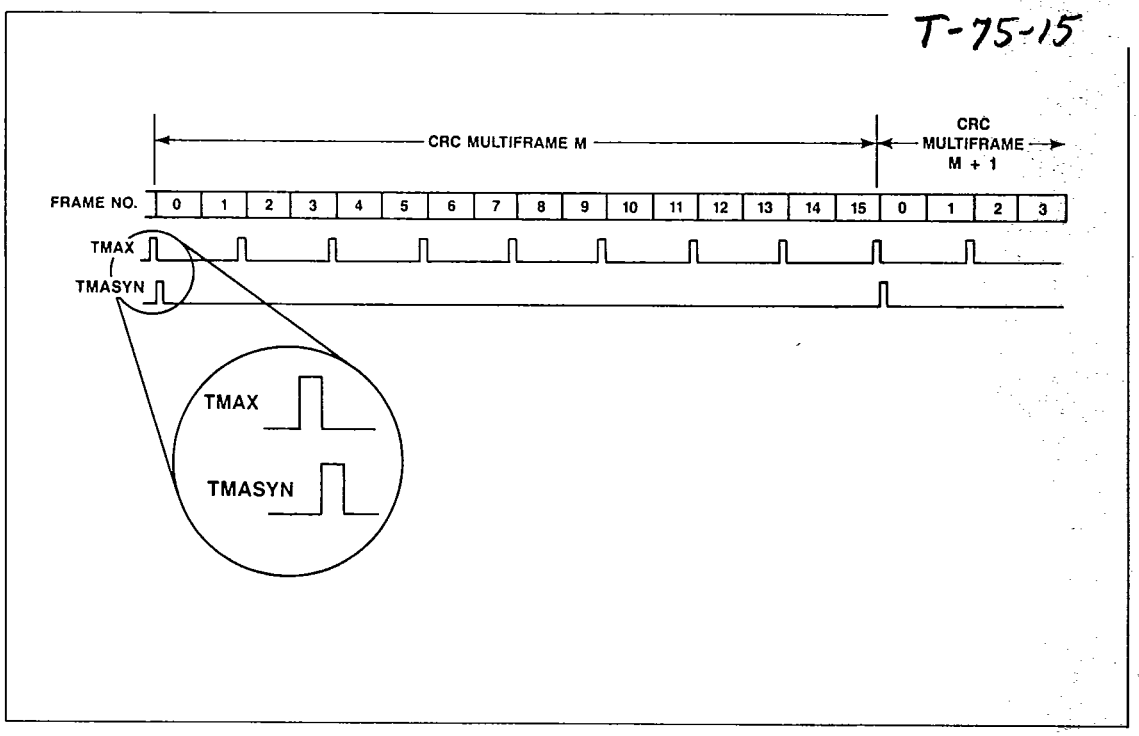

Figure 10. Transmit CRC Multiframe - R8070 Mode 256N

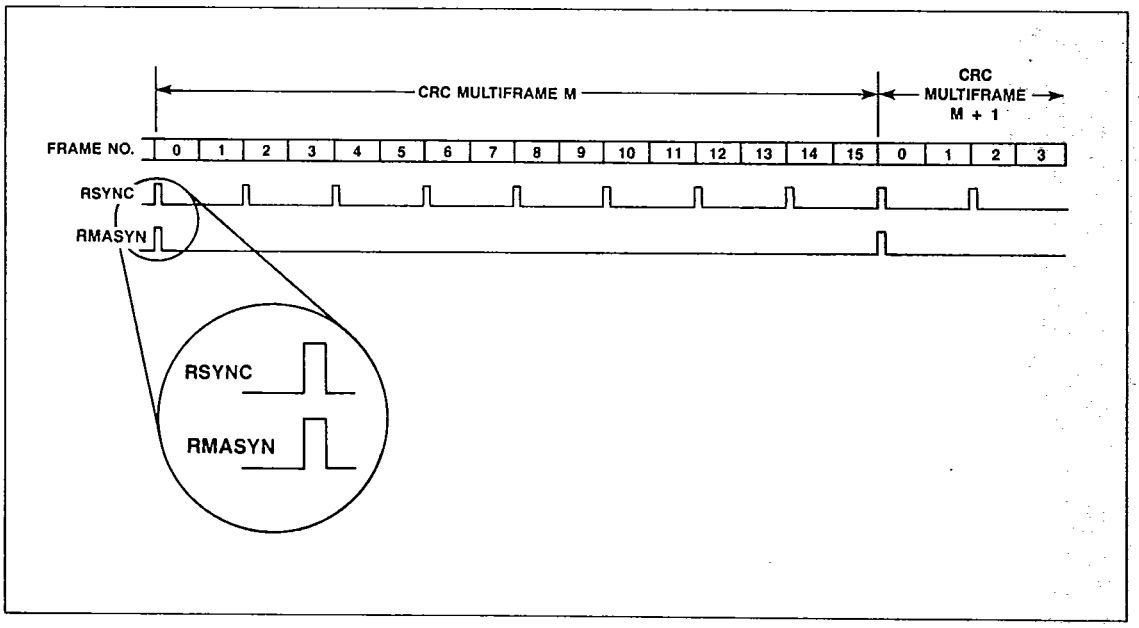

Figure 11. Receive CRC Multiframe - R8070 Mode 256N

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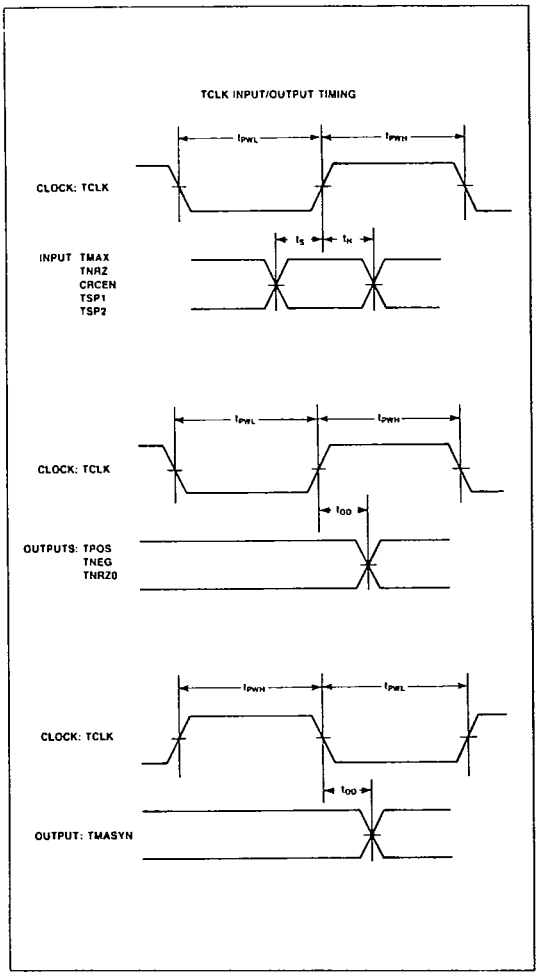

Figure 12. Input Timing

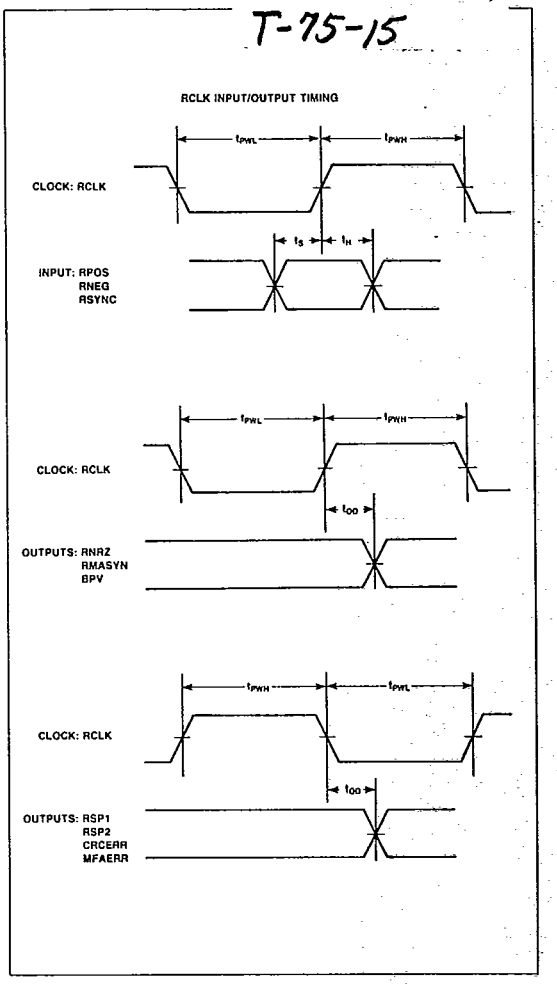

Figure 13. Output Timing

Table 3. Input and Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock Pulse Width High, Low	t_{PWH}, t_{PWL}	200	244	–	ns
Input Setup Time	t_S	60	–	–	ns
Input Hold Time	t_H	60	–	–	ns
Output Delay Time	t_{OD}	–	–	60	ns

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	Vdc
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{STG}	−55 to + 150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}	−0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	VCC +0.3	V	
Output Low Voltage	V_{OL}	–	–	+0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage TTL	V_{OH}	+2.4	–	–	V	I_{LOAD} = −100 µA
CMOS	V_{OH}	+3.5	–	–	V	I_{LOAD} = −100 µA
Output Low Current	I_{OL}	−1.6	–	–	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	−100	–	–	µA	V_{OH} = 2.4V
Input Capacitance	C_{IN}	–	–	5	pF	
Power Dissipation	P_D	–	–	100	mW	

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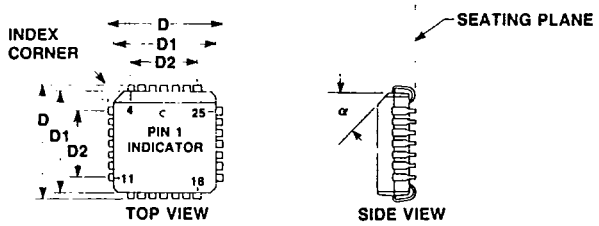
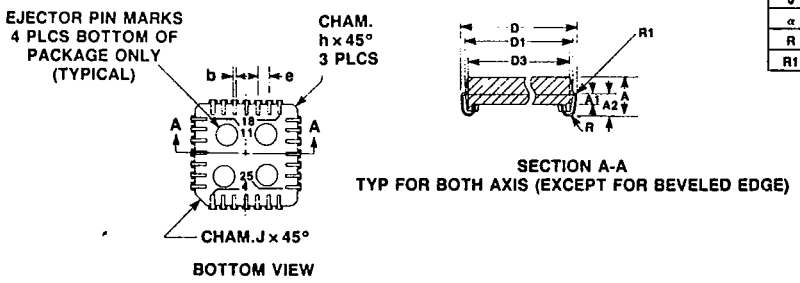
PACKAGE DIMENSIONS



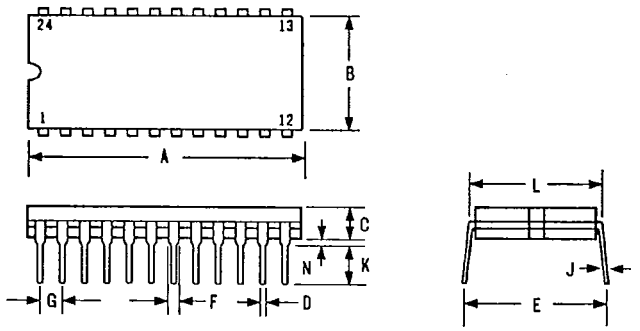
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	12.37	12.52	0.487	0.493
D1	11.43	11.53	0.450	0.454
D2	7.54	7.70	0.297	0.303
D3	10.67 REF		0.420 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	



28-Pin PLCC

PACKAGE DIMENSIONS (CONT'D)

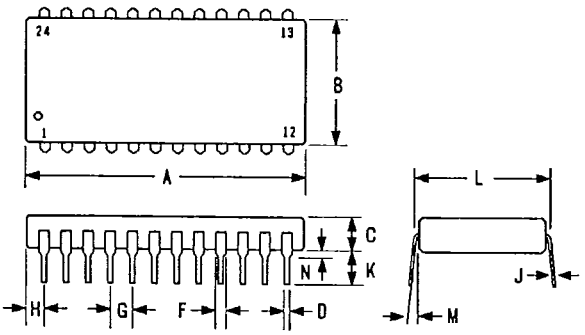
T-75-15



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	31.24	32.26	1.230	1.270
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
E	16.51	17.27	0.650	0.680
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	4.19	4.95	0.165	0.195
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°

REF: PD24S/GP00-D300

24-Pin CERDIP



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	31.24	32.00	1.230	1.260
B	13.46	13.97	0.530	0.550
C	3.56	4.06	0.140	0.160
D	0.38	0.53	0.015	0.021
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

REF: PD24P/GP00-D132

24-Pin Plastic DIP