Integrated Device Technology, Inc.

FAST CMOS EEPROM WITH SERIAL PROTOCOL CHANNEL (SPC™) 16K (2K x 8-BIT)

IDT78C18A

FEATURES:

- 2K x 8 EEPROM with serial write and readback
- 5 volt only operation
- Fast access times
  - Military: 75ns (max.)
  - Commercial: 70ns (max.)
- Low-power CEMOS™ technology
  - Active Current: 125mA
  - Standby Current (full CMOS): 0.9mA
- Serial Protocol Channel (SPC) allows load and readout of the memory array over a 4-wire channel
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{DATA}$ Polling—detection of write cycle completion
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Available in 28-pin THINDIP and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

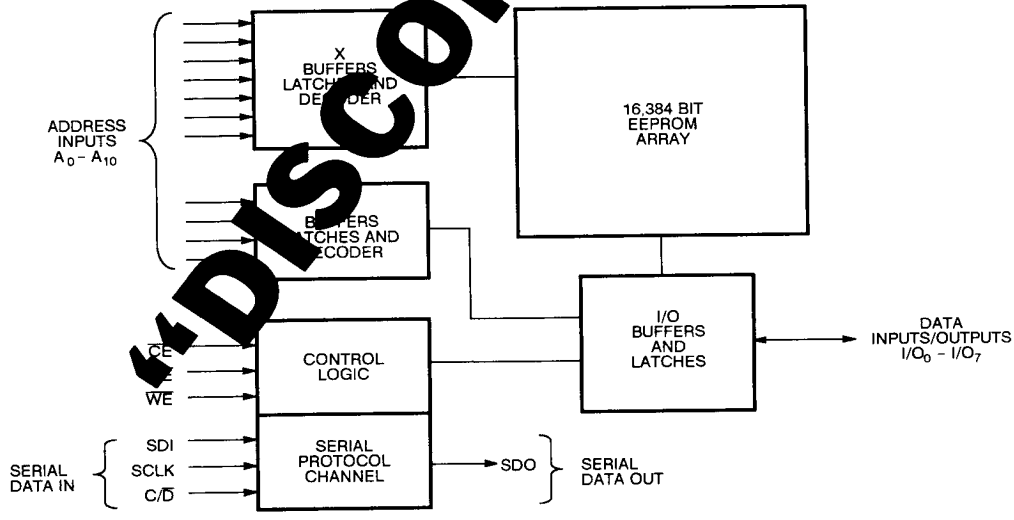
The IDT78C18A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM) with Serial Protocol Channel (SPC). SPC complements the EEPROM's parallel information path by providing a serial link (4 additional pins) by which its nonvolatile array can be loaded or read. The IDT78C18A is written on a byte basis and provides 16,384 bits of nonvolatile data storage (data retention in excess of 100 years). Fast read access times allow zero-wait state cycles with high-performance microprocessors.

Writing is simplified by an internal charge-pump and timer circuit which eliminates the need for external programming voltage and write pulse shaping circuits. Internal latches free the host system for other tasks during a write cycle. Byte erase before write occurs automatically. A DATA Polling mode is provided for determining write cycle completion.

The IDT78C18A is ideal for systems requiring nonvolatility and in-system data modifications. With SPC, a serial link can be established on board layout for easy field updates of code changes. The IDT78C18A military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

DISCONTINUED

FUNCTIONAL BLOCK DIAGRAM



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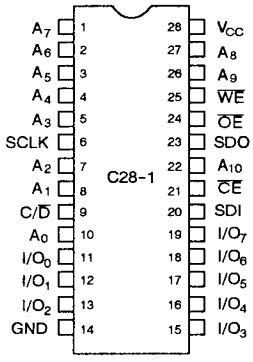
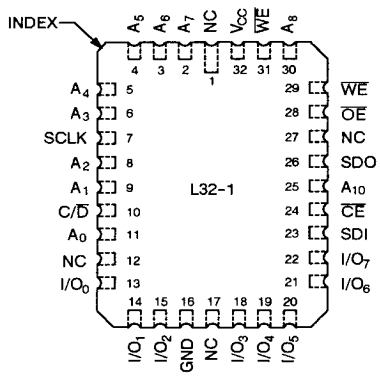
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

DEVICE OPERATIONAL MODE [1,2]

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	$Data_{OUT}$ ($O_0 - O_7$)
Byte Write	V_{IL}	V_{IH}	V_{IL}	$Data_{IN}$ ($I_0 - I_7$)
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z
Chip Erase	V_{IL}	V_H (2)	V_H (2)	High Z

NOTES:
1. All control inputs are TTL-compatible.
2. V_H = High Voltage; optional function, consult IDT for more details.

PIN NAMES

$A_0 - A_3$	Addresses-Column
$A_4 - A_{10}$	Addresses-Row
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$I/O_0 - I/O_7$	Data Input ($I_0 - I_7$) during write; Data Output ($O_0 - O_7$) during read
SDI	Serial Data Input
SDO	Serial Data Output
SCLK	Data Clock Input
C/$\overline{D}$	Command/$\overline{Data}$

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SPC OPERATIONAL MODES [1]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	C/$\overline{D}$	SCLK	FUNCTION
Command	X	X	X	H	⎍	Shift bit into command register
Data	X	X	X	L	⎍	Shift bit into data register
Execute	X	X	X	⎺_	⎍	Execute command during time between C/$\overline{D}$ and SCLK

NOTE:
1. X = Don't Care

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READ MODE

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be logically active in order for data to be available at the outputs. After a selected byte address is stable, $\overline{CE}$ is taken to a TTL LOW (enabling chip). The Write Enable ($\overline{WE}$) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the $\overline{OE}$ pin (TTL LOW). For serial read function, see description within "Serial Protocol Channel" section.

WRITE MODE

The IDT78C18A is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78C18A is as easy as writing to a static RAM. When a write cycle is initiated, the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The IDT78C18A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. All inputs, except for data, are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is then latched in by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms. For serial write function, see description within "Serial Protocol Channel" section.

STANDBY MODE

The IDT78C18A features a standby mode which reduces the maximum active current from 125mA to 20mA for TTL levels and to 0.9mA for CMOS levels. With $\overline{CE} \geq V_{IH}$ all outputs are in the high impedance state.

DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

Power Up/Down

On-chip circuitry provides protection against false write during V_{CC} power up/down. The IDT78C18A features an internal sensing circuit that disables the internal programming circuit if $V_{CC} < 3.8V$. This prevents input signals at $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ from triggering a write cycle during a V_{CC} power up/down event.

Noise Protection

The IDT78C18A will typically reject write pulses that are less than 15ns. This prevents the initiation of a write cycle by a noise occurrence.

Write Inhibit

Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during a power-on and power-off, will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The IDT78C18A has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine ($\overline{DATA}$ Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78C18A is still writing, the inverse of the most significant bit (I/O_7 pin) of the last byte written will be present. The most significant bit becomes valid when the write cycle is completed. Thus, a $\overline{DATA}$ Polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

CHIP ERASE

In particular applications, erasure of the entire chip (all bytes simultaneously) may be desired. An optional chip erase feature of the IDT78C18A allows erasure of the entire chip within 5ms. Contact IDT for more details regarding this optional function.

ENDURANCE

IDT's EEPROM technology employs the Fowler-Nordheim method of tunneling across a thin oxide. IDT78C18A EEPROMs are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle and eventually become large enough to prevent reliable writing to the bit cell. Since some bits are more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, sample devices are written 10,000 times at every byte location and checked for data retention capability. IDT's tests ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

SERIAL PROTOCOL CHANNEL

The Serial Protocol Channel (SPC™) provides a method by which data can be entered or extracted from the memory array via four unique pins $C\overline{D}$, SCLK, SDI and SDO. SPC logic consists of a 24-bit data shift register, a 4-bit command register and clock logic consisting of gates and a flip-flop (see block diagram). From the outside, SPC appears like two parallel serial shift registers; one for command and the other data. Data is clocked in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of data is controlled by a serial clock (SCLK) and a Command/$\overline{Data}$ mode input ($C/\overline{D}$). The serial clock (SCLK input) shifts information and the Command/$\overline{Data}$ ($C/\overline{D}$) input selects the register that will be shifted. The command register (when loaded and executed) controls the loading of data into and out of the data register with regard to writing to or reading from an addressed location of the memory array.

There are two modes for the shift operation: when $C/\overline{D}$ input is LOW, data information is shifted through the device and, when $C/\overline{D}$ is HIGH, command is shifted through. As the $C/\overline{D}$ line transitions from HIGH (command) to LOW (data), a clock pulse is internally generated to the command decode logic and is used to execute the instruction in the command register (clock pulse ends when serial clock transitions from LOW to HIGH). There are four steps to executing an SPC command: data is shifted in, command bits are then shifted in, the command is then executed and data is clocked (shifted) out. (Note: The data to the SPC is shifted in LSB first.) During the data mode, data is simultaneously shifted into the serial data register while data in the register is shifted out.

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Command codes that are utilized for read/write operations are shown below:

Command Words (4-bit Command Register):

0000	Read
0001	Write (Byte)
0010	Invalid Command—Reserved for Optional Chip Erase
3 ↓ 15	No Operation

All functions can be performed serially, including $\overline{DATA}$ Polling. The operation of serial $\overline{DATA}$ Polling is the same as SPC read. The byte being written is read and bit 23 (representing I/O_7) will be the complement of the most significant data bit until the write cycle is completed. (After completion of the write cycle, bit 23 will show true data.)

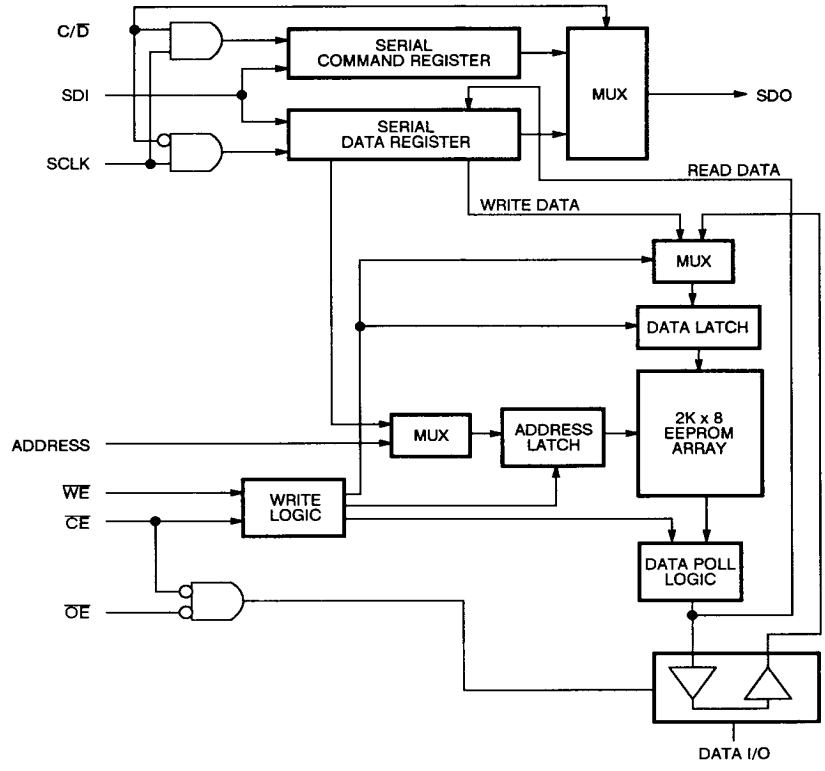

Figure 1. Detailed SPC Block Diagram

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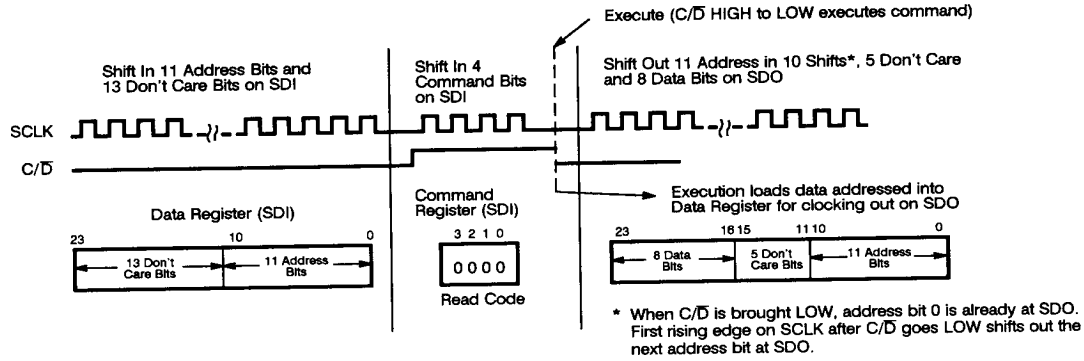
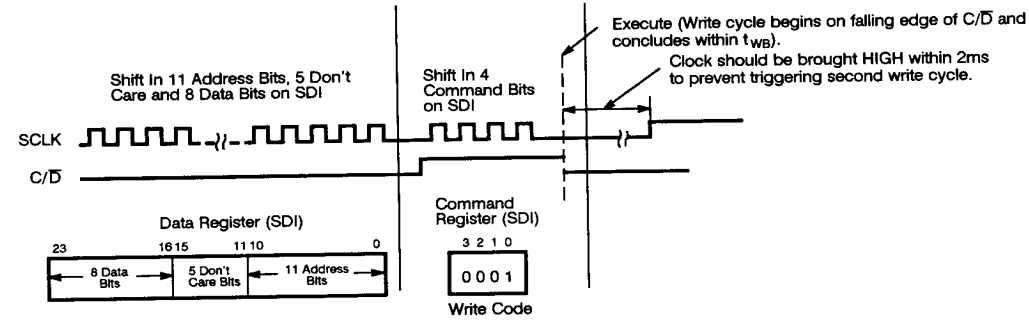
To Read Data Out:



To Write Data In:



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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ENDURANCE

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.3	0.4	0.8	V
V_{WI}	Write Inhibit	3.8	–	–	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C — V_{CC} = 5.0V ±10% (Commercial)
T_A = -55°C to +125°C — V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V — V_{HC} = V_{CC} - 0.2V
C_L = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	10	µA
I_{CC1}	Operating Power Supply Current V_{CC} = Max., f = 0	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	—	125	mA
I_{CC2}	Dynamic Operating Current V_{CC} = Max., f = f_{MAX}	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	—	125	mA
I_{SB}	Standby Power Supply Current (TTL Level)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., $I_{I/O}$ = 0mA V_{IN} ≥ V_{IH} or 0 ≤ V_{IN} ≤ V_{IL}	—	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max., $I_{I/O}$ = 0mA V_{IN} ≥ V_{CC} -0.2V or 0 ≤ V_{IN} ≤ 0.2V	—	0.9	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2mA	2.4	–	V

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges; C_L = 30pF)

SYMBOL	PARAMETER	COM'L. ONLY IDT78C18A70 MIN.	MAX.	COMMERCIAL/MILITARY IDT78C18A75[2]/90 MIN.	MAX.	IDT78C18A100/120 MIN.	MAX.	IDT78C18A150/200 MIN.	MAX.	UNIT
READ CYCLE										
t_{CE}	Chip Enable Access Time	–	70	–	75/90	–	100/120	–	150/200	ns
t_{AA}	Address Access Time	–	70	–	75/90	–	100/120	–	150/200	ns
t_{OE}	Output Enable to Output Valid	–	50	–	50/60	–	65/70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z[1]	0	20	0	20/30	0	20/30	0	20/30	ns
t_{OHZ}	Output Disable to Output in High Z[1]	0	20	0	20/30	0	20/30	0	20/30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns

NOTES:
1. This parameter is guaranteed but not tested.
2. Military temperature range only.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges, [illegible] = 30pF)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE CYCLE				
t_{AS}	Address Set-up Time	5	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{DS}	Data Set-up Time	20	–	ns
t_{DH}	Data Hold from Write Time	15	–	ns
t_{OES}	Output Enable Set-up Time	5	–	ns
t_{OEH}	Chip Enable Hold from Write Time	15	–	ns
t_{CES}	Chip Enable Set-up Time	0	–	ns
t_{CEH}	Chip Enable Hold Time	0	–	ns
t_{WP}	Write Pulse Width	50	–	ns
t_{WB}	Byte Write Cycle	–	10	ms
t_{DBV}	$\overline{DATA}$ Polling to $\overline{DATA}$ Valid	–	t_{OE}	
t_{WH}	Write Hold Time	15	–	ns
t_{DP}	End of Write Pulse to $\overline{DATA}$ P[illegible]g	15	–	ns
t_{WES}	Write Enable Set-up Time	0	–	ns
t_{WEH}	Write Enable Hold Time	0	–	ns
t_{DV}	Data Valid Time [1, 2]	–	1	µs

NOTES:
1. Data must be valid within 1µs maxim[illegible]d must remain valid if t_{WP} is longer than 1µs.
2. This parameter is guaranteed but not tes[illegible]

DISCONTINUED

AC TEST CONDITIO[illegible]

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

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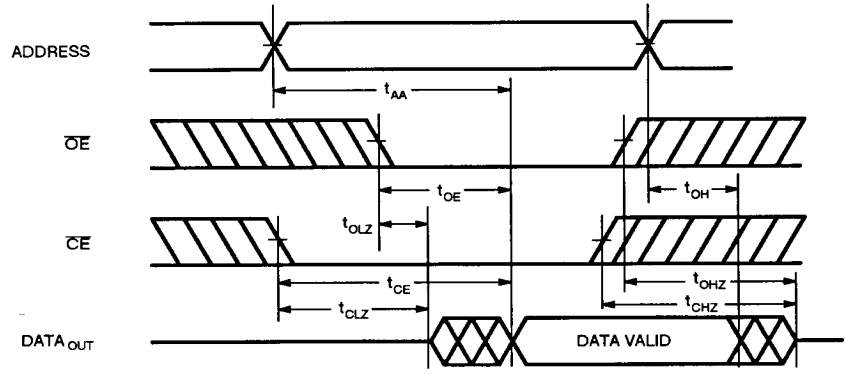
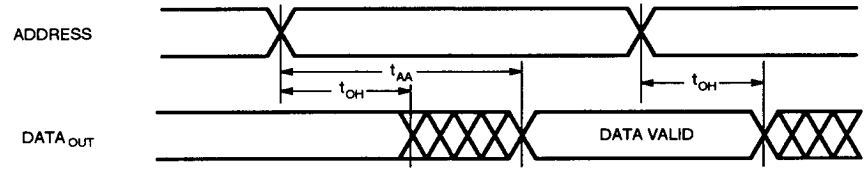
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



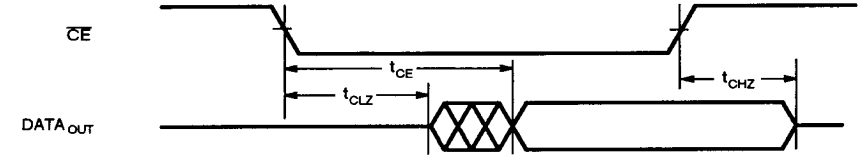
NOTE:
1. $\overline{WE}$ is HIGH for Read Cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2[1]



NOTE:
1. $\overline{WE}$ is HIGH; $\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IL}

TIMING WAVEFORM OF READ CYCLE NO. 3[1]



NOTE:
1. $\overline{WE}$ is HIGH; $\overline{OE}$ = V_{IL}; address valid prior to or coincident with $\overline{CE}$ transition LOW.

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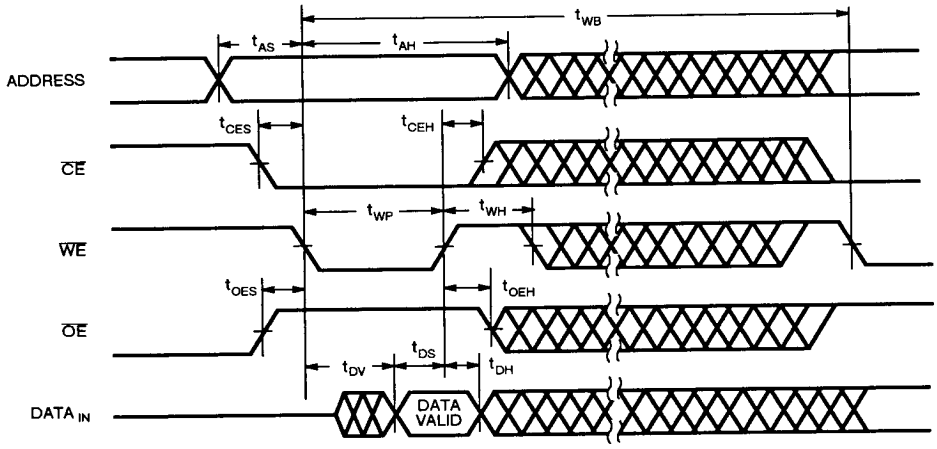
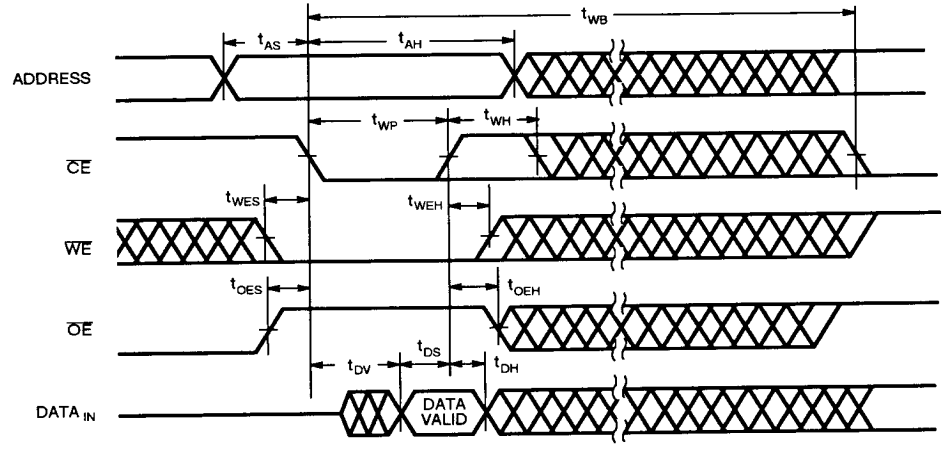
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{WE}$ CONTROLLED



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED



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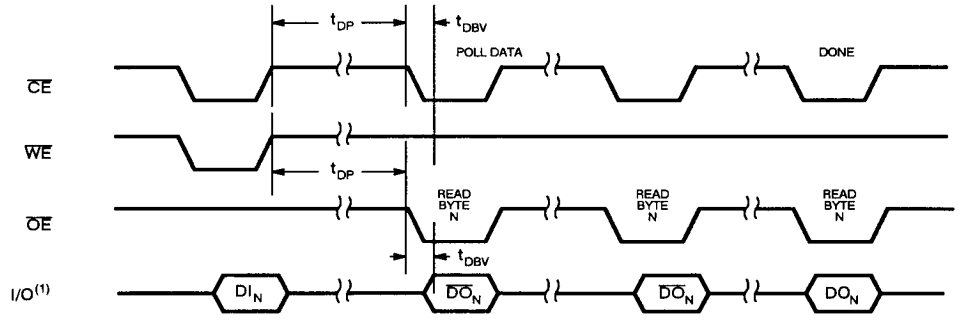
$\overline{\text{DATA}}$ POLLING



NOTE:
1. Most significant bit of the byte being written is inverted and available at I/O_7 if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

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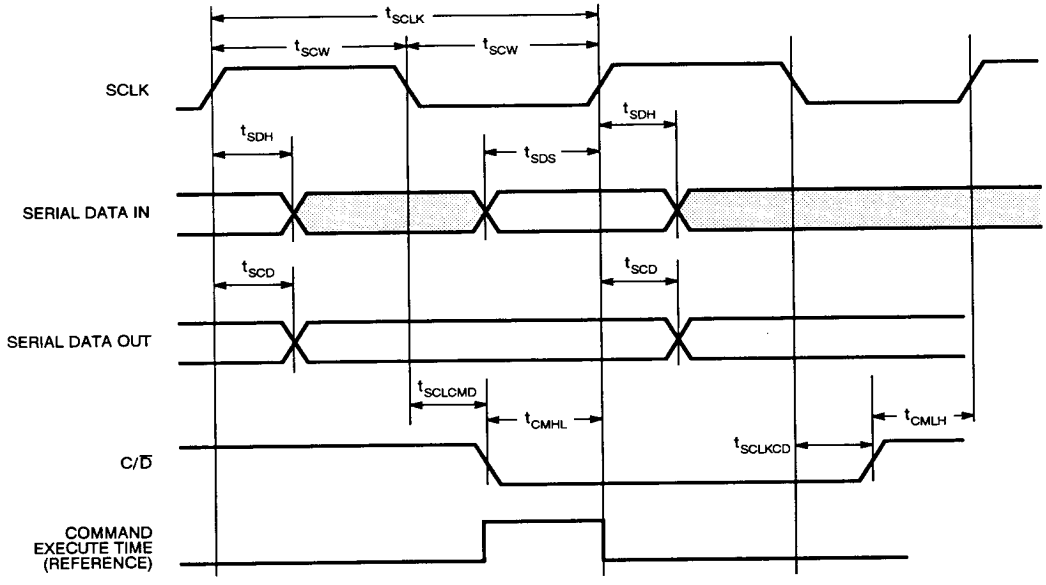
SPC AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER		COMMERCIAL[1] MIN.	COMMERCIAL[1] MAX.	MILITARY[1] MIN.	MILITARY[1] MAX.	UNIT
t_{SCLK}	SCLK Period		100	–	100	–	ns
t_{SCW}	SCLK Pulse Width		50	–	50	–	ns
t_{SDS}	Serial Data Set-up Time		15	–	15	–	ns
t_{SDH}	Serial Data Hold Time		5	–	5	–	ns
t_{SCD}	Clock to Serial Data Output Delay		4	25	4	25	ns
t_{SCLCMD}	Clock to Command Set-up Time[3]		50	–	50	–	ns
t_{CMLH}	Command/Data Set-up Time, LOW to HIGH		50	–	50	–	ns
t_{CMHL}	Command Set-up Time, HIGH to LOW (Execution Time)[4]	Read Cycle	t_{AA}	–	t_{AA}	–	ns
		Write/Erase Cycle	100	2(10)[6]	100	2(10)[6]	
t_{SCLKCD}	Clock LOW to C/$\overline{D}$ HIGH		0	–	0	–	ns

NOTES:
1. These specifications apply to all speed grades of the product.
2. This parameter guaranteed but not tested.
3. C/$\overline{D}$ cannot change while clock is high.
4. During a write/erase cycle SCLK should be brought HIGH within 2ms to prevent triggering another write/erase cycle.



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

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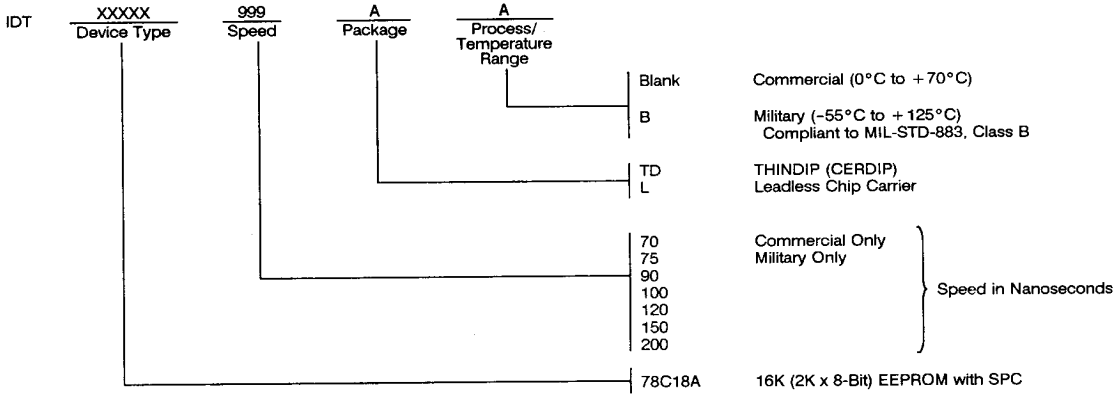
ORDERING INFORMATION



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