MITEL
SEMICONDUCTOR

MT9040
T1/E1 Synchronizer
Advance Information

DS5406 ISSUE 2 January 2001

Features

- Supports AT&T TR62411 and Bellcore GR-1244-CORE and Stratum 4 timing for DS1 interfaces
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 interfaces
- Selectable 19.44 MHz, 1.544MHz, 2.048MHz or 8kHz input reference signals
- Provides C1.5, C2, $\overline{\text{C4}}$, C6, C8, $\overline{\text{C16}}$, and C19 (STS-3/OC3 clock divided by 8) output clock signals
- Provides 5 different styles of 8 KHz framing pulses
- Attenuates wander from 1.9Hz
- Fast lock mode
- JTAG Boundary Scan

Applications

- Synchronization and timing control for multitrunk T1 and E1 systems
- ST-BUS clock and frame pulse source

Ordering Information	
MT9040AN	48 Pin SSOP
-40 to +85°C	

Description

The MT9040 T1/E1 System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for T1 and E1 primary rate transmission links.

The MT9040 generates ST-BUS clock and framing signals that are phase locked to either a 19.44 MHz, 2.048MHz, 1.544MHz, or 8kHz input reference.

The MT9040 is compliant with AT&T TR62411 and Bellcore GR-1244-CORE, Stratum 4; and ETSI ETS 300 011. It will meet the jitter/wander tolerance, jitter transfer, intrinsic jitter, frequency accuracy and capture range for these specifications.

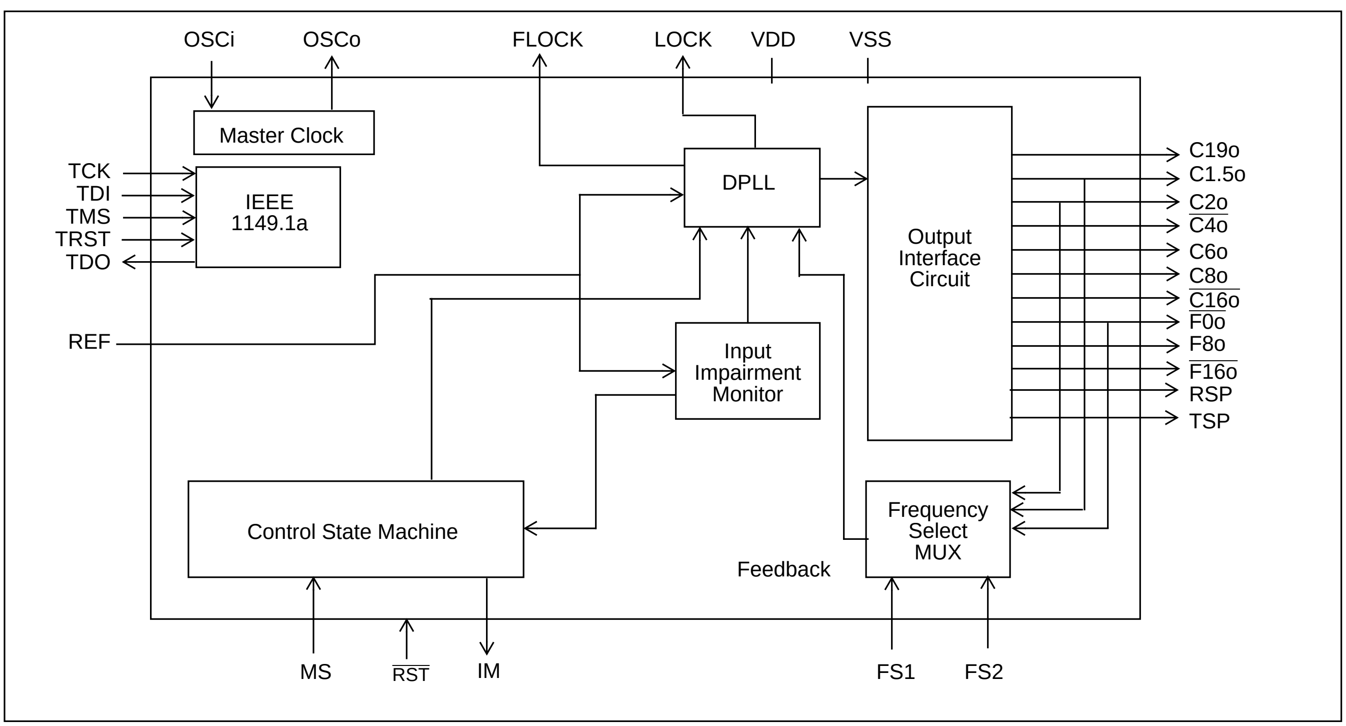


Figure 1 - Functional Block Diagram

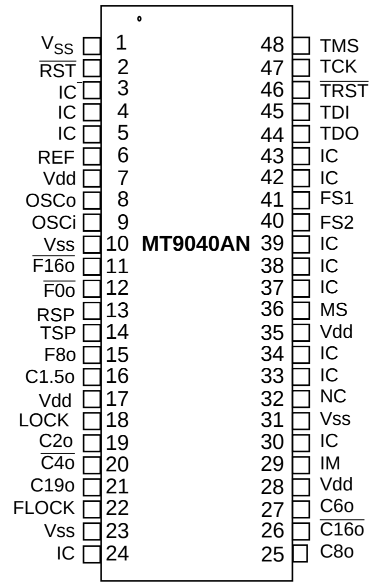


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1,10, 23,31	V_{SS}	**Ground.** 0 Volts. (Vss pads).
2	$\overline{RST}$	**Reset (Input).** A logic low at this input resets the MT9040. To ensure proper operation, the device must be reset after reference signal frequency changes and power-up. The $\overline{RST}$ pin should be held low for a minimum of 300ns. While the $\overline{RST}$ pin is low, all frame and clock outputs are at logic high. Following a reset, the input reference source and output clocks and frame pulses are phase aligned as shown in Figure 9.
3,4,5, 38,43	IC	**Internal Connection.** Leave open circuit.
6	REF	**Reference (Input).** This is the input reference source (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used.
7,17 28,35	V_{DD}	**Positive Supply Voltage.** +3.3V_{DC} nominal.
8	OSCo	**Oscillator Master Clock (CMOS Output).** For crystal operation, a 20MHz crystal is connected from this pin to OSCi, see Figure 6. For clock oscillator operation, this pin is left unconnected, see Figure 5.
9	OSCi	**Oscillator Master Clock (CMOS Input).** For crystal operation, a 20MHz crystal is connected from this pin to OSCo, see Figure 6. For clock oscillator operation, this pin is connected to a clock source, see Figure 5.
11	$\overline{F16o}$	**Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s. See Figure 10.
12	$\overline{F0o}$	**Frame Pulse ST-BUS 2.048Mb/s (CMOS Output).** This is an 8kHz 244ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s. See Figure 10.
13	RSP	**Receive Sync Pulse (CMOS Output).** This is an 8kHz 488ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device. See Figure 11.

Pin Description (continued)

Pin #	Name	Description
14	TSP	**Transmit Sync Pulse (CMOS Output).** This is an 8kHz 488ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device. See Figure 11.
15	F8o	**Frame Pulse (CMOS Output).** This is an 8kHz 122ns active high framing pulse, which marks the beginning of a frame. See Figure 10.
16	C1.5o	**Clock 1.544MHz (CMOS Output).** This output is used in T1 applications.
18	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is frequency locked to the input reference.
19	C2o	**Clock 2.048MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s.
20	$\overline{\text{C4o}}$	**Clock 4.096MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.
21	C19o	**Clock 19.44MHz (CMOS Output).** This output is used in OC3/STS3 applications.
22	FLOCK	**Fast Lock Mode (Input).** Set high to allow the PLL to quickly lock to the input reference (less than 500 ms locking time).
24	IC	**Internal Connection.** Tie low for normal operation.
25	C8o	**Clock 8.192MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192Mb/s.
26	$\overline{\text{C16o}}$	**Clock 16.384MHz (CMOS Output).** This output is used for ST-BUS operation with a 16.384MHz clock.
27	C6o	**Clock 6.312 Mhz (CMOS Output).** This output is used for DS2 applications.
29	IM	**Impairment Monitor (CMOS Output).** A logic high on this pin indicates that the Input Impairment Monitor has automatically put the device into Freerun Mode.
30	IC	**Internal Connection.** Tie high for normal operation.
32	NC	**No Connection.** Leave open circuit**.**
33,34, 42	IC	**Internal Connection.** Tie low for normal operation.
36	MS	**Mode/Control Select (Input).** This input determines the state (Normal or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. See Table 2.
37, 39	IC	**Internal Connection.** Tie low for normal operation.
40	FS2	**Frequency Select 2 (Input).** This input, in conjunction with FS1, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the REF input. See Table 1.
41	FS1	**Frequency Select 1 (Input).** See pin description for FS2.
44	TDO	**Test Serial Data Out (CMOS Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
45	TDI	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}.
46	$\overline{\text{TRST}}$	**Test Reset (Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state.
47	TCK	**Test Clock (Input).** Provides the clock to the JTAG test logic.
48	TMS	**Test Mode Select (Input).** JTAG signal that controls the state transitions of the TAP controller.

Functional Description

The MT9040 is a T1/E1 Trunk Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links. Figure 1 is a functional block diagram which is described in the following sections.

Frequency Select MUX Circuit

The MT9040 operates on the falling edge of the reference. It operates with one of four possible input reference frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). The frequency select inputs (FS1 and FS2) determine which of the four frequencies may be used at the reference input. A reset ($\overline{\text{RST}}$) must be performed after every frequency select input change. See Table 1.

FS2	FS1	Input Frequency
0	0	19.44MHz
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Table 1 - Input Frequency Selection

Digital Phase Lock Loop (DPLL)

As shown in Figure 3, the DPLL of the MT9040 consists of a Phase Detector, Loop Filter, Digitally Controlled Oscillator and a Control Circuit.

Phase Detector - the Phase Detector compares the reference signal with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Loop Filter. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8kHz, 1.544MHz, 2.048MHz or 19.44MHz).

Loop Filter - the Loop Filter is similar to a first order low pass filter with a 1.9 Hz cutoff frequency for all four reference frequency selections (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). This filter ensures that the network jitter transfer requirements are met.

Control Circuit - the Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The two possible modes are Normal and Freerun.

Digitally Controlled Oscillator (DCO) - the DCO receives the filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT9040.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the input reference signal.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20MHz source.

Lock Indicator - If the PLL is in frequency lock (frequency lock means the center frequency of the PLL is identical to the line frequency), and the input phase offset is small, then the lock signal will be set high.

Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 4. The Output Interface Circuit uses four Tapped Delay Lines followed by a T1 Divider Circuit, an E1 Divider Circuit, and a DS2 Divider Circuit to generate the required output signals.

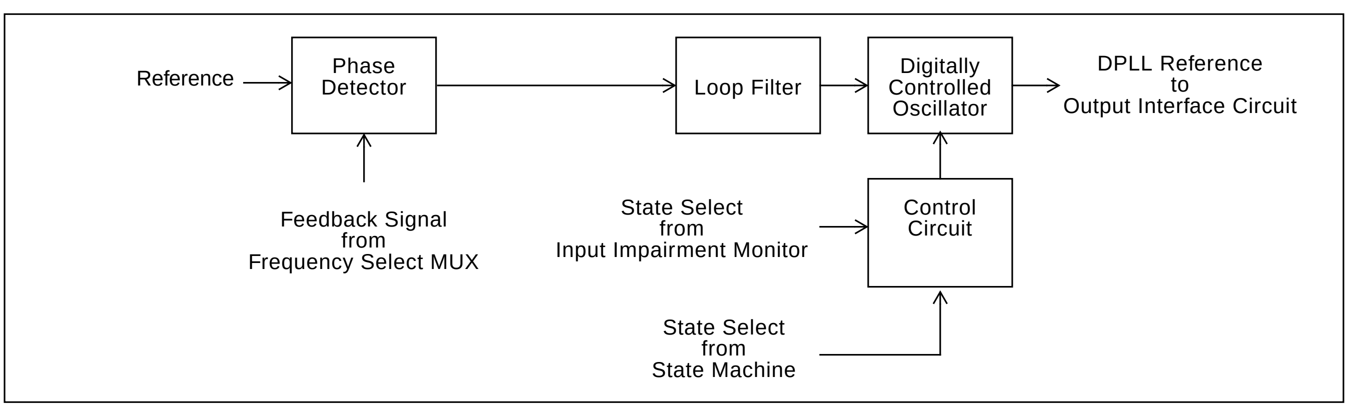


Figure 3 - DPLL Block Diagram

Four tapped delay lines are used to generate 16.384MHz, 12.352MHz, 12.624MHz and 19.44 MHz signals.

The E1 Divider Circuit uses the 16.384MHz signal to generate four clock outputs and five frame pulse outputs. The C8o, $\overline{\text{C4o}}$ and C2o clocks are generated by simply dividing the $\overline{\text{C16o}}$ clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle.

The T1 Divider Circuit uses the 12.384MHz signal to generate the C1.5o clock by dividing the internal C12 clock by eight. This output has a nominal 50% duty cycle.

The DS2 Divider Circuit uses the 12.624 MHz signal to generate the clock output C6o. This output has a nominal 50% duty cycle.

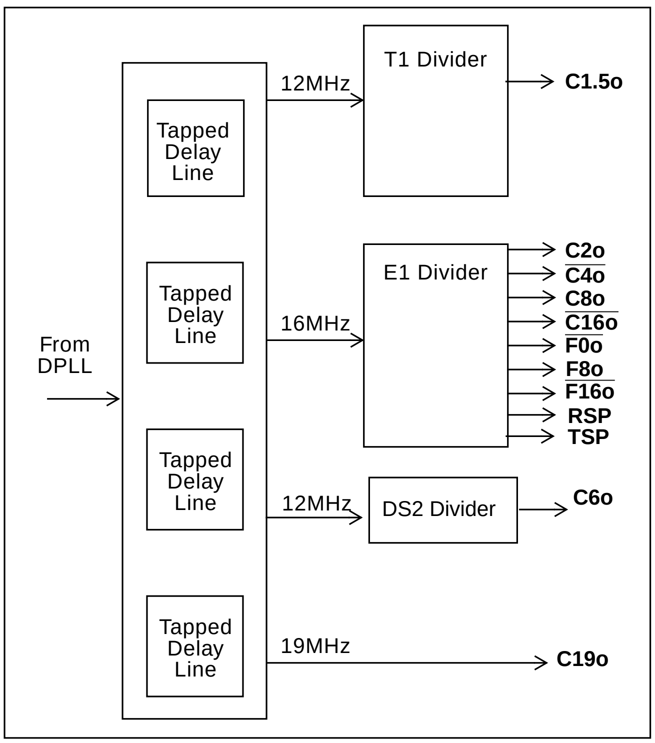


Figure 4 - Output Interface Circuit Block Diagram

The frame pulse outputs ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$, TSP, and RSP) are generated directly from the C16 clock.

The T1 and E1 signals are generated from a common DPLL signal. Consequently, all frame pulse and clock outputs are locked to one another for all operating states, and are also locked to the input reference in Normal Mode. See Figures 9,10 and 11.

All frame pulse and clock outputs have limited driving capability, and should be buffered when driving high capacitance (e.g., 30pF) loads.

Input Impairment Monitor

This circuit monitors the input signal to the DPLL for a complete loss of incoming signal, or a large frequency shift in the incoming signal. If the input signal is outside the Impairment Monitor Capture Range the PLL automatically changes from Normal Mode to Free Run Mode. See AC Electrical Characteristics - Performance for the Impairment Monitor Capture Range. When the incoming signal returns to normal, the DPLL is returned to Normal Mode.

Master Clock

The MT9040 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

Control and Mode of Operation

The MT9040 has two possible modes of operation, Normal and Freerun. As shown in Table 2, the Mode/ Control Select pin MS selects the mode.

MS	Mode
0	NORMAL
1	FREERUN

Table 2 - Operating Modes and States

Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the MT9040 provides timing (C1.5o, C2o, $\overline{\text{C4o}}$, C8o, $\overline{\text{C16o}}$ and C19o) and frame synchronization ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$, TSP and RSP) signals, which are synchronized to the reference input. The input reference signal may have a nominal frequency of 8kHz, 1.544MHz, 2.048MHz or 19.44MHz.

From a reset condition, the MT9040 will take up to 30 seconds (see AC Electrical Characteristics) of input reference signal to output signals which are synchronized (phase locked) to the reference input.

The reference frequencies are selected by the frequency control pins FS2 and FS1 as shown in Table 1.

Fast Lock Mode

Fast Lock Mode is a submode of Normal Mode, it is used to allow the MT9040 to lock to a reference more quickly than Normal mode will allow. Typically, the PLL will lock to the incoming reference within 500 ms if the FLOCK pin is set high.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the MT9040 provides timing and synchronization signals which are based on the master clock frequency (OSCi) only, and are not synchronized to the reference signal.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32ppm output clock is required, the master clock must also be ±32ppm. See Applications - Crystal and Clock Oscillator sections.

MT9040 Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

Intrinsic Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is free running by measuring the output jitter of the device. Intrinsic jitter is usually measured with various bandlimiting filters depending on the applicable standards. In the MT9040, the intrinsic Jitter is limited to less than 0.02UI on the 2.048MHz and 1.544MHz clocks.

Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT9040, the jitter attenuation is determined by the 1.9Hz low pass loop filter.

The MT9040 has twelve outputs with three possible input frequencies (except for 19.44MHz, which is internally divided to 8KHz) for a total of 36 possible jitter transfer functions. Since all outputs are derived from the same signal, the jitter transfer values for the four cases, 8kHz to 8kHz, 1.544MHz to 1.544MHz and 2.048MHz to 2.048MHz can be applied to all outputs.

It should be noted that 1UI at 1.544MHz is 644ns, which is not equal to 1UI at 2.048MHz, which is 488ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

What is the T1 and E1 output jitter when the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB?

$$OutputT1 = InputT1 \times 10^{\left(\frac{-A}{20}\right)}$$

$$OutputT1 = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI(T1)$$

$$OutputE1 = OutputT1 \times \frac{(1UIT1)}{(1UIE1)}$$

$$OutputE1 = OutputT1 \times \frac{(644ns)}{(488ns)} = 3.3UI(T1)$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8kHz, 1.544MHz, 2.048MHz) and outputs (8kHz, 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, 19.44MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT9040, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT9040 capture range is equal to $\pm$230 ppm minus the accuracy of the master clock (OSCi). For example, a 32 ppm master clock results in a capture range of 198 ppm.

Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT9040.

Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

i) initial input to output phase difference

ii) initial input to output frequency difference

iii) synchronizer loop filter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. See AC Electrical Characteristics - Performance for Maximum Phase Lock Time.

MT9040 provides a fast lock pin (FLOCK), which, when set high enables the PLL to lock to an incoming reference within approximately 500 ms.

MT9040 and Network Specifications

The MT9040 fully meets all applicable PLL requirements (intrinsic jitter, jitter/wander tolerance, jitter/wander transfer, frequency accuracy and capture range for the following specifications.

1. Bellcore GR-1244-CORE June 1995 for Stratum 4
2. AT&T TR62411(DS1) December 1990 for Stratum 4
3. ANSI T1.101 (DS1) February 1994 for Stratum 4
4. ETSI 300 011 (E1) April 1992
5. TBR 4 November 1995
6. TBR 12 December 1993
7. TBR 13 January 1996
8. ITU-T I.431 March 1993

Applications

This section contains MT9040 application specific details for clock and crystal operation, reset operation, power supply decoupling, and control operation.

Master Clock

The MT9040 can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be ±100ppm. For applications requiring an accurate Freerun Mode, such as AT&T TR62411, the tolerance of the master timing source must be no greater than ±32ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT9040 will always equal 230ppm. For example, if the master timing source is 100ppm, then the capture range will be 130ppm.

Clock Oscillator - when selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle.

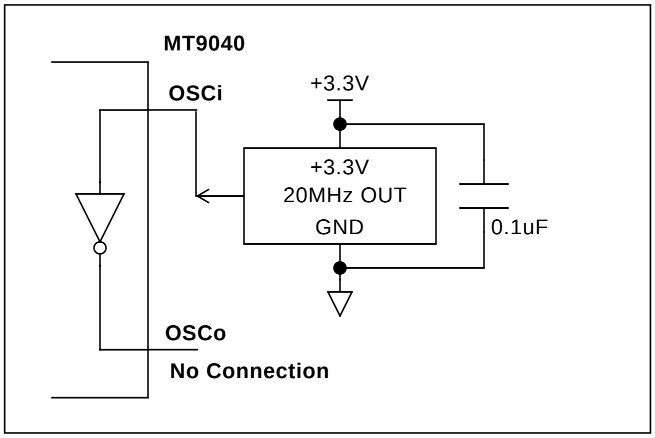


Figure 5 - Clock Oscillator Circuit

For applications requiring ±32ppm clock accuracy, the following clock oscillator module may be used.

FOX F7C-2E3-20.0MHz

Frequency:	*20MHz*
Tolerance:	*25ppm 0C to 70C*
Rise & Fall Time:	*10ns (0.33V 2.97V 15pF)*
Duty Cycle:	*40% to 60%*

CTS CB3LV-5I-20.0 MHz

Frequency:	*20MHz*
Tolerance:	*25ppm*
Rise & Fall Time:	*10ns*
Duty Cycle:	*45% to 55%*

The output clock should be connected directly (not AC coupled) to the OSCi input of the MT9040, and the OSCo output should be left open as shown in Figure 8.

Crystal Oscillator - Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 6.

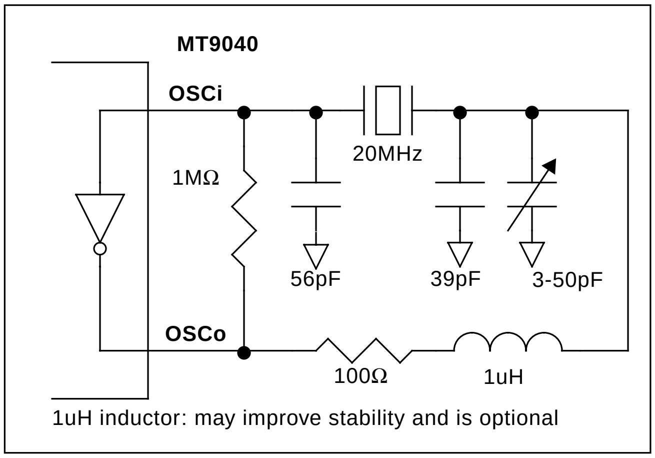


Figure 6 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20MHz crystal specified with a 32pF load capacitance, each 1pF change in load capacitance contributes approximately 9ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 6 may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39pF capacitor may be increased to 56pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

Frequency:	*20MHz*
Tolerance:	*As required*
Oscillation Mode:	*Fundamental*
Resonance Mode:	*Parallel*
Load Capacitance:	*32pF*
Maximum Series Resistance:	*35Ω*
Approximate Drive Level:	*1mW*

e.g., R1B23B32-20.0MHz
(20ppm absolute, ±6ppm 0C to 50C, 32pF, 25Ω)

Reset Circuit

A simple power up reset circuit with about a 50us reset low time is shown in Figure 7. Resistor R_P is for protection only and limits current into the $\overline{\text{RST}}$ pin during power down conditions. The reset low time is not critical but should be greater than 300ns.

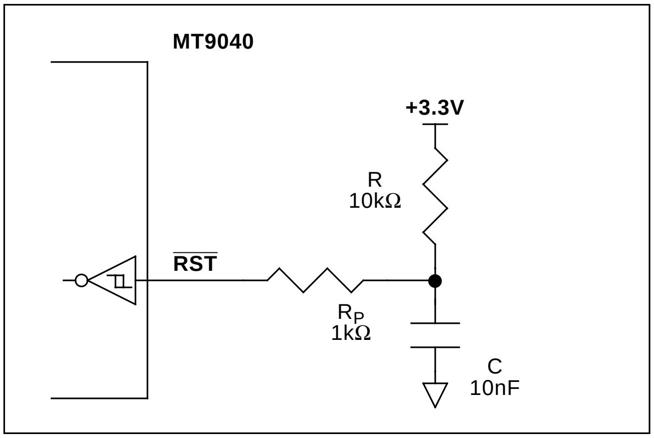


Figure 7 - Power-Up Reset Circuit

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	V_{DD}	-0.5	5.0	V
2	Voltage on any pin	V_{PIN}	-.05	V_{DD}+0.5	V
3	Current on any pin	I_{PIN}	-0.5	30	mA
4	Storage temperature	T_{ST}	-55	125	°C
5	48 SSOP package power dissipation	P_{PD}		200	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Max	Units
1	Supply voltage	V_{DD}	3.0	3.6	V
2	Operating temperature	T_A	-40	85	°C

DC Electrical Characteristics* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Max	Units	Conditions/Notes
1	Supply current with: OSCi = 0V	I_{DDS}		1.8	uA	Outputs unloaded
2	OSCi = Clock	I_{DD}		50	mA	Outputs unloaded
3	CMOS high-level input voltage	V_{CIH}	0.7V_{DD}		V	OSCi
4	CMOS low-level input voltage	V_{CIL}		0.3V_{DD}	V	OSCi
5	Input leakage current	I_{IL}		15	µA	V_I=V_{DD} or 0V
6	High-level output voltage	V_{OH}	2.4		V	I_{OH}= 10 mA
7	Low-level output voltage	V_{OL}		0.4	V	I_{OL}= 10 mA

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

AC Electrical Characteristics - Performance

	Characteristics	Sym	Min	Max	Units	Conditions/ Notes†
1	Freerun Mode accuracy with OSCi at: ±0ppm		-0	+0	ppm	4-8
2	±32ppm		-32	+32	ppm	4-8
3	±100ppm		-100	+100	ppm	4-8
4	Capture range with OSCi at: ±0ppm		-230	+230	ppm	1-3,5-8
5	±32ppm		-198	+198	ppm	1-3,5-8
6	±100ppm		-130	+130	ppm	1-3,5-8
7	Phase lock time			30	s	1-3,5-14
8	Impairment Monitor Capture Range at: 8kHz, 19.44MHz		-18k	+18k	ppm	1-3,5,8,9-11
9	1.544MHz		-36k	+36k	ppm	1-3,6,9-11
10	2.048MHz		-36k	+36k	ppm	1-3,7,9-11

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels* - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	CMOS	Units
1	Threshold Voltage	V_T	$0.5V_{DD}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Timing for input and output signals is based on the worst case result of the CMOS thresholds.
* See Figure 8.

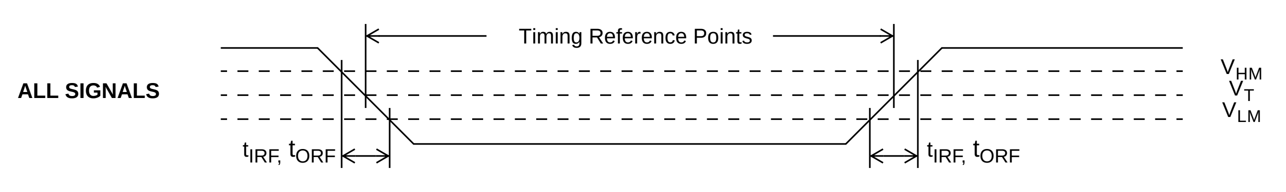
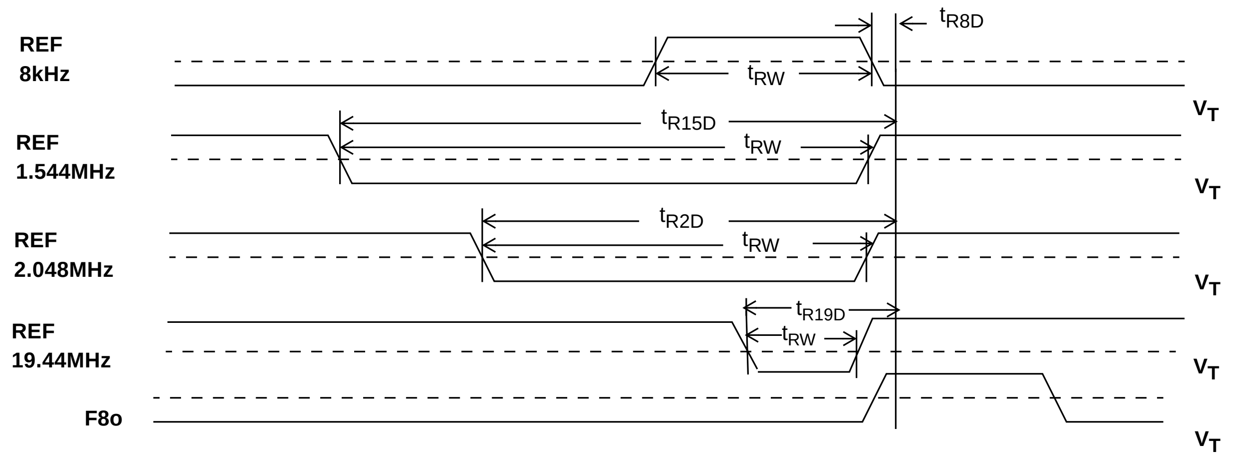


Figure 8 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics - Input/Output Timing

	Characteristics	Sym	Min	Max	Units
1	Reference input pulse width high or low	t_{RW}	100		ns
2	Reference input rise or fall time	t_{IRF}		10	ns
3	8kHz reference input to F8o delay	t_{R8D}	-21	6	ns
4	1.544MHz reference input to F8o delay	t_{R15D}	337	363	ns
5	2.048MHz reference input to F8o delay	t_{R2D}	222	238	ns
6	19.44MHz reference input to F8o delay	t_{R19D}	46	57	ns
7	F8o to $\overline{\text{F0o}}$ delay	t_{F0D}	111	130	ns
8	$\overline{\text{F16o}}$ setup to $\overline{\text{C16o}}$ falling	t_{F16S}	25	40	ns
9	$\overline{\text{F16o}}$ hold to $\overline{\text{C16o}}$ rising	t_{F16H}	-10	10	ns
10	F8o to C1.5o delay	t_{C15D}	-45	-25	ns
11	F8o to C6o delay	t_{C6D}	-10	10	ns
12	F8o to C2o delay	t_{C2D}	-11	5	ns
13	F8o to $\overline{\text{C4o}}$ delay	t_{C4D}	-11	5	ns
14	F8o to C8o delay	t_{C8D}	-11	5	ns
15	F8o to $\overline{\text{C16o}}$ delay	t_{C16D}	-11	5	ns
16	F8o to TSP delay	t_{TSPD}	-6	10	ns
17	F8o to RSP delay	t_{RSPD}	-8	8	ns
18	F8o to C19o delay	t_{C19D}	-15	5	ns
19	C1.5o pulse width high or low	t_{C15W}	309	339	ns
20	C6o pulse width high or low	t_{C6W}	70	86	ns
21	C2o pulse width high or low	t_{C2W}	230	258	ns
22	$\overline{\text{C4o}}$ pulse width high or low	t_{C4W}	111	133	ns
23	C8o pulse width high or low	t_{C8W}	52	70	ns
24	$\overline{\text{C16o}}$ pulse width high or low	t_{C16WL}	24	35	ns
25	TSP pulse width high	t_{TSPW}	478	494	ns
26	RSP pulse width high	t_{RSPW}	474	491	ns
27	C19o pulse width high	t_{C19WH}	25	35	ns
28	C19o pulse width low	t_{C19WL}	17	25	ns
29	$\overline{\text{F0o}}$ pulse width low	t_{F0WL}	234	254	ns
30	F8o pulse width high	t_{F8WH}	109	135	ns
31	$\overline{\text{F16o}}$ pulse width low	t_{F16WL}	47	75	ns
32	Output clock and frame pulse rise or fall time	t_{ORF}		9	ns
33	Input Controls Setup Time	t_S	100		ns
34	Input Controls Hold Time	t_H	100		ns



NOTES:

1. Input to output delay values are valid after a $\overline{\text{RST}}$ with no further state changes

Figure 9 - Input to Output Timing (Normal Mode)

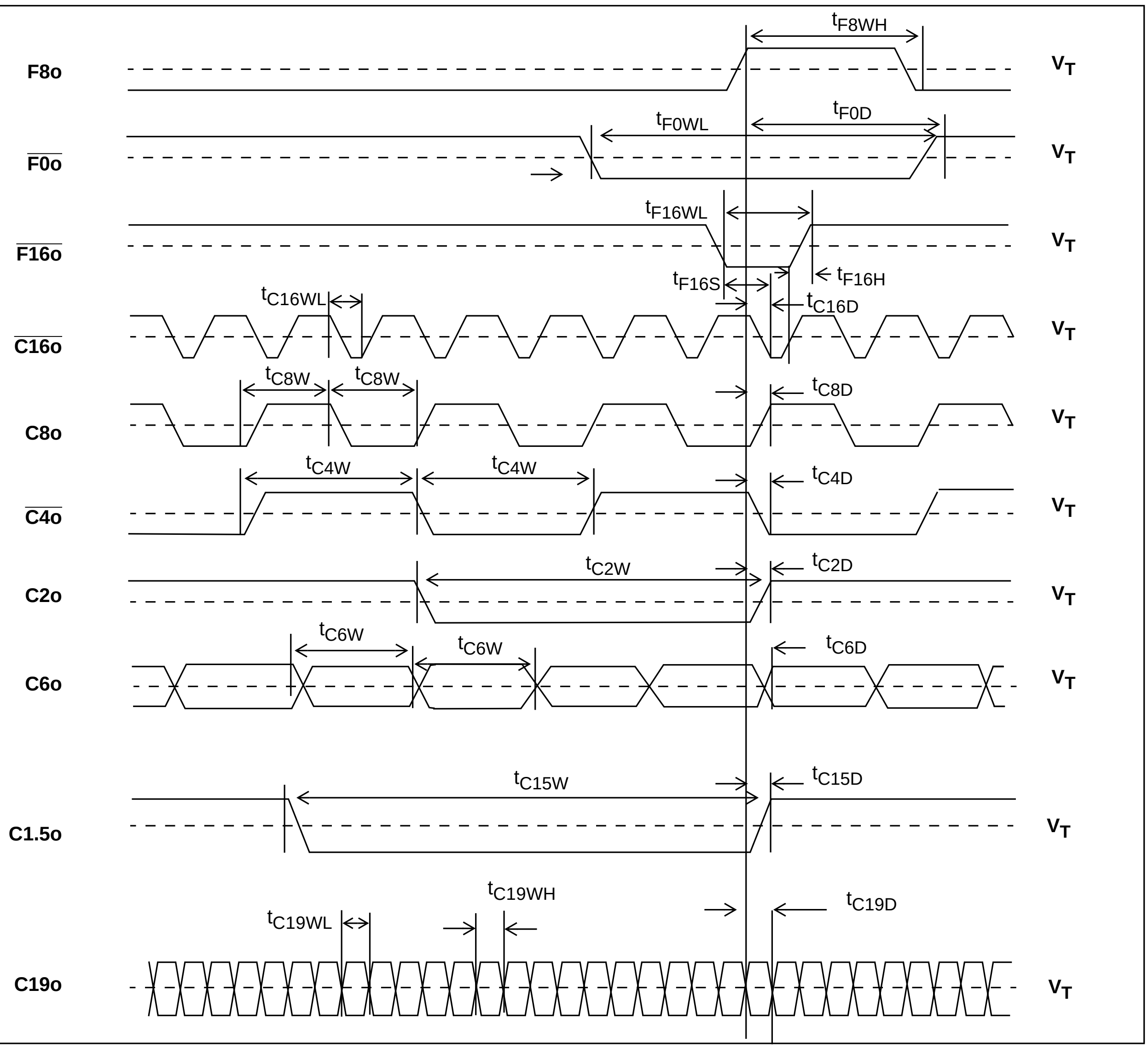


Figure 10 - Output Timing 1

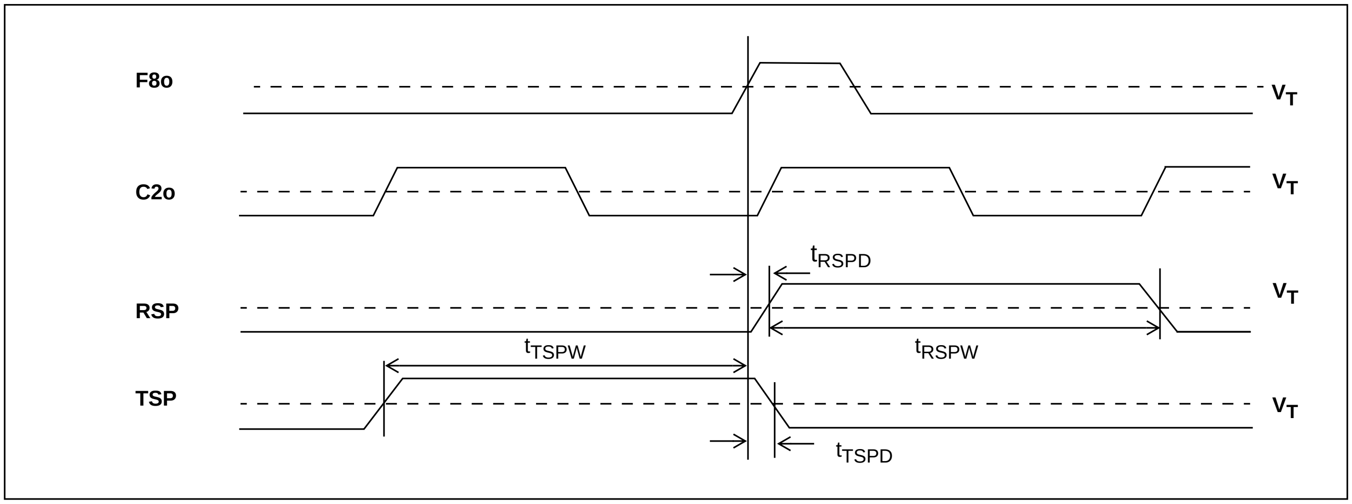


Figure 11 - Output Timing 2

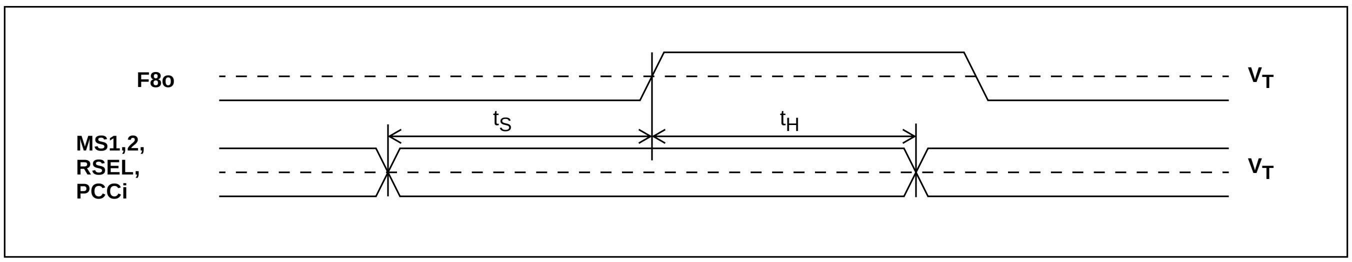


Figure 12 - Input Controls Setup and Hold Timing

AC Electrical Characteristics - Intrinsic Jitter Unfiltered

	Characteristics	Sym	Max	Units	Conditions/Notes†
1	Intrinsic jitter at F8o (8kHz)		0.0002	UIpp	1-12,19-22,26
2	Intrinsic jitter at $\overline{\text{F0o}}$ (8kHz)		0.0002	UIpp	1-12,19-22,26
3	Intrinsic jitter at $\overline{\text{F16o}}$ (8kHz)		0.0002	UIpp	1-12,19-22,26
4	Intrinsic jitter at C1.5o (1.544MHz)		0.030	UIpp	1-12,19-22,27
5	Intrinsic jitter at C2o (2.048MHz)		0.040	UIpp	1-12,19-22,28
6	Intrinsic jitter at C6o (6.312MHz)		0.120	UIpp	1-12,19-22,29
7	Intrinsic jitter at $\overline{\text{C4o}}$ (4.096MHz)		0.080	UIpp	1-12,19-22,30
8	Intrinsic jitter at C8o (8.192MHz)		0.104	UIpp	1-12,19-22,31
9	Intrinsic jitter at $\overline{\text{C16o}}$ (16.384MHz)		0.104	UIpp	1-12,19-22,32
10	Intrinsic jitter at TSP (8kHz)		0.0002	UIpp	1-12,19-22,26
11	Intrinsic jitter at RSP (8kHz)		0.0002	UIpp	1-12,19-22,26
12	Intrinsic jitter at C19o (19.44MHz)		0.27	UIpp	1-12,19-22,33

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - C1.5o (1.544MHz) Intrinsic Jitter Filtered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter (4Hz to 100kHz filter)			0.015	UIpp	1-12,19-22,27
2	Intrinsic jitter (10Hz to 40kHz filter)			0.010	UIpp	1-12,19-22,27
3	Intrinsic jitter (8kHz to 40kHz filter)			0.010	UIpp	1-12,19-22,27
4	Intrinsic jitter (10Hz to 8kHz filter)			0.005	UIpp	1-12,19-22,27

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - C2o (2.048MHz) Intrinsic Jitter Filtered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter (4Hz to 100kHz filter)			0.015	UIpp	1-12,19-22,28
2	Intrinsic jitter (10Hz to 40kHz filter)			0.010	UIpp	1-12,19-22,28
3	Intrinsic jitter (8kHz to 40kHz filter)			0.010	UIpp	1-12,19-22,28
4	Intrinsic jitter (10Hz to 8kHz filter)			0.005	UIpp	1-12,19-22,28

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8kHz Input to 8kHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter attenuation for 1Hz@0.01UIpp input		0	6	dB	1,3,7-12, 19-20, 22, 26, 34
2	Jitter attenuation for 1Hz@0.54UIpp input		6	16	dB	1,3,7-12, 19-20, 22, 26, 34
3	Jitter attenuation for 10Hz@0.10UIpp input		12	22	dB	1,3,7-12, 19-20, 22, 26, 34
4	Jitter attenuation for 60Hz@0.10UIpp input		28	38	dB	1,3,7-12, 19-20, 22, 26, 34
5	Jitter attenuation for 300Hz@0.10UIpp input		42		dB	1,3,7-12, 19-20, 22, 26, 34
6	Jitter attenuation for 3600Hz@0.005UIpp input		45		dB	1,3,7-12, 19-20, 22, 26, 34

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544MHz Input to 1.544MHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter attenuation for 1Hz@20UIpp input		0	6	dB	1,4,7-12, 19-20,22,27,34
2	Jitter attenuation for 1Hz@104UIpp input		6	16	dB	1,4,7-12, 19-20,22,27,34
3	Jitter attenuation for 10Hz@20UIpp input		12	22	dB	1,4,7-12, 19-20,22,27,34
4	Jitter attenuation for 60Hz@20UIpp input		28	38	dB	1,4,7-12, 19-20,22,27,34
5	Jitter attenuation for 300Hz@20UIpp input		42		dB	1,4,7-12, 19-20,22,27,34
6	Jitter attenuation for 10kHz@0.3UIpp input		45		dB	1,4,7-12, 19-20,22,27,34
7	Jitter attenuation for 100kHz@0.3UIpp input		45		dB	1,4,7-12, 19-20,22,27,34

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048MHz Input to 2.048MHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter at output for 1Hz@3.00UIpp input with 40Hz to 100kHz filter			2.9	UIpp	1,5,7-12,19-20, 22,28,34
2				0.09	UIpp	1,5,7-12,19-20, 22,28,35
3	Jitter at output for 3Hz@2.33UIpp input with 40Hz to 100kHz filter			1.3	UIpp	1,5,7-12,19-20, 22,28,34
4				0.10	UIpp	1,5,7-12,19-20, 22,28,35
5	Jitter at output for 5Hz@2.07UIpp input with 40Hz to 100kHz filter			0.80	UIpp	1,5,7-12,19-20, 22,28,34
6				0.10	UIpp	1,5,7-12,19-20, 22,28,35
7	Jitter at output for 10Hz@1.76UIpp input with 40Hz to 100kHz filter			0.40	UIpp	1,5,7-12,19-20, 22,28,34
8				0.10	UIpp	1,5,7-12,19-20, 22,28,35
9	Jitter at output for 100Hz@1.50UIpp input with 40Hz to 100kHz filter			0.06	UIpp	1,5,7-12,19-20, 22,28,34
10				0.05	UIpp	1,5,7-12,19-20, 22,28,35
11	Jitter at output for 2400Hz@1.50UIpp input with 40Hz to 100kHz filter			0.04	UIpp	1,5,7-12,19-20, 22,28,34
12				0.03	UIpp	1,5,7-12,19-20, 22,28,35
13	Jitter at output for 100kHz@0.20UIpp input with 40Hz to 100kHz filter			0.04	UIpp	1,5,7-12,19-20, 22,28,34
14				0.02	UIpp	1,5,7-12,19-20, 22,28,33

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8kHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		0.80		UIpp	1,3,7 -12,19-20,22-24,26
2	Jitter tolerance for 5Hz input		0.70		UIpp	1,3,7 -12,19-20,22-24,26
3	Jitter tolerance for 20Hz input		0.60		UIpp	1,3,7 -12,19-20,22-24,26
4	Jitter tolerance for 300Hz input		0.20		UIpp	1,3,7 -12,19-20,22-24,26
5	Jitter tolerance for 400Hz input		0.15		UIpp	1,3,7 -12,19-20,22-24,26
6	Jitter tolerance for 700Hz input		0.08		UIpp	1,3,7 -12,19-20,22-24,26
7	Jitter tolerance for 2400Hz input		0.02		UIpp	1,3,7 -12,19-20,22-24,26
8	Jitter tolerance for 3600Hz input		0.01		UIpp	1,3,7 -12,19-20,22-24,26

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544MHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		150		UIpp	1,4,7-12,19-20,22-24,27
2	Jitter tolerance for 5Hz input		140		UIpp	1,4,7-12,19-20,22-24,27
3	Jitter tolerance for 20Hz input		130		UIpp	1,4,7-12,19-20,22-24,27
4	Jitter tolerance for 300Hz input		35		UIpp	1,4,7-12,19-20,22-24,27
5	Jitter tolerance for 400Hz input		25		UIpp	1,4,7-12,19-20,22-24,27
6	Jitter tolerance for 700Hz input		15		UIpp	1,4,7-12,19-20,22-24,27
7	Jitter tolerance for 2400Hz input		4		UIpp	1,4,7-12,19-20,22-24,27
8	Jitter tolerance for 10kHz input		1		UIpp	1,4,7-12,19-20,22-24,27
9	Jitter tolerance for 100kHz input		0.5		UIpp	1,4,7-12,19-20,22-24,27

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048MHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		150		UIpp	1,5,7 -12,19-20,22-24,28
2	Jitter tolerance for 5Hz input		140		UIpp	1,5,7 -12,19-20,22-24,28
3	Jitter tolerance for 20Hz input		130		UIpp	1,5,7 -12,19-20,22-24,28
4	Jitter tolerance for 300Hz input		50		UIpp	1,5,7 -12,19-20,22-24,28
5	Jitter tolerance for 400Hz input		40		UIpp	1,5,7 -12,19-20,22-24,28
6	Jitter tolerance for 700Hz input		20		UIpp	1,5,7 -12,19-20,22-24,28
7	Jitter tolerance for 2400Hz input		5		UIpp	1,5,7 -12,19-20,22-24,28
8	Jitter tolerance for 10kHz input		1		UIpp	1,5,7 -12,19-20,22-24,28
9	Jitter tolerance for 100kHz input		1		UIpp	1,5,7 -12,19-20,22-24,28

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - OSCi 20MHz Master Clock Input

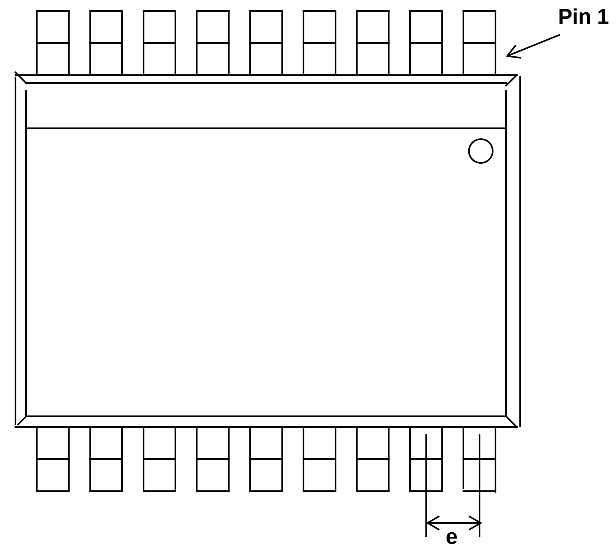
	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Tolerance		-0	+0	ppm	13,16
2			-32	+32	ppm	14,17
3			-100	+100	ppm	15,18
4	Duty cycle		40	60	%	
5	Rise time			10	ns	
6	Fall time			10	ns	

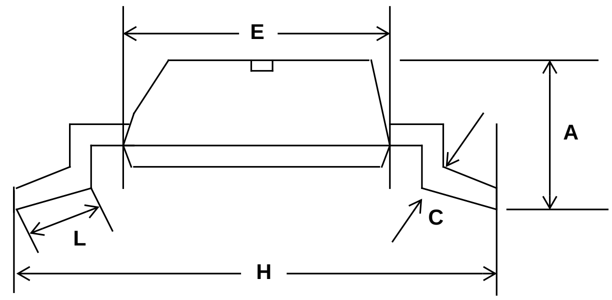
† See "Notes" following AC Electrical Characteristics tables.

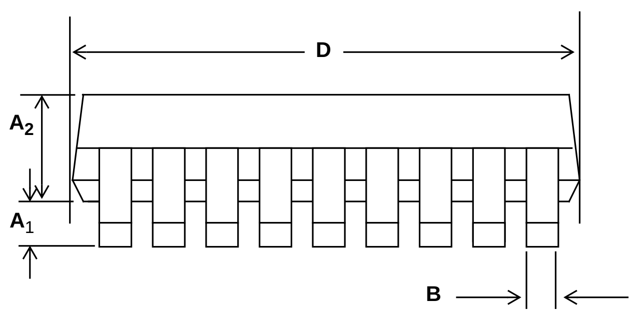
† Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Supply voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1. Normal Mode selected.
2. Freerun Mode selected.
3. 8kHz Frequency Mode selected.
4. 1.544MHz Frequency Mode selected.
5. 2.048MHz Frequency Mode selected.
6. 19.44MHz Frequency Mode selected.
7. Master clock input OSCi at 20MHz ±0ppm.
8. Master clock input OSCi at 20MHz ±32ppm.
9. Master clock input OSCi at 20MHz ±100ppm.
10. Reference input at ±0ppm.
11. Reference input at ±32ppm.
12. Reference input at ±100ppm.
13. For Freerun Mode of ±0ppm.
14. For Freerun Mode of ±32ppm.
15. For Freerun Mode of ±100ppm.
16. For capture range of ±230ppm.
17. For capture range of ±198ppm.
18. For capture range of ±130ppm.
19. 25pF capacitive load.
20. OSCi Master Clock jitter is less than 2nspp, or 0.04UIpp where1UIpp=1/20MHz.
21. Jitter on reference input is less than 7nspp.
22. Applied jitter is sinusoidal.
23. Minimum applied input jitter magnitude to regain synchronization.
24. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
25. Within 10ms of the state, reference or input change.
26. 1UIpp = 125us for 8kHz signals.
27. 1UIpp = 648ns for 1.544MHz signals.
28. 1UIpp = 488ns for 2.048MHz signals.
29. 1UIpp = 158ns for 6.312MHz signals.
30. 1UIpp = 244ns for 4.096MHz signals.
31. 1UIpp = 122ns for 8.192MHz signals.
32. 1UIpp = 61ns for 16.384MHz signals.
33. 1UIpp = 51.44ns for 19.44MHz signals.
34. No filter.
35. 40Hz to 100kHz bandpass filter.
36. With respect to reference input signal frequency.
37. After a $\overline{\text{RST}}$.
38. Master clock duty cycle 40% to 60%.







Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) Ref. JEDEC Standard M0-150/M0118 for 48 Pin
5) A & B Maximum dimensions include allowable mold flash

Dim	20-Pin		24-Pin		28-Pin		48-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max
A		0.079 (2)	-	0.079 (2)		0.079 (2)	0.095 (2.41)	0.110 (2.79)
A_1	0.002 (0.05)		0.002 (0.05)		0.002 (0.05)		0.008 (0.2)	0.016 (0.406)
B	0.0087 (0.22)	0.013 (0.33)	0.0087 (0.22)	0.013 (0.33)	0.0087 (0.22)	0.013 (0.33)	0.008 (0.2)	0.0135 (0.342)
C		0.008 (0.21)		0.008 (0.21)		0.008 (0.21)		0.010 (0.25)
D	0.27 (6.9)	0.295 (7.5)	0.31 (7.9)	0.33 (8.5)	0.39 (9.9)	0.42 (10.5)	0.62 (15.75)	0.63 (16.00)
E	0.2 (5.0)	0.22 (5.6)	0.2 (5.0)	0.22 (5.6)	0.2 (5.0)	0.22 (5.6)	0.291 (7.39)	0.299 (7.59)
e	0.025 BSC (0.635 BSC)		0.025 BSC (0.635 BSC)		0.025 BSC (0.635 BSC)		0.025 BSC (0.635 BSC)	
A_2	0.065 (1.65)	0.073 (1.85)	0.065 (1.65)	0.073 (1.85)	0.065 (1.65)	0.073 (1.85)	0.089 (2.26)	0.099 (2.52)
H	0.29 (7.4)	0.32 (8.2)	0.29 (7.4)	0.32 (8.2)	0.29 (7.4)	0.32 (8.2)	0.395 (10.03)	0.42 (10.67)
L	0.022 (0.55)	0.037 (0.95)	0.022 (0.55)	0.037 (0.95)	0.022 (0.55)	0.037 (0.95)	0.02 (0.51)	0.04 (1.02)

Small Shrink Outline Package (SSOP) - N Suffix

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