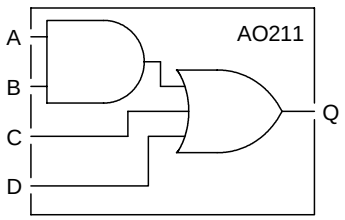
AO211 is an AND/OR circuit providing the logical function Q = (A.B+C+D).

Truth Table

A	B	C	D	Q
L	X	L	L	L
X	L	L	L	L
X	X	X	H	H
X	X	H	X	H
H	H	X	X	H



Capacitance

	Ci (pF)
A	0.058
B	0.053
C	0.044
D	0.044

Area

0.95 mils^2

Power

3.44 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.65	2.06	2.71	0.85	2.23	2.88
	tpdaf	0.65	1.76	2.33	0.77	1.90	2.42
Delay B to Q	tpdbr	0.66	2.06	2.74	0.76	2.13	2.79
	tpdbf	0.70	1.82	2.39	0.82	1.94	2.49
Delay C to Q	tpdcr	0.61	1.96	2.71	0.89	2.25	2.88
	tpdcf	0.64	1.76	2.34	0.78	1.90	2.45
Delay D to Q	tpddr	0.54	1.89	2.64	0.77	2.12	2.78
	tpddf	0.57	1.68	2.26	0.79	1.89	2.46
Output Slope A to Q	op_slar	0.98	5.30	7.53	0.92	5.27	7.50
	op_slaf	0.71	3.48	5.01	0.73	3.56	5.28
Output Slope B to Q	op_slbr	0.98	5.30	7.52	0.93	5.26	7.48
	op_slbf	0.71	3.58	4.98	0.71	3.76	4.98
Output Slope C to Q	op_slcr	0.93	5.30	7.40	0.91	5.25	7.47
	op_slcf	0.71	3.61	5.28	0.73	3.52	5.08
Output Slope D to Q	op_sldr	0.91	5.30	7.52	0.88	5.22	7.47
	op_sldf	0.71	3.67	5.00	0.72	3.48	5.07