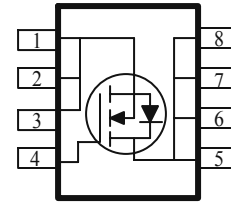
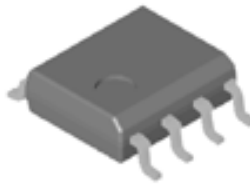


N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	26 @ $V_{GS} = 4.5V$	9.0
	50 @ $V_{GS} = 2.5V$	6.5



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	± 9.0	A
	$T_A = 70^\circ C$		± 7.3	
Pulsed Drain Current ^b		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	2.3	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	3.1	W
	$T_A = 70^\circ C$		2.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	$R_{\theta JA}$	50	$^\circ C/W$
	Steady State		92	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		1.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	uA
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = \pm 12\text{ V}$	20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$			26	m Ω
		$V_{GS} = 2.5\text{ V}, I_D = 6.5\text{ A}$			50	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 9\text{ A}$		40		S
Diode Forward Voltage	V_{SD}	$I_S = 2.3\text{ A}, V_{GS} = 0\text{ V}$		0.7		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V},$ $I_D = 9\text{ A}$		5.5		nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_G			1.3		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25\text{ V}, R_L = 25\text{ }\Omega, I_D = 1\text{ A},$ $V_{GEN} = 10\text{ V}$		20		nS
Rise Time	t_r			9		
Turn-Off Delay Time	$t_{d(off)}$			70		
Fall-Time	t_f			20		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\text{ A}, Di/Dt = 100\text{ A/uS}$		41		

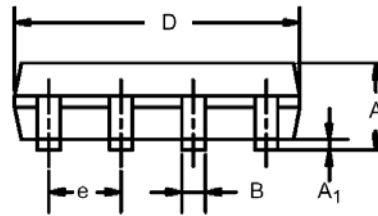
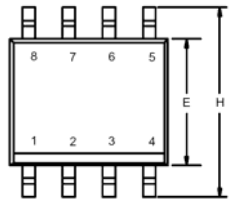
Notes

- Pulse test: PW \leq 300us duty cycle \leq 2%.
- Guaranteed by design, not subject to production testing.

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Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

