REVISION HISTORY

REVISION	DESCRIPTION	Released Date
Preliminary Rev. 0.5	1. Original.	Mar, 2001
Rev. 1.0	1. The symbols CE# and OE# and WE# are revised as. $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2. Separate Industrial and Commercial SPEC. 3. Add access time 55ns range.	Jun 21, 2001
Rev. 1.1	1. The extended temperature range is revised. -20℃~80℃⇨-20℃~85℃	Aug 24, 2001
Rev. 1.2	1. Revised Power supply a、 55ns (max.) for Vcc=2.7V~3.6V b、 70/100ns (max.) for Vcc=2.5V~3.6V 2. Revised block diagram 3. Revised DC ELECTRICAL CHARACTERISTICS： a、 Revised V_{IH} as 2.2V b、 Revised standby current I_{SB1} of LL-version Typical : 3uA⇨2uA Maximum : 25uA⇨20uA 4. Revised AC ELECTRICAL CHARACTERISTICS： c、 Revised symbol name t_{HZB} as t_{BHZ} d、 Revised symbol name t_{LZB} as t_{BLZ} e、 Revised symbol name t_{PWB} as t_{BW} f、 Revised t_{BLZ} as 10ns (min.) g、 Revised t_{OH} as 10ns (min.) 5. Revised waveforms 6. Revised 48-pin TFBGA package outline dimension： h、 Rev. 1.1 ball diameter=0.3mm i、 Rev. 1.2 ball diameter=0.35mm	Apr 15, 2002
Rev. 1.3	Order information : add 100ns parts	Aug 05, 2002
Rev. 1.4	Add order information for lead free product	May 09, 2003

FEATURES

- Fast access time :
  55ns (max.) for Vcc=2.7V~3.6V
  70/100ns (max.) for Vcc=2.5V~3.6V
- CMOS low power operating
  Operating current : 45/35/25mA (Icc max.)
  Standby current : 20uA (typ.) L-version
  2uA (typ.) LL-version
- Single 2.5V~3.6V power supply
- Operating temperature :
  Commercial : 0℃~70℃
  Extended : -20℃~85℃
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min.)
- Data byte control : $\overline{LB}$ (I/O1~I/O8)
  $\overline{UB}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP-Ⅱ
  48-pin 6mm × 8mm TFBGA

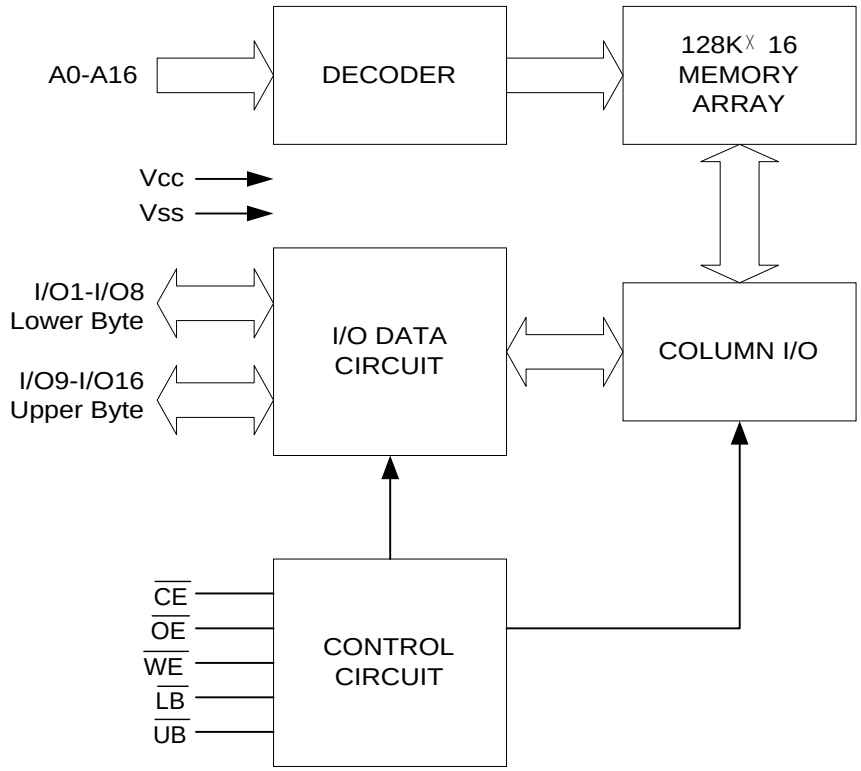
GENERAL DESCRIPTION

The UT62L12816 is a 2,097,152-bit low power CMOS static random access memory organized as 131,072 words by 16 bits.

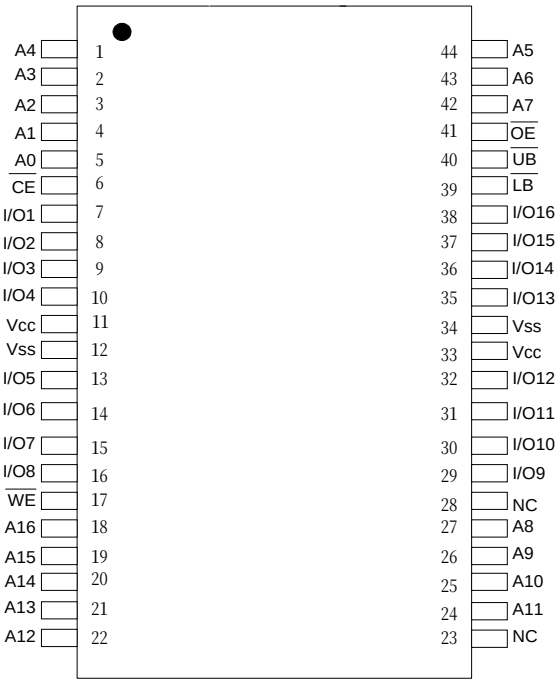
The UT62L12816 operates from a single 2.5V~3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L12816 is designed for low power system applications.

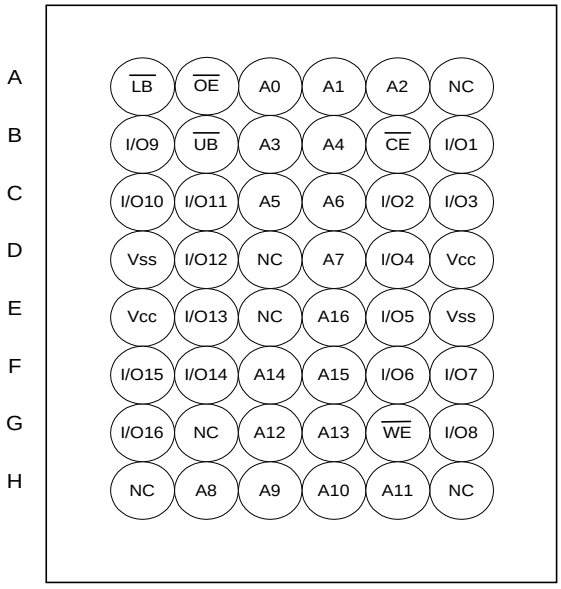
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSOP II



TFBGA

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Control
$\overline{UB}$	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	L	X	High – Z	High – Z	I_{CC},I_{CC1},I_{CC2}
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D_{OUT}	High – Z	I_{CC},I_{CC1},I_{CC2}
	L	L	H	H	L	High – Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High – Z	I_{CC},I_{CC1},I_{CC2}
	L	X	L	H	L	High – Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70	℃
	Extended	T_A	-20 to 85	℃
Storage Temperature		T_{STG}	-65 to +150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5V~3.6V, T_A = 0℃ to 70℃ / -20℃ to 85℃(E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}		55	2.7	3.0	3.6	V
			70/100	2.5	--	3.6	V
Input High Voltage	V_{IH}*1			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}*2			-0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC;}$ Output Disable		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH}= -1mA		2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty $I_{I/O}$=0mA, $\overline{CE}$=V_{IL}	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
Average Operation Current	Icc1	100%duty, $I_{I/O}$=0mA $\overline{CE} \leqq$0.2V, other pins at 0.2V or Vcc-0.2V	TCycle= 1μs	-	4	5	mA
	Icc2		TCycle= 500ns	-	8	10	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$=V_{IH}, other pins =V_{IL} or V_{IH}		-	0.3	0.5	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}$=V_{CC}-0.2V other pins at 0.2V or Vcc-0.2V	-L	-	20	80	μA
			-LL	-	2	20	μA

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 10ns.
2. Undershoot : Vss-3.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE (T_A=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -1mA/2.1mA

AC ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C / -20°C to 85°C(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L12816-55 V_{CC} =2.7V~3.6V		UT62L12816-70 V_{CC} =2.5V~3.6V		UT62L12816-100 V_{CC} =2.5V~3.6V		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	55	-	70	-	100	ns
$\overline{LB}$, $\overline{UB}$ to High-Z Output	t_{BHZ}	-	25	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	t_{BLZ}	10	-	10	-	10	-	ns

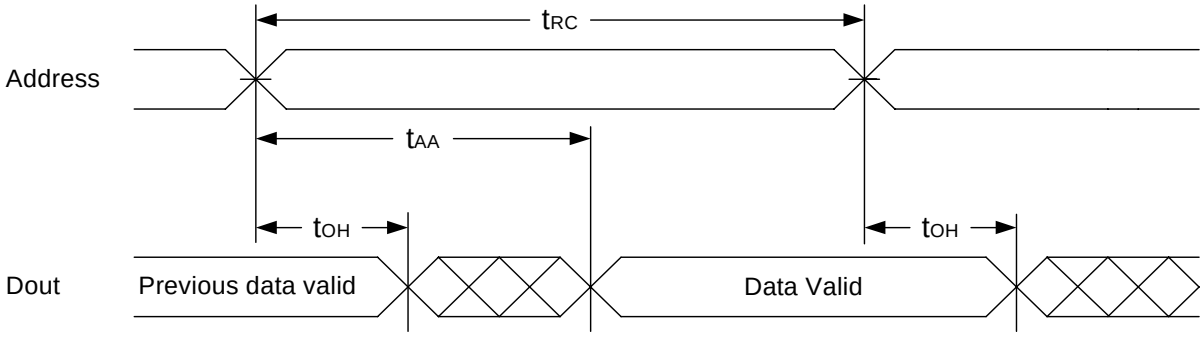
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L12816-55 V_{CC} =2.7V~3.6V		UT62L12816-70 V_{CC} =2.5V~3.6V		UT62L12816-100 V_{CC} =2.5V~3.6V		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	45	-	60	-	80	-	ns

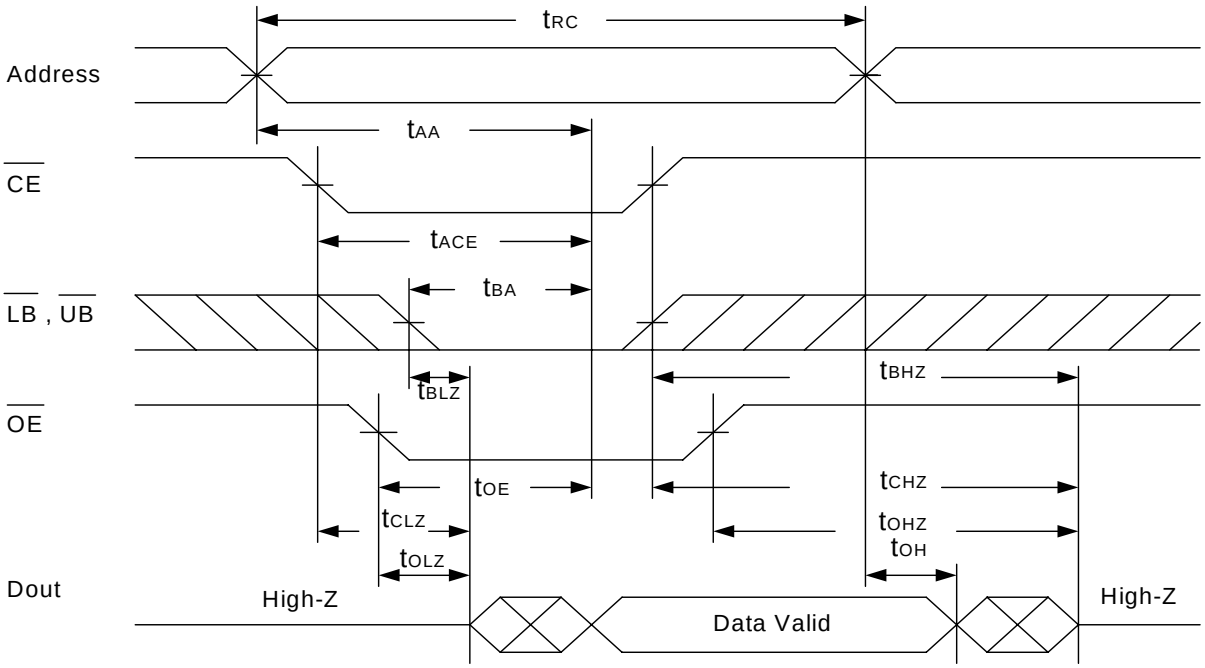
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



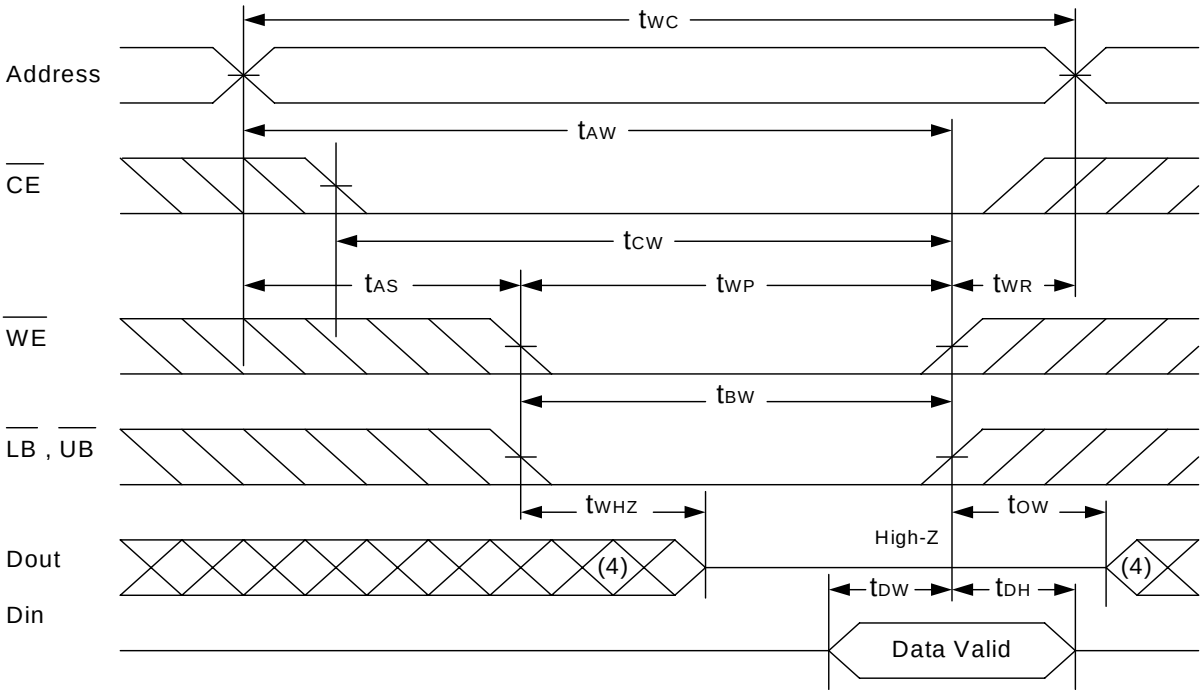
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,4,5)



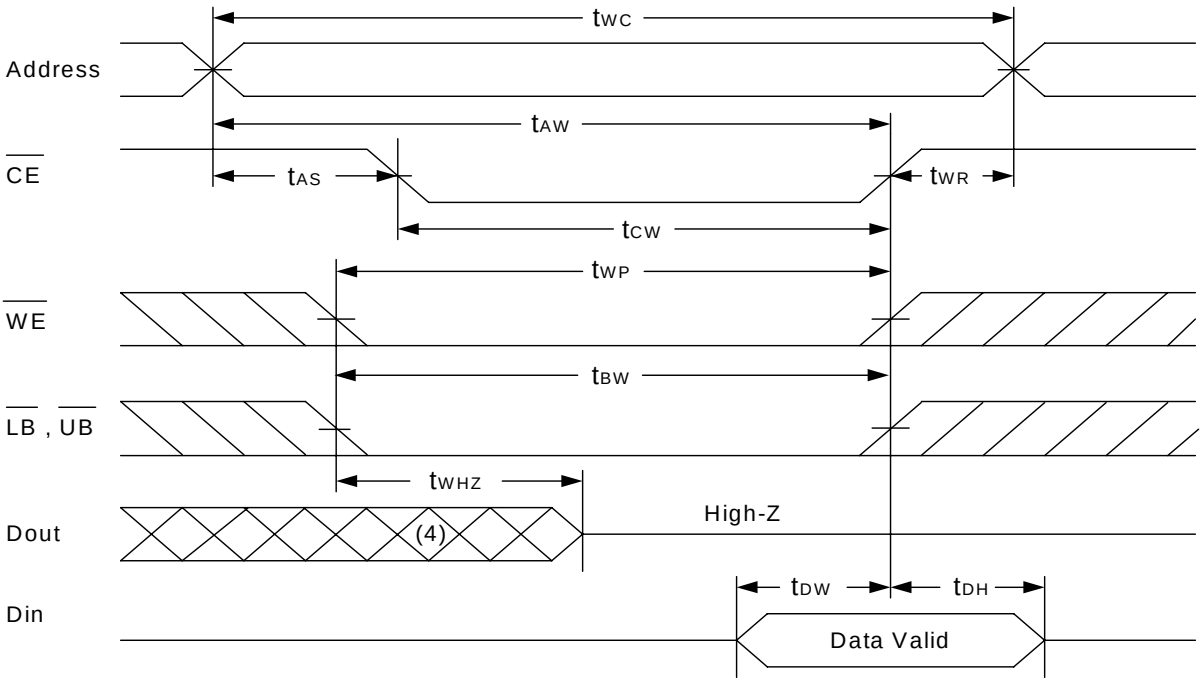
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low, $\overline{LB}$ or $\overline{UB}$ =low.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, $\overline{LB}$ or $\overline{UB}$ =low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

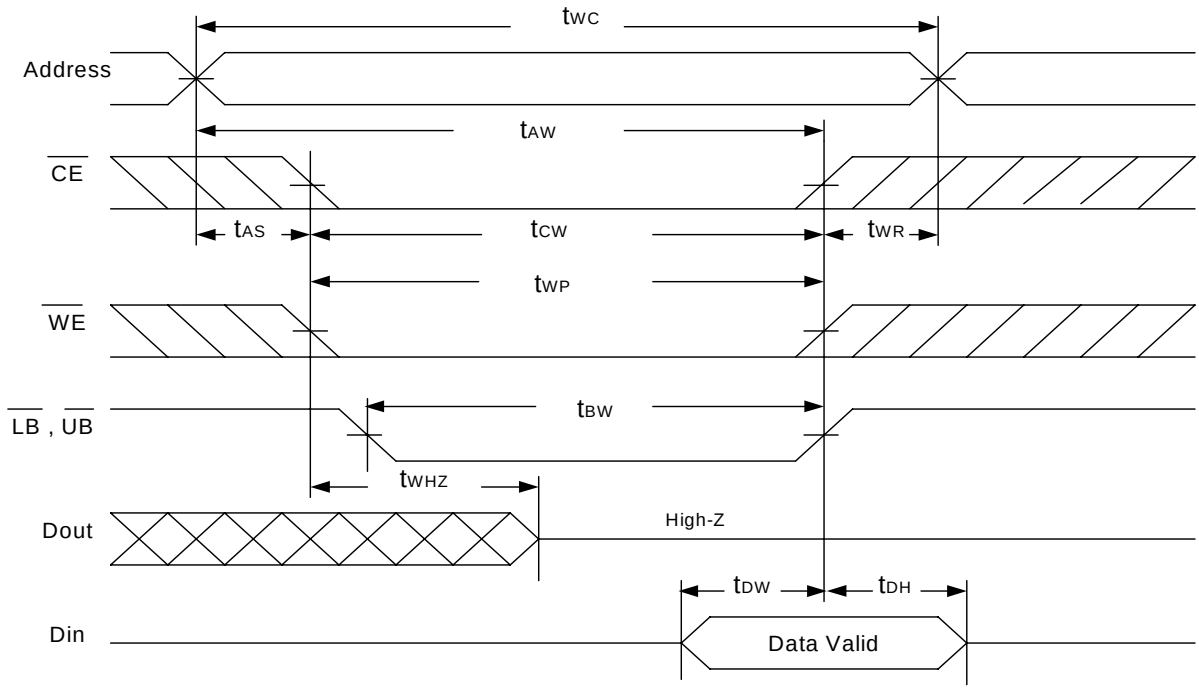
WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5,6)



WRITE CYCLE 3 ($\overline{LB}$, $\overline{UB}$ Controlled) (1,2,5,6)



Notes :

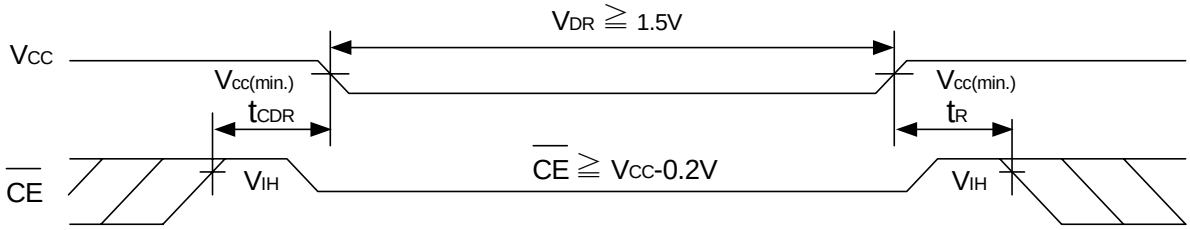
1. $\overline{WE}$, $\overline{CE}$, $\overline{LB}$, $\overline{UB}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, low $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ =low.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$, $\overline{LB}$, $\overline{UB}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured $\pm$500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = 0℃ to 70℃ / -20℃ to 85℃(E))

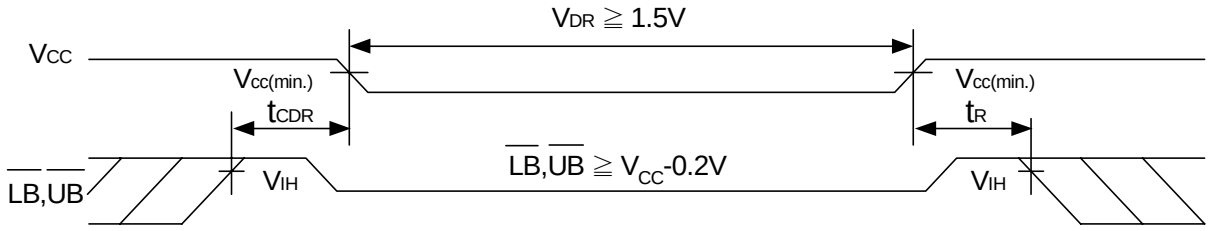
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=1.5V	- L	-	1	50	µA
		$\overline{CE} \geqq V_{CC}$-0.2V	- LL	-	0.5	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ms
Recovery Time	t_R			5	-	-	ms

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE}$ controlled)

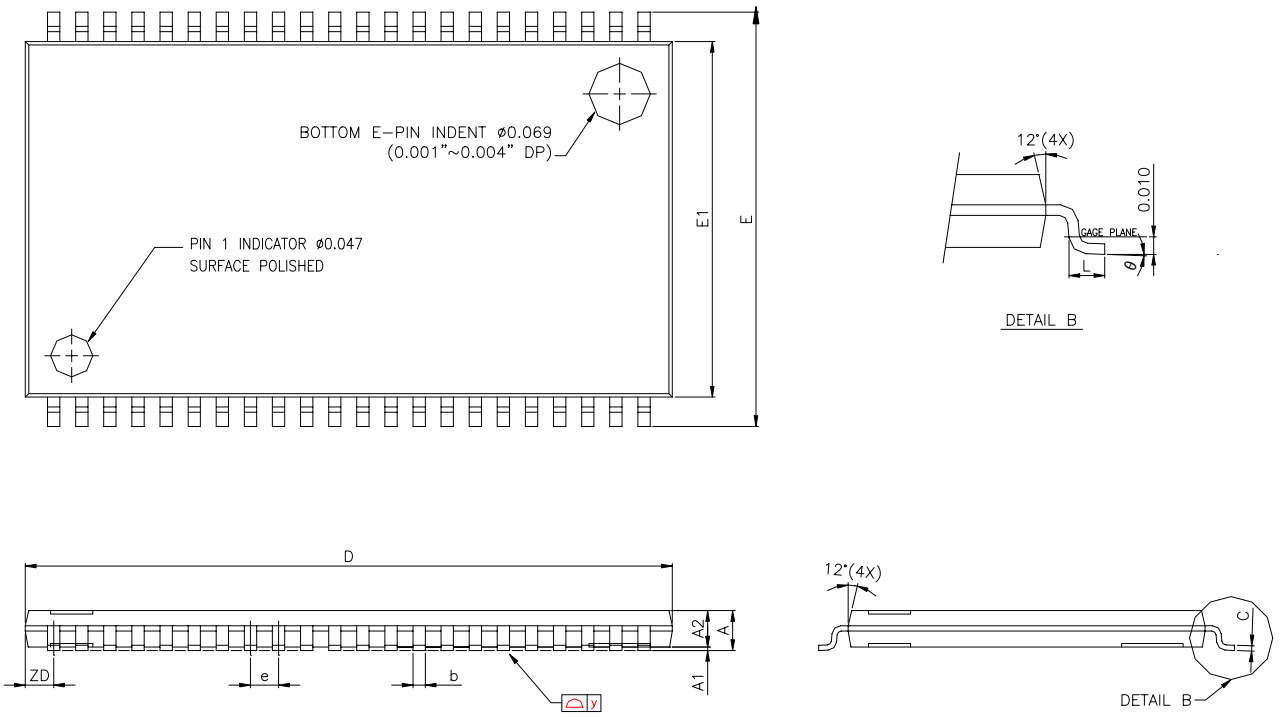


Low Vcc Data Retention Waveform (2) ($\overline{LB}$, $\overline{UB}$ controlled)



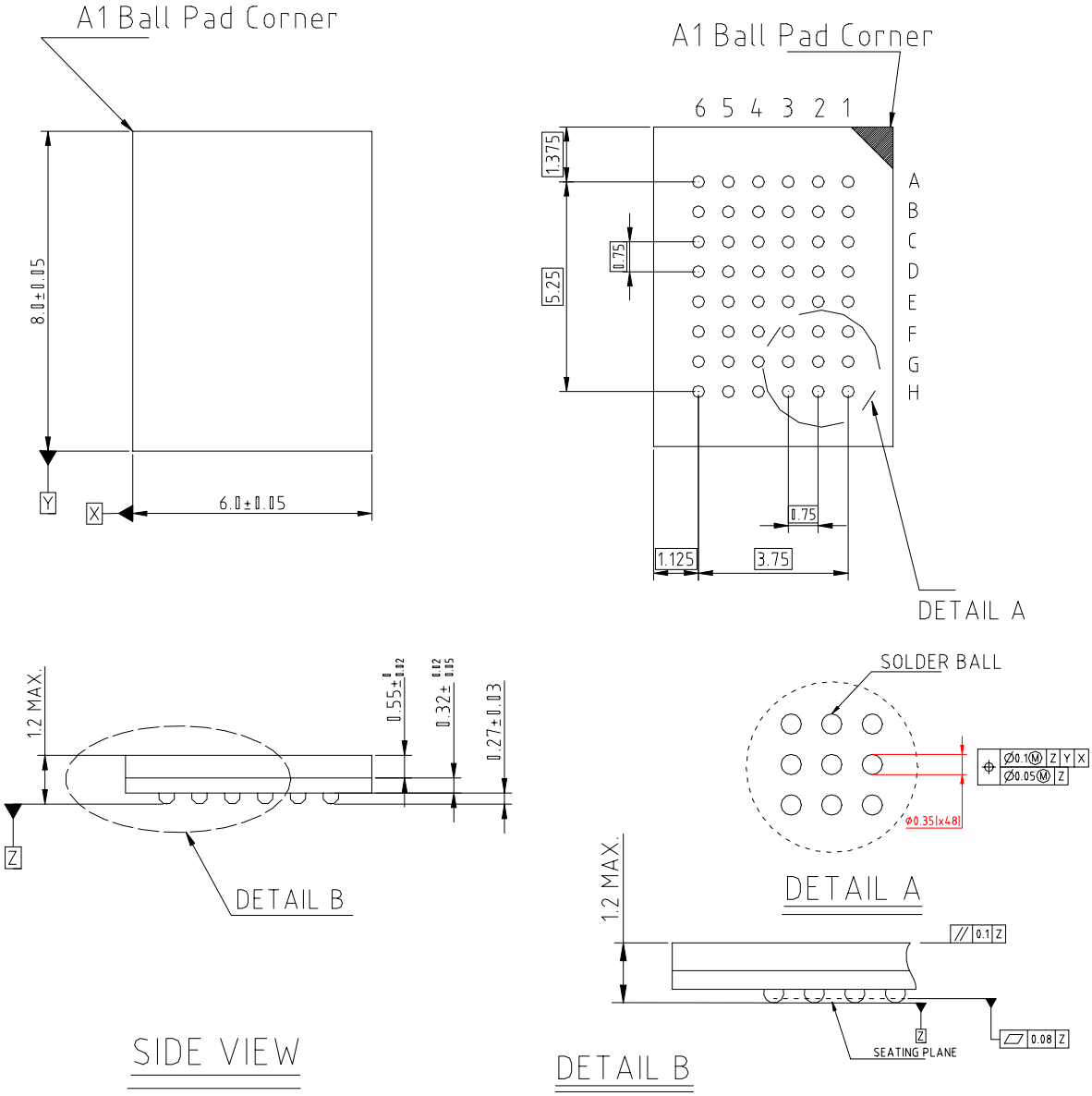
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-Ⅱ Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0^o	-	5^o	0^o	-	5^o

48-pin 6mm × 8mm TFBGA Package Outline Dimension



ORDERING INFORMATION

COMMERCIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L12816MC-55L	55	20	44 PIN TSOP-II
UT62L12816MC-55LL	55	2	44 PIN TSOP-II
UT62L12816MC-70L	70	20	44 PIN TSOP-II
UT62L12816MC-70LL	70	2	44 PIN TSOP-II
UT62L12816MC-100L	100	20	44 PIN TSOP-II
UT62L12816MC-100LL	100	2	44 PIN TSOP-II
UT62L12816BS-55L	55	20	48 PIN TFBGA
UT62L12816BS-55LL	55	2	48 PIN TFBGA
UT62L12816BS-70L	70	20	48 PIN TFBGA
UT62L12816BS-70LL	70	2	48 PIN TFBGA
UT62L12816BS-100L	100	20	48 PIN TFBGA
UT62L12816BS-100LL	100	2	48 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L12816MC-55LE	55	20	44 PIN TSOP-II
UT62L12816MC-55LLE	55	2	44 PIN TSOP-II
UT62L12816MC-70LE	70	20	44 PIN TSOP-II
UT62L12816MC-70LLE	70	2	44 PIN TSOP-II
UT62L12816MC-100LE	100	20	44 PIN TSOP-II
UT62L12816MC-100LLE	100	2	44 PIN TSOP-II
UT62L12816BS-55LE	55	20	48 PIN TFBGA
UT62L12816BS-55LLE	55	2	48 PIN TFBGA
UT62L12816BS-70LE	70	20	48 PIN TFBGA
UT62L12816BS-70LLE	70	2	48 PIN TFBGA
UT62L12816BS-100LE	100	20	48 PIN TFBGA
UT62L12816BS-100LLE	100	2	48 PIN TFBGA

ORDERING INFORMATION (for lead free product)

COMMERCIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L12816MCL-55L	55	20	44 PIN TSOP-II
UT62L12816MCL-55LL	55	2	44 PIN TSOP-II
UT62L12816MCL-70L	70	20	44 PIN TSOP-II
UT62L12816MCL-70LL	70	2	44 PIN TSOP-II
UT62L12816MCL-100L	100	20	44 PIN TSOP-II
UT62L12816MCL-100LL	100	2	44 PIN TSOP-II
UT62L12816BSL-55L	55	20	48 PIN TFBGA
UT62L12816BSL-55LL	55	2	48 PIN TFBGA
UT62L12816BSL-70L	70	20	48 PIN TFBGA
UT62L12816BSL-70LL	70	2	48 PIN TFBGA
UT62L12816BSL-100L	100	20	48 PIN TFBGA
UT62L12816BSL-100LL	100	2	48 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L12816MCL-55LE	55	20	44 PIN TSOP-II
UT62L12816MCL-55LLE	55	2	44 PIN TSOP-II
UT62L12816MCL-70LE	70	20	44 PIN TSOP-II
UT62L12816MCL-70LLE	70	2	44 PIN TSOP-II
UT62L12816MCL-100LE	100	20	44 PIN TSOP-II
UT62L12816MCL-100LLE	100	2	44 PIN TSOP-II
UT62L12816BSL-55LE	55	20	48 PIN TFBGA
UT62L12816BSL-55LLE	55	2	48 PIN TFBGA
UT62L12816BSL-70LE	70	20	48 PIN TFBGA
UT62L12816BSL-70LLE	70	2	48 PIN TFBGA
UT62L12816BSL-100LE	100	20	48 PIN TFBGA
UT62L12816BSL-100LLE	100	2	48 PIN TFBGA

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