GENERAL DESCRIPION

Samsung's BW0407X is high resolution, single-chip stereo ADC and DAC that employs the Sigma-Delta modulation technique. With a resolution of 16bit, oversampling of 64X and a 90dB Signal-to-Noise ratio, BW0407X is suitable for applications in consumer digital audio system, multimedia and digital systems.

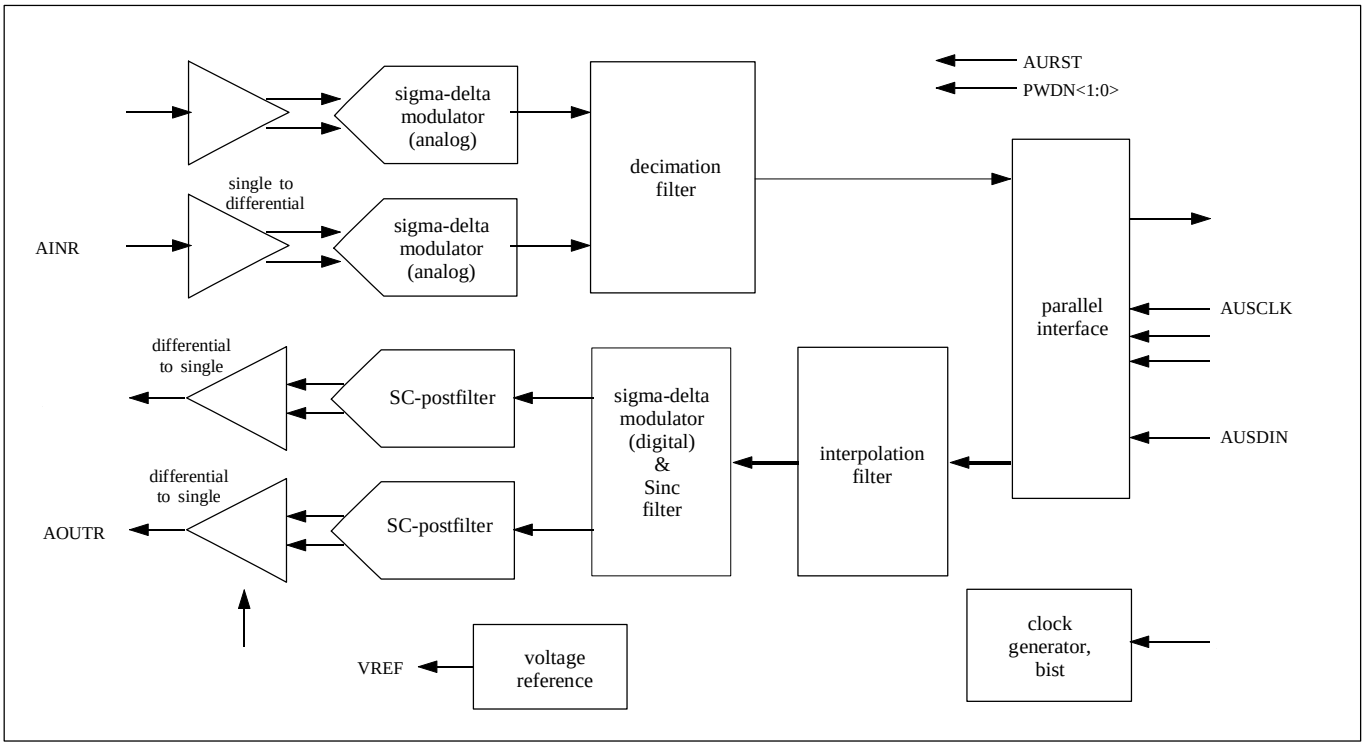
TYPICAL APPLICATIONS

- multi-media applications
- consumer digital audio
- digital systems

FEATURES

- 1 chip stereo A/D, D/A converter
- 4-th order Sigma-Delta modulator
- Sigma-Delta Stereo ADC.
  - * 64X Oversampling
  - * On-chip Decimation Filter
  - * On-chip Anti-Aliasing Filter
  - * 90dB Signal to Noise Ratio.
- Sigma-Delta Stereo DAC.
  - * 64X Oversampling
  - * On-chip 4X Interpolation Filter
  - * On-chip Analog Postfilter
  - * 90dB Signal to Noise Ratio
- Mute for Analog Output of DAC
- Zero detection mute for DAC
- Analog Single-ended Input and Output.
- Sampling Rate of 48KHz
- Single +3.3V Power Supply

FUNCTIONAL BLOCK DIAGRAM



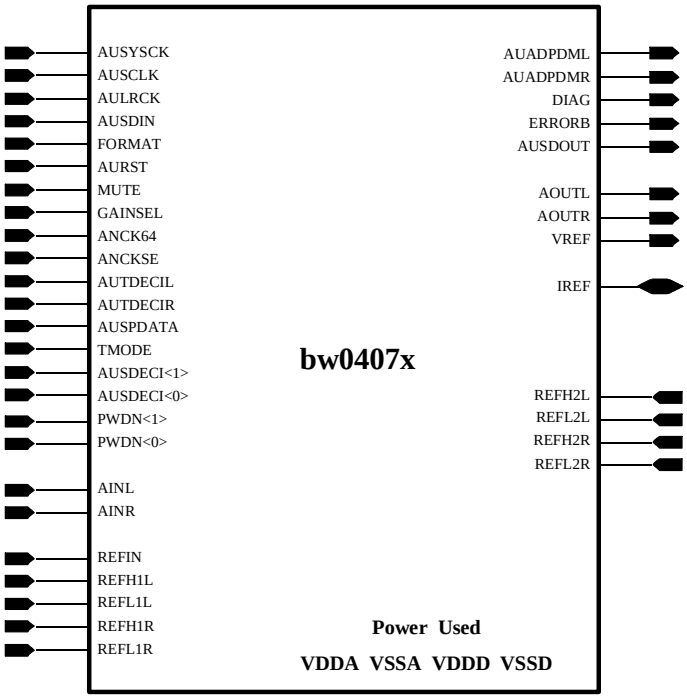
CORE PIN DESCRIPTION

NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
Analog Pins			
AINL	AI	pia_bb_50option	Analog Left Input
AINR	AI	pia_bb_50option	Analog Right Input
AOUTL	AO	poa_bb_50option	Analog Left output
AOUTR	AO	poa_bb_50option	Analog Right output
VREF	AO	poar10_bb	Voltage reference output for bypass filtering
REFIN	AI		Each Pin Must be Tie to VREF PAD respectively
REFH1L	AI		
REFH1R	AI		
REFH2L	AI		
REFH2R	AI		
REFL1L	AI		Each Pin Must be Tie to AVSS PAD respectively
REFL1R	AI		
REFL2L	AI		
REFL2R	AI		
Digital Pins			
AUSYSCK	DI	piccbb_bb	Master clock(256*Fs)
AUSCLK	DI	piccbb_bb	Serial interface clock(32*Fs)
AULRCK	DI	piccbb_bb	Sampling Frequency clock(Fs)
AUSDIN	DI	piccbb_bb	Digital serial input for DAC
FORMAT	DI	piccbb_bb	Serial interface format select
AURST	DI	piccbb_bb	Digital reset
MUTE	DI	piccbb_bb	Analog output mute on/off ("H" is mute enable)
PWDN<1>	DI	piccbb_bb	Power down control pin
PWDN<0>	DI	piccbb_bb	
AUSDOUT	DO	pot2bb_bb	Digital serial output for ADC
Power Pins			
VDDA	AP	vdd3t_bb	Analog supply
VSSA	AG	vsst_bb	Analog ground
VDDD	DP	vdd3t_bb	Digital supply
VSSD	DG	vsst_bb	Digital ground

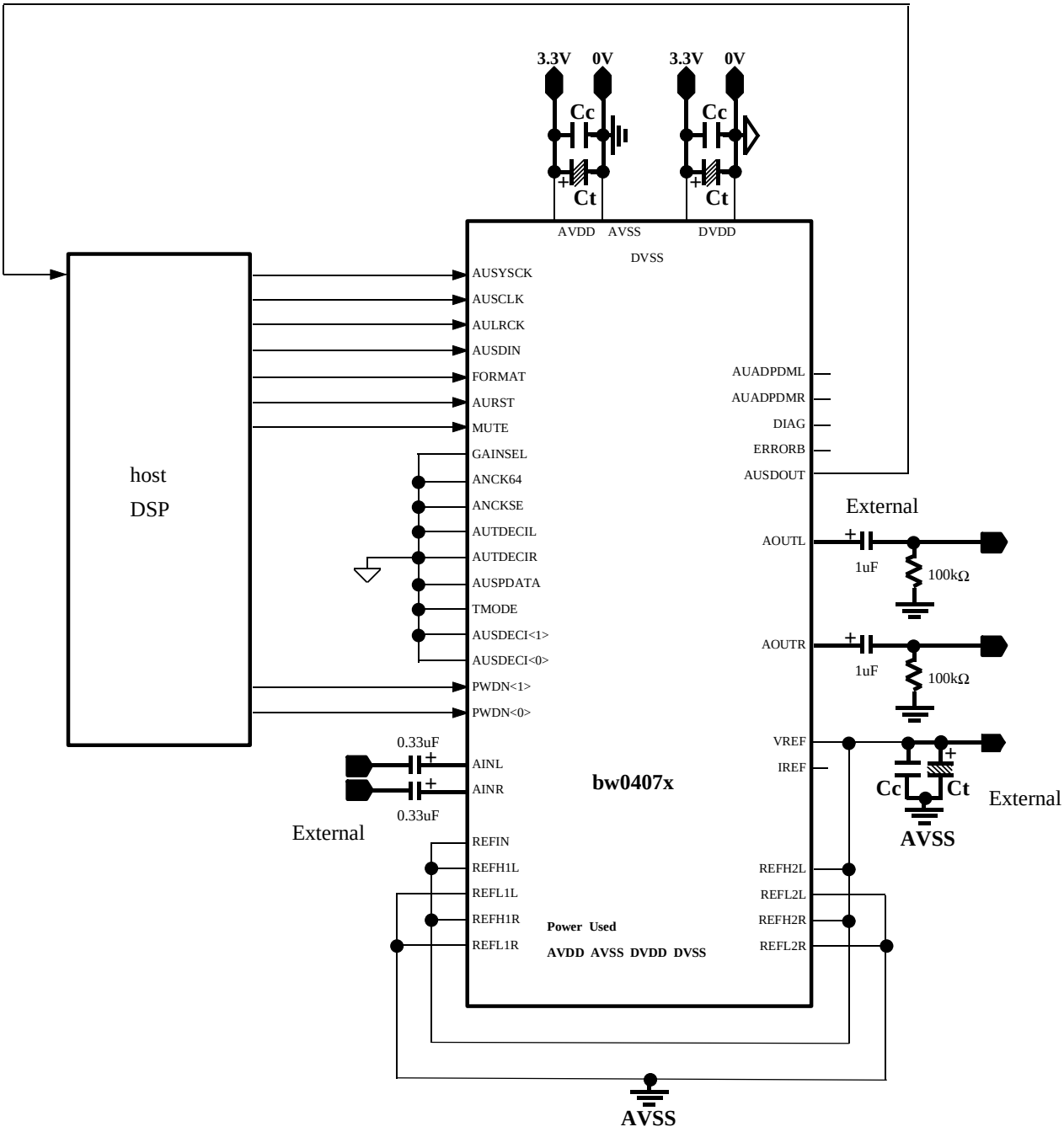
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
Core Interanl Block Test Pins **These pins are only used for core internal block evaluation. So don't use these pins.** **You must be tie the digital input pins to DVSS for disable state, and output and bidrections pins leave floating.**			
TMODE	DI	piccbb_bb	Test mode selection pin for digital filter (normal "L")
DIAG	DO	pot2bb_bb	BIST output(sram)
ERRORB	DO	pot2bb_bb	BIST output(sram)
AUSDECI<1>	DI	piccbb_bb	Test pin for internal block loop path selection (normal "L")
AUSDECI<0>	DI	piccbb_bb	Test pin for internal block loop path selection (normal "L")
GAINSEL	DI	piccbb_bb	Test input pin for decimation filter (normal "L")
ANCK64	DI	piccbb_bb	Test clock for analog block loop test (normal "L")
ANCKSE	DI	piccbb_bb	Test pin for analog clock selection (normal "L")
AUTDECIL	DI	piccbb_bb	Test input for decimation and post left channel filter (normal "L)
AUTDECIR	DI	piccbb_bb	Test input for decimation and post right channel filter (normal "L)
AUSPDATA	DI	piccbb_bb	Test input for ADC,DAC loop back test (normal "L")
AUADPDML	DO	pot2bb_bb	Test pin for analog modulator left output monitoring.
AUADPDMR	DO	pot2bb_bb	Test pin for analog modulator right output monitoring.
IREF	AB	piar50bb_bb	Test pin for analog reference current control

I/O Type	Description
AP	Analog Power
AG	Analog Ground
AI	Analog Input
AO	Analog Output
AB	Analog Bidirection
DP	Digital Power
DG	Digital Ground
DI	Digital Input
DO	Digital Output
DB	Digital Bidrection

CORE CONFIGURATION



CORE EVALUATION GUIDE



LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR

Note : The Analog Power/Ground must be seperated Digital Power/Ground.
As possible as, the L/R channel input/output line must be symmetrical routing on the test board.

Absolute Maximum Ratings

Charateritics	Min.	Typ.	Max.	Units
Supply Vtg.	-0.3		3.8	V
Digital Input Voltage range	-0.3		3.6	V
Storage Temp.	-65		150	°C

Recommanded Operating Condtions

Charateritics	Min.	Typ.	Max.	Units
Supply Vtg.	3.135	3.3	3.465	V
Operating Temp.	-40	25	85	°C

Digital Filter Characteristics

Characteristics	Min.	Typ.	Max.	Units
Sampling Frequency	4	48	50	KHz
ADC :				
Passband	0	0.4Fs		KHz
Stopband		0.6Fs	∞	KHz
Transition band		0.4Fs~0.6Fs		KHz
Passband ripple		±0.1		dB
Stopband attenuation		74		dB
Group delay distortion		0		us
DAC :				
Passband	0	0.4Fs		KHz
Stopband		0.6Fs	∞	KHz
Transition band		0.4Fs~0.6Fs		KHz
Passband ripple		±0.1		dB
Stopband attenuation		74		dB
Group delay distortion		0		us

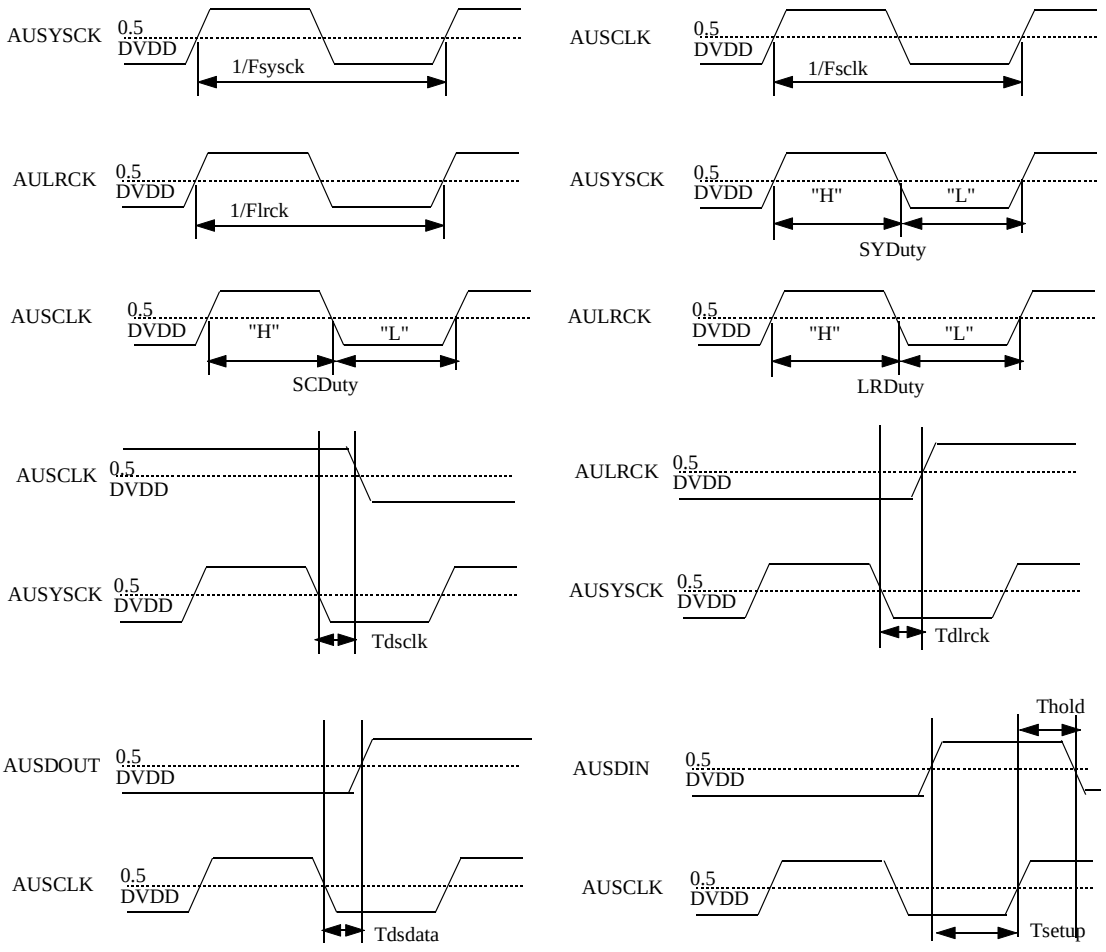
Electrical Characteristics

(Measurement Bandwidth is 20Hz ~ 20KHz, Full scale input sine wave 1KHz, Fs=48KHz, AVDD=3.3V, DVDD=3.3V, 10kΩ/25pF load, Ta=25°C, Unless otherwise specified)

Characteristics	Min.	Typ.	Max.	Units
Resolution			16	Bits
Sampling rate	4	48	50	KHz
Reference Voltage Output		1.55		V
ADC Characteristics				
S/N (EIAJ)	85	90		dB
THD	70	77		dB
S/(N+D)	70	77		dB
Dynamic Range	80	85		dB
Interchannel Isolation	70	77		dB
Offset Error		50		mV
Maximum Input Voltage Range		2		Vpp
Input Impedance	20	25		kΩ
DAC Characteristics				
S/N (EIAJ)	85	90		dB
THD	70	77		dB
S/(N+D)	70	77		dB
Dynamic Range	80	85		dB
Interchannel Isolation	70	77		dB
Offset Error		50		mV
Maximum Output Voltage Range		2		Vpp
Power Supply				
Supply Current		30		mA
Power Dissipation		95		mW
Power Supply Rejection Ratio		40		dB

Timing Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
AUSYSCK Frequency	Fsysck	1.024	12.288	12.8	MHz
AUSCLK Frequency	Fsclk	0.128	1.536	1.6	MHz
AULRCK Frequency	Flrck	4	48	50	KHz
AUSYSCK Duty cycle (H:L)	SYDuty	40:60	50:50	60:40	%
AUSCLK Duty cycle (H:L)	SCDuty	40:60	50:50	60:40	%
AULRCK Duty cycle (H:L)	LRDuty	50:50	50:50	50:50	%
AUSYSCK Falling and AUSCLK Edge Delay(Hold)	Tdsclk	-	10	15	ns
AUSYSCK Falling and AULRCK Edge Delay(Hold)	Tdlrck	-	10	15	ns
AUSCLK Falling and AUSDOUT Delay	Tdsdata	-	10	15	ns
AUSCLK Rising and AUSDIN Setup	Tsetup	10	15	-	ns
AUSCLK Rising and AUSDIN Hold	Thold	10	15	-	ns



*Notes : AUSCLK rising edge must NOT occur at the same time as AULRCK edge.

CODEC Digital Data Interface

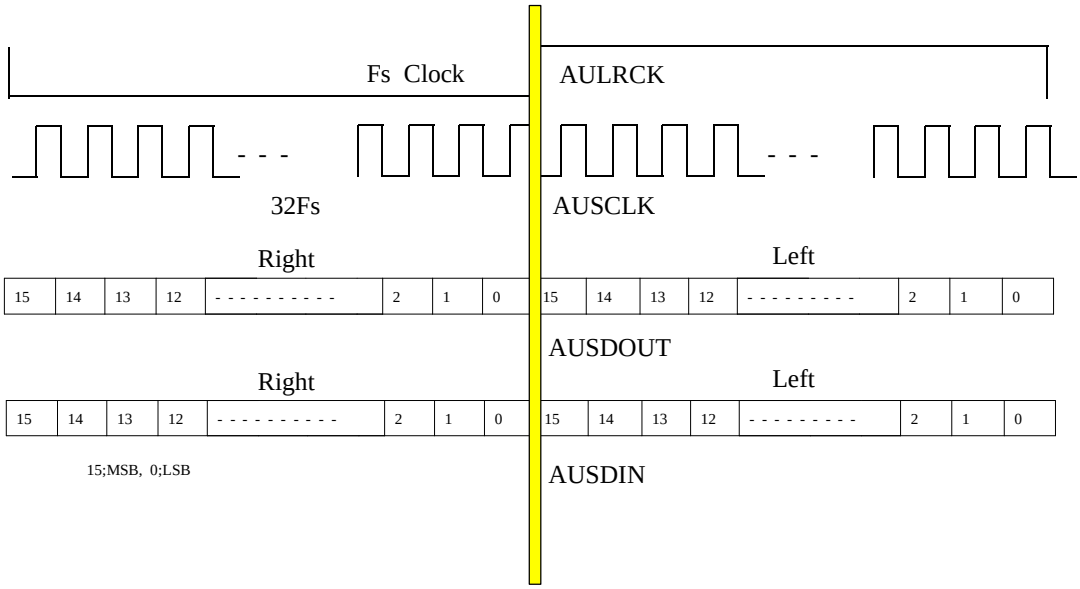
The CODEC provides stereo, 16-bit ADC & DAC functions. The digital input and output of the CODEC is through the serial input and output ports. All the Codec related clock and signals are provided externally. The ADC of CODEC and the other digital block communicates through a serial output. The interface consists of a serial input clock(AUSCLK), a frame sync input clock(AULRCK), a serial data output(AUSDOUT). The Codec DAC and the other digital block communicates through a serial input. The interface consists of a serial input clock(AUSCLK), a frame sync input clock (AULRCK), a serial data input(AUSDIN). On digital reset or power down, the serial input of the DAC is disabled(all zeros). There are two kind of serial interface for CODEC digital data.. Serial interface format is controlled by FORMAT pin.

a. SEC serial format. (when FORMAT pin is "H")
b. I2S serial format. (when FORMAT pin is "L")

a. SEC serial interface format

- The frame sync clock transitions determine the start of the serial data.
- Input data :
  * MSB first and no trailing or leading unused bits. AULRCK transition marks the end of the LSB out
  * 16bit, 2's complement.
- Output data :
  * MSB first and no trailing or leading unused bits. MSB is put out immediately on the first negative AUSCLK tranisiton after an AULRCK transition.
  * 16bit, 2's complement.

AULRCK	ADC OUT[AUSDOUT]	DAC INPUT[AUSDIN]
LOW	Right Channel	Right Channel
HIGH	Left Channel	Left Channel



Codec SEC serial interface timing diagram.

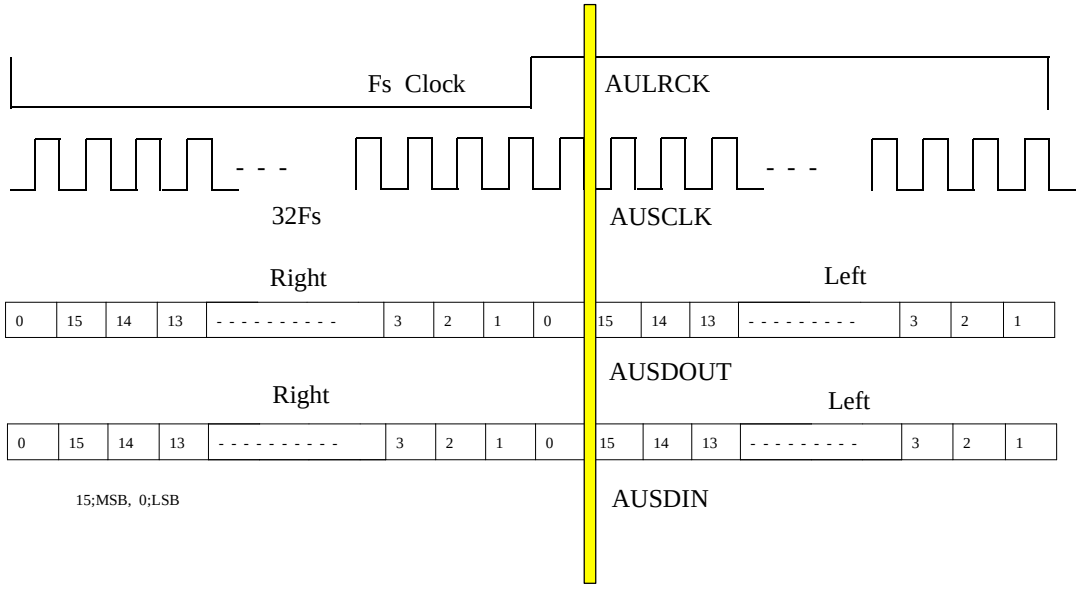
b. I2S serial format

* All data input and output changes occurs on the falling edge of AUSCLK.

* Pay careful attention to the LSB, after the AULRCK transition.

* AULRCK is at sampling rate Fs. Take note of the AULRCK polarity.

AULRCK	ADC OUT[AUSDOUT]	DAC INPUT[AUSDIN]
LOW	Right Channel	Right Channel
HIGH	Left Channel	Left Channel



Codec I2S serial interface timing diagram.

OVER Range

The digital output of the CODEC ADC will produce a positive full scale[7FFF(h)] output for analog input signal above the maximum input voltage range and a negative full scale [8000(h)] for input below the minimum input voltage range.

Power Down

Threr are three power down mode, see the below the table.

Input PIN	Value	Condition
PWDN<1:0>	00	All On
	01	ADC Off, DAC On
	10	DAC Off, ADC On
	11	All Off

Reset

The BW0407X digital block is placed in the reset mode by bringing AURST "H". But Analog block is still alive. To exit the reset mode, bring AURST to "L", In the reset mode all clock is still operating, the internal register is in the reset mode.

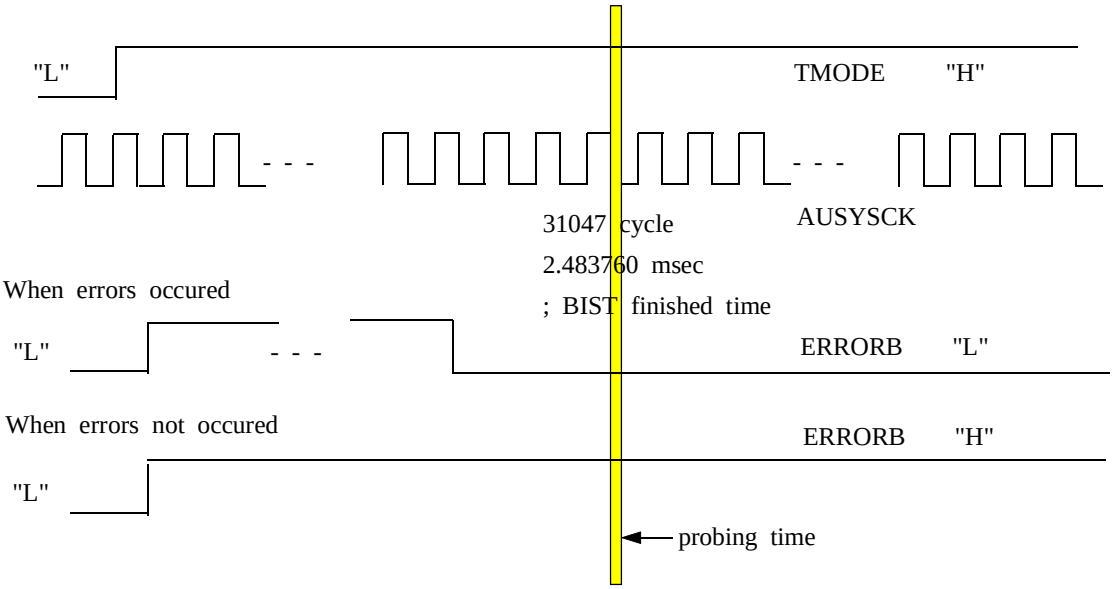
ZERO DETECTION MUTE FOR DAC

The anlaog 2-CH output of the CODEC DAC will produce common level [VREF] for digital zero input signal above the number of 8192 times sample cycle[AULRCK] input, either Left CH or Right CH.

CORE INTERNAL BLOCK TESTABILITY

- Embedded Memory test

TMODE= "H" is Built In Self Test (BIST) mode for embedded memor



Memory BIST mode timing diagram

Application Notes

Power Supply and Grounding

The analog power pins of codec should be derived from the cleanest power source available. The decoupling capacitors are placed as close as possible to the device. The lowest value capacitor is placed closest to the codec.

The circuit board layout should have separate analog and digital regions and ground planes. All signal, especially clocks should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators and postfilter.

Analog and Digital Connections

The analog inputs presented to the BW0407X are single-ended input voltage. The input range is approximately 2.0Vp-p. The analog outputs are also single-ended and the output range are typically 2.0Vp-p.

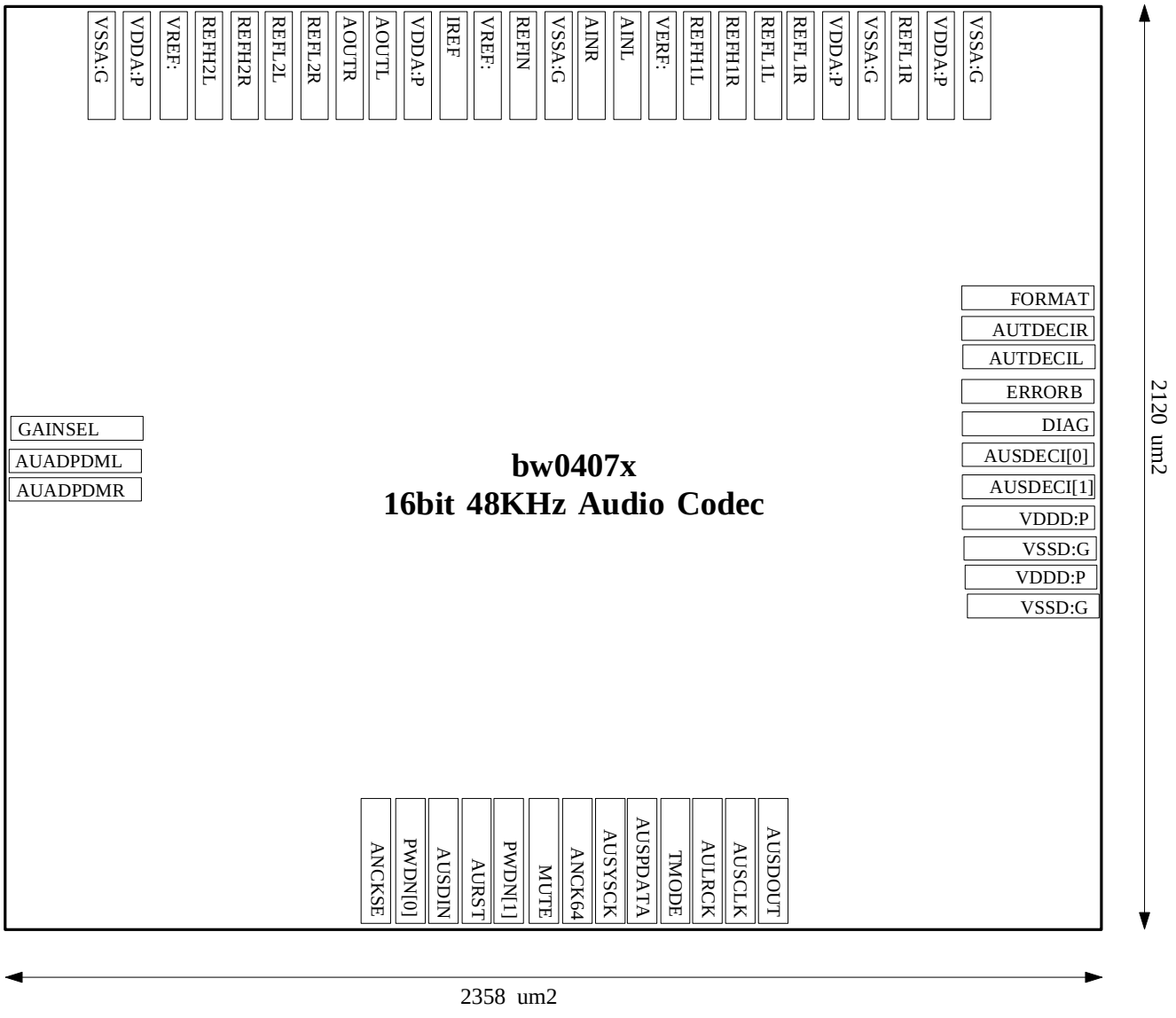
The on-chip voltage reference is output on the VREF pin. A electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. No load current may be driven from the VREF output pin.

Parameter definitions

- Resolution: The number of bits in the input words to the DACs, and in the output words in the ADCs.
- Dynamic range: The dynamic range available at any instant in time. It is measured using S/(N+D) with a 1KHz. -60dB input signal with 60dB added to compensate for the small input signal. Use of a small input signal reduces to harmonic distortion components of the noise to insignificance. Units in dB
- Signal to Noise and distortion Ratio. SNDR: The rms value of a full scale signal to the lowest obtainable noise floor and distortion. It is measured by comparing a full scale signal to the lowest noise floor and distortion possible in the codec. Unit in dB
- Total Harmonic Distortion. THD: The rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor in the codec. Unit in dB. The lowest noise floor is acquired when the analog input is tied Vref.
- Interchannel Isolation: The amount of 1KHz signal present on the output of the grounded input channel with 1KHz 0dB signal present on the other channel. Unit in dB.
- Offset Error: For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input at VREFH. For the DACs, the deviation of the output from VREFH with mid-scale input code. Units in volts.

PHANTOM CELL INFORMATION

- Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
  The term "External" implies that the pins should be assigned externally like power pins.
  The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
Power Pins		
VDDD:P	External/Internal	- Maintain the large width of lines as far as the pads. - place the port positions to minimize the length of power lines. - Do not merge the analog powers with another power from other blocks. - Use good power and ground source on board.
VSSD:G	External/Internal	
VDDA:P	External	
VSSA:G	External	
Analog Pins		
AINL	External	- Do not overlap with digtal lines. - Maintain the shotest path to pads.
AINR	External	
AOUTL	External	
AOUTR	External	
VREF:	External	
REFH1L REFH2L REFH1R REFH2R REFIN	Internal	- Do not overlap with digital line - Each Pin Must be Tie to VREF PAD respectively
REFL1L REFL2L REFL1R REFL2R	Internal	- Do not overlap with digital line - Each Pin Must be Tie to VSSA:G PAD respectively
Digital Pins		
AUSYSCK AUSCLK AULRCK	External/Internal	- Separate from all other analog signals
AUSDOUT	External/Internal	
PWDN[0] PWDN[1] AURST MUTE	Internal	- Separated from the analog clean signals if possible.
TMODE	Internal	
DIAG ERRORB	Internal	
Internal Block Test Pins		
ANCKSE ANCK64 AUSPDATA GAINSEL AUTDECIL AUTDECIR AUSDECI[0] AUSDECI[1]	Internal	- In normal mode, these pins are not used, Each Pin Must be Tie to VSSD:G
AUADPDML	Internal	- Separate from all other analog signals
AUADPDMR	Internal	
IREF	Internal	- Do not overlap with digital line

FEEDBACK REQUEST

It should be quite helpful to our CODEC core development if you specify your system requirements on CODEC in the following characteristic checking table and fill out the additional questions. We appreciate your interest in our products. Thank you very much.

- Could you explain external/internal pin configurations as required?
- Specially requested function list :

Parameter	Min	Typ	Max	Unit	Remarks
supply voltage				V	
Max master clock frequency				Hz	
Operating temperature				°C	
Sampling Frequency				Hz	
ADC					
Dynamic range				dB	
Total harmonic distortion				dB	
Signal-to-noise ratio				dB	
Output format resolution (Serial/Parallel interface)				Bit	
Channel		Mono	Stereo		
Power dissipation				mW	
Input voltage range				Vpp	
ADC offset error				V	
ADC group delay				sec	
Phase linearity deviation for passband region				° (Deg)	
Peak-to-peak frequency response ripple for passband region				dB	
DAC					
Dynamic range				dB	
Total harmonic distortion				dB	
Signal-to-noise ratio				dB	
Input format resolution (Serial/Parallel interface)				Bit	
Channel		Mono	Stereo		
Power dissipation				mW	
Full scale output voltage range				Vpp	
DAC group delay				sec	
Phase linearity deviation for passband region				° (Deg)	
Peak-to-peak frequency response ripple for passband region				dB	

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0	99.1.4	Original version published (preliminary)	
ver 1.1	00.1.30	Release the datasheet (according to Slilicon proven data)	
ver 1.2	02.4.23	Appending the phantom(GDS2) information	