54F/74F548

Octal Decoder/Demultiplexer With Acknowledge

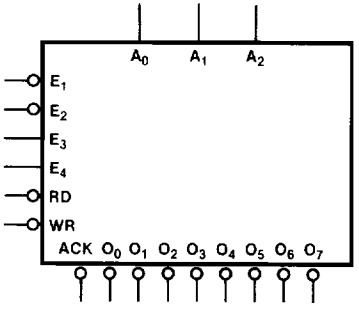
Description

The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are Active LOW and two are Active HIGH for maximum addressing versatility. Also provided is an Active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

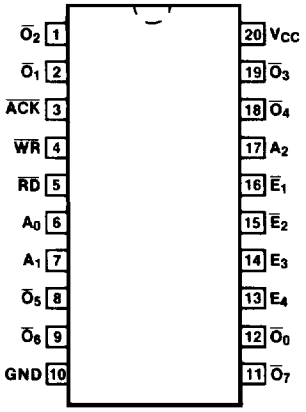
- **3-to-8 Line Address Decoder**
- **Multiple Enables for Address Extension**
- **Open Collector Acknowledge Output**
- **Active LOW Decoder Outputs**

Ordering Code: See Section 5

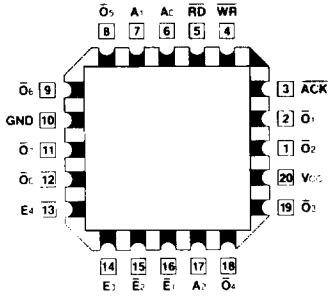
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



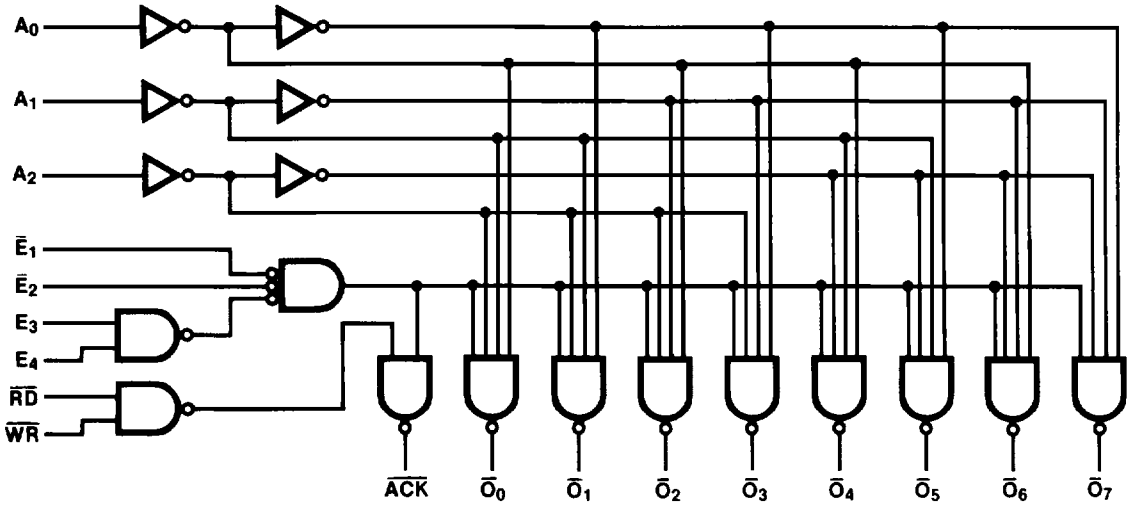
Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Chip Enable Inputs (Active LOW)	0.5/0.375
E_3, E_4	Chip Enable Inputs	0.5/0.375
$\overline{RD}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{WR}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{ACK}$	Open Collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0$-$\overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

When enabled, the 'F548 accepts the A_0-A_2 Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. When one or more Enables is inactive, all decoder outputs are HIGH. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The open collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when the Enables are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

Inputs						Output
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Decoder Truth Table

Inputs							Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		14	21	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.0 4.0	5.5 8.0	7.5 10.5	3.0 4.0	10.0 12.0	3.0 4.0	8.5 11.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.0 3.5	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	3.0 3.5	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to $\overline{O}_n$	5.0 4.0	8.5 8.5	11.0 11.0	5.0 4.0	13.0 12.5	5.0 4.0	12.0 12.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{ACK}$	6.5 3.0	11.0 7.5	14.0 9.5	6.5 3.0	16.5 11.0	6.5 3.0	15.0 10.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to $\overline{ACK}$	8.0 4.0	13.0 8.5	16.5 11.0	8.0 4.0	19.5 13.0	8.0 4.0	17.5 12.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	5.5 2.5	10.0 5.0	12.5 6.5	5.5 2.5	16.5 8.5	5.5 2.5	13.5 7.5	ns	3-1 3-4