QE1F-*Plus* Device
Quad E1 Framer-*Plus*
TXC-03114

DATA SHEET

FEATURES

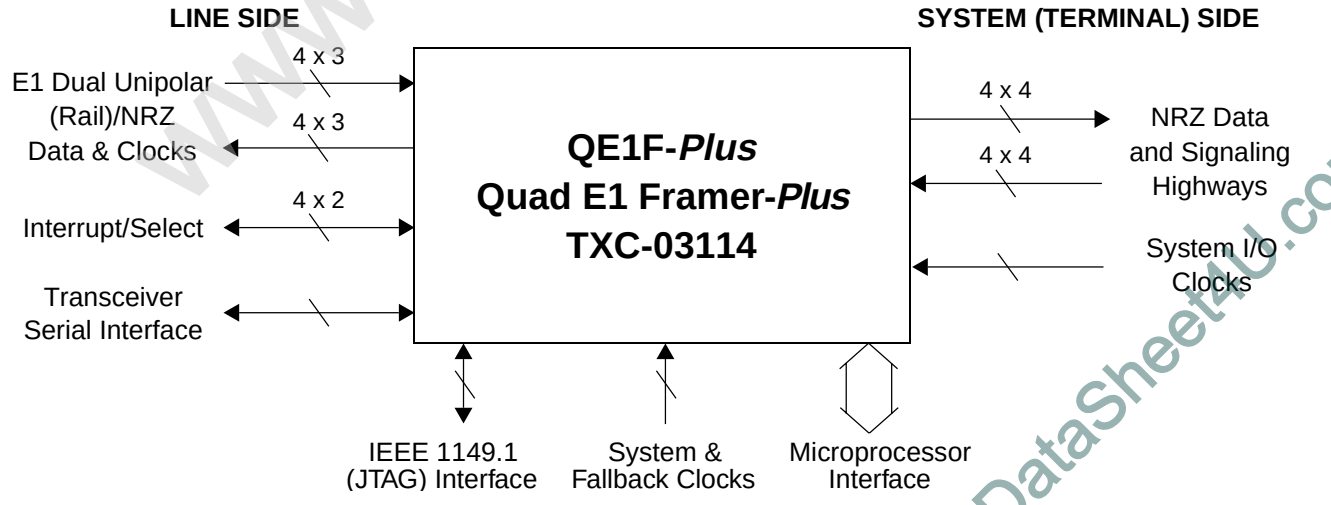
- Offline framer supports Standard and Frame Hold-Off frame alignment with CRC-4 multiframe check and selectable out of frame criteria, and transparent non-framing mode
- Frame alignment detection and loss of frame alignment declaration comply with ITU-T G.706
- Dual unipolar (HDB3/AMI) or NRZ line interface
- Two-frame slip buffers in both receive and transmit directions
- Supports Channel Associated Signaling in Time Slot 16
- Detects and forces RAI and AIS alarms; detects OOF and CFA framing conditions
- HDLC processing using national bits in Time Slot 0 (up to 20 kbit/s)
- Detects, counts and forces line code errors (BPVs), CRC-4 errors, and frame bit errors
- System Interfaces
  - 2 Mbit/s, 8 Mbit/s and 16 Mbit/s Transmission Modes with gapped clock option for 2 Mbit/s
  - 2 Mbit/s MVIP® Mode, 8 Mbit/s H-MVIP® /H.100 Mode and 16 Mbit/s PCM Highway Mode with gapped clock option for 2 Mbit/s MVIP
- Motorola/Intel-compatible microprocessor interface
- One-second interrupt input latches counter values and line events into shadow registers
- Local and remote line loopbacks
- Boundary scan capability (IEEE 1149.1)
- Single +3.3 or +5 volt, ±5% power supply
- 128-pin low profile plastic quad flat package

DESCRIPTION

The QE1F-*Plus* is a four-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703. The transmit and receive sections of each of the four framers are independent, with individual two-frame slip buffers, which allows operation with a wide range of switching and transmission products. Framing algorithm support for ITU-T G.704, G.706 and ETS 300 011. Access and control for signaling and data are provided via a Motorola/Intel-compatible microprocessor interface. For HDLC link applications, each framer supplies a full duplex HDLC controller in addition to on-board latching of all required performance parameters; minimal software overhead is required. Diagnostic, test, and maintenance functions are provided, including E1 local and remote loopbacks, time slot loopbacks and boundary scan (IEEE 1149.1).

APPLICATIONS

- SDH terminal or add/drop multiplexers supporting E1 byte synchronous operation
- DCS, digital central office or remote digital terminals
- E1 multiplexers
- E1 and fractional E1 CSUs
- ATM products with integrated E1 interfaces
- LAN routers with integrated E1 interfaces
- Multichannel E1 test equipment



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QUAD E1 FRAMER-*Plus* FEATURES

The Quad E1 Framer-*Plus* (QE1F-*Plus*) device is a highly-featured four-channel E1 framer for use in a wide variety of interface, transmission and switching applications. Four independent E1 framers are provided in a single monolithic VLSI device using sub-micron CMOS technology. Powered from a single +5.0 volt supply, the four framers dissipate less than one half of a watt typically. Powered from a single +3.3 volt supply, the four framers dissipate less than one sixth of a watt typically. The QE1F-*Plus* is provided in a rectangular 128-pin low profile quad flat package. Its ambient operating temperature range extends from -40 ^{o}C to +85 ^{o}C.

The QE1F-*Plus* device has been designed to meet the latest industry standards, namely:

- ITU-T G.703 Physical/Electrical Characteristics of Hierarchical Digital Interfaces
- ITU-T G.704 Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels
- ITU-T G.706 Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704
- ITU-T G.732 Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s
- ITU-T G.735 Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 384 kbit/s and/or 64 kbit/s
- ITU-T G.775 Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria
- ITU-T G.821 Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network
- ITU-T G.823 The Control of Jitter and Wander within Digital Networks Which are Based on the 2048 kbit/s Hierarchy
- ITU-T I.431 ISDN User-Network Interfaces. Primary Rate User-Network Interface - Layer 1 Specification
- ITU-T O.151 Error Performance Measuring Equipment Operating at the Primary Rate and Above
- ITU-T Q.516 Operation and Maintenance Functions
- prETS 300 011 Integrated Services Digital Network (ISDN); Primary rate user-network. Nov. 1996 Draft
- IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, May 1990
- MVIP, H-MVIP Multi-Vendor Integration Protocol. Working Document, April 1995
- Enterprise Computer Telephony Forum, H.100 Rev. 1.0 Hardware Compatibility Spec. CT Bus

The following features are available in the QE1F-*Plus* device:

Framing Modes:

- Off line framer (data passes un-interrupted from line to system in or out of frame alignment)
- Follows ITU-T G.706 (‘88 or ‘91) frame alignment detection and loss of alignment declaration
- Thirty-two 64 kbit/s time slots Basic Frame structure
- TS0/CRC-4 Multiframe
  - Two FAS selectable algorithms (Standard and Frame Hold-off)
  - Frame alignment and multiframe alignment per ETS 300 011
  - CRC-4 and non CRC-4 multiframing automatic interworking per ITU-T G.706 (1991 Annex B)
- TS16/Signaling Multiframe
  - Two MAS selectable algorithms (Standard and Enhanced)

Line Codes:

- AMI
- HDB3
- NRZ (Unipolar)

Signaling methods:

- Common Channel Signaling (CCS) with inversion of transmit or receive and substitution of 0000 with 1111 to the transmit line
- Channel Associated Signaling (CAS) in Time Slot 16

Signaling access:

- Dedicated signaling bus
- Data stream embedded
- Internal registers (microprocessor interface)

System interface:

- Separate transmit and receive paths for all modes
- 2048 kbit/s separate data and signaling bus for each of the 4 framers
  - Transmission Mode with 500 Hz multiframe signal each direction and 8 signaling bits per frame
  - MVIP mode with 8 kHz framing signal each direction and all signaling bits per frame
- 2048 kbit/s separate data bus for each of the 4 framers with continuous and gapped clock Transmission Mode with 500 Hz multiframe signal and selectable per time slot clock each direction
- 8192 kbit/s separate data and signaling bus byte-interleaved by all 4 framers with 16384 kbit/s clock
  - Transmission Mode with 500 Hz multiframe signal each direction and 8 signaling bits per frame
  - H-MVIP/H.100 mode with 8 kHz framing signal each direction and all signaling bits per frame
- 16384 kbit/s combined data and signaling bus bit-interleaved by all 4 framers with 16384 kbit/s clock
  - Transmission Mode with 500 Hz multiframe signal each direction and 8 signaling bits per frame
  - PCM Highway mode with 8 kHz framing signal each direction and all signaling bits per frame
- Dual Reference clock outputs; any 2 E1s brought to bus pins for multiple QE1F-*Plus* Tri-statable output ports
- Gapped clock option for fractional E1 support in Transmission Mode in place of signaling highways
- Programmable sync start position

Microprocessor interface:

- Intel compatible interface
- Motorola compatible interface
- Directly addressable control and status registers
- All interrupts are maskable

External line interface unit port:

- Serial port for the control of external line interface components
- Programmable for unipolar or bipolar interface
- Individual chip select and interrupt signals for each transceiver
- Integration of line interface unit alarms

Maintenance functions:

- Loopbacks
  - Local
  - Line remote
  - Payload remote
  - Per time slot remote in Transmission Mode only
- Pattern generation/detection per E1
  - Force programmable code in any time slot via slip buffer access
  - Transmit and detect loop codes via read and write of the slip buffer RAM
  - PRBS Generator/Analyzer (2^{15}-1) with out of lock pin for board testing available in 2 Mbit/s Transmission Mode
  - Transmit AIS
  - All 1's only in the information bits
  - Idle code insertion
- Error Insertion
  - BPV
  - CRC-4
  - FAS/nFAS
  - LOS
- Data Link Access
  - Full-duplex HDLC message controller supporting back to back frames
  - 8-bit access via microprocessor interface
  - Uses any combination of the TS0 National Spare bits
  - A 16-byte message buffer per transmit and receive directions per E1
- E1 Monitor Access for multiplexed applications
  - Select any E1 transmit or receive direction
  - Clock and NRZ data brought to bus pins for multiple QE1F-*Plus*

Alarm Indications:

- Programmable alarm generation and consequent actions
- Out of Frame
- Out of Signaling Multiframe
- Out of CRC Multiframe
- Remote Frame Alarm
- Remote Multiframe Alarm
- All 1's Received
- TS16 AIS Detection
- Change of Frame Alignment
- Frame Alignment Error
- CRC Multiframe Error
- Signaling Multiframe Error (TS 16)
- Excessive CRC Errors
- Slip (Transmit and Receive)
- Line Code Violation
- Loss of Signal

Error Reporting:

- CRC-4 errors
- Framing bit errors
- Far end Block errors
- Line code violations count
- Buffer slips
- Error counter roll-over generates a maskable processor interrupt
- 1-second interrupt input will latch counter values into shadow registers

Clocks:

- System clock
- Line clock
- External clock inputs (2048 kbit/s and 1 Hz)
- Flexible Rx and Tx clock selection

Slip control:

- Two-frame elastic store for plesiochronous operation (slip buffer)
- One slip buffer per transmit and receive E1

System Test:

- External boundary scan plus external pin 3-state control
- Hardware and software resets

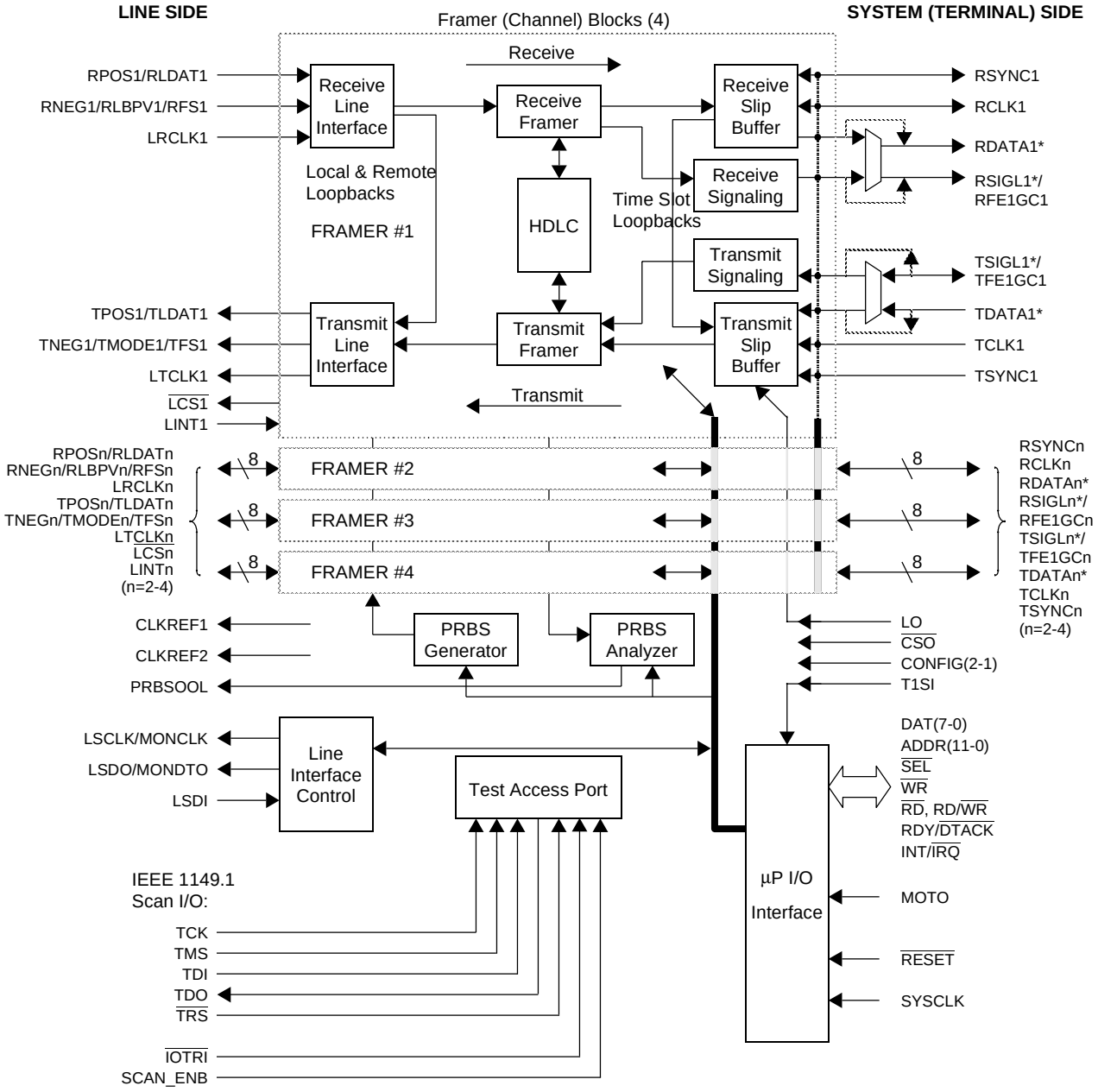
Power, Package and Environment

- 3.3 volt ±5% supply or 5.0 volt ±5% supply
- 128-pin low profile plastic quad flat package
- Power dissipation 125 mW (all channels operational @ 3.3 volt in Transmission Mode)
- Operating temperature range of -40 to + 85 ^{o}C

The QE1F-*Plus* has the following feature enhancements relative to the QE1F device (TXC-03104)

- >75% lower power by using 0.5 micron technology (with 3.3 volt power supply)
- >40% lower power by using 0.5 micron technology (with 5.0 volt power supply)
- Loopbacks per time slot or group of time slots
- Payload loopback corrected
- Fractional E1 support providing gapped clocks for assigned time slots (Tx and Rx independent assignments) optional in place of signaling highways
- ETSI 300 011 support (G.706-1988 as option to G.706-1991 current support)
- H.100 frame pulse compliance option to H-MVIP (SC Bus)
- All QE1F deviations addressed

BLOCK DIAGRAM



* Note: Signaling and data for all four framers are multiplexed on framer 1 signaling and/or data leads for all modes with bit rates above 2 Mbit/s.

Figure 1. QE1F-*Plus* TXC-03114 Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the Quad E1 Framer-*Plus* (QE1F-*Plus*) is shown in Figure 1. The QE1F-*Plus* consists of the following major blocks: four Framer blocks, Line Interface Control, PRBS Generator, PRBS Analyzer, Microprocessor Input/Output Interface, and Test Access Port.

Each of the four identical Framer blocks consists of the following blocks: Receive and Transmit Line Interface blocks, Receive and Transmit Framer blocks, HDLC block, Receive and Transmit Slip Buffer blocks, and Receive and Transmit Signaling blocks.

The Receive and Transmit Line Interface blocks connect each of the four framers to an external line interface transceiver, which performs the LIU and clock recovery functions. The interface to the external line interface transceiver can be configured for two interface modes: a dual unipolar (rail) interface or a NRZ interface.

When the dual unipolar interface mode is selected, input data from the external line interface transceiver is clocked into the QE1F-*Plus* on pins RPOSn and RNEGn using the recovered receive clock present on the LRCLKn input pin (where n=1-4 identifies one of the four framers). In the transmit direction, unipolar data is clocked out of the QE1F-*Plus* on pins TPOSn and TNEGn by the transmit line clock present on the LTCLKn output pin. For reduced power dissipation in protection switching applications, the LTCLKn, TPOSn, and TNEGn pins for the four framers may be forced low, by placing a low on the $\overline{\text{CSO}}$ pin. Control bits are provided in the memory map which enable the unipolar data to be clocked in and out of the QE1F-*Plus* on either edge of the clocks. For the dual unipolar interface mode, the QE1F-*Plus* provides either a High Density Bipolar of order 3 (HDB3), or an Alternate Mark Inversion (AMI), coder and decoder function, and Loss Of Signal detection. The Loss Of Signal detector meets the requirements specified in the ITU-T Recommendation G.775. In addition, the detect and recovery intervals for the Loss Of Signal detector circuit are programmable. A sixteen-bit performance counter is provided for each framer, for counting HDB3 coding violation errors. A power-down mode is also provided in the transmit direction.

When the NRZ interface mode is selected, NRZ data is clocked in at the RLDATn pin by the recovered received clock present on the LRCLKn pin. The NRZ data is clocked out of the QE1F-*Plus* on the TLDATn pin by the transmit system clock present on the LTCLKn pin. Control bits are provided in the memory map which enable the NRZ data to be clocked in and out of the QE1F-*Plus* on either edge of the clocks. In NRZ interface mode, the HDB3 or AMI coder and decoder functions are bypassed. However, bipolar violations which are detected in the external line interface transceiver may be clocked into the QE1F-*Plus* on the RLBPVn pin and counted in the associated 16-bit coding violation performance counter. The Remote Line Loopback function for each framer is also implemented in the Line Interface blocks.

The Receive Framer block for each framer performs two basic functions: frame synchronization and Channel Associated Signaling (CAS) multiframe alignment. The frame synchronization circuit has two framing options: frame synchronization based on the frame alignment signal (FAS) carried in Time Slot 0, or frame synchronization based on the frame alignment signal and validation by the CRC-4 multiframe alignment signal. The frame synchronizing circuit meets the framing requirements specified in ITU-T Recommendations G.704 and G.706. The frame synchronization Out Of Frame alarm criteria can be programmed to use 3 or 4 frame alignment patterns in error, with or without the inclusion of 3 or 4 non-frame alignment patterns in error. Framing word errors and CRC-4 errors are counted in performance counters. The Receive Framer block also monitors and detects a remote alarm A-bit (bit 3) in Time Slot 0 as specified in ITU-T Recommendation G.704. A non-framing mode can be enabled when the QE1F-*Plus* is configured in the Transmission Modes. The non-framing mode bypasses the Receive Framer block and the Receive Slip Buffer.

When frame alignment is acquired, the CAS multiframe pattern in Time Slot 16 is detected for alignment. After multiframe alignment is established, the signaling bits are forwarded to the Receive Signaling block for buffering, microprocessor access, and formatting into the signaling highway data stream.

Each Receive Slip Buffer controls time slot access and retiming for framer n by using a two-frame receive buffer that can be optionally bypassed in the 2 Mbit/s Transmission Mode. When the receive buffer is enabled,

received time slots are written into the buffer by recovered receive clock LRCLKn, and read out as data (RDATAn) from the slip buffer by the system input clock RCLKn. A phase shift between the two clocks is detected in this block and a deletion or repetition of one frame of data (31 time slots, or 30 time slots if Time Slot 16 is assigned for signaling) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access to the read and write pointers is also provided. Channel 0 and channel 16 (when channel 16 is assigned for Channel Associated Signaling) are not affected by a slip. Slip alarm indications are provided for the microprocessor. The slip buffer may be recentered by the microprocessor, or automatically. Individual time slots can be accessed by the microprocessor for the insertion of system idle or out of service codes. When the receive slip buffer is bypassed, the receive clock (RCLKn) and data (RDATAn) are provided as outputs, along with a receive sync signal (RSYNCn).

For Channel Associated Signaling (in Time Slot 16), a 120-bit signaling buffer is used to store the signaling bits which have been extracted by the Receive Framer. The signaling bits are stored sequentially in the signaling buffer in the order that they were received. The signaling buffer may be read, frozen and written to by the microprocessor. If signaling is disabled for a particular channel, the ABCD signaling bits for that time slot will be frozen in their present states. When a loss of signal or an out of frame condition is detected, the signaling bits are also automatically frozen in their present states. The signaling bit states are held until framing has been recovered.

On the terminal side, the system interface interconnects the four framers with the system. For each framer there is a separate receive and transmit highway for the 2 Mbit/s Transmission and MVIP interface modes of operation. The receive highway consists of a data bus (RDATAn), a signaling bus (RSIGLn), a clock (RCLKn), and a synchronization signal (RSYNCn). The transmit highway consists of a data bus (TDATAn), a signaling bus (TSIGLn), a clock (TCLKn), and a synchronization signal (TSYNCn). In the 2 Mbit/s Transmission Mode, the system interface operates at 2.048 MHz, with time slots in the data highway, and signaling and alarms on the signaling highway. The receive and transmit system interfaces are synchronized by multiframe pulses that occur at 2-millisecond intervals. Sixteen frames are sent on the data and signaling highways within the 2-millisecond period, with each of the sixteen frames consisting of 32 time slots, which correspond to an E1 frame. The receive and transmit slip buffers can be individually bypassed in this mode. The Transmission Mode is the only mode that supports gapped clocks in place of signaling (RSIGLn/RFE1GCn and TSIGLn/TFE1GCn) and permits time slot level remote loopbacks if RSYNCn = TSYNCn and RCLKn = TCLKn.

When the 2 Mbit/s MVIP Mode is selected, the system interface also consists of receive and transmit data highways. However, the receive and transmit system interfaces are synchronized by pulses occurring at 125-microsecond intervals in this mode. The receive and transmit slip buffers are always enabled in this mode. Each frame consists of 32 time slots which correspond to an E1 frame on the data highway. The signaling highway also carries 32 time slots which contain the Channel Associated Signaling states for each channel, the signaling multiframe alignment pattern, the signaling channel spare bits and alarm, plus a time slot that corresponds to Time Slot 0 from the E1 frame.

The system interface also supports four additional system interface modes: an 8 Mbit/s Transmission Mode, a 16 Mbit/s Transmission Mode, an 8 Mbit/s H-MVIP/H.100 Mode, and a 16 Mbit/s PCM Highway Mode. For these Modes, the four framers' signaling and data frames are either byte- or bit-multiplexed onto the signaling and/or data highway leads that are used by framer 1. All of the six modes are described in detail in the Operation section below.

The 8 Mbit/s Transmission Mode provides dual receive and transmit highways, which are shared by the four framers. The receive highway consists of a data bus (RDATA1), a signaling bus (RSIGL1), a clock (RCLK1), and a synchronization signal (RSYNC1). The transmit highway consists of a data bus (TDATA1), a signaling bus (TSIGL1), a clock (TCLK1), and a synchronization signal (TSYNC1). The data and signaling time slots for each of the four framers are byte-interleaved on the data and signaling highways, starting with framer 1 bit 1 of Time Slot 0, followed by framer 1 bits 2 through 8 of Time Slot 0, then framer 2 bits 1 through 8 of Time Slot 0, and so on, ending with framer 4 bits 1 through 8 of Time Slot 31. In this mode, the separate data and signaling highways operate at 8.192 Mbit/s. However, the clock rate is 16.384 MHz. The receive and transmit system interfaces are synchronized by multiframe pulses that occur at 2-millisecond intervals. The receive and trans-

mit slip buffers must be enabled in each of the framers. Within the 2-millisecond period, the 32 data and signaling time slots for each of the four framers are repeated 16 times.

The 16 Mbit/s Transmission Mode provides single receive and transmit highways which are shared by the four framers. The receive highway consists of a data bus (RDATA1), a clock (RCLK1), and a synchronization signal (RSYNC1). The transmit highway consists of a data bus (TDATA1), a clock (TCLK1), and a synchronization signal (TSYNC1). The data and signaling time slots for each of the four framers are bit-interleaved on the data highway, starting with framer 1 data Time Slot 0 bit 1, followed by framer 1 signaling Time Slot 0 bit 1, framer 2 data Time Slot 0 bit 1, framer 2 signaling Time Slot 0 bit 1, and so on, and ending with framer 4 signaling Time Slot 31 bit 8. In this mode, the single data highway operates at 16.384 Mbit/s. The receive and transmit system interfaces are synchronized by pulses that occur at 2-millisecond intervals. The receive and transmit slip buffers must be enabled in each of the framers. Within the 2-millisecond period, the 32 data and signaling time slots for each of the four framers are repeated 16 times.

The 8 Mbit/s H-MVIP/H.100 Mode provides dual receive and transmit highways, which are shared by the four framers. The receive highway consists of a data bus (RDATA1), a signaling bus (RSIGL1), a clock (RCLK1), and a synchronization signal (RSYNC1). The transmit highway consists of a data bus (TDATA1), a signaling bus (TSIGL1), a clock (TCLK1), and a synchronization signal (TSYNC1). The data and signaling time slots for each of the four framers are byte-interleaved on the data and signaling highways, starting with framer 1 bit 1 of Time Slot 0, followed by framer 1 bits 2 through 8 of Time Slot 0, then framer 2 bits 1 through 8 of Time Slot 0, and so on, ending with framer 4 bits 1 through 8 of Time Slot 31. In this mode, the separate data and signaling highways operate at 8.192 Mbit/s. However, the clock rate is 16.384 MHz. The receive and transmit system interfaces are synchronized by pulses that occur at 125-microsecond intervals. The receive and transmit slip buffers must be enabled in each of the framers.

The 16 Mbit/s PCM Highway Mode provides single receive and transmit highways which are shared by the four framers. The receive highway consists of a data bus (RDATA1), a clock (RCLK1), and a synchronization signal (RSYNC1). The transmit highway consists of a data bus (TDATA1), a clock (TCLK1), and a synchronization signal (TSYNC1). The data and signaling time slots for each of the four framers are bit-interleaved on the data highway, starting with framer 1 data Time Slot 0 bit 1, followed by framer 1 signaling Time Slot 0 bit 1, framer 2 data Time Slot 0 bit 1, framer 2 signaling Time Slot 0 bit 1, and ending with framer 4 signaling Time Slot 31 bit 8. In this mode, the single data highway operates at 16.384 Mbit/s. The receive and transmit system interfaces are synchronized by pulses that occur at 125-microsecond intervals. The receive and transmit slip buffers must be enabled in each of the framers.

For the framer 1 terminal side interface, multiplexers are used to distribute the data and signaling highways from the 8 Mbit/s and 16 Mbit/s Transmission Modes, the 8 Mbit/s H-MVIP/H.100 Mode, and the 16 Mbit/s PCM Highway Mode, to the four individual framers. For the 2 Mbit/s Transmission Mode, and the 2 Mbit/s MVIP Mode, separate data and signaling highways are used for the four framers.

A transmit buffer is provided to absorb low speed jitter in the transmit data. Each Transmit Slip Buffer block controls time slot access and retiming for the framer by using a two-frame buffer that can be optionally bypassed in the Transmission Modes. When the transmit buffer is enabled, transmit time slots are written into the buffer by the transmit system clock (TCLKn), and they are read out from the buffer by the receive clock (LRCLKn), local oscillator (LO), or transmit system clock (TCLKn). A phase shift between the two clocks is detected in this block, and a deletion or repetition of one frame of data (i.e., 31 time slots, or 30 time slots if Time Slot 16 is assigned for signaling) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access to the read and write pointers is also provided. Buffer alarm indications are also provided. The slip buffer may be recentered by the microprocessor, or automatically. Individual time slots can be accessed by the microprocessor for the insertion of system idle or out of service codes.

The Transmit Framer block forms the frame (with or without the CRC multiframe) with time slots read from the Transmit Slip Buffer block, and signaling information from the Transmit Signaling block. The international bits from the signaling highway are inserted into Time Slot 0 via a buffer when the framing mode is selected. The national bits in Time Slot 0 can be inserted from the HDLC block or from the system interface via a buffer. The

CRC-4 is calculated as specified in ITU-T Recommendation G.706 and inserted in Time Slot 0. The Remote Alarm Indication for Time Slot 0 is inserted as a result of a receiver loss of frame alignment alarm, or by the microprocessor, or via the signaling highway (TSIGLn). A single frame bit error, or CRC-4 error, can be generated for test purposes. The Transmit Framer and Transmit Slip Buffer can be bypassed if the unframed mode of operation is selected in the 2 Mbit/s Transmission Mode.

Each framer has a full duplex HDLC block. The HDLC block can be configured to send and receive messages using any of the five spare bits reserved for national use (Sa bits) in Time Slot 0 in alternating frames. A 16-byte FIFO is provided in each direction. Interrupt and status alarm support is provided to facilitate FIFO servicing for long messages. The HDLC controller supports zero bit stuffing/destuffing, ITU-T CRC generation/checking, flag generation/detection, abort generation/detection, start of frame detection, end of frame detection, and FIFO underflows and overflows.

The Line Interface Control block provides a serial port for communicating with an external line interface transceiver. This allows the system microprocessor to control the transceiver through the QE1F-*Plus*. The interface consists of a data output pin (LSDO), clock output pin (LSCLK), and a data input pin (LSDI). These signals are shared between all of the transceivers. Each transceiver is selected by the QE1F-*Plus*, using individual chip select output signals ($\overline{\text{LCSn}}$). In addition, a general purpose input pin (LINTn) can be used to generate a maskable interrupt.

The Test Access Port block includes a five-pin Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This Test Access Port block provides external boundary scan to read and write the QE1F-*Plus* input and output pins from the TAP for board and component testing. In addition, a four-byte read only memory location is provided for reading the JEDEC manufacturer ID, QE1F-*Plus* part number, and version number of the part.

To assist in testing, built-in Pseudo Random Binary Sequence (PRBS) Generator and Analyzer blocks are provided. The PRBS Generator and Analyzer support the 2^{15}-1 bit pseudo random binary sequence which is specified in the ITU-T Recommendation O.151. Each framer may select the PRBS Generator and Analyzer. The output of the Analyzer is provided on pin PRBSOOL. The PRBS framed mode is selected by writing a 1 to bit 6 in register 013H and is intended for use as a self-test feature. In this mode, the PRBS Generator and Analyzer can only communicate and frame up within the framer itself. The QE1F-*Plus* also provides local loopback, remote line loopback, remote time slot loopback and payload remote loopback options for each framer.

The QE1F-*Plus* can be configured to operate with either Intel or Motorola compatible microprocessors via the Microprocessor Input/Output Interface block. Interrupt capability is provided with global and individual framer mask bits. An option is provided in software which permits the interrupt polarity to be inverted. An external system clock is used to run the internal state machines.

PIN DIAGRAM

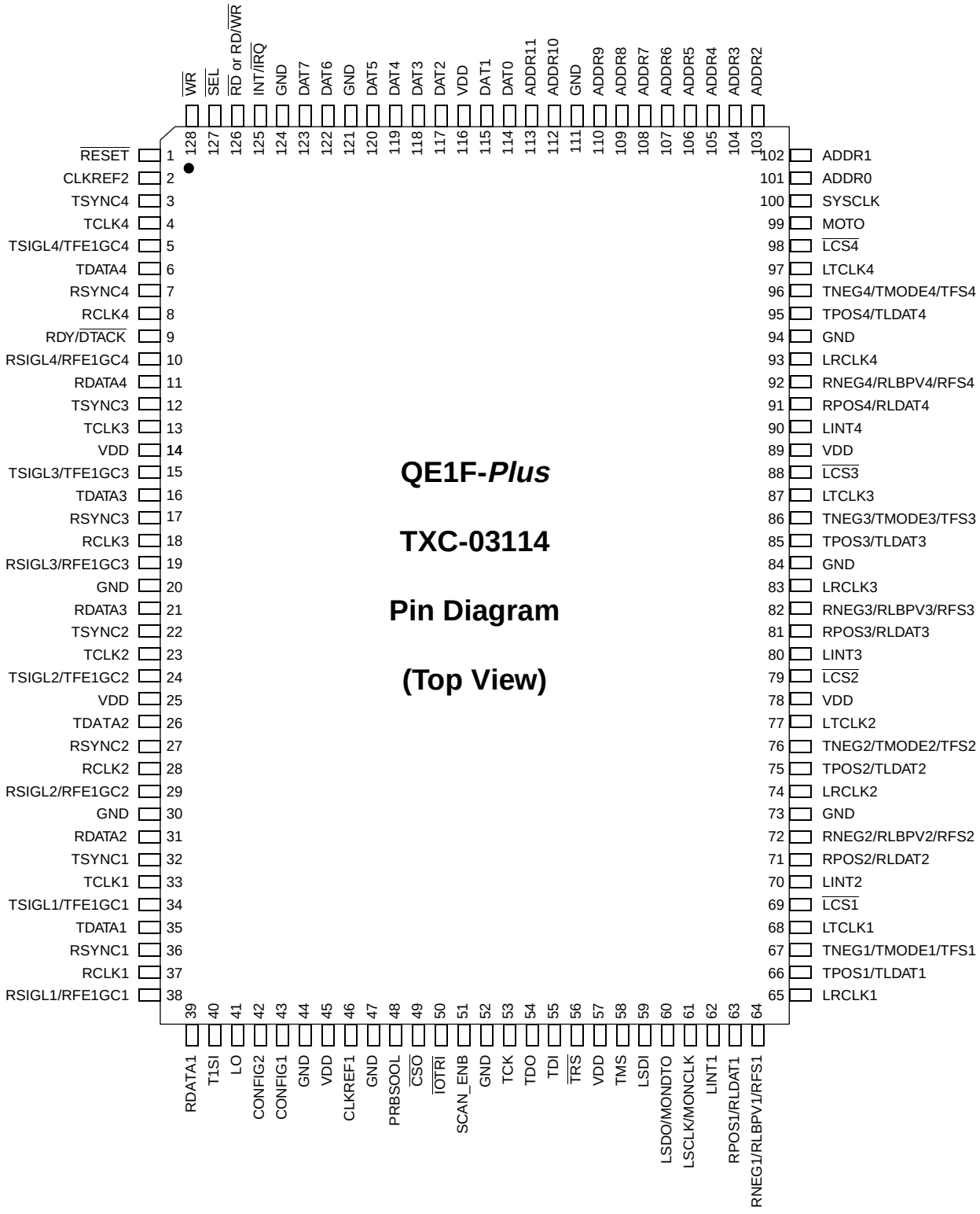


Figure 2. QE1F-*Plus* TXC-03114 Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	14, 25, 45, 57, 78, 89, 116	P		**Power Supply:** +3.3 or +5 volt supply voltage, ±5%.
GND	20, 30, 44, 47, 52, 73, 84, 94, 111, 121, 124	P		**Ground:** 0 volt reference.

* Note: I = Input; O = Output; P = Power; T=Tri-state.

Line Interface Signals

Symbol	Pin No.	I/O/P	Type *	Name/Function **
RPOSn/ RLDATn (n=4-1)	91 81 71 63	I	CMOS	**Receive Unipolar Positive Signal Input:** When control bit RAIL (bit 7 in X00H) is a 1, the dual unipolar mode is selected, and the RPOSn pin carries the receive positive rail input signal. RPOSn is high whenever a positive pulse is received by the external line interface transceiver. **Receive Line (NRZ) Data Input:** When control bit RAIL (bit 7 in X00H) is a 0, the NRZ mode is selected, and the RLDATn pin carries the receive NRZ data input signal. RLDATn is normally active high whenever a positive or negative pulse is received by the external line interface transceiver. When control bit RXNRZP (bit 0 in register X01H) is a 1, the QE1F-*Plus* accepts an inverted data signal and RLDATn is active low.
RNEGn/ RLBPVn/ RFSn (n=4-1)	92 82 72 64	I	CMOS	**Receive Unipolar Negative Signal Input:** When control bit RAIL (bit 7 in X00H) is a 1, the dual unipolar mode is selected, and the RNEGn pin carries the receive negative rail input signal. RNEGn is high whenever a negative pulse is received by the external line interface transceiver. **External Receive Bipolar Violation Indication Input:** When control bit RAIL (bit 7 in X00H) is a 0 and the fast sync option is not selected (control bit RXFS, bit 1 in X06H, is a 0), the RLBPVn pin provides an input for indications of external bipolar violations detected in the external line interface transceiver. A high indicates a bipolar violation, and increments the internal 16-bit coding violation counter once on a clock cycle. A bipolar violation is clocked in on rising edges of the receive line clock LRCLKn. **Receive Fast Sync:** When control bit RAIL (bit 7 in X00H) is a 0 and the fast sync mode is selected (control bit RXFS, bit 1 in X06H, is 1), this pin is used for a fast sync feature. A pulse on this pin is interpreted as identifying bit 256 of the last frame of the multiframe.

* Note: See Input, Output and I/O Parameters section for Type definitions.

** Note: The value of X (hex.), which is used as the MS digit of register addresses for per channel memory bits, such as X01H, is equal to the value of n (dec.) used in pin symbols when both relate to the same channel or framer (number n, where n=1-4). Register addresses such as 006H, which have 0 as the MS digit instead of X, contain bits that are common to all four framers.

Symbol	Pin No.	I/O/P	Type *	Name/Function **
LRCLKn (n=4-1)	93 83 74 65	I	CMOS	**Receive Line Clock:** An input for the 2048 kHz recovered clock from the external line interface transceiver. Control bit RXCP (bit 6 in X01H) determines the clock edge on which the receive line signals RPOSn/ RNEGn and RLDATn are to be clocked in (1 for rising edge). This pin is active only in the NRZ mode.
TPOSn/ TLDATn (n=4-1)	95 85 75 66	O	CMOS 2mA	**Transmit Unipolar Positive Signal Output:** When control bit RAIL (bit 7 in X00H) is a 1, the dual unipolar mode is selected, and the TPOSn pin carries the transmit positive rail output signal. TPOSn is high whenever a positive pulse is to be transmitted by the external line interface transceiver. **Transmit Line (NRZ) Data Output:** When control bit RAIL (bit 7 in X00H) is a 0, the NRZ mode is selected, and the TLDATn pin carries the transmit NRZ data output signal. TLDATn is normally active high whenever a positive or negative pulse is to be transmitted by the external line interface transceiver. When control bit TXNRZP (bit 5 in register X01H) is a 1, the data output TLDATn is inverted and it is active low.
TNEGn/ TMODEn/ TFSn (n=4-1)	96 86 76 67	O	CMOS 2mA	**Transmit Unipolar Negative Signal Output:** When control bit RAIL (bit 7 in X00H) is a 1, the dual unipolar mode is selected, and the TNEGn pin carries the transmit negative rail output signal. TNEGn is high whenever a negative pulse is to be transmitted by the external line interface transceiver. **Transmit Mode General Purpose Output:** When control bit RAIL (bit 7 in X00H) is a 0 and the fast sync mode is not selected (control bit TXFS, bit 0 in X06H, is a 0), the state written into bit BE (bit 6 in X00H) is clocked out on rising edges of the transmit line clock LTCLKn. **Transmit Fast Sync:** When control bit RAIL (bit 7 in X00H) is a 0 and the fast sync mode is selected (control bit TXFS, bit 0 in X06H is a 1), this pin is used for a fast sync feature. A pulse is sent on this pin every 2 ms, corresponding to bit 256 of the last frame in the multiframe.
LTCLKn (n=4-1)	97 87 77 68	O	CMOS 2mA	**Transmit Line Clock:** A 2048 kHz clock output. Control bit TXCP (bit 7 in X01H) determines the clock edge on which the transmit line signals TPOSn/TNEGn and TLDATn are to be clocked out (1 for rising edge).

* Note: See Input, Output and I/O Parameters section for Type definitions.

** Note: The value of X (hex.), which is used as the MS digit of register addresses for per channel memory bits, such as X01H, is equal to the value of n (dec.) used in pin symbols when both relate to the same channel or framer (number n, where n=1-4). Register addresses such as 006H, which have 0 as the MS digit instead of X, contain bits that are common to all four framers.

Line Interface Control Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
LINTn (n=4-1)	90 80 70 62	I	CMOS	**General Purpose Interrupt Input Port:** When enabled by control bit LIE (bit 1 in X00H) being set to 1, the signal on this pin is logically or-gated with the internal loss of signal indication to cause a loss of signal alarm and (if enabled) an interrupt. Control bit LPOL (bit 0 in X00H) selects the input sense of this pin (1 for active low).
$\overline{\text{LCSn}}$ (n=4-1)	98 88 79 69	O	CMOS 2mA	**Line Interface Transceiver Chip Select:** An active low signal that enables communications in both directions between the external line interface transceiver for channel n and the QE1F-*Plus*.
LSCLK/ MONCLK	61	O(T)	CMOS 2mA	**Line Interface Transceiver Clock Signal:** The clock for the transceiver is enabled when the CONFIG2 pin (pin 42) is low. This clock is shared between the four external transceivers. It is used to clock input data, and output data, between the external line interface transceiver and the QE1F-*Plus*. Output data (LSDO) is clocked out of the QE1F-*Plus* on falling edges of this clock. Input data (LSDI) is clocked into the QE1F-*Plus* on rising edges of this clock. This clock is derived from the signal at the LO pin (pin 41). **Monitor Clock Signal:** The monitor feature is enabled when the CONFIG2 pin (pin 42) is high. The MONCLK pin provides either a receive or transmit NRZ clock. The clock in this mode can be tri-stated by writing a 0 to control bit ESP/EMON (bit 4 in 013H).
LSDO/ MONDTO	60	O(T)	CMOS 2mA	**Line Interface Transceiver Data Output Signal:** The output data signal for the transceivers is enabled when the CONFIG2 pin (pin 42) is low. The output data signal is shared between the four transceivers. **Monitor Data Signal:** The monitor feature is enabled when the CONFIG2 pin (pin 42) is high. The MONDTO pin provides either a NRZ receive or transmit data signal. This pin can be tri-stated in this mode by writing a 0 to control bit ESP/EMON (bit 4 in 013H).
LSDI	59	I	CMOS	**Line Interface Transceiver Data Input Signal:** The input data signal from the transceivers is enabled when the CONFIG2 pin (pin 42) is low. The input data signal is shared between the four transceivers.

Clock Reference Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
CLKREF1	46	O(T)	CMOS 2mA	**Clock Reference 1:** This clock reference output is enabled when control bit ENREF1 (bit 3 in 019H) is a 1. The clock reference signal can be either a 2048 kHz clock or an 8 kHz clock. When control bit 2048KHZ (bit 4 in 019H) is a 1, the 2048 kHz reference is selected. The framer from which the clock is derived is determined by selection bits CR1S1 and CR1S0 (bits 1 and 0 in 019H). This pin is forced low when a loss of signal alarm occurs for the framer selected.
CLKREF2	2	O(T)	CMOS 2mA	**Clock Reference 2:** This clock reference output is enabled when control bit ENREF2 (bit 5 in 019H) is a 1. The clock reference signal can be either a 2048 kHz clock or an 8 kHz clock. When control bit 2048KHZ (bit 4 in 019H) is a 1, the 2048 kHz reference is selected. The framer from which the clock is derived is determined by selection bits CR2S1 and CR2S0 (bits 7 and 6 in 019H). This pin is forced low when a loss of signal alarm occurs for the framer selected.

System Interface Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
TSYNCn (n=4-1)	3 12 22 32	I	CMOS	**Transmit Sync Pulse**: This signal is used to synchronize both the frame sync and signaling multiframe sync counters within a QE1F-*Plus* framer and is sourced by the system. The following table is a summary of the sync pulse characteristics used for the various system interfaces. Interface / Width / Polarity / Period / Lead Used 2 Mbit/s Trans / 1 Clk Cyc / High / 2 ms / TSYNCn 8 Mbit/s Trans / 2 Clk Cyc / High / 2 ms / TSYNC1 16 Mbit/s Trans / 1 Clk Cyc / High / 2 ms / TSYNC1 2 Mbit/s MVIP / 1 Clk Cyc / Low / 125 µs / TSYNCn 8 Mbit/s H-MVIP / 4 Clk Cyc / Low / 125 µs / TSYNC1 8 Mbit/s H.100 / 2 Clk Cyc / Low / 125 µs / TSYNC1 16 Mbit/s PCM / 1 Clk Cyc / High / 125 µs / TSYNC1 Note: The sync pulse is also programmable with respect to the transmit data highway.
TCLKn (n=4-1)	4 13 23 33	I	CMOS	**Transmit Clock:** This clock is sourced from the system. It is used to clock in the TSYNCn, TSIGLn, and TDATAn signals from the system. The following table is a summary of the clock rates and clock transitions used for clocking in data (D), signaling (S), and the sync. Interface / Rate / Clk in D/S / Clk in Sync / Lead Used 2 Mbit/s Trans / 2.048 MHz / Pos. / Pos. / TCLKn 8 Mbit/s Trans / 16.384 MHz / Pos. / Pos. / TCLK1 16 Mbit/s Trans / 16.384 MHz / Pos. / Pos. / TCLK1 2 Mbit/s MVIP / 2.048 MHz / Neg. / Pos. / TCLKn 8 Mbit/s H-MVIP/H.100 / 16.384 MHz / Pos. / Neg. / TCLK1 16 Mbit/s PCM / 16.384 MHz / Pos. / Pos. / TCLK1

Symbol	Pin No.	I/O/P	Type	Name/Function
TDATAn (n=4-1)	6 16 26 35	I	CMOS	**Transmit Data Highway Input:** This lead carries the data time slots from the system interface to the QE1F-*Plus*. The following table is a summary of the transmit data highway format. Interface — Format 2 Mbit/s Trans — E1 frame repeated 16 times on TDATAn 8 Mbit/s Trans — Four E1 frames repeated 16 times, byte-interleaved on TDATA1 16 Mbit/s Trans — Four E1 and signaling frames repeated 16 times, bit-interleaved on TDATA1 2 Mbit/s MVIP — E1 frame on TDATAn 8 Mbit/s H-MVIP/H.100 — Four E1 frames, byte-interleaved on TDATA1 16 Mbit/s PCM — Four E1 and signaling frames, bit-interleaved on TDATA1
TSIGLn/ TFE1GCn (n=4-1)	5 15 24 34	I/O	CMOS 2mA	**Transmit Signaling Highway Input:** This lead carries from the system the signals that represent the international bits, national bits, and remote alarm associated with Time Slot 0, signaling information, and system alarm information, according to the table given below. Interface — Format 2 Mbit/s Trans — 32 time slots repeated 16 times on TSIGLn 8 Mbit/s Trans — 32 time slots for 4 framers repeated 16 times, byte-interleaved on TSIGL1 16 Mbit/s Trans — Not Used 2 Mbit/s MVIP — 32 time slots on TSIGLn 8 Mbit/s H-MVIP/H.100 — 32 time slots for 4 framers repeated 16 times byte-interleaved on TSIGL1 16 Mbit/s PCM — Not used **Transmit Fractional E1 Gapped Clock Output:** The Transmit Fractional E1 gapped clock feature is enabled when the CONFIG1 pin is low, control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are both set to 0 (2 Mbit/s Transmission Mode) and control bit FE1M (bit 0 in register X02H) is written with a 1. A gapped clock is provided on the pin for the Fractional E1 channel(s) selected. One or more time slots may be selected by writing a 1 to control bits TFTS31-TFTS0 in registers X3CH-X3FH. The gapped clock has the same phase as the TCLKn clock.

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>RSYNCn
(n=4-1)</td><td>7
17
27
36</td><td>I/O</td><td>CMOS
2mA</td><td>Receive Sync Pulse: This signal is used to synchronize external system circuitry from the QE1F-Plus. The following table is a summary of the sync pulses used for the various system interfaces.

<table>
<tr><th>Interface</th><th>Width</th><th>Polarity</th><th>Period</th><th>Lead Used</th></tr>
<tr><td>2 Mbit/s Trans</td><td>1 Clk Cyc</td><td>High</td><td>2 ms</td><td>RSYNCn</td></tr>
<tr><td>8 Mbit/s Trans</td><td>2 Clk Cyc</td><td>High</td><td>2 ms</td><td>RSYNC1</td></tr>
<tr><td>16 Mbit/s Trans</td><td>1 Clk Cyc</td><td>High</td><td>2 ms</td><td>RSYNC1</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>1 Clk Cyc</td><td>Low</td><td>125 µs</td><td>RSYNCn</td></tr>
<tr><td>8 Mbit/s H-MVIP</td><td>4 Clk Cyc</td><td>Low</td><td>125 µs</td><td>RSYNC1</td></tr>
<tr><td>8 Mbit/s H.100</td><td>2 Clk Cyc</td><td>Low</td><td>125 µs</td><td>RSYNC1</td></tr>
<tr><td>16 Mbit/s PCM</td><td>1 Clk Cyc</td><td>High</td><td>125 µs</td><td>RSYNC1</td></tr>
</table>
Note: In the 2 Mbit/s Transmission Mode, the QE1F-Plus can source the sync pulse and clock. The sync pulse is also programmable with respect to the receive data highway.</td></tr>
<tr><td>RCLKn
(n=4-1)</td><td>8
18
28
37</td><td>I/O</td><td>CMOS
2mA</td><td>Receive Clock: This clock is used to clock the RDATAn, RSIGLn, and RSYNCn signals from the system or (for RSYNCn) into the system. The following table is a summary of the clock rates and clock transitions used for clocking data (D), signaling (S), and the sync pulse.

<table>
<tr><th></th><th></th><th>Clk out</th><th>Clk in</th><th></th></tr>
<tr><th>Interface</th><th>Rate</th><th>D/S</th><th>Sync</th><th>Lead Used</th></tr>
<tr><td>2 Mbit/s Trans</td><td>2.048 MHz</td><td>Neg.</td><td>Pos.</td><td>RCLKn</td></tr>
<tr><td>8 Mbit/s Trans</td><td>16.384 MHz</td><td>Neg.</td><td>Pos.</td><td>RCLK1</td></tr>
<tr><td>16 Mbit/s Trans</td><td>16.384 MHz</td><td>Neg.</td><td>Pos.</td><td>RCLK1</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>2.048 MHz</td><td>Pos.</td><td>Pos.</td><td>RCLKn</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>16.384 MHz</td><td>Neg.</td><td>Pos.</td><td>RCLK1</td></tr>
<tr><td>16 Mbit/s PCM</td><td>16.384 MHz</td><td>Neg.</td><td>Pos.</td><td>RCLK1</td></tr>
</table>
Note: In the 2 Mbit/s Transmission Mode, RSYNCn is clocked out on negative clock transitions when the sync pulse is an output.</td></tr>
<tr><td>RDATAn
(n=4-1)</td><td>11
21
31
39</td><td>O</td><td>CMOS
2mA
for
n=4-2

CMOS
8mA
for n=1</td><td>Receive Data Highway Output: This lead carries the time slots from the QE1F-Plus to the system. The following table is a summary of the receive data highway format.

<table>
<tr><th>Interface</th><th>Format</th></tr>
<tr><td>2 Mbit/s Trans</td><td>E1 frame repeated 16 times on RDATAn</td></tr>
<tr><td>8 Mbit/s Trans</td><td>Four E1 frames repeated 16 times, byte-interleaved on RDATA1</td></tr>
<tr><td>16 Mbit/s Trans</td><td>Four E1 and signaling frames repeated 16 times, bit-interleaved on RDATA1</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>E1 frame on RDATAn</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>Four E1 frames, byte-interleaved on RDATA1</td></tr>
<tr><td>16 Mbit/s PCM</td><td>Four E1 and signaling frames, bit-interleaved on RDATA1</td></tr>
</table></td></tr>
</table>

Symbol	Pin No.	I/O/P	Type	Name/Function
RSIGLn/ RFE1GCn (n=4-1)	10 19 29 38	O	CMOS 2mA for n=4-2 CMOS 8mA for n=1	**Receive Signaling Highway Output:** This lead carries to the system the signals that represent the international bits, national bits, and remote alarm associated with Time Slot 0, signaling information, and system alarm information, according to the table given below. Interface — Format 2 Mbit/s Trans — 32 time slots repeated 16 times on RSIGLn 8 Mbit/s Trans — 32 time slots for 4 framers repeated 16 times, byte-interleaved on RSIGL1 16 Mbit/s Trans — Not Used 2 Mbit/s MVIP — 32 time slots on RSIGLn 8 Mbit/s H-MVIP/H.100 — 32 time slots for 4 framers repeated 16 times, byte-interleaved on RSIGL1 16 Mbit/s PCM — Not used **Receive Fractional E1 Gapped Clock Output:** The Received Fractional E1 gapped clock feature is enabled when the CONFIG1 pin is low, control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are both set to 0 (2 Mbit/s Transmission Mode) and control bit FE1M (bit 0 in register X02H) is written with a 1. A gapped clock is provided on this pin for the Fractional E1 channel(s) selected. One or more time slots may be selected by writing a 1 to control bits RFTS31-RFTS0 in registers X38H-X3BH. The gapped clock has the same phase as the RCLKn clock.
LO	41	I	CMOS	**Local Oscillator Input:** This independent 2048 kHz ± 50 ppm (50 ± 10)% duty cycle clock is an alternate clock source for the transmit line clock (LTCLKn), and for clocking out data from the slip buffer. This clock is selected as the transmit clock source when control bits TXC1 and TXC0 (bits 7 and 6 in X02H) are both set to 0. On detection of Loss of Signal, this clock is substituted for the receive line clock (LRCLKn) which becomes RCLKn when control bit RXC (bit 5 in register X02H) is set to a 1. This clock is required for generating LSCLK (pin 61) and the PRBS generator function. When used for the PRBS generator, the input LO must be synchronous and in phase with TCLKn.

Other Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
T1SI	40	I	CMOS	**One Second Shadow Register Signal**: A positive pulse occurring every second which operates the latched performance counters and shadow registers when the shadow register feature is enabled. The shadow register feature is enabled when a 1 is written to control bit ENPMFM (bit 3 in 006H).

Symbol	Pin No.	I/O/P	Type	Name/Function
CONFIG2	42	I	CMOS	**Configuration 2 Select Pin**: A low enables the line control interface for communications between the QE1F-*Plus* and the external line interface transceivers. A high disables the line control interface, and configures clock and data pins for a monitor interface. The selection is common to all four framers.
CONFIG1	43	I	CMOS	**Configuration 1 Select Pin**: A low configures the QE1F-*Plus* for the Transmission Modes of operation (2, 8, and 16 Mbit/s) at the system interface. A high configures the QE1F-*Plus* for the 2 Mbit/s MVIP, the 8 Mbit/s H-MVIP/ H.100, and the 16 Mbit/s PCM Highway Modes of operation at the system interface. The selection is common to all four framers.
$\overline{\text{CSO}}$	49	I	CMOS	**Power Down**: An active low on this pin forces the transmit clock (LTCLKn), and the transmit unipolar leads (TPOSn and TNEGn) for rail data output signals, of all four framers to the active low state for protection switching purposes.
PRBSOOL	48	O	CMOS 2mA	**PRBS Out Of Lock:** Enabled only in the 2 Mbit/s Transmission Mode and when control bit PRBSEN (bit 5 in 013H) is a 1. A high indicates the analyzer is out of lock. This pin is low when lock is acquired or when this feature is disabled.
$\overline{\text{IOTRI}}$	50	I	TTL	**High Z State:** An active low placed on this pin forces all output pins (except TDO) to a high impedance state for test purposes. This pin must be held high for normal operation.
SCAN_ENB	51	I	CMOS	**TranSwitch Test Pin:** This pin is used for manufacturing tests only and must be held low for normal operation.

Boundary Scan

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	53	I	TTL	**IEEE 1149.1 Test Port Serial Scan Clock:** This clock is used to shift data in from pin TDI on rising edges, and to shift data out on pin TDO on falling edges. The maximum clock frequency is 10 MHz.
TMS	58	I	TTLp	**IEEE 1149.1 Test Port Mode Select:** This signal is clocked in on rising edges of the clock TCK, and is used to place the Test Access Port Controller into various states as defined in the IEEE 1149.1 standard. This pin must be high for normal framer operation.
TDI	55	I	TTLp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked in to this pin on rising edges of clock TCK.

Symbol	Pin No.	I/O/P	Type	Name/Function
TDO	54	O (T)	TTL 4mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this pin on falling edges of clock TCK. When inactive (i.e., $\overline{\text{TRS}}$ is low), this output is forced to the high impedance state.
$\overline{\text{TRS}}$	56	I	TTLp	**IEEE 1149.1 Test Port Reset Pin:** This pin must either be held low, asserted low, or asserted low then high (pulsed low, minimum 10 ns) to asynchronously reset the Test Access Port (TAP) controller. Failure to do so may cause the TAP controller to take control of the QE1F-*Plus* output pins.

Microprocessor Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
MOTO	99	I	TTL	**Motorola/Intel Processor Select:** This pin defines the operating mode of the Microprocessor Input/Output Interface. When it is high, Motorola (M) Mode is selected. When it is low, Intel (I) Mode is selected.
ADDR(11-0)	113, 112 110-101	I	TTL	**Address Bus (Motorola/Intel Buses):** These pins are address line inputs that are used for accessing a register location for a read/write cycle. High is logic 1.
DAT(7-0)	123, 122, 120-117, 115, 114	I/O (T)	TTL 8mA	**Data Bus:** Bidirectional data lines used for transferring data. High is logic 1.
$\overline{\text{SEL}}$	127	I	TTLp	**Select:** A low enables data transfers between the microprocessor and the QE1F-*Plus* during a read/write cycle.
$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	126	I	TTL	**Read (I Mode) or Read/Write (M Mode):** Intel Mode - An active low signal generated by the microprocessor for reading the QE1F-*Plus* register locations. Motorola Mode - An active high signal generated by the microprocessor for reading the QE1F-*Plus* register locations. An active low signal is used to write to QE1F-*Plus* register locations.
$\overline{\text{WR}}$	128	I	TTL	**Write (I Mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the QE1F-*Plus* register locations. Motorola Mode - Not used (should be set high).

Symbol	Pin No.	I/O/P	Type	Name/Function
RDY/$\overline{\text{DTACK}}$	9	O(T)	TTL 8mA	**Ready (I Mode) or Data Transfer Acknowledge (M Mode):** Intel Mode - A high is an acknowledgment from the addressed register location that the transfer can be completed. A low indicates that the QE1F-*Plus* cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data. This lead is tri-stated after the low signal.
INT/$\overline{\text{IRQ}}$	125	O	TTL 4mA	**Interrupt:** Intel Mode - A high on this output pin signals an interrupt request to the microprocessor. Motorola Mode - A low on this output pin signals an interrupt request to the microprocessor. The interrupt sense is inverted when a 1 is written to control bit IPOL (bit 4 in 006H).
$\overline{\text{RESET}}$	1	I	TTLp	**Reset:** A low placed on this pin resets the QE1F-*Plus*. The reset must be placed on this pin after the clocks become stable, and must have a minimum duration of 10 cycles of the SYSCLK system clock.
SYSCLK	100	I	TTL	**System Clock:** This asynchronous clock is used by the QE1F-*Plus* to run the internal state machines and counters. The nominal frequency of this clock is 19-22 MHz with a duty cycle of (50 ± 10)%. When recovered receive line clock (LRCLKn) is used for system side receive clock (RCLKn) by setting control bit RXC to a 1, the nominal frequency of this clock is 19-22 MHz with a duty cycle of (50 ± 10)%. When the QE1F-*Plus* is used in a gapped or jittered clock situation, the SYSCLK minimum frequency must guarantee at least 9 rising edges of SYSCLK to occur between any two consecutive rising or falling edges of any particular LRCLKn. The following table can be used to determine the required minimum SYSCLK frequency.

LRCLKn Minimum t_{CYC} (ns)	SYSCLK Minimum frequency (MHz)
480	19
456	20
435	21

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1,3
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. V_{IN} may not exceed the actual operating supply voltage (V_{DD}) by more than 0.5 volt.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			24.8	$^oC/W$	0 ft/min linear airflow.

POWER REQUIREMENTS FOR V_{DD} = 5 VOLT

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
Power dissipation, P_{DD}, with all channels operating:		300		mW	SYSCLK = 19 MHz, 25 ^oC ambient, bit rate = 2 Mbit/s, with 10 pF output load
			440	mW	SYSCLK = 22 MHz, 85 ^oC ambient, bit rate = 2 Mbit/s, with 10 pF output load

POWER REQUIREMENTS FOR V_{DD} = 3.3 VOLT

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.3	3.45	V	
Power dissipation, P_{DD}, with all channels operating:		125		mW	SYSCLK = 19 MHz, 25 ^oC ambient, bit rate = 2 Mbit/s, with 10 pF output load
			165	mW	SYSCLK = 22 MHz, 85 ^oC ambient, bit rate = 2 Mbit/s, with 10 pF output load

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR 5 VOLT OPERATION

Input Parameters for CMOS at V_{DD} = 5 Volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters for TTL at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters for TTLp at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volt
Input capacitance		3.5		pF	

Note: Input has a 9k (nominal) internal pull-up resistor.

OUTPUT PARAMETERS FOR 5 VOLT OPERATION

Output Parameters for CMOS2mA/CMOS8mA at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0/-8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0/8.0
I_{OL}			2.0/8.0	mA	
I_{OH}			-2.0/-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tri-state			±10	µA	0 to 5.25 V input

Output Parameters for TTL4mA at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			8	ns	C_{LOAD} = 15 pF
t_{FALL}			5	ns	C_{LOAD} = 15 pF

Output Parameters for TTL8mA at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

INPUT/OUTPUT PARAMETERS FOR 5 VOLT OPERATION

Input/Output Parameters for CMOS2mA at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tri-state			±10	µA	0 to 5.25 V input

Input/Output Parameters for TTL8mA (slew rate controlled) at V_{DD} = 5 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		7.0		pF	
V_{OH}	2.4		V_{DD}	V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

INPUT PARAMETERS FOR 3.3 VOLT OPERATION

Input Parameters for CMOS at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.2		V_{DD} + 0.5	V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			1.0	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		3.5		pF	

Input Parameters for TTL at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.5	V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		3.5		pF	

Input Parameters for TTLp at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.5	V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current		0.5	1.4	mA	V_{DD} = 3.45; Input = 0 volt
Input capacitance		3.5		pF	

Note: Input has a 9k (nominal) internal pull-up resistor.

OUTPUT PARAMETERS FOR 3.3 VOLT OPERATION

Output Parameters for CMOS2mA/CMOS8mA at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -2.0/-8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 2.0/8.0
I_{OL}			2.0/8.0	mA	
I_{OH}			-2.0/-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tri-state			±10	µA	0 to 3.45 V input

Output Parameters for TTL4mA at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			8	ns	C_{LOAD} = 15 pF
t_{FALL}			5	ns	C_{LOAD} = 15 pF

Output Parameters for TTL8mA at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

INPUT/OUTPUT PARAMETERS FOR 3.3 VOLT OPERATION

Input/Output Parameters for CMOS2mA at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.2		V_{DD} + 0.5	V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			1.0	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tri-state			±10	µA	0 to 3.45 V input

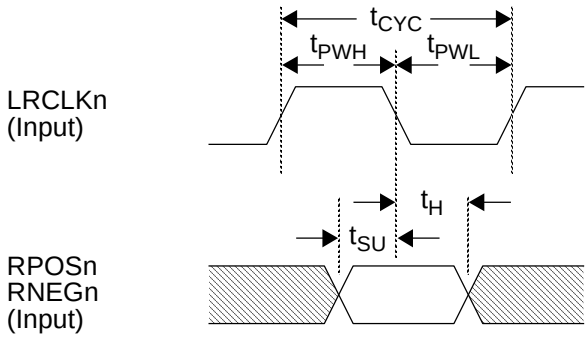
Input/Output Parameters for TTL8mA (slew rate controlled) at V_{DD} = 3.3 volt

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.5	V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		7.0		pF	
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the QE1F-*Plus* are illustrated in Figures 3 through 34, with values of the timing intervals tabulated below the waveform diagrams in each figure. All output times are measured with a maximum 25 pF load capacitance, unless otherwise indicated. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals, unless otherwise indicated.

Figure 3. Dual Unipolar (Rail) Receive Interface Timing



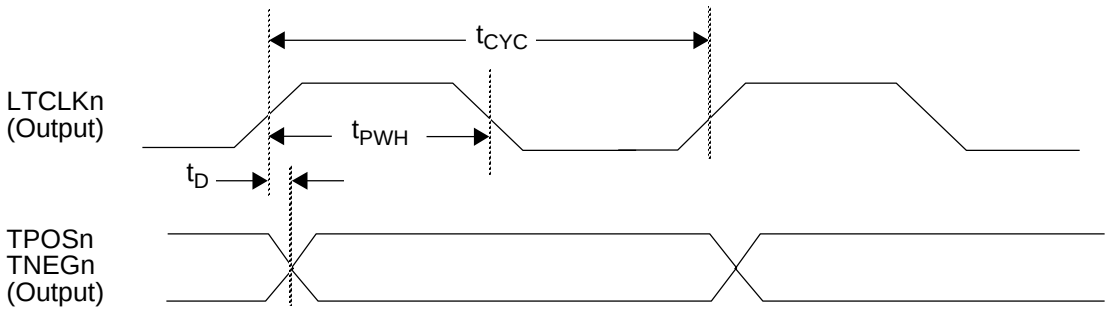
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period	t_{CYC}	435	488.3		ns
LRCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
LRCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RPOSn/RNEGn setup time to LRCLKn↓	t_{SU}	10			ns
RPOSn/RNEGn hold time after LRCLKn↓	t_H	10			ns

Notes:

1. LRCLKn is shown for control bit RXCP (bit 6) in register X01H set to 0. Data (RPOSn/RNEGn) is clocked in on the rising edges of LRCLKn when control bit RXCP is a 1.
2. The minimum frequency of SYSCLK must guarantee at least 9 rising edges of SYSCLK to occur between any two consecutive rising or falling edges of any particular LRCLKn.

Figure 4. Dual Unipolar (Rail) Transmit Interface Timing

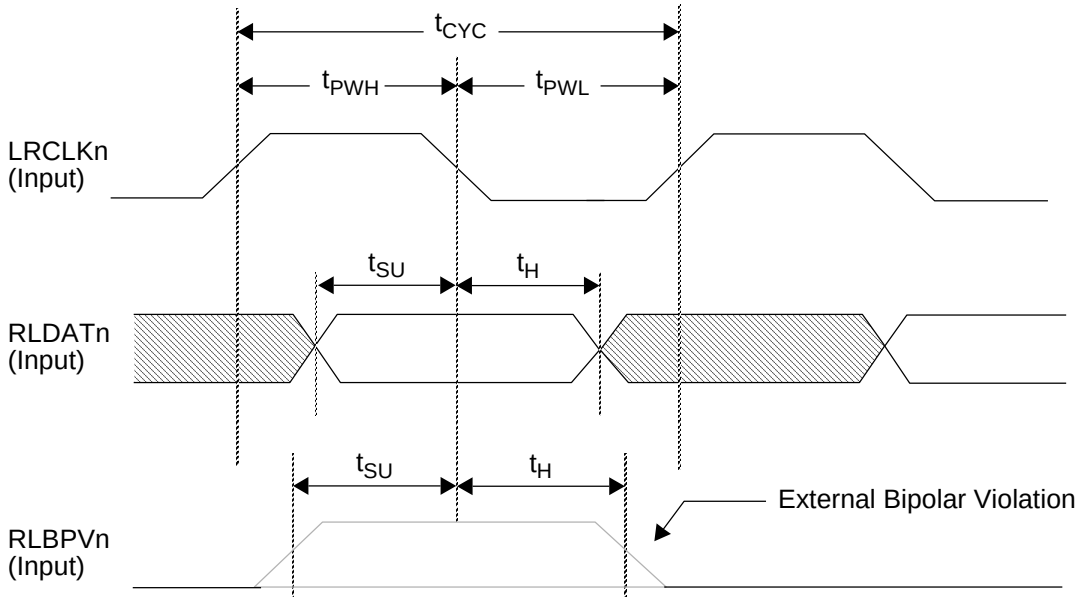


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	t_{CYC}		488.3		ns
LTCLKn duty cycle (t_{PWH}/t_{CYC})	--		50		%
TPOSn/TNEGn delay after LTCLKn↑	t_D	0.0	5.0	20	ns

Note: LTCLKn is shown for control bit TXCP (bit 7) in register X01H set to 1. Data is clocked out on falling edges of LTCLKn when control bit TXCP is a 0. If transmit clock selection chooses recovered receive line clock (pin LRCLKn) by setting control bits TXC1 to a 1 and TXC0 to a 0, the clock period and duty cycle will be the same as that received at LRCLKn (pins 65, 74, 83 and 93). If the transmit clock selection is local oscillator LO (pin 41) or transmit clock TCLKn (pins 33, 23, 13 and 4), the clock period and duty cycle will be the same as that received at the selected clock input pin.

Figure 5. NRZ Receive Interface Timing (External Transceiver)



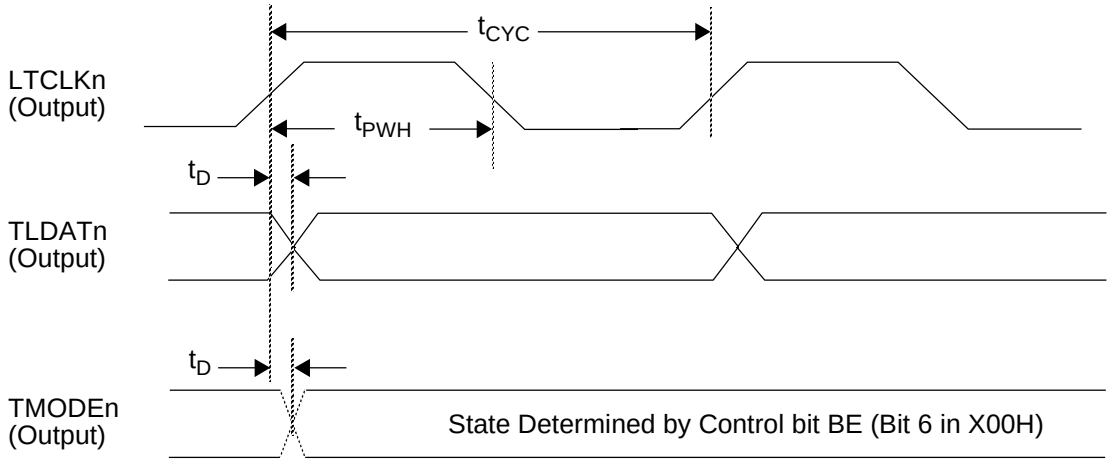
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period	t_{CYC}	435	488.3		ns
LRCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
LRCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RLDATn/RLBPVn setup time to LRCLKn↓	t_{SU}	10			ns
RLDATn/RLBPVn hold time after LRCLKn↓	t_H	10			ns

Notes:

1. LRCLKn is shown for control bit RXCP (bit 6 in register X01H) set to 0. RLDATn and RLBPVn are clocked in on rising edges of LRCLKn when control bit RXCP is a 1. The QE1F-*Plus* accepts an inverted RLDATn signal when control bit RXNRZP (bit 0 in register X01H) is a 1. Control bit RXFS (bit 1 in register X06H) must be set to 0 to use the RLBPVn input.
2. The minimum frequency of SYSCLK must guarantee at least 9 rising edges of SYSCLK to occur between any two consecutive rising or falling edges of any particular LRCLKn.

Figure 6. NRZ Transmit Interface Timing (External Transceiver)

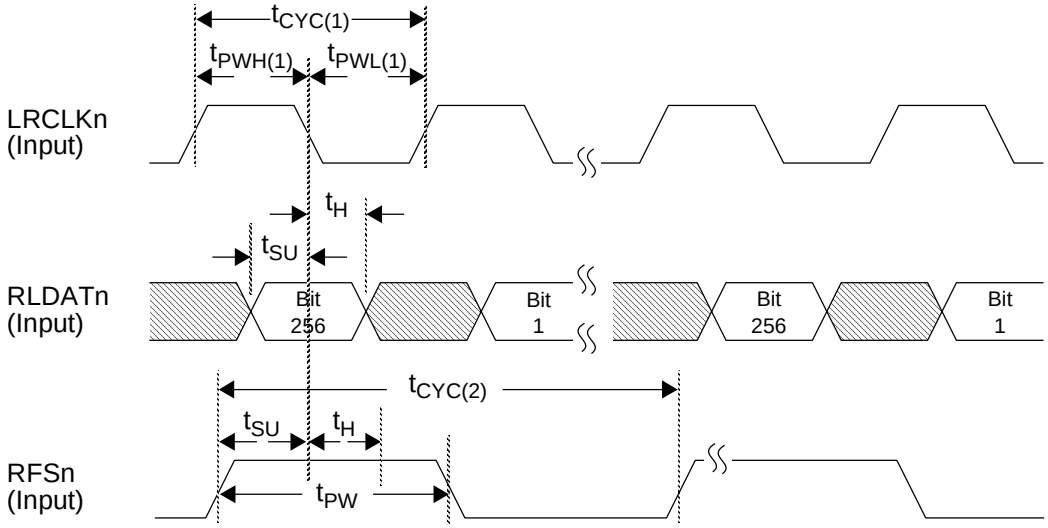


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	t_{CYC}		488.3		ns
LTCLKn duty cycle (t_{PWH}/t_{CYC})	--		50		%
TLDATn/TMODEn delay after LTCLKn↑	t_D	0.0	5.0	20	ns

Note: LTCLKn is shown for control bit TXCP (bit 7 in register X01H) set to 1. TLDATn and TMODEn are clocked out on falling edges of LTCLKn when control bit TXCP is a 0. The QE1F-*Plus* provides an inverted TLDATn signal when control bit TXNRZP (bit 5 in register X06H) is a 1. Control bit TXFS (bit 0 in register X06H) must be set to 0 to obtain the TMODEn output. If transmit clock selection chooses recovered receive line clock (pin LRCLKn) by setting control bits TXC1 to a 1 and TXC0 to a 0, the clock period and duty cycle will be the same as that received at LRCLKn (pins 65, 74, 83 and 93). If the transmit clock selection is local oscillator LO (pin 41) or transmit clock TCLKn (pins 33, 23, 13 and 4), the clock period and duty cycle will be the same as that received at the selected clock input pin.

Figure 7. NRZ Receive Interface Timing (Fast Sync Mode)

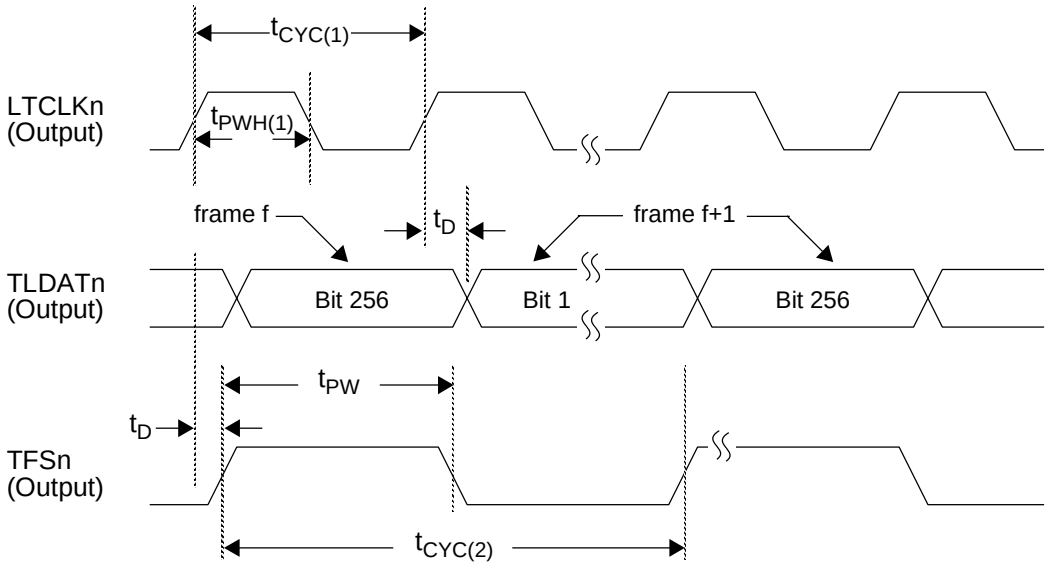


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period	$t_{CYC(1)}$	435	488.3		ns
LRCLKn high time	$t_{PWH(1)}$	180	0.5 x $t_{CYC(1)}$		ns
LRCLKn low time	$t_{PWL(1)}$	180	0.5 x $t_{CYC(1)}$		ns
RLDATn/RFSn setup time to LRCLKn↓	t_{SU}	10			ns
RLDATn/RFSn hold time after LRCLKn↓	t_{H}	10			ns
RFSn period	$t_{CYC(2)}$		256 x 16 x $t_{CYC(1)}$		ns
RFSn pulse width high time	t_{PW}	0.5 x $t_{CYC(1)}$	1 x $t_{CYC(1)}$	1.5 x $t_{CYC(1)}$	ns

Note: LRCLKn is shown for control bit RXCP (bit 6 in register X01H) set to 0. Data is clocked in on rising edges when control bit RXCP is a 1. The QE1F-*Plus* will accept an inverted RLDATn signal when a 1 is written to control bit RXNRZP (bit 0 in register X01H). The fast sync mode is selected by writing a 1 to control bit RXFS (bit 1 in register X06H).

Figure 8. NRZ Transmit Interface Timing (Fast Sync Mode)

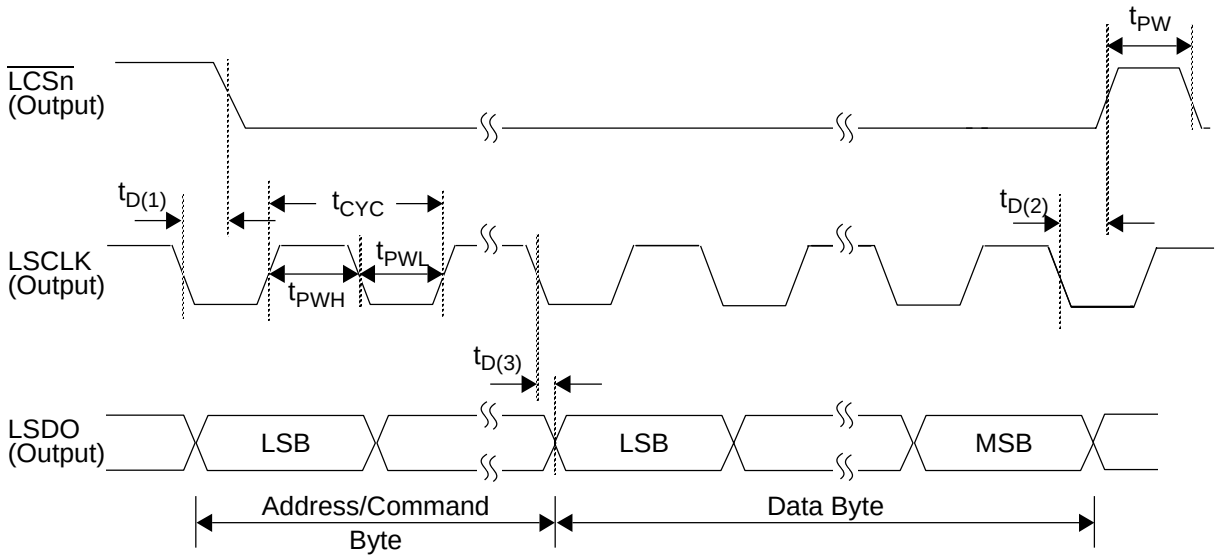


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	$t_{CYC(1)}$		488.3		ns
LTCLKn duty cycle $t_{PWH(1)}/t_{CYC(1)}$			50		%
TLDATn/TFSn delay after LTCLKn↑	t_D	0.0	5.0	20	ns
TFSn pulse width high time	t_{PW}		1 x $t_{CYC(1)}$		ns
TFSn period	$t_{CYC(2)}$		256 x 16 x $t_{CYC(1)}$		ns

Note: LTCLKn is shown for control bit TXCP (bit 7 in register X01H) set to 1. TLDATn/TFSn are clocked out on falling edges of LTCLKn when control bit TXCP is a 0. The QE1F-*Plus* will output an inverted TLDATn signal when control bit TXN-RZP (bit 5 in register X06H) is a 1. The fast sync mode is selected by writing a 1 to control bit TXFS (bit 0 in register X06H). If transmit clock selection chooses recovered receive line clock (pin LRCLKn) by setting control bits TXC1 to a 1 and TXC0 to a 0, the clock period and duty cycle will be the same as that received at LRCLKn (pins 65, 74, 83 and 93). If the transmit clock selection is local oscillator LO (pin 41) or transmit clock TCLKn (pins 33, 23, 13 and 4), the clock period and duty cycle will be the same as that received at the selected clock input pin.

Figure 9. Serial Port Write Timing



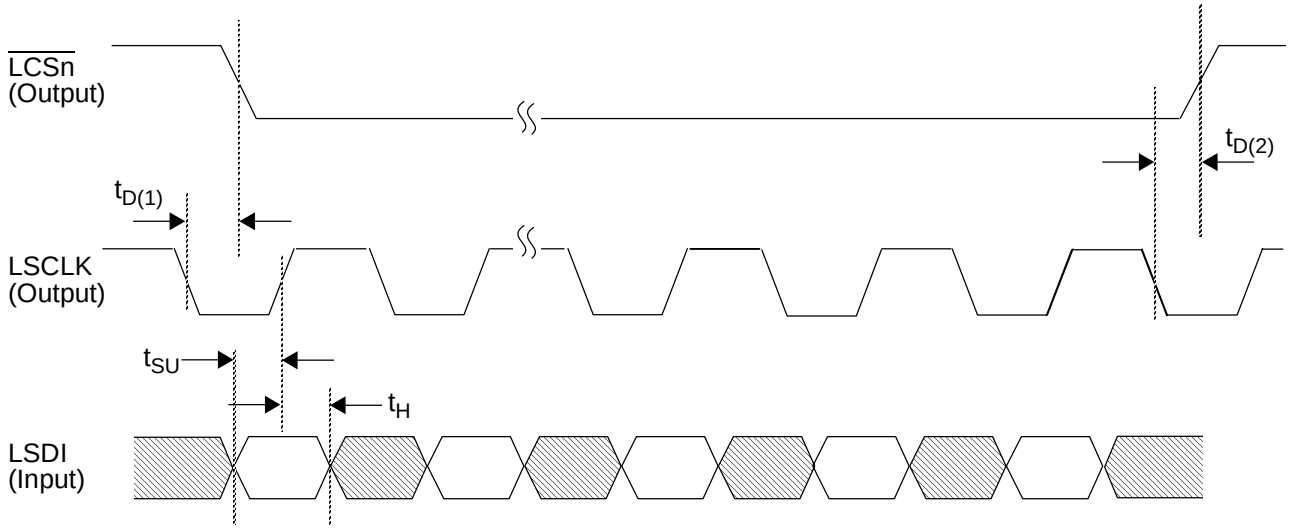
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{LCSn}}$ pulse width high time	t_{PW}	300			ns
LSCLK clock period (Note 2)	t_{CYC}	480	488.3		ns
LSCLK high time	t_{PWH}	190	0.5 x t_{CYC}		ns
LSCLK low time	t_{PWL}	190	0.5 x t_{CYC}		ns
$\overline{\text{LCSn}}\downarrow$ delay after LSCLK$\downarrow$	$t_{D(1)}$	10	15	20	ns
$\overline{\text{LCSn}}\uparrow$ delay after LSCLK$\downarrow$	$t_{D(2)}$	10	15	20	ns
LSDO delay after LSCLK$\downarrow$	$t_{D(3)}$	15	25	50	ns

Notes:

1. The serial port interface for the line interface transceiver is selected when an active low is placed on the CONFIG2 pin (pin 42).
2. The clock period for LSCLK is the same as provided on the LO pin (pin 41) since LSCLK is derived from the signal at LO.

Figure 10. Serial Port Read Timing

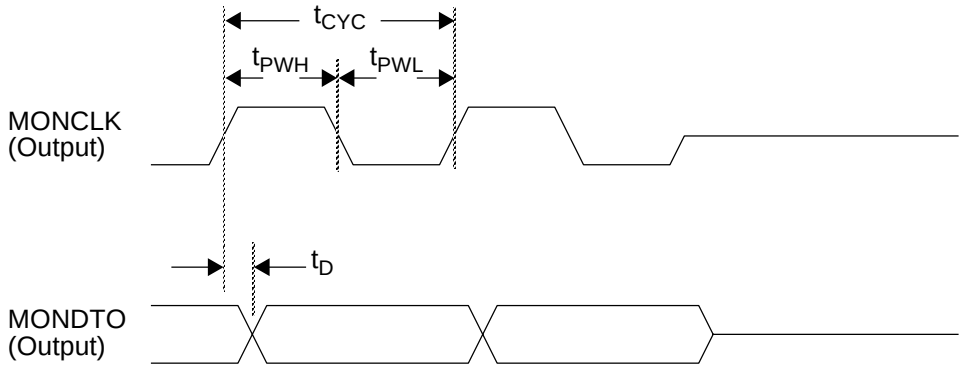


Parameter	Symbol	Min	Typ	Max	Unit
LSDI setup time to LSCLK↑	t_{SU}	10	15		ns
LSDI hold time after LSCLK↑	t_H	10	15		ns
$\overline{LCSn}$↓ delay after LSCLK↓	$t_{D(1)}$	5.0	10	15	ns
$\overline{LCSn}$↑ delay after LSCLK↓	$t_{D(2)}$	5.0	10	15	ns

Notes:

1. The serial port interface for the line interface transceiver is selected when an active low is placed on the CONFIG2 pin (pin 42).
2. The clock period for LSCLK is the same as provided on the LO pin (pin 41) since LSCLK is derived from the signal at LO.

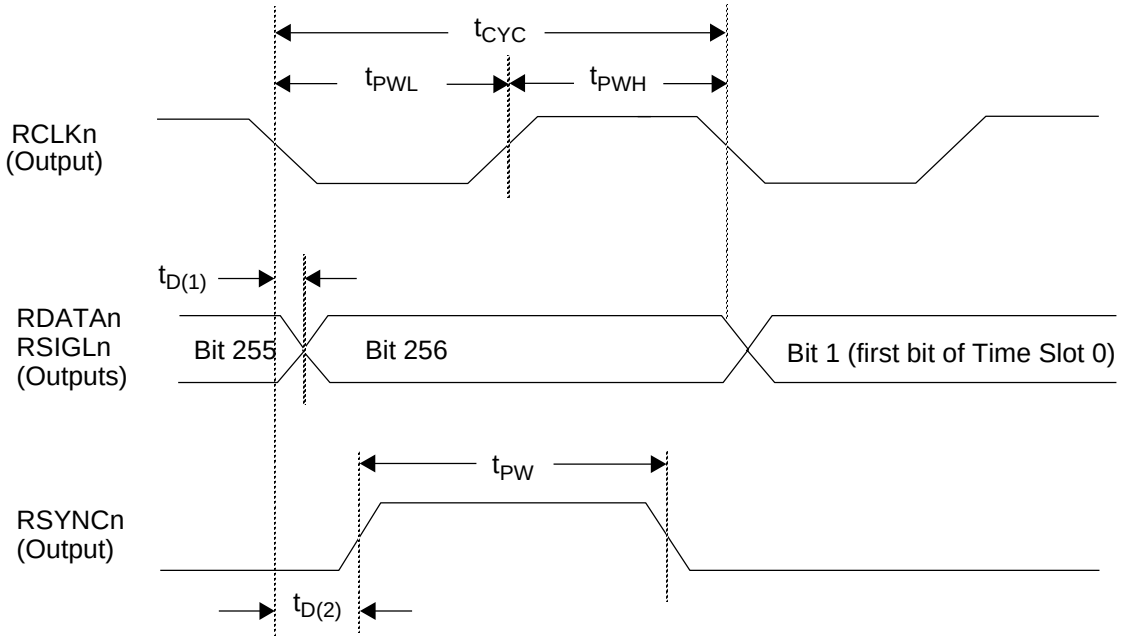
Figure 11. Monitor Mode Timing



Parameter	Symbol	Min	Typ	Max	Unit
MONCLK clock period	t_{CYC}		488.3		ns
MONCLK high time	t_{PWH}		0.5 x t_{CYC}		ns
MONCLK low time	t_{PWL}		0.5 x t_{CYC}		ns
MONDTO delay after MONCLK↑	t_D	70	75	90	ns

Note: The Monitor port is enabled when an active high is placed on the CONFIG2 pin (pin 42). Control bits E1CHCS1 and E1CHCS0 (bits 1, 0 in register 013H) select the channel to be monitored. Control bit RXTX (bit 3 in register 013H) selects either the receive side or transmit side to be monitored. Writing a 0 to control bit ESP/EMON (bit 4 in register 013H) tri-states both outputs. The clock period and duty cycle depend on the particular signal being monitored.

Figure 12. Receive Highway Timing - 2 Mbit/s Transmission Mode (Recovered Receive Line Clock)

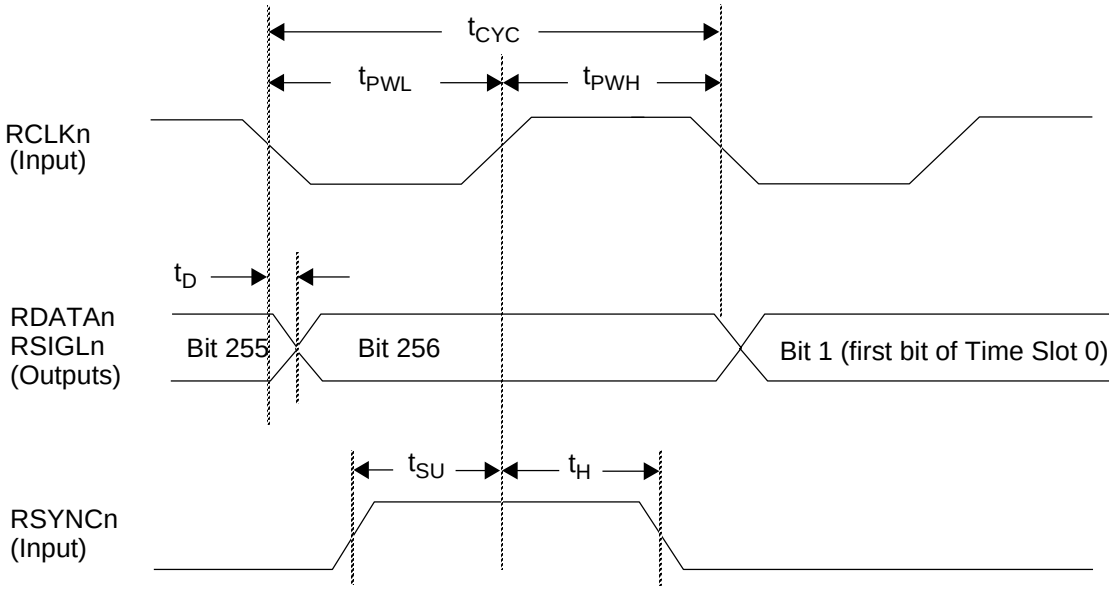


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	435	488.3		ns
RCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RDATAn/RSIGLn delay after RCLKn↓	$t_{D(1)}$	10	15	20	ns
RSYNCn delay after RCLKn↓	$t_{D(2)}$	10	15	20	ns
RSYNCn pulse width	t_{PW}	435	488.3		ns

Note: The 2 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 00. The recovered receive line clock (RCLKn) and an internal sync pulse are used to clock out data (RDATAn), signaling (RSIGLn), and the sync pulse (RSYNCn) to the system, when control bits RXC and RSE (bits 5 and 3 in register X02H) are 10 or 11. Control bit RXC selects the clock source, while RSE enables/disables the receive slip buffer.

Figure 13. Receive Highway Timing - 2 Mbit/s Transmission Mode (System Clock)

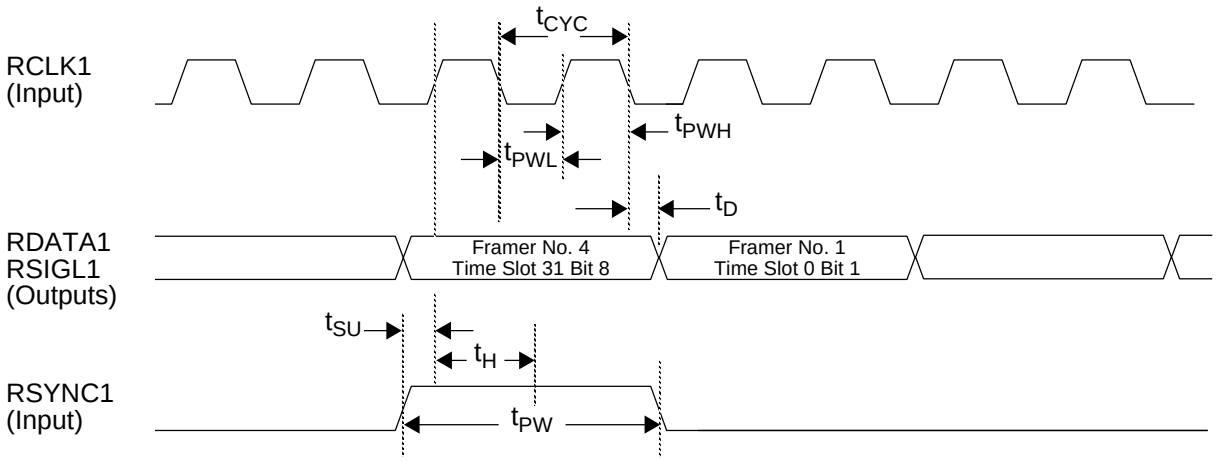


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	465	488.3		ns
RCLKn low time	t_{PWL}	233	0.5 x t_{CYC}		ns
RCLKn high time	t_{PWH}	233	0.5 x t_{CYC}		ns
RDATAn/RSIGLn delay after RCLKn↓	t_D	20	25	35	ns
RSYNCn setup time to RCLKn↑	t_{SU}	5.0			ns
RSYNCn hold time after RCLKn↑	t_H	5.0			ns

Note: The 2 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 00. The system clock (RCLKn) and sync pulse (RSYNCn) are used to clock data out of the slip buffer when control bits RXC and RSE (bits 5 and 3 in register X02H) are 01. Control bit RXC selects the clock source, while RSE enables/disables the receive slip buffer. The position of RSYNCn with respect to the RDATAn/RSIGLn signals can be offset.

Figure 14. Receive Highway Timing - 8 Mbit/s Transmission Mode



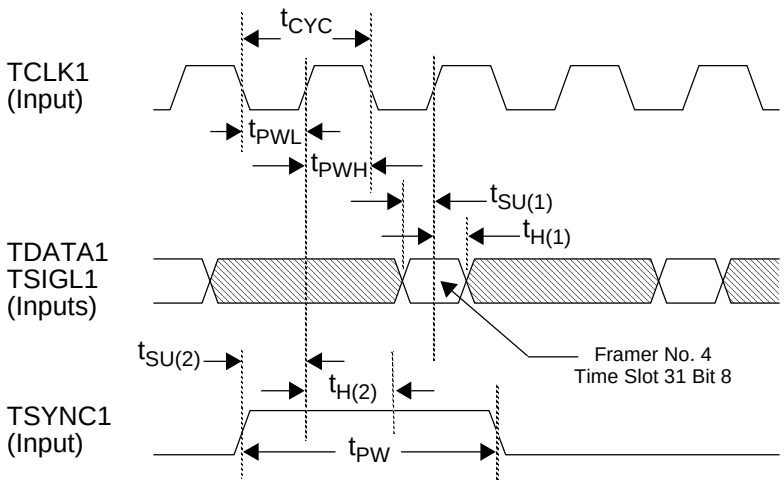
Note: See Note 1 below. All frame time slots are byte-interleaved on data and signaling highways.

Parameter	Symbol	Min	Typ	Max	Unit
RCLK1 clock period	t_{CYC}	58	61		ns
RCLK1 low time	t_{PWL}	28	0.5 x t_{CYC}		ns
RCLK1 high time	t_{PWH}	28	0.5 x t_{CYC}		ns
RDATA1/RSIGL1 delay after RCLK1↓	t_D	20	25	35	ns
RSYNC1 setup time to RCLK1↑	t_{SU}	5.0			ns
RSYNC1 hold time after RCLK1↑	t_H	5.0			ns
RSYNC1 pulse width high time (Note 2)	t_{PW}	2 x t_{CYC}	2 x t_{CYC}	< 3 x t_{CYC}	ns

Notes:

1. The 8 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 10. The receive slip buffer must be enabled for this mode. The position of RSYNC1 may be offset with respect to the RDATA1 and RSIGL1 signals. The value written to register 018H compensates for any offset. RSYNC1 is shown for an offset equal to zero.
2. RSYNC1 pulse width may be wider than two RCLK1 clock periods as long as only two rising edges of RCLK1 occur during the RSYNC1 pulse.

Figure 15. Transmit Highway Timing - 8 Mbit/s Transmission Mode



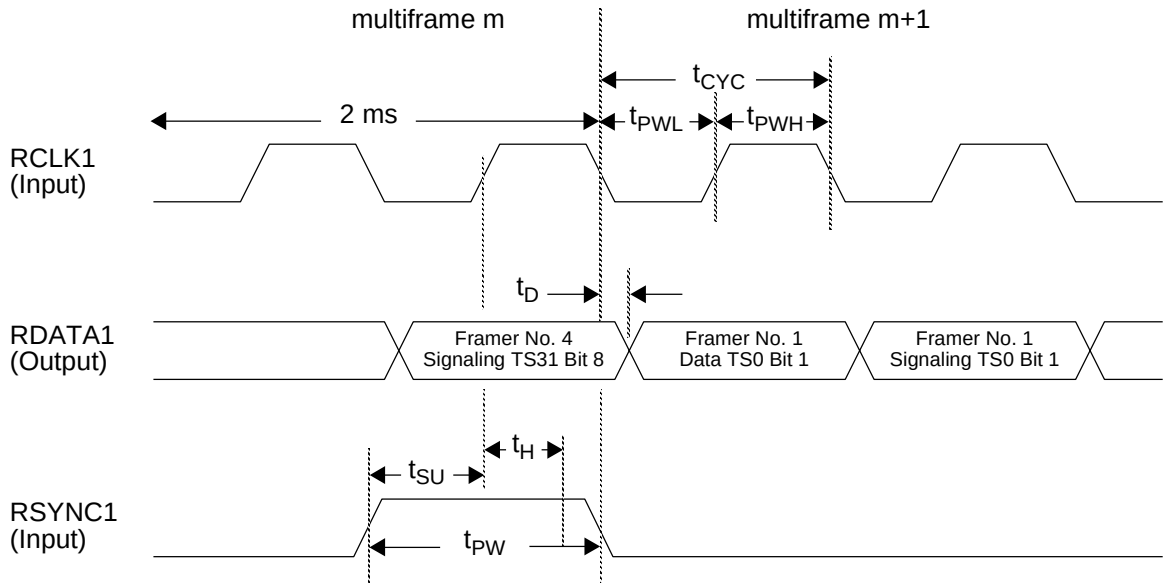
See Note 1 below.

Parameter	Symbol	Min	Typ	Max	Unit
TCLK1 clock period	t_{CYC}	58	61		ns
TCLK1 low time	t_{PWL}	28	0.5 x t_{CYC}		ns
TCLK1 high time	t_{PWH}	28	0.5 x t_{CYC}		ns
TDATA1/TSIGL1 setup time to TCLK1↑	$t_{SU(1)}$	5.0			ns
TDATA1/TSIGL1 hold time after TCLK1↑	$t_{H(1)}$	5.0			ns
TSYNC1 setup time to TCLK1↑	$t_{SU(2)}$	5.0			ns
TSYNC1 hold time after TCLK1↑	$t_{H(2)}$	5.0			ns
TSYNC1 pulse width (Note 2)	t_{PW}	2 x t_{CYC}	2 x t_{CYC}	< 3 x t_{CYC}	ns

Notes:

1. The 8 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 10. The position of TSYNC1 may be offset with respect to the TDATA1 signal. The value written to register 017H compensates for any offset. TSYNC1 is shown for an offset equal to zero.
2. TSYNC1 pulse width may be wider than two TCLK1 clock periods as long as only two rising edges of TCLK1 occur during the TSYNC1 pulse.

Figure 16. Receive Highway Timing - 16 Mbit/s Transmission Mode



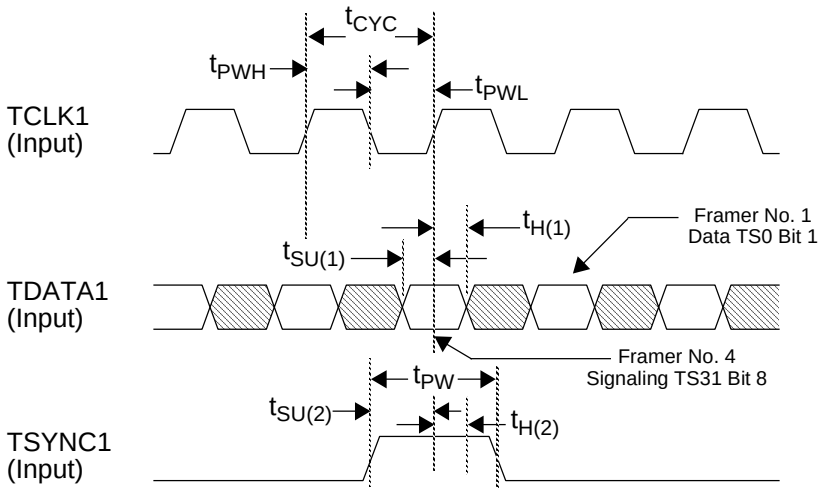
Note: See Note 1 below. All four framers' data and signaling time slots are bit-interleaved. A multiframe is 16 frames long (2 ms).

Parameter	Symbol	Min	Typ	Max	Unit
RCLK1 clock period	t_{CYC}	58	61		ns
RCLK1 low time	t_{PWL}	28	0.5 x t_{CYC}		ns
RCLK1 high time	t_{PWH}	28	0.5 x t_{CYC}		ns
RDATA1 delay after RCLK1↓	t_D	20	25	35	ns
RSYNC1 setup time to RCLK1↑	t_{SU}	5.0			ns
RSYNC1 hold time after RCLK1↑	t_H	5.0			ns
RSYNC1 pulse width high time (Note 2)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:

1. The 16 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 01. The receive slip buffer must be enabled for this mode. The position of RSYNC1 may be offset with respect to the RDATA1 signal. The value written to register 018H compensates for any offset. RSYNC1 is shown for an offset equal to zero.
2. RSYNC1 pulse width may be wider than one RCLK1 clock period as long as only a single rising edge of RCLK1 occurs during the RSYNC1 pulse.

Figure 17. Transmit Highway Timing - 16 Mbit/s Transmission Mode



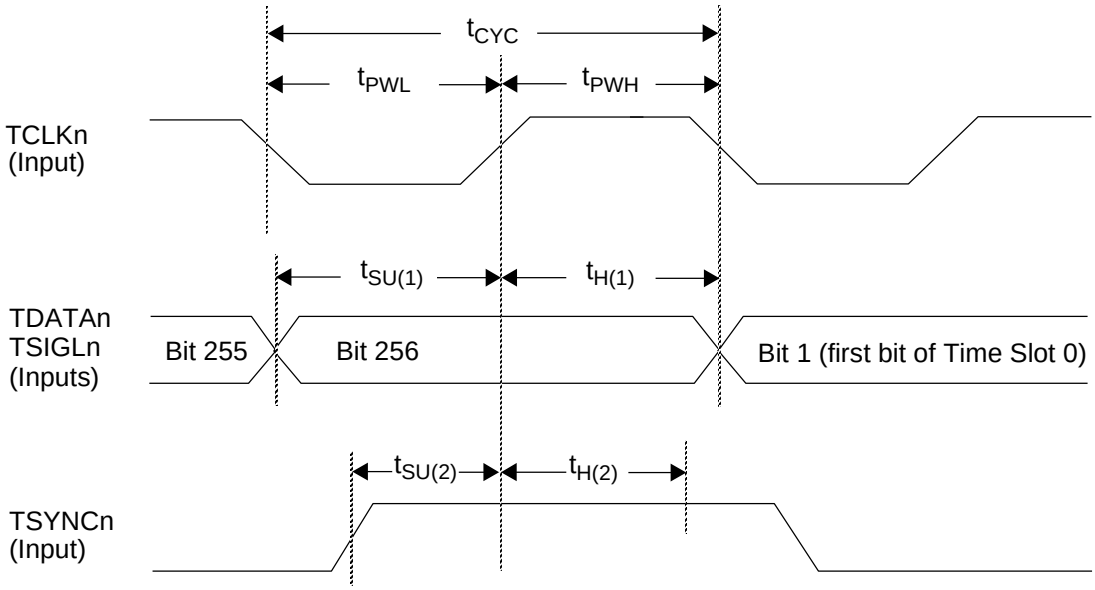
Note: See Note 1 below. All four framers' data and signaling time slots are bit-interleaved. A multiframe is 16 frames long (2 ms).

Parameter	Symbol	Min	Typ	Max	Unit
TCLK1 clock period	t_{CYC}	58	61	70	ns
TCLK1 low time	t_{PWL}	28	0.5 x t_{CYC}	35	ns
TCLK1 high time	t_{PWH}	28	0.5 x t_{CYC}	35	ns
TDATA1 setup time to TCLK1↑	$t_{SU(1)}$	5.0			ns
TDATA1 hold time after TCLK1↑	$t_{H(1)}$	5.0			ns
TSYNC1 setup time to TCLK1↑	$t_{SU(2)}$	5.0			ns
TSYNC1 hold time after TCLK1↑	$t_{H(2)}$	5.0			ns
TSYNC1 pulse width high time (Note 2)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:

1. The 16 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 01. The position of TSYNC1 may be offset with respect to the TDATA1 signal. The value written to register 017H compensates for any offset. TSYNC1 is shown for an offset equal to zero.
2. TSYNC1 pulse width may be wider than one TCLK1 clock period as long as only a single rising edge of TCLK1 occurs during the TSYNC1 pulse.

Figure 18. Transmit Highway Timing - 2 Mbit/s Transmission Mode

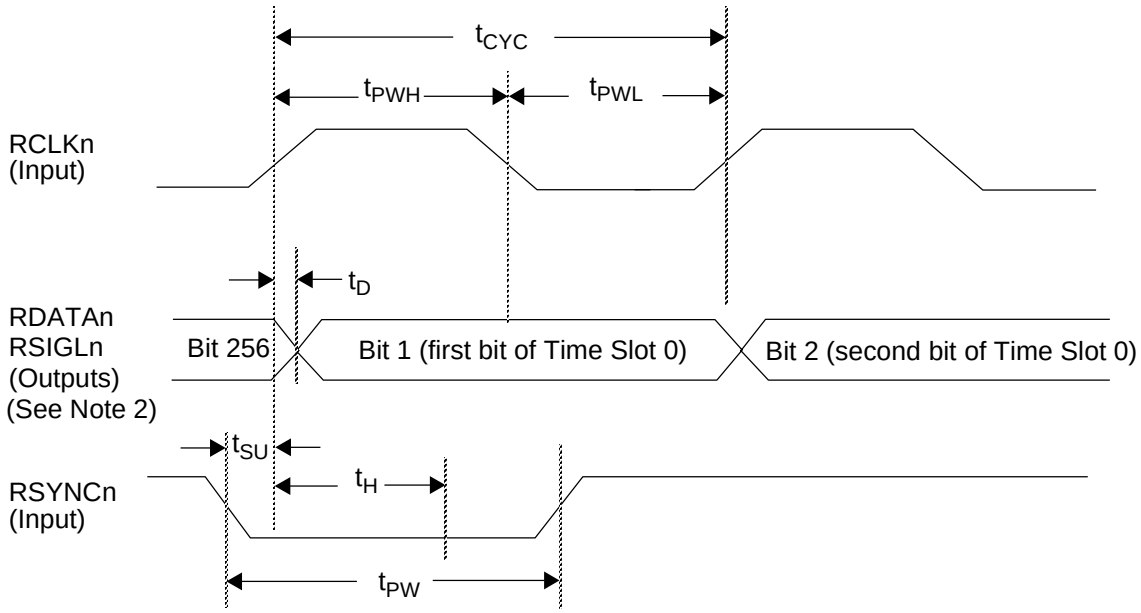


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	435	488.3		ns
TCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
TCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
TDATAn/TSIGLn setup time to TCLKn↑	$t_{SU(1)}$	5.0			ns
TDATAn/TSIGLn hold time after TCLKn↑	$t_{H(1)}$	5.0			ns
TSYNCn setup time to TCLKn↑	$t_{SU(2)}$	5.0			ns
TSYNCn hold time after TCLKn↑	$t_{H(2)}$	5.0			ns

Note: The 2 Mbit/s Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 00. The position of TSYNCn may be offset with respect to the TDATAn/TSIGLn signals. The value written to register 017H compensates for any offset. TSYNCn is shown for an offset equal to zero.

Figure 19. Receive Highway Timing - 2 Mbit/s MVIP Mode



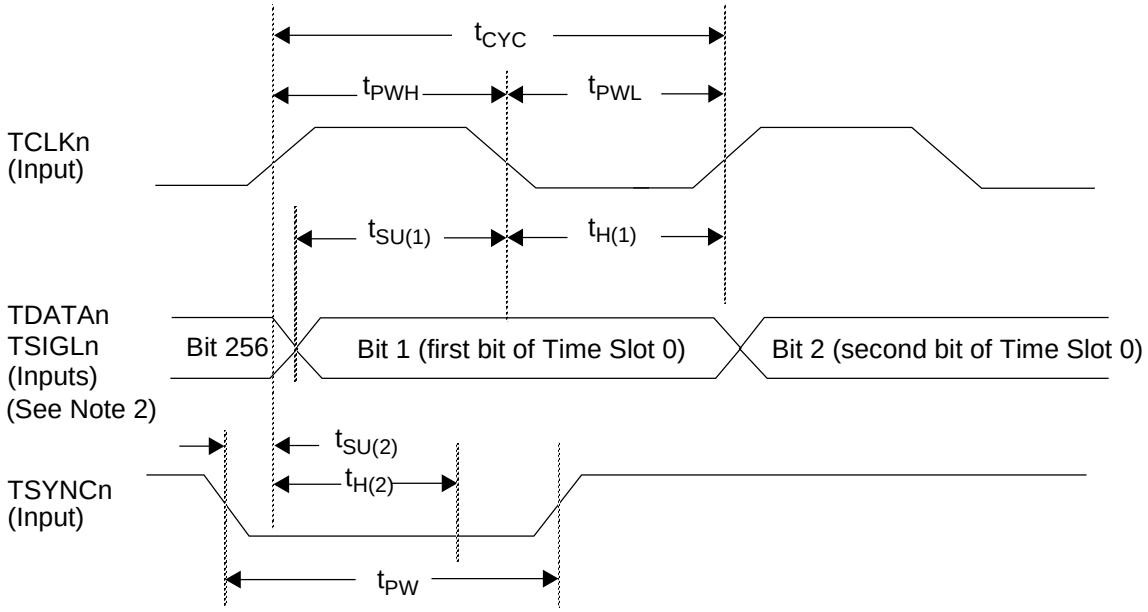
Note: See Note 1 below. n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	465	488.3		ns
RCLKn low time	t_{PWL}	233	0.5 x t_{CYC}		ns
RCLKn high time	t_{PWH}	233	0.5 x t_{CYC}		ns
RDATAn/RSIGLn delay after RCLKn↑	t_D	25	35	50	ns
RSYNCn setup time to RCLKn↑	t_{SU}	0.0			ns
RSYNCn hold time after RCLKn↑	t_H	10			ns
RSYNCn pulse width low time (Note 3)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:

1. The 2 Mbit/s MVIP Mode is selected when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 00. The receive slip buffer is always enabled in this mode. The position of RSYNCn may be offset with respect to the RDATAn/RSIGLn signals. The value written to register 018H compensates for any offset. RSYNCn is shown for an offset equal to zero.
2. For bit number per MVIP bit identification nomenclature, bit 256 is bit 0 of Time Slot 31, bit 1 is bit 7 of Time Slot 0 and bit 2 is bit 6 of Time Slot 0.
3. RSYNCn pulse width may be wider than one RCLKn clock period as long as only a single rising edge of RCLKn occurs during the RSYNCn pulse.

Figure 20. Transmit Highway Timing - 2 Mbit/s MVIP Mode



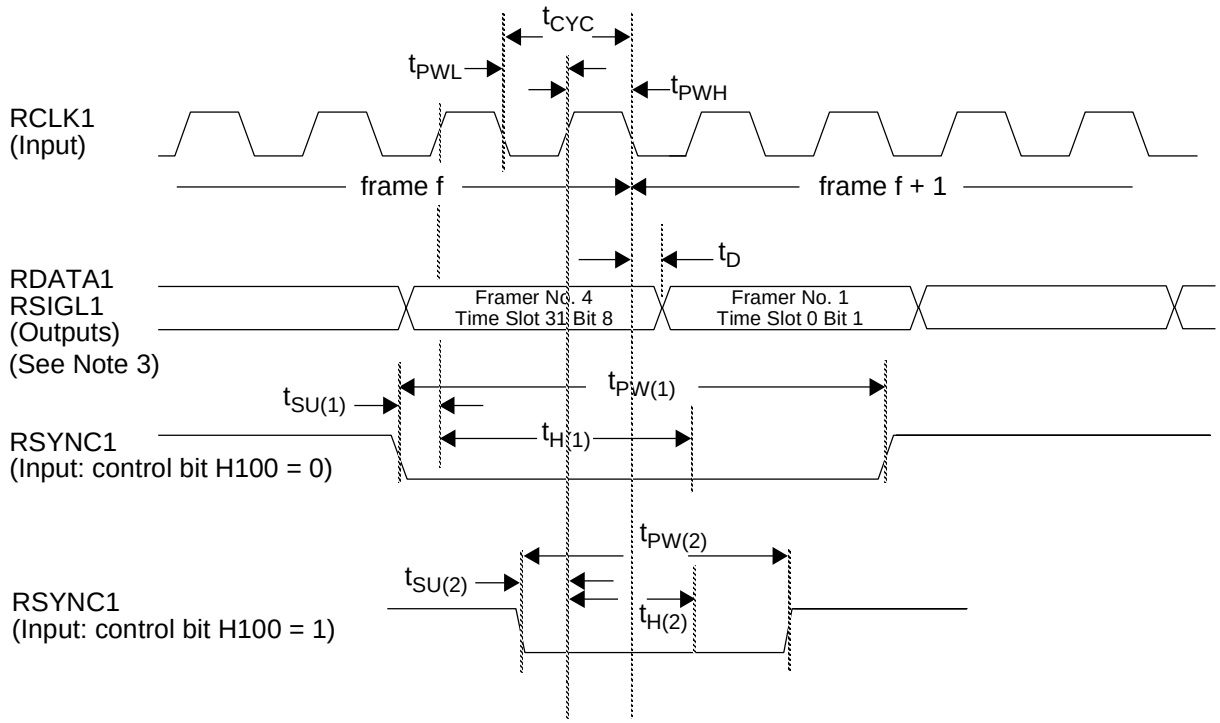
Note: See Note 1 below. n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	465	488.3		ns
TCLKn low time	t_{PWL}	233	0.5 x t_{CYC}		ns
TCLKn high time	t_{PWH}	233	0.5 x t_{CYC}		ns
TDATAn/TSIGLn setup time to TCLKn↓	$t_{SU(1)}$	0.0			ns
TDATAn/TSIGLn hold time after TCLKn↓	$t_{H(1)}$	5.0			ns
TSYNCn setup time to TCLKn↑	$t_{SU(2)}$	15			ns
TSYNCn hold time after TCLKn↑	$t_{H(2)}$	15			ns
TSYNCn pulse width low time (Note 3)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:

1. The 2 Mbit/s MVIP Mode is selected when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 00. The transmit slip buffer is always enabled in this mode. The position of TSYNCn may be offset with respect to the TDATAn/TSIGLn signals. The value written to register 017H compensates for any offset. TSYNCn is shown for an offset equal to zero.
2. For bit number per MVIP bit identification nomenclature, bit 256 is bit 0 of Time Slot 31, bit 1 is bit 7 of Time Slot 0 and bit 2 is bit 6 of Time Slot 0.
3. TSYNCn pulse width may be wider than one TCLKn clock period as long as only a single rising edge of TCLKn occurs during the TSYNCn pulse.

Figure 21. Receive Highway Timing - 8 Mbit/s H-MVIP/ H.100 Mode



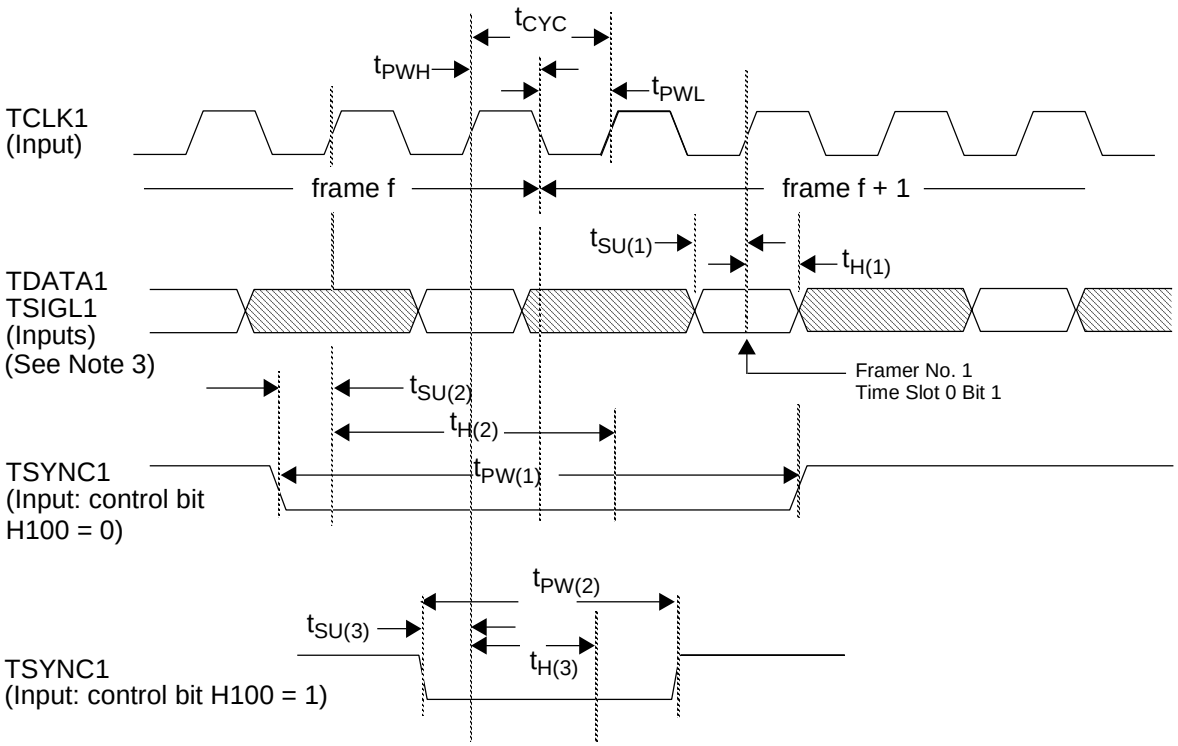
Note: See Note 1 below. All four framers' time slots are byte-interleaved.

Parameter	Symbol	Min	Typ	Max	Unit
RCLK1 clock period	t_{CYC}	60	61		ns
RCLK1 low time	t_{PWL}	30	0.5 x t_{CYC}		ns
RCLK1 high time	t_{PWH}	30	0.5 x t_{CYC}		ns
RDATA1/RSIGL1 delay after RCLK1↓	t_D	10	15	20	ns
RSYNC1 setup time to RCLK1↑; H-MVIP	$t_{SU(1)}$	9.0			ns
RSYNC1 hold time after RCLK1↑; H-MVIP	$t_{H(1)}$	5.0			ns
RSYNC1 setup time to RCLK1↑; H.100	$t_{SU(2)}$	9.0			ns
RSYNC1 hold time after RCLK1↑; H.100	$t_{H(2)}$	5.0			ns
RSYNC1 pulse width low time; H-MVIP (Note 2)	$t_{PW(1)}$	4 x t_{CYC}	4 x t_{CYC}	< 5 x t_{CYC}	ns
RSYNC1 pulse width low time; H.100 (Note 2)	$t_{PW(2)}$	2 x t_{CYC}	2 x t_{CYC}	< 3 x t_{CYC}	ns

Notes:

1. The 8 Mbit/s H-MVIP/H.100 Mode is selected when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 10. The receive slip buffer must be enabled for this mode. The position of RSYNC1 may be offset with respect to the RDATA1 and RSIGL1 signals. The value written to register 018H compensates for any offset. RSYNC1 is shown for an offset equal to zero. Control bit H100 (bit 2 of register 0FFH) controls the pulse width criteria of RSYNC1 required by the QE1F-*Plus*.
2. RSYNC1 pulse width may be wider than 4 or 2 clock periods as long as only either 4 or 2 rising edges of RCLK1 occur during the RSYNC1 pulse (for H-MVIP and H.100, respectively).
3. In MVIP nomenclature, Time Slot 31 bit 8 is known as Time Slot 31 bit 0 and Time Slot 0 bit 1 is Time Slot 0 bit 7.

Figure 22. Transmit Highway Timing - 8 Mbit/s H-MVIP/H.100 Mode



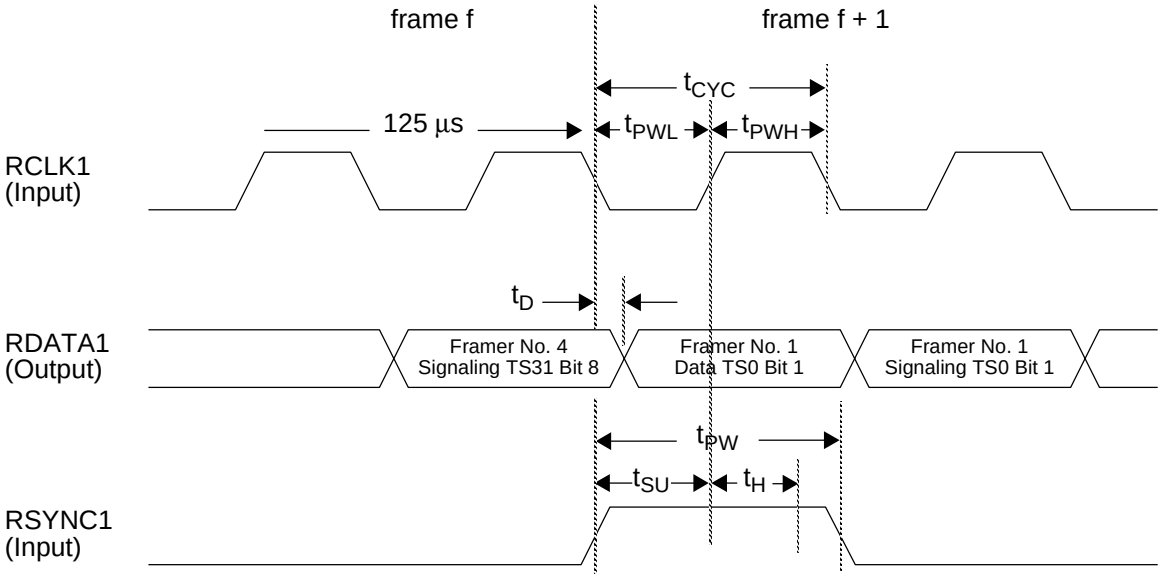
Note: See Note 1 below. All four framers' time slots are byte-interleaved.

Parameter	Symbol	Min	Typ	Max	Unit
TCLK1 clock period	t_{CYC}	60	61		ns
TCLK1 low time	t_{PWL}	30	0.5 x t_{CYC}		ns
TCLK1 high time	t_{PWH}	30	0.5 x t_{CYC}		ns
TDATA1/TSIGL1 setup time to TCLK1↑	$t_{SU(1)}$	7.0			ns
TDATA1/TSIGL1 hold time after TCLK1↑	$t_{H(1)}$	2.0			ns
TSYNC1 setup time to TCLK1↑; H-MVIP	$t_{SU(2)}$	10			ns
TSYNC1 hold time after TCLK1↑; H-MVIP	$t_{H(2)}$	5.0			ns
TSYNC1 setup time to TCLK1↑; H.100	$t_{SU(3)}$	10			ns
TSYNC1 hold time after TCLK1↑; H.100	$t_{H(3)}$	5.0			ns
TSYNC1 pulse width low time; H-MVIP (Note 2)	$t_{PW(1)}$	4 x t_{CYC}	4 x t_{CYC}	< 5 x t_{CYC}	ns
TSYNC1 pulse width low time; H.100 (Note 2)	$t_{PW(2)}$	2 x t_{CYC}	2 x t_{CYC}	< 3 x t_{CYC}	ns

Notes:

1. The 8 Mbit/s H-MVIP/H.100 Mode is selected when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 10. The position of TSYNC1 may be offset with respect to the TDATA1 signal. The value written to register 017H compensates for any offset. TSYNC1 is shown for an offset equal to zero.
2. TSYNC1 pulse width may be wider than 4 or 2 TCLK1 clock periods as long as only either 4 or 2 rising edges of TCLK1 occur during the TSYNC1 pulse (for H-MVIP or H.100, respectively).
3. In MVIP nomenclature, Time Slot 31 bit 8 is known as Time Slot 31 bit 0 and Time Slot 0 bit 1 is Time Slot 0 bit 7.

Figure 23. Receive Highway Timing - 16 Mbit/s PCM Highway Mode



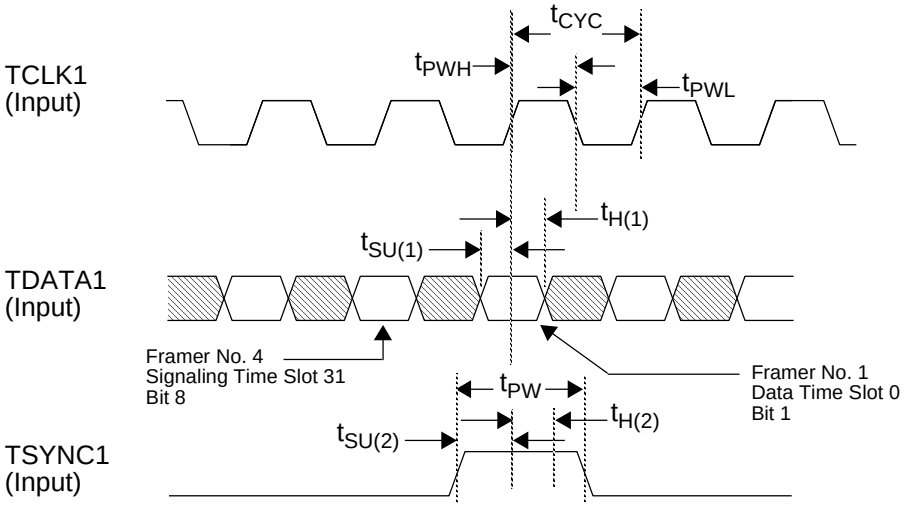
Note: See Note 1 below. All four framers' data and signaling time slots are bit-interleaved.

Parameter	Symbol	Min	Typ	Max	Unit
RCLK1 clock period	t_{CYC}	60	61		ns
RCLK1 low time	t_{PWL}	30	0.5 x t_{CYC}		ns
RCLK1 high time	t_{PWH}	30	0.5 x t_{CYC}		ns
RDATA1 delay after RCLK1↓	t_D	15	25	30	ns
RSYNC1 setup time to RCLK1↑	t_{SU}	6.0			ns
RSYNC1 hold time after RCLK1↑	t_H	0.0			ns
RSYNC1 pulse width high time (Note 2)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:

1. The 16 Mbit/s PCM Highway Mode is selected when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 01. The receive slip buffer must be enabled for this mode. The position of RSYNC1 may be offset with respect to the RDATA1 signal. The value written to register 018H compensates for any offset. RSYNC1 is shown for an offset equal to zero.
2. RSYNC1 pulse width may be wider than one RCLK1 clock period as long as only a single rising edge of RCLK1 occurs during the RSYNC1 pulse.

Figure 24. Transmit Highway Timing - 16 Mbit/s PCM Highway Mode



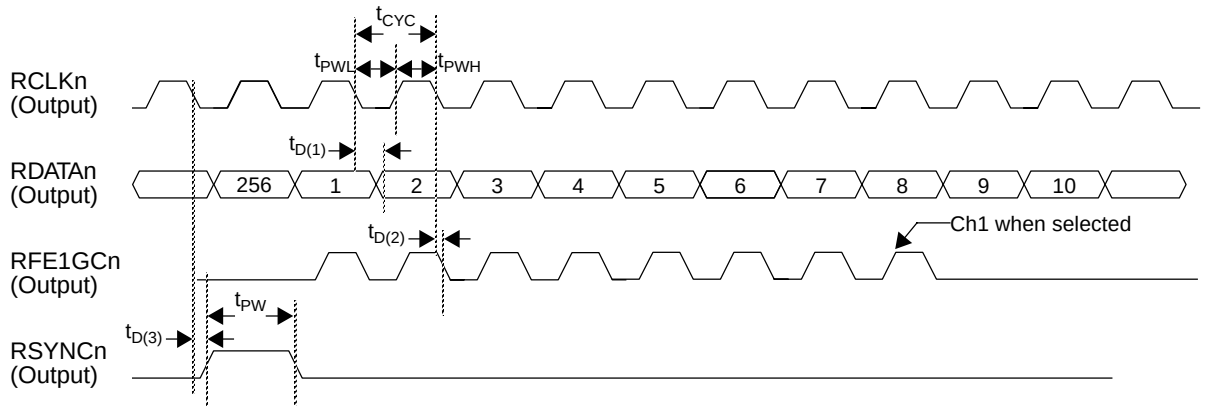
Note: See Note 1 below. All four framers' data and signaling time slots are bit-interleaved.

Parameter	Symbol	Min	Typ	Max	Unit
TCLK1 clock period	t_{CYC}	60	61		ns
TCLK1 low time	t_{PWL}	30	0.5 x t_{CYC}		ns
TCLK1 high time	t_{PWH}	30	0.5 x t_{CYC}		ns
TDATA1 setup time to TCLK1↑	$t_{SU(1)}$	5.0			ns
TDATA1 hold time after TCLK1↑	$t_{H(1)}$	0.0			ns
TSYNC1 setup time to TCLK1↑	$t_{SU(2)}$	2.0			ns
TSYNC1 hold time after TCLK1↑	$t_{H(2)}$	0.0			ns
TSYNC1 pulse width high time (Note 2)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:

1. The 16 Mbit/s PCM Highway Mode is selected when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP and MTP16M (bits 2 and 1 in register 006H) are 01. The transmit slip buffer must be enabled for this mode. The position of TSYNC1 may be offset with respect to the TDATA1 signal. The value written to register 017H compensates for any offset. TSYNC1 is shown for an offset equal to zero.
2. TSYNC1 pulse width may be wider than one TCLK1 clock period as long as only a single rising edge of TCLK1 occurs during the TSYNC1 pulse.

Figure 25. Receive Highway Timing - Fractional E1 Gapped Clock (Transmission Mode; Receive Line Clock)

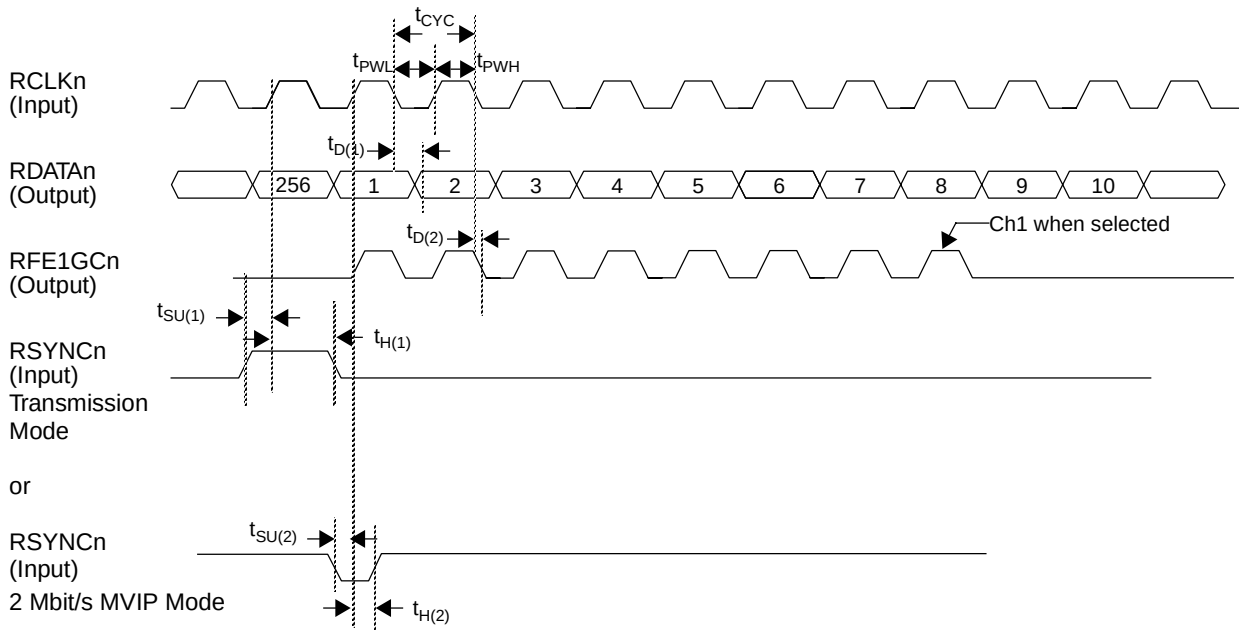


Note: n = 1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	435	488.3		ns
RCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RDATAn delay after RCLKn↓	$t_{D(1)}$	10	15	23	ns
RFE1GCn↓ delay after RCLKn↓	$t_{D(2)}$	10	15	20	ns
RSYNCn delay after RCLKn↓	$t_{D(3)}$	10	15	20	ns
RSYNCn pulse width	t_{PW}	435	488.3		ns

Note: The fractional E1 gapped clock feature is enabled when the CONFIG1 pin is low, control bit FE1M (bit 0 in register X02H) is written with a 1 and control bits HMVIP and MTP16M are both set to 0 (bits 2 and 1 of register 006H). One or more time slots may be selected by writing a 1 to one or more control bits RFTS0-RFTS31 (in registers X38H-X3BH).

Figure 26. Receive Highway Timing - Fractional E1 Gapped Clock (Transmission and 2 Mbit/s MVIPModes; System Clock)



Note: n = 1, 2, 3, 4

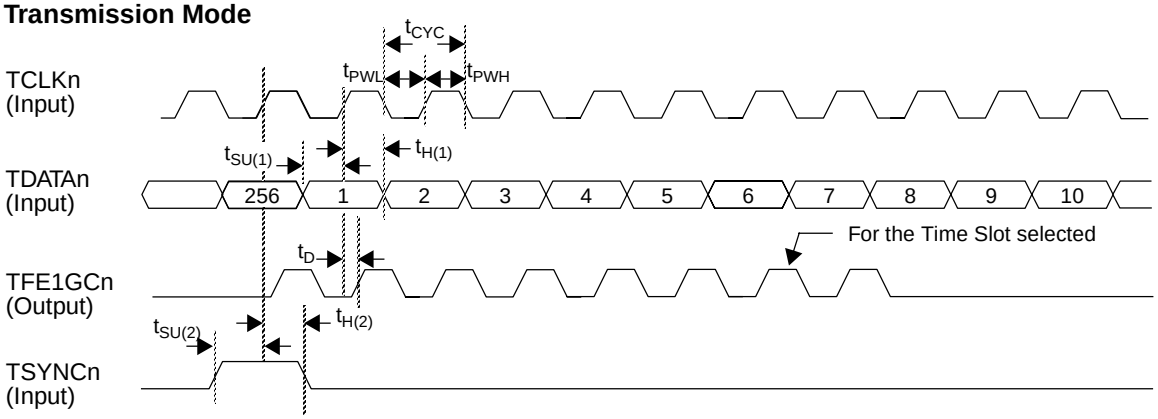
Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	465	488.3		ns
RCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RDATAn delay after RCLKn↓	$t_{D(1)}$	20	25	30	ns
RFE1GCn↓ delay after RCLKn↓	$t_{D(2)}$	20	25	30	ns
RSYNCn↑ setup time to RCLKn↑ (Transmission)	$t_{SU(1)}$	5.0			ns
RSYNCn↑ hold time after RCLKn↑ (Transmission)	$t_{H(1)}$	5.0			ns
RSYNCn↓ setup time to RCLKn↑ (MVIP)	$t_{SU(2)}$	0.0			ns
RSYNCn↓ hold time after RCLKn↑ (MVIP)	$t_{H(2)}$	10			ns

Note: The fractional E1 gapped clock feature is enabled when the CONFIG1 pin is low (Transmission Modes), or high (MVIP Modes), control bit FE1M (bit 0 in register X02H) is written with a 1, and control bits HMVIP and MTP16M are both set to 0 (bits 2 and 1 of register 006H). One or more time slots may be selected by writing a 1 to one or more control bits RFTS0-RFTS31 (in registers X38H-X3BH).

Figure 27. Transmit Highway Timing - Fractional E1 Gapped Clock (Transmission and 2 Mbit/s MVIP Modes)

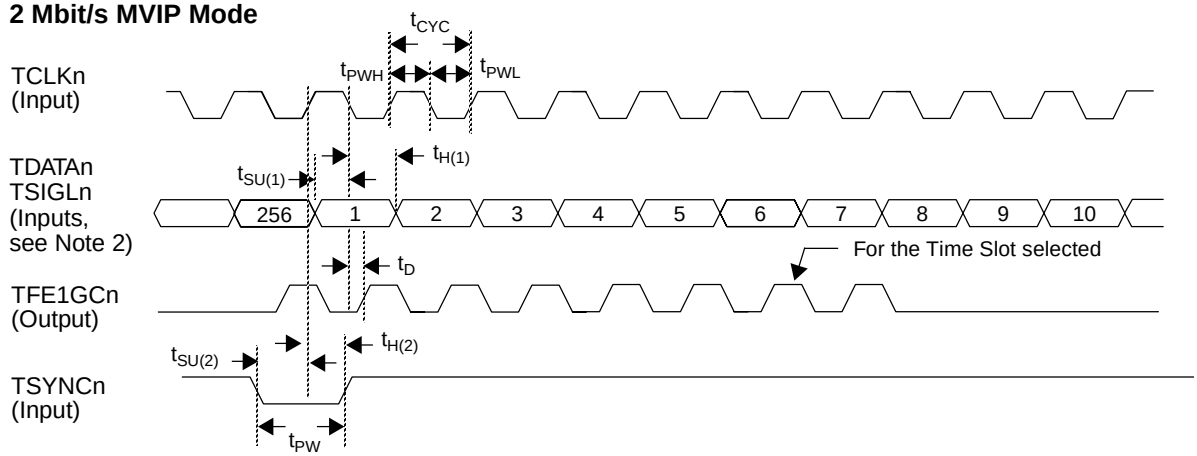
Note: The fractional E1 gapped clock feature is enabled when the CONFIG1 pin is low (Transmission Modes), or high (MVIP Modes), control bit FE1M (bit 0 in register X02H) is written with a 1, and control bits HMVIP and MTP16M (bits 2 and 1 in control register 006H) are both written with a 0. One or more time slots may be selected by writing a 1 to one or more control bits TFTS0-TFTS31 (in registers X3CH-X3FH). n = 1,2,3,4.

Transmission Mode



Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	435	488.3		ns
TCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
TCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
TDATAn setup time to TCLKn↑	$t_{SU(1)}$	5.0			ns
TDATAn hold time after TCLKn↑	$t_{H(1)}$	5.0			ns
TSYNCn setup time to TCLKn↑	$t_{SU(2)}$	5.0			ns
TSYNCn hold time after TCLKn↑	$t_{H(2)}$	5.0			ns
TFE1GCn output delay from TCLKn↑	t_D	5.0	10	27	ns

2 Mbit/s MVIP Mode



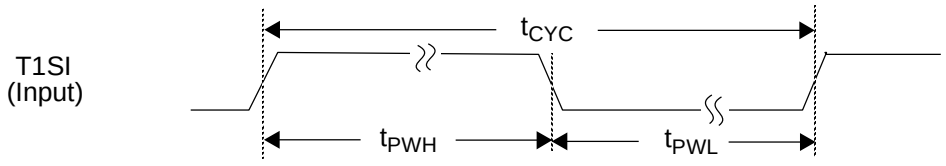
(Cont. on next page)

Figure 27. (cont.)

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	465	488.3		ns
TCLKn low time	t_{PWL}	233	0.5 x t_{CYC}		ns
TCLKn high time	t_{PWH}	233	0.5 x t_{CYC}		ns
TDATAn/TSIGLn setup time to TCLKn↓	$t_{SU(1)}$	0.0			ns
TDATAn/TSIGLn hold time after TCLKn↓	$t_{H(1)}$	5.0			ns
TFE1GCn output delay from TCLKn↓	t_D	5.0	10	27	ns
TSYNCn setup time to TCLKn↑	$t_{SU(2)}$	15			ns
TSYNCn hold time after TCLKn↑	$t_{H(2)}$	15			ns
TSYNCn pulse width low time (Note 3)	t_{PW}	1 x t_{CYC}	1 x t_{CYC}	< 2 x t_{CYC}	ns

Notes:
1. See Figure 20 for additional detail.
2. For bit number per MVIP bit identification nomenclature, bit 256 is bit 0 of Time Slot 31, bit 1 is bit 7 of Time Slot 0 and bit 2 is bit 6 of Time Slot 0.
3. TSYNCn pulse width may be wider than one TCLKn clock period as long as only a single rising edge of TCLKn occurs during the TSYNCn pulse.

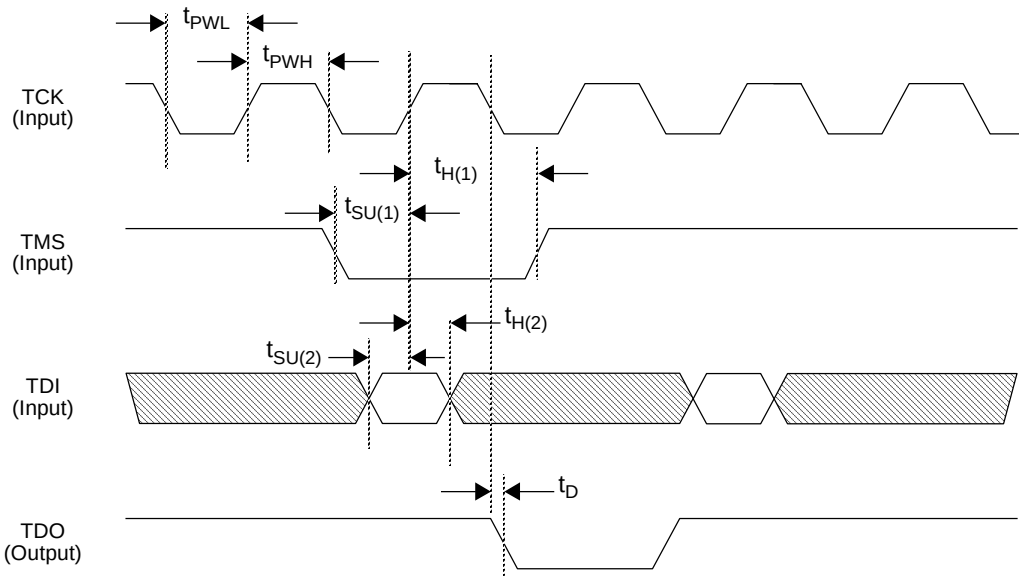
Figure 28. Shadow Register Timing



Parameter	Symbol	Min	Typ	Max	Unit
T1SI cycle time	t_{CYC}			1000	ms
T1SI pulse width high (Note 1)	t_{PWH}	20	50		ms
T1SI pulse width low	t_{PWL}		950	980	ms

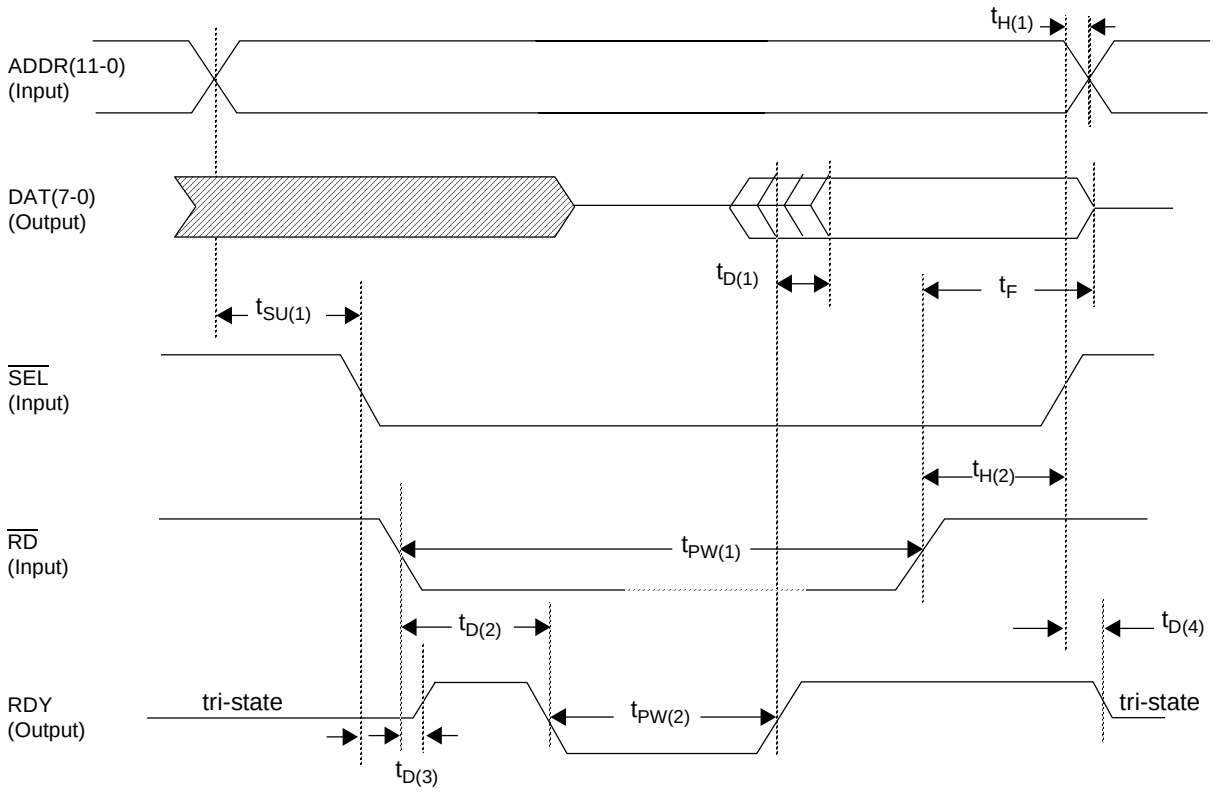
Notes:
1. A duty cycle (t_{PWH}/t_{CYC}) of 50% for the T1SI signal is permitted.
2. The shadow register feature and this input are enabled when a 1 is written to control bit ENPMFM (bit 3 in register 006H).

Figure 29. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	5.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	5.0		ns
TDI setup time to TCK↑	$t_{SU(2)}$	5.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	10		ns
TDO delay from TCK↓	t_D	6.5	13	ns

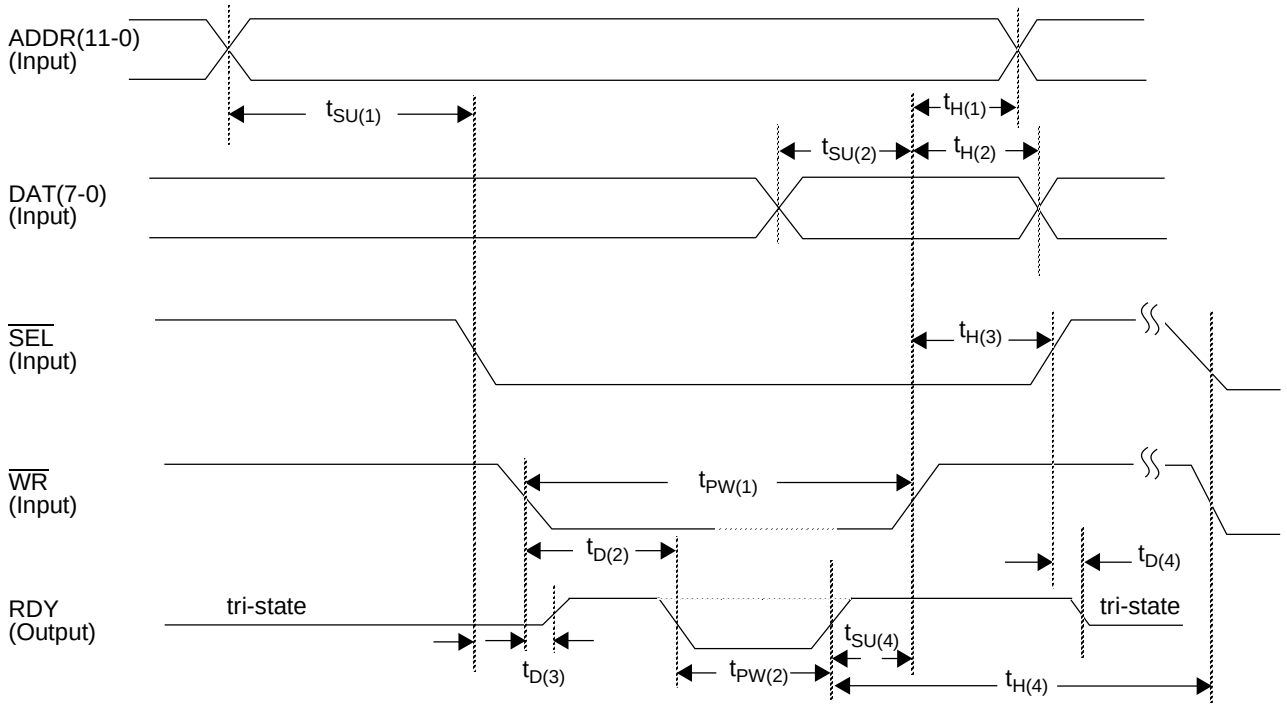
Figure 30. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
ADDR hold after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
DAT valid delay after RDY$\uparrow$	$t_{D(1)}$		-1/2 cycle of SYSCLK	-10	ns
DAT float time after $\overline{RD}\uparrow$	t_F	5.0	10	15	ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	10			ns
$\overline{RD}$ pulse width low time (Note 3)	$t_{PW(1)}$	25			ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(2)}$	5.0	20	25	ns
RDY pulse width low time	$t_{PW(2)}$	2 cycles of SYSCLK	10 cycles of SYSCLK	15 cycles of SYSCLK	ns
RDY tri-state to high delay after the latter of $\overline{SEL}\downarrow$ or $\overline{RD}\downarrow$	$t_{D(3)}$	5.0		25	ns
RDY high to tri-state delay after $\overline{SEL}\uparrow$	$t_{D(4)}$	17			ns

Notes:
1. The Intel microprocessor bus is selected by placing a low on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 19-22 MHz.
3. Both $\overline{SEL}$ and $\overline{RD}$ must be simultaneously low for the specified $t_{PW(1)}$ interval.

Figure 31. Intel Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	5.0			ns
ADDR hold time after $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{H(1)}$	10			ns
DAT valid setup time to $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{SU(2)}$	10			ns
DAT hold time after $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{H(2)}$	10			ns
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$ (Note 5)	$t_{H(3)}$	0.0			ns
$\overline{WR}$ pulse width low time/$\overline{SEL}$ pulse width low time (Note 5)	$t_{PW(1)}$	50			ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$	15	20	25	ns
RDY pulse width low time	$t_{PW(2)}$	0.0	7 cycles of SYSCLK*	10 cycles of SYSCLK*	ns
RDY tri-state to high delay after the latter of $\overline{SEL}\downarrow$ or $\overline{WR}\downarrow$	$t_{D(3)}$	5.0		25	ns
RDY high to tri-state delay after $\overline{SEL}\uparrow$	$t_{D(4)}$	17	20	25	ns
RDY high setup time to $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{SU(4)}$	0.0			ns
RDY$\uparrow$ to $\overline{WR}\downarrow$, or $\overline{SEL}\downarrow$ (Note 6)	$t_{H(4)}$	2 cycles of SYSCLK			ns

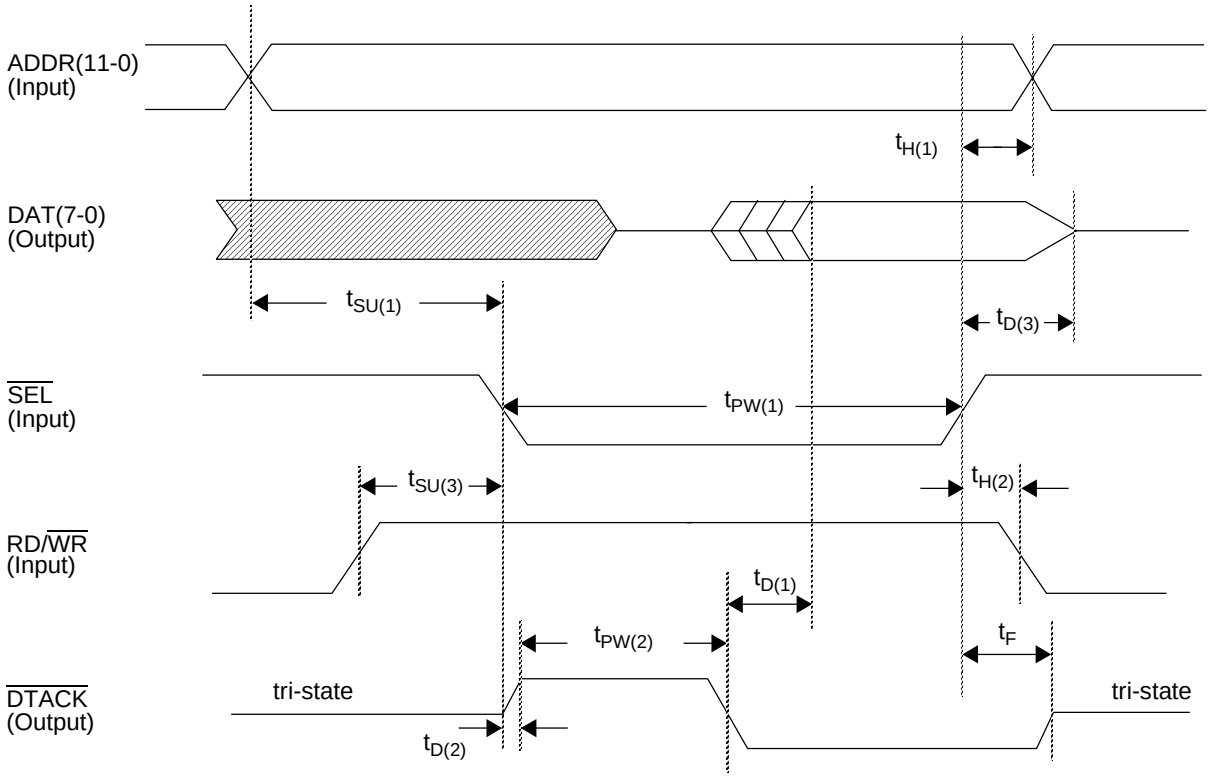
(Cont. on next page)

Figure 31. (cont.)

Notes:

1. The Intel microprocessor bus is selected by placing a low on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 19-22 MHz.
3. * Wait states only occur if a write cycle immediately follows a previous read/write cycle (e.g., read, modify, write or word-wide write).
4. The timing is with respect to the earlier of the two rising edges.
5. As long as both $\overline{SEL}$ and $\overline{WR}$ are simultaneously low for the specified $t_{PW(1)}$ interval, $\overline{SEL}$ may rise prior to $\overline{WR}\uparrow$ ($t_{H(3)}$ is a negative Min).
6. When writing to address X0AH (HDLC transmit FIFO) only, allow a minimum of 2 cycles of SYSCLK between RDY$\uparrow$ and $\overline{SEL}\downarrow$ or $\overline{WR}\downarrow$.

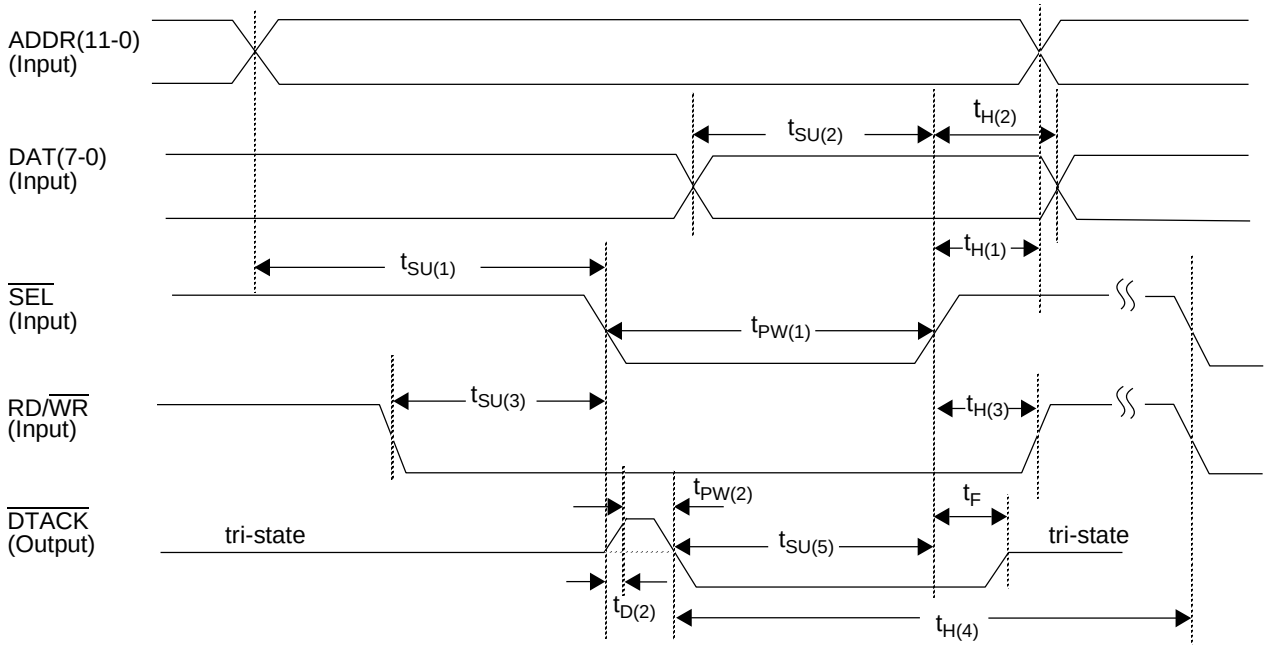
Figure 32. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
DAT delay to tri-state after $\overline{SEL}\uparrow$	$t_{D(3)}$	10			ns
DAT valid output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$	-1 cycle of SYSCLK	-1/2 cycle of SYSCLK	-10	ns
$\overline{SEL}$ pulse width low time	$t_{PW(1)}$	50			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	10			ns
$\overline{DTACK}$ pulse width high time	$t_{PW(2)}$	2 cycles of SYSCLK	10 cycles of SYSCLK	15 cycles of SYSCLK	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	7.0	8.0	12	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	9.0	10	12	ns
ADDR hold after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
RD/$\overline{WR}$ hold after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns

Notes:
1. The Motorola microprocessor bus is selected by placing a high on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 19-22 MHz.

Figure 33. Motorola Microprocessor Write Cycle Timing

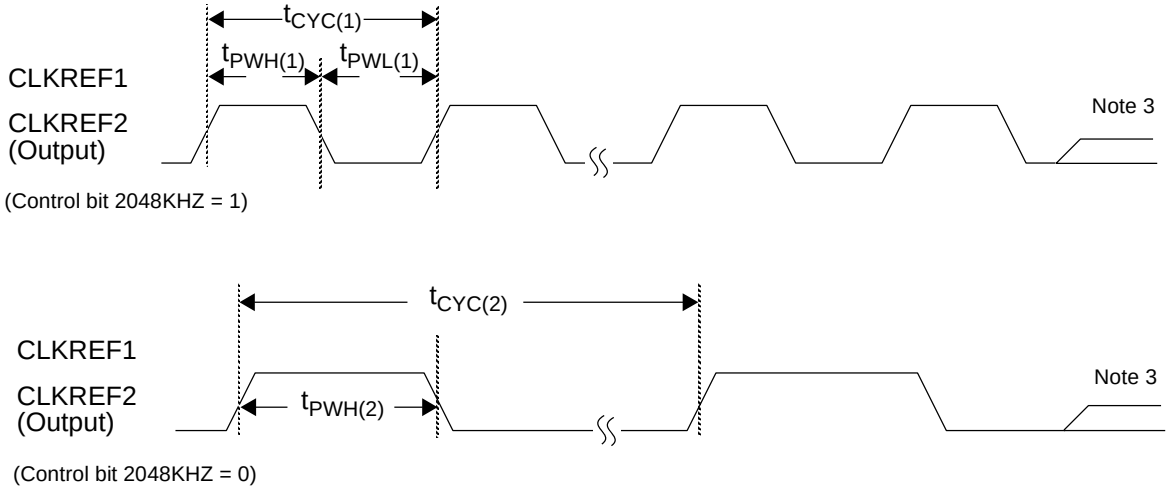


Parameter	Symbol	Min	Typ	Max	Unit
ADDR valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
ADDR hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	10			ns
DAT valid setup time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	15			ns
$\overline{SEL}$ pulse width low time (Note 4)	$t_{PW(1)}$	50			ns
DAT hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	10			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	10			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	10			ns
$\overline{DTACK}$ pulse width high time	$t_{PW(2)}$	0.0	10 cycles of SYSCLK*	15 cycles of SYSCLK*	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	7.0	7.0	10	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	10	12	15	ns
$\overline{DTACK}$ low setup time to $\overline{SEL}\uparrow$	$t_{SU(5)}$	0.0			ns
$\overline{DTACK}\downarrow$ to $\overline{SEL}\downarrow$ or RD/ $\overline{WR}\downarrow$ (Note 5)	$t_{H(4)}$	2 cycles of SYSCLK			ns

Notes:

1. The Motorola microprocessor bus is selected by placing a high on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 19-22 MHz.
3. * Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g., read, modify, write or word-wide write).
4. $\overline{SEL}$ and RD/$\overline{WR}$ must both be low simultaneously for the specified $t_{PW(1)}$ period.
5. When writing to address X0AH (HDLC transmit FIFO) only, allow a minimum of 2 cycles of SYSCLK between $\overline{DTACK}\downarrow$ and $\overline{SEL}\downarrow$ or RD/$\overline{WR}\downarrow$.

Figure 34. Clock Reference Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKREF1,2 clock period when control bit 2048KHZ = 1; (Note 2)	$t_{CYC(1)}$		488.3		ns
CLKREF1,2 high time when control bit 2048KHZ = 1; (Note 2)	$t_{PWH(1)}$		$0.5 \times t_{CYC(1)}$		ns
CLKREF1,2 low time when control bit 2048KHZ = 1; (Note 2)	$t_{PWL(1)}$		$0.5 \times t_{CYC(1)}$		ns
CLKREF1,2 clock period when control bit 2048KHZ = 0; (Note 2)	$t_{CYC(2)}$		125		µs
CLKREF1,2 high time when control bit 2048KHZ = 0; (Note 2)	$t_{PWH(2)}$		$1 \times t_{CYC(1)}$		ns

Notes:

1. CLKREF1 and CLKREF2 output pins are controlled by register 019H. Control bit 2048KHZ selects either a direct clock output when set to 1 or via a divide by 256 circuit when set to 0. Control bits ENREF1 and ENREF2 enable output pins CLKREF1 and CLKREF2 when set to 1; when ENREF1 and ENREF2 are set to 0 CLKREF1 and CLKREF2 are tri-stated. The particular receive clock LRCLKn used as a reference is selected by control bits CR1S1,2 for CLKREF1 and control bits CR2S1,2 for CLKREF2.
2. The actual clock period and high or low times are a function of the selected clock LRCLKn.
3. A fault detected (LOS or LINT pin active if enabled by control bit LIE) by the particular channel selected for the reference clock will cause CLKREF1,2 to stay low. The output only goes to tri-state if control bit ENREF1 or ENREF2 is set to 0.

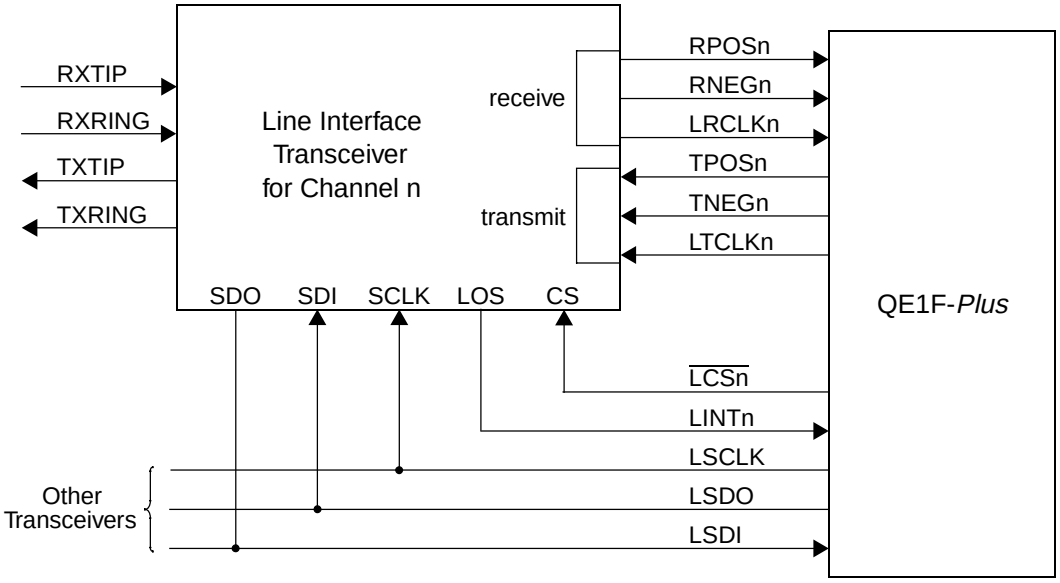
OPERATION

The following sections detail the internal operation of the QE1F-*Plus*.

LINE INTERFACE SELECTION

Each of the four framers in the QE1F-*Plus* can be programmed to provide either a dual unipolar interface or a NRZ interface. The dual unipolar interface is selected when a 1 is written into control bit RAIL (bit 7) in the Framer Configuration register located at address X00H in the memory map. The X stands for the framer selected, and will be equal to the value n used to identify the framer (1 for framer 1, 2 for framer 2, etc.). The HDB3 line coder/decoder (CODEC) feature is usually selected for the dual unipolar interface. The HDB3 CODEC is selected by writing a 1 to control bit BE (bit 6) in the Framer Configuration register X00H. A 0 will select an AMI CODEC. The HDB3 stands for High Density Bipolar of Order 3, which is described in ITU-T Recommendation G.703.

The clock polarity of the input and output line clocks is selectable by writing the sense required to control bits TXCP and RXCP (bits 7 and 6) in the Framer Configuration register X01H. When a framer is configured for the dual unipolar mode, the line signal is monitored for loss of signal. The LOS detection and recovery periods for all four framers are programmable by writing the two consecutive pulse count values to the Global Configuration registers 01AH and 01BH. Typical values are 255 for detection and 32 for recovery. The connections between a QE1F-*Plus* framer and external line interface transceivers are shown in Figure 35 below for dual unipolar mode.

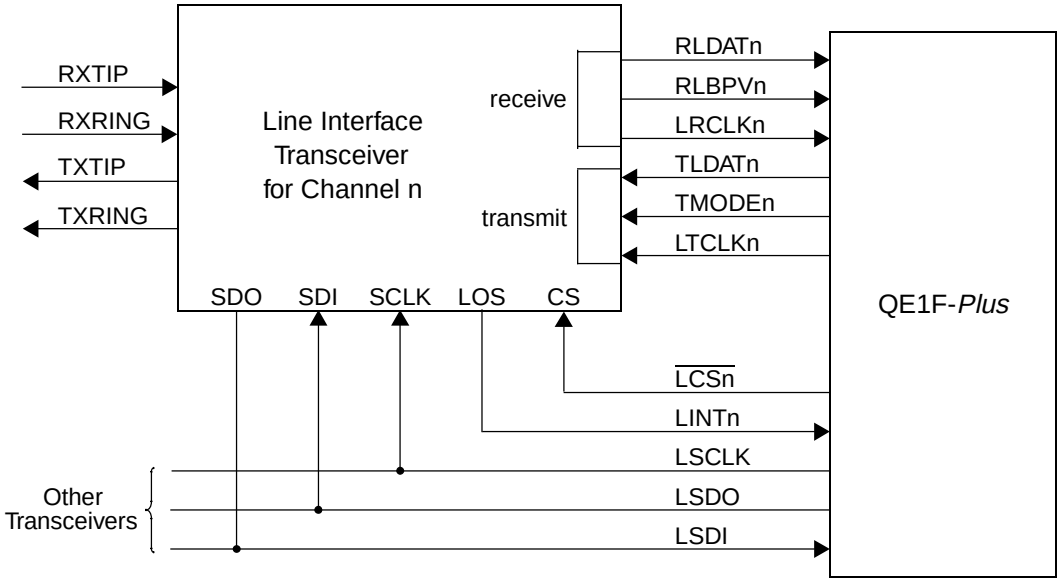


Note: n is the channel number (1, 2, 3, 4)

Figure 35. Line Interface for Dual Unipolar Mode

The NRZ interface is selected when a 0 is written into control bit RAIL (bit 7) in register X00H. The clock polarity of the line input and output clocks is selectable by writing to control bits TXCP and RXCP (bits 7 and 6) in the Framer Configuration register X01H. Options are provided for inverting the polarity of the transmit and receive data pins. A 1 written to control bit TXNRZP (bit 5) in register X01H inverts the polarity of the transmit data signal, TLDATn, while a 1 written to control bit RXNRZP (bit 0) in the same register inverts the polarity of the receive data signal RLDATn. In NRZ mode, the RNEGn pin may be used to input an external indication of coding violations (RLBPVn) or a fast sync pulse for testing purposes (RFSn). External coding violations are counted in a 16-bit performance counter when control bit RXFS (bit 1) in register X06H is a 0. Coding violations are counted when the input is high for rising edges of the line clock LRCLKn. When control bit RXFS is a 1, this pin is used for inputting a receive fast sync pulse.

In the transmit direction, when the NRZ mode is selected, the TNEGn pin becomes a TFSn or TMODEn pin. The pin may be used to output a fast sync pulse (TFSn), or it may be used as a general purpose output pin (TMODEn). When control bit TXFS (bit 0) in register X06H is a 1, a fast sync output pulse is provided on this pin. When control bit TXFS is a 0, this pin can be used as a general purpose output pin. The output state is defined by the value written to bit BE (bit 6) in register X00H. A typical interface between a framer in the QE1F-*Plus* and an external line transceiver is shown in Figure 36 below for NRZ mode.



Note: n is the channel number (1, 2, 3, 4)

Figure 36. Line Interface for NRZ Mode

LINE INTERFACE CONTROL

This interface permits the microprocessor to have complete control of the four external line interface transceivers through the QE1F-*Plus*. This interface is selected by placing a low on the CONFIG2 pin (pin 42). The line interface control leads are common to all four framers and comprise a data input pin (LSDI), a data output pin (LSDO), and a clock output pin (LSCLK). The clock signal LSCLK is derived from the signal at the LO pin (pin 41); it is the same frequency as the signal applied to the LO pin. Individual chip select pins ($\overline{\text{LCSn}}$) are used between the QE1F-*Plus* and the external transceivers to determine which of the four external transceivers is to be accessed through the QE1F-*Plus*. In addition, general purpose input leads (LINTn) are provided. The signal on this lead is locally or-gated with the internal loss of signal alarm when control bit LIE (bit 1) in the Framer Configuration register X00H is a 1. The operating sense of this lead is programmable by control bit LPOL (bit 0) in the Framer Configuration register X00H. The status indication of this pin is given by the LINT status bit (bit 0) in register X15H. A typical interface between the QE1F-*Plus* and external line interface transceivers using the line interface control pins is shown in Figures 35 and 36, for the dual unipolar and NRZ interface modes respectively.

Data to be written to the external transceiver is formatted as a two-byte message. The first byte is an address/command byte and the second byte contains the data to be written. Figure 37 illustrates the message and control formats associated with the transceiver serial I/O timing.

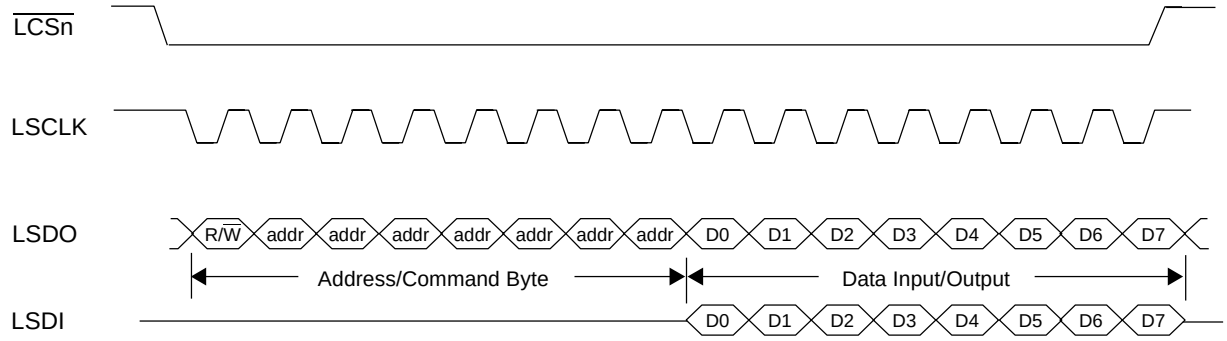


Figure 37. Transceiver Serial I/O Timing

The format of the address/command byte depends upon the external transceiver being controlled. Please refer to the transceiver's data sheet for the command/data formats. The interface for controlling the external transceiver operates in the following way. The external transceiver selection (via $\overline{\text{LCSn}}$) is determined by the value written to two E1CHCS bits (bits 1 and 0) in register 013H. For example, a 00 value selects the transceiver for framer 1 while a 11 value selects the transceiver for framer 4. The microprocessor writes the command byte to LCB7-LCB0 in the Line Interface Control register 010H. This is followed by writing the data byte to LDO7-LDO0 in Line Interface Control register 011H. The serial message is sent on LSDO when a 1 is written to replace the 0 in the ESP/EMON bit (bit 4) in register 013H. The ESP/EMON bit must be first written with a 0, followed by a 1, before another transfer can take place between the QE1F-*Plus* and the external transceiver selected. Broadcast capability to all transceivers is enabled when the control bit BDCST (bit 7) in register 013H is written with a 1. Eight clock cycles later, the selected transceiver will respond by sending serial data on the LSDI input pin. The data is shifted in LSB first to LDI7-LDI0 in the Serial Port Data Input Register 012H.

MONITOR MODE

The monitor mode interface permits the QE1F-*Plus* to provide an external receive or transmit NRZ signal from one of the framers to an external device. This interface is selected by placing a high on the CONFIG2 pin (pin 42). Please note that the pins for this mode are shared with the line control interface, and if the monitor mode is selected, these pins cannot be used to provide a serial interface between the external transceivers and the QE1F-*Plus*. In addition, a 1 must be written into the ESP/EMON control bit (bit 4) in the Global Configuration register 013H to enable the monitor mode interface output pins. A 0 written into this control bit causes these data and clock pins to be tri-stated.

A 1 written to control bit RXTX (bit 3) in register 013H selects the receive side, while a 0 selects the transmit side. The framer to be monitored is selected by the value written into the two E1CHCS bits (bits 1 and 0) in register 013H. For example, a value of 00 selects framer 1, and a value of 11 selects framer 4. The selected framer NRZ signal is provided on output pin MONDTO (pin 60). The NRZ receive or transmit data is clocked out on rising edges of the clock MONCLK (pin 61).

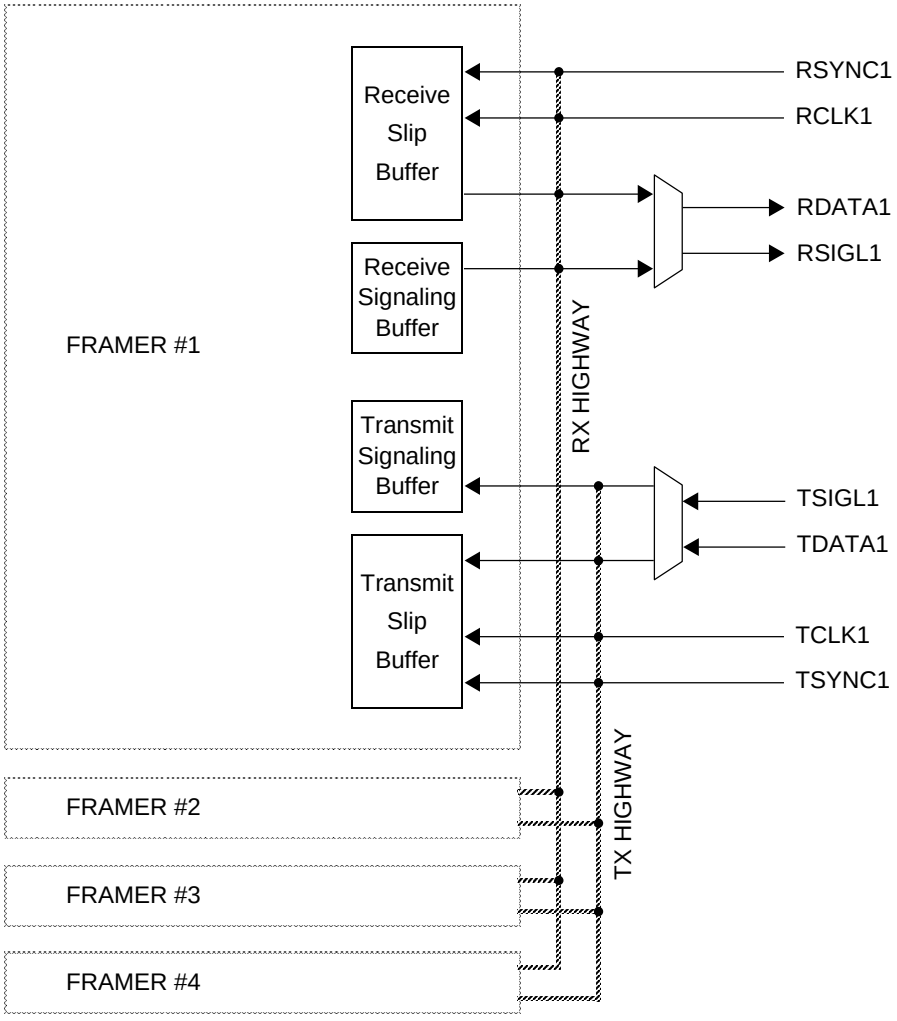
SYSTEM INTERFACE

The system interface connects each of the four framers within the QE1F-*Plus* to and from the system. The system interface is selected by one input pin and two control bits, according to the table given below.

CONFIG1 Pin 43	HMVIP Bit 2 006H	MTP16M Bit 1 006H	System Interface
Low	0	0	**2 Mbit/s Transmission Mode.** Data highway, signaling highway, 2 MHz clock and 2 ms sync pulse for each framer in both transmit and receive directions. Sync pulse is positive, and one clock cycle wide. The system receive clock and sync pulse may be outputs when slip buffer is bypassed.
Low	0	1	**16 Mbit/s Transmission Mode,** bit-interleaved. One shared data highway, 16 MHz clock and 2 ms sync pulse in both transmit and receive directions. The system receive clock and sync pulse must be inputs to the QE1F-*Plus*. The positive sync pulses are one clock cycle wide. The slip buffers for each framer must be enabled.
Low	1	0	**8 Mbit/s Transmission Mode,** byte-interleaved. One shared data highway, signaling highway, 16 MHz clock and 2 ms sync pulse in both transmit and receive directions. The positive sync pulses are two clock cycles wide. The system receive clock and sync pulse must be inputs to the QE1F-*Plus*. The slip buffers for each framer must be enabled.
High	0	0	**2 Mbit/s MVIP Mode:** Data highway, signaling highway, 2 MHz clock, and 125 microsecond sync pulse for each framer in both transmit and receive directions. The slip buffers are always enabled. The system receive and transmit clock and sync pulses are inputs to the QE1F-*Plus*. The negative sync pulses are one clock cycle wide.
High	0	1	**16 Mbit/s PCM Highway Mode,** bit-interleaved. One shared data highway, 16 MHz clock and 125 microsecond sync pulse in both transmit and receive directions. The slip buffers are always enabled. The system receive and transmit clock and sync pulses are inputs to the QE1F-*Plus*. The positive sync pulses are one clock cycle wide.
High	1	0	**8 Mbit/s H-MVIP/H.100 Mode,** byte-interleaved. One shared data highway, signaling highway, 16 MHz clock and 125 microsecond sync pulse in both transmit and receive directions. The slip buffers are always enabled. The system receive and transmit clock and sync pulses are inputs to the QE1F-*Plus*. The negative sync pulses are four clock cycles wide if control bit H100 (bit 2) in register 0FFH is set to a 0 and two clock cycles wide if set to a 1.
X	1	1	Illegal State. Do not use this combination.

For the 2 Mbit/s Transmission and 2 Mbit/s MVIP Modes, each framer has separate transmit and receive interfaces that are referred to as receive and transmit highways. Each highway consists of a data bus (i.e., data highway) RDATAn/TDATAn, a signaling bus (i.e., signaling highway) RSIGLn/TSIGLn, a clock RCLKn/TCLKn, and a synchronization signal RSYNCn/TSYNCn. Internally, each data bus is connected to a two-frame slip buffer, and each signaling bus is connected to a 120-bit signaling buffer. Please note that control bits are provided which enable the slip and signaling buffers to be bypassed when the 2 Mbit/s Transmission Mode is selected. For the 8 Mbit/s and 16 Mbit/s Transmission Modes, 2 Mbit/s MVIP Mode, 8 Mbit/s H-MVIP/H.100 Mode and 16 Mbit/s PCM Highway Mode, the receive and transmit slip buffers must be enabled.

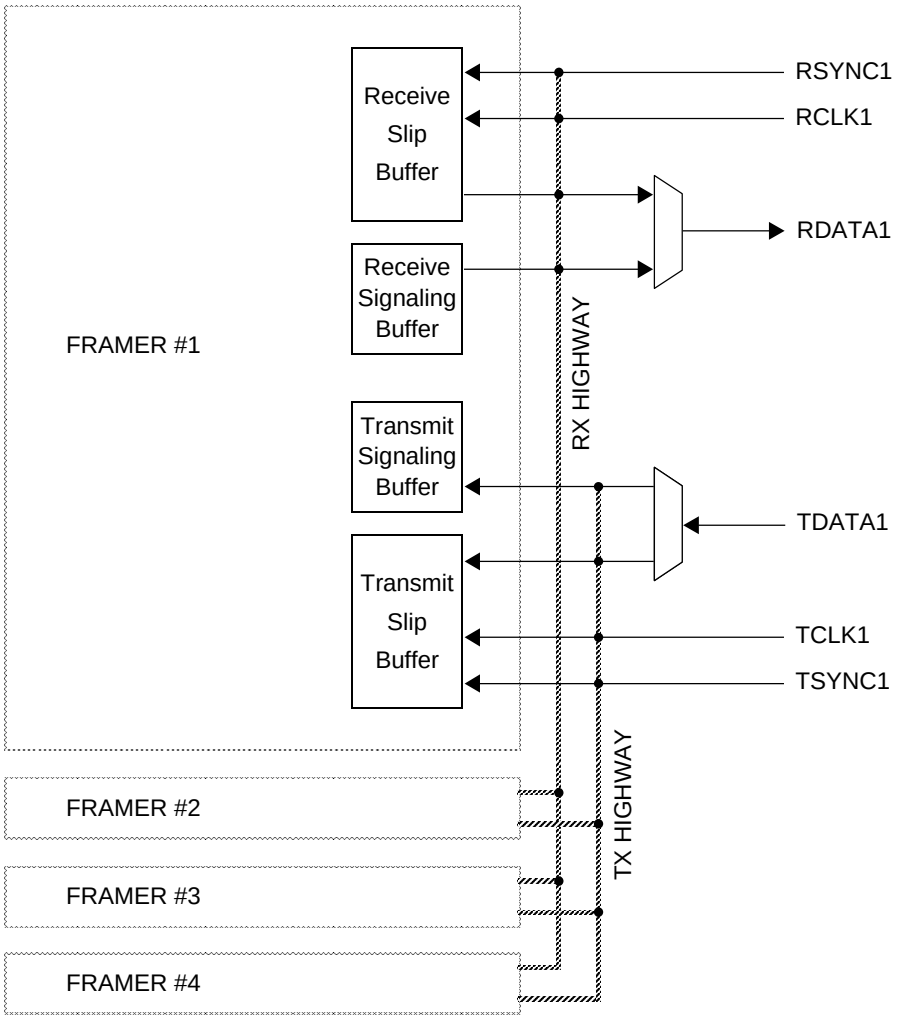
For the 8 Mbit/s Transmission Mode system interface, and the 8 Mbit/s H-MVIP/H.100 Mode system interface, common data (RDATA1 and TDATA1) and signaling (RSIGL1 and TSIGL1) buses are used to interface the four framers, as shown in Figure 38.



Note: The time slots of all four framers are byte-interleaved, with separate data and signaling buses, for both receive and transmit.

Figure 38. 8 Mbit/s Transmission Mode and 8 Mbit/s H-MVIP/H.100 Mode System Interfaces

For the 16 Mbit/s Transmission Mode system interface and the 16 Mbit/s PCM Highway Mode system interface, a common data bus (RDATA1 and TDATA1) is used to interface the four framers, as shown in Figure 39.



Note: The time slots of all four framers are bit-interleaved, with the data and signaling combined on the data bus, for both receive and transmit.

Figure 39. 16 Mbit/s Transmission Mode and 16 Mbit/s PCM Highway Mode System Interfaces

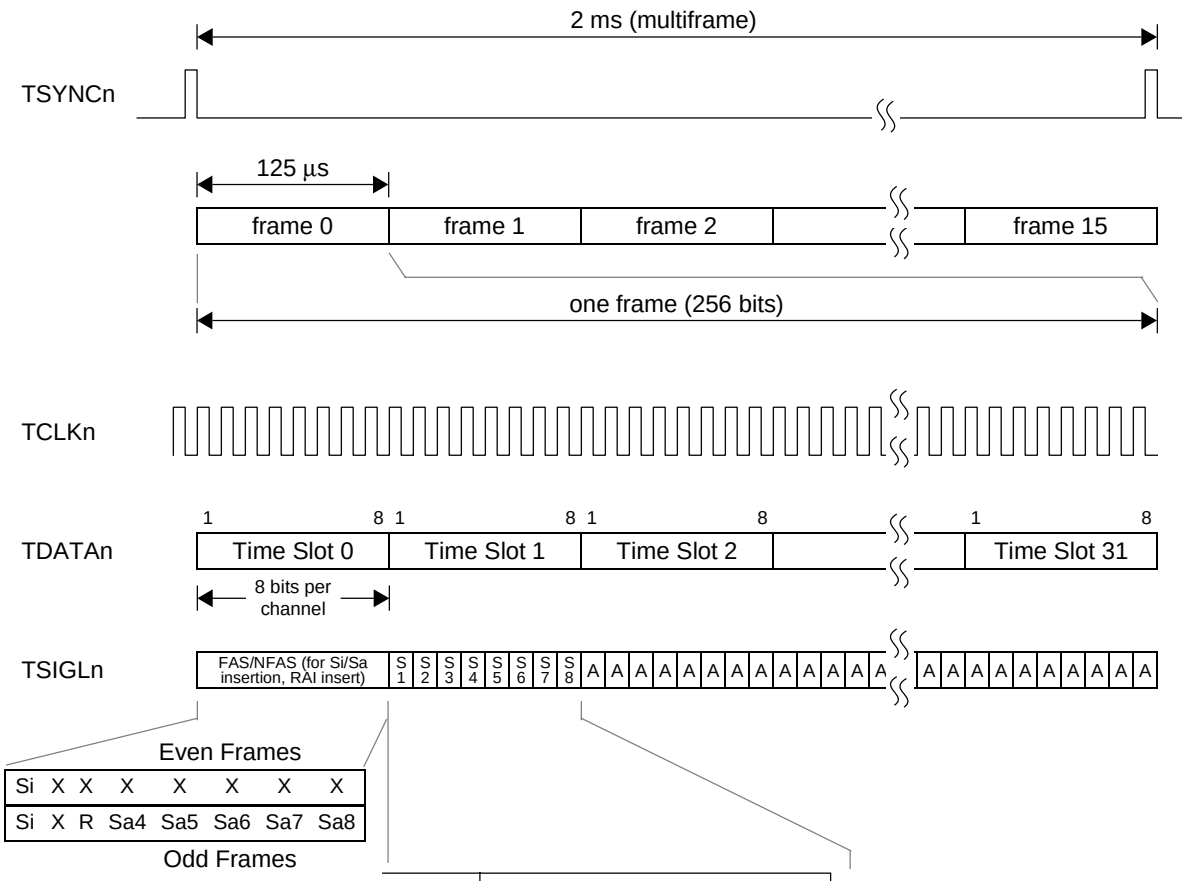
2 MBIT/S TRANSMISSION MODE

The 2 Mbit/s Transmission Mode is enabled when a low is placed on the CONFIG1 pin (pin 43), and control bits 2 (HMVIP) and 1 (MTP16M) in register 006H are set to 0.

Transmit Highway

When the 2 Mbit/s Transmission Mode is selected, the transmit highway carries information from the system to the QE1F-*Plus* for each framer. The highway is subdivided into two time division multiplexed buses, one for data (TDATAn), and the other one for signaling, alarms, and selected bits that may be multiplexed into Time Slot 0 (TSIGLn). The n in the TDATAn and TSIGLn signals represents one of the four framers. The two buses are synchronous with respect to the highway clock (TCLKn), which has a clock rate of 2048 kHz. The data highway is a single bit-serial bus organized into 256-bit groups called frames, with the bits in each group numbered 1 through 256. Each frame consists of 32 time slots, numbered from 0 to 31, as shown in Figure 40. Also note that sixteen frames form a multiframe, with the beginning of each multiframe identified by an active high synchronization pulse (TSYNCn), one (TCLKn) clock cycle wide, which occurs every 2 ms, normally at the end of frame 15. The position of the TSYNCn pulse is programmable to any bit position within the data bus frame using control bits TSD7-TSD0 in register 017H as described below in the Transmit and Receive Synchronization subsection. The synchronization pulse is aligned to bit 8 in Time Slot 31 in frame 15 when a value of 00H is written into this register.

The signaling bus (TSIGLn) is also divided into 256-bit frames. Each signaling frame consists of 256 bits of signaling and alarm information for the 30 telephone data channels, numbered from 1 to 30, that are carried on the data bus (i.e., Time Slots 1-15 and 17-31). The first time slot (Time Slot 0) is assigned to carry the two international bits in bit 1 of alternate frames (bit Si), and the five national bits in bits 4 through 8 and the remote alarm indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The positions of the Time Slot 0 bits in this frame are the same as found in Time Slot 0 of the E1 frame format. It is not required that the Time Slot 0 from the signaling bus carry the frame alignment pattern in FAS frames, or have bit 2 in the alternating NFAS frames set to 1. Time Slot 1 in the signaling bus carries the Channel Associated Signaling (CAS) multiframe format. The multiframe is repeated every 16 frames. The multiframe alignment pattern (0000), and the spare and multiframe alarm bits (X0, Y, X1, X2) occur in frame 0, followed by the ABCD signaling bits for channels 1 through 30 (starting with channels 1 and 16 in frame 1, and ending with channels 15 and 30 in frame 15). The remaining bits, which are marked "A" in Time Slots 2 through 31, carry a system AIS indication. Status bits TUAIS (bit 3) and TURAI (bit 2) in register X14H provide the active states of the AIS bit and the remote failure alarm indication (RFI) bit on the transmit signaling bus in the Transmission Mode. These TU alarms correspond to a system SDH byte-synchronous interface.



Frame	TSIGL; S1 - S8
0	0, 0, 0, 0, X0, Y, X1, X2,
1	A1, B1, C1, D1, A16, B16, C16, D16
2	A2, B2, C2, D2, A17, B17, C17, D17
3	A3, B3, C3, D3, A18, B18, C18, D18
4	A4, B4, C4, D4, A19, B19, C19, D19
5	A5, B5, C5, D5, A20, B20, C20, D20
6	A6, B6, C6, D6, A21, B21, C21, D21
7	A7, B7, C7, D7, A22, B22, C22, D22
8	A8, B8, C8, D8, A23, B23, C23, D23
9	A9, B9, C9, D9, A24, B24, C24, D24
10	A10, B10, C10, D10, A25, B25, C25, D25
11	A11, B11, C11, D11, A26, B26, C26, D26

Notes:
Si = International Bits
R = Remote Alarm Indication (RAI) bit, known as TS0 A-bit
San = National bits (n = 4-8)
X = don't care bit state
Xb = Spare bits (b = 0-2)
Y = Multiframe Alarm
Ac Bc Cc Dc = ABCD signal bits for channel c (1-30)
A = Alarm Bits (AIS)

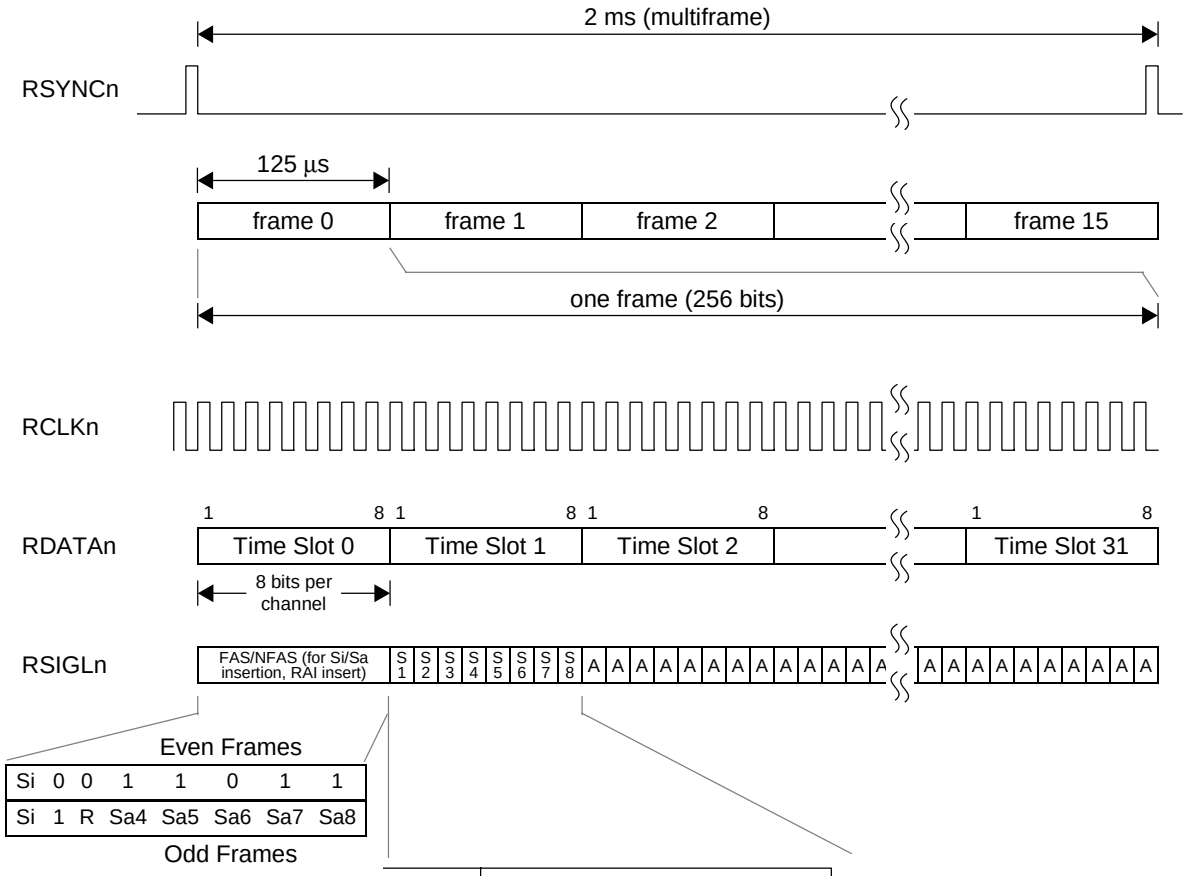
Figure 40. Transmit Highway - 2 Mbit/s Transmission Mode

Receive Highway

In the 2 Mbit/s Transmission Mode, the receive highway for each framer carries information from the QE1F-*Plus* to the system. Like the transmit path, the receive highway is subdivided into two time division multiplexed buses, one for data (RDATAn), and one for signaling and alarms (RSIGLn), where n represents one of the four framers. The two buses are synchronous with the highway clock (RCLKn), which has a clock rate of 2048 kHz. The clock (RCLKn) is either an output to the system or an input from the system. The system clock (RCLKn) or the line clock (LRCLKn) may be the input clock source for the slip buffer when it is enabled. Usually the system clock (RCLKn) is used. The QE1F-*Plus* sources the clock (RCLKn) as an output when the slip buffer is bypassed. The receive slip buffer for a framer is disabled when a 0 is written to the RSE bit (bit 3) in the Framer Configuration register X02H. The clock source selection is determined by the RXC bit (bit 5) in register X02H, when the signaling buffer is enabled. A 0 written into this bit position selects the system clock (RCLKn) as the source clock. In addition to controlling the source of the clock, control bit RXC also controls the source of the sync pulse.

The data bus is a single bit-serial bus organized into 256-bit groups called frames, as shown in Figure 41. Each frame consists of 32 time slots, as shown for the transmit interface. Sixteen frames form a multiframe, with the beginning of each multiframe identified by an active high synchronization pulse (RSYNCn), one (RCLKn) clock cycle wide, which occurs every 2 ms, normally at the end of frame 15. The position of the RSYNCn pulse is programmable to any bit position within the frame using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned to bit 8 in Time Slot 31 in frame 15 when a value of 00H is written into this register.

The signaling bus (RSIGLn) is also divided into 256-bit frames. Each signaling frame consists of 256 bits of signaling and alarm information for the 30 data channels carried on the data bus. The first eight bits (which correspond to Time Slot 0 in the received frame) are assigned to carry the two international bits in bit 1 of alternate frames, and the five national bits in bits 4 through 8 and the remote alarm indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The other (FAS) frames carry a regenerated frame alignment pattern in Time Slot 0. Time Slot 1 in the signaling bus carries the Channel Associated Signaling multiframe format. The multiframe is repeated every 16 frames. The multiframe alignment pattern (0000), and the spare and multiframe alarm bits (X0, Y, X1, X2) occur in frame 0 followed by the ABCD signaling bits for channels 1 through 30 (starting with channels 1 and 16 in frame 1, and ending with channels 15 and 30 in frame 15). The remaining bits, which are marked "A" in Time Slots 2 through 31, carry a system AIS indication.



Frame	RSIGL; S1 - S8
0	0, 0, 0, 0, X0, Y, X1, X2,
1	A1, B1, C1, D1, A16, B16, C16, D16
2	A2, B2, C2, D2, A17, B17, C17, D17
3	A3, B3, C3, D3, A18, B18, C18, D18
4	A4, B4, C4, D4, A19, B19, C19, D19
5	A5, B5, C5, D5, A20, B20, C20, D20
6	A6, B6, C6, D6, A21, B21, C21, D21
7	A7, B7, C7, D7, A22, B22, C22, D22
8	A8, B8, C8, D8, A23, B23, C23, D23
9	A9, B9, C9, D9, A24, B24, C24, D24
10	A10, B10, C10, D10, A25, B25, C25, D25
11	A11, B11, C11, D11, A26, B26, C26, D26

Notes:
Si = International Bits
R = Remote Alarm Indication (RAI) bit, known as TS0 A-bit
San = National bits (n = 4-8)
Xb = Spare bits (b = 0-2)
Y = Multiframe Alarm
Ac Bc Cc Dc = ABCD signal bits for channel c (1-30)
A = Alarm Bits (AIS)

Figure 41. Receive Highway - 2 Mbit/s Transmission Mode

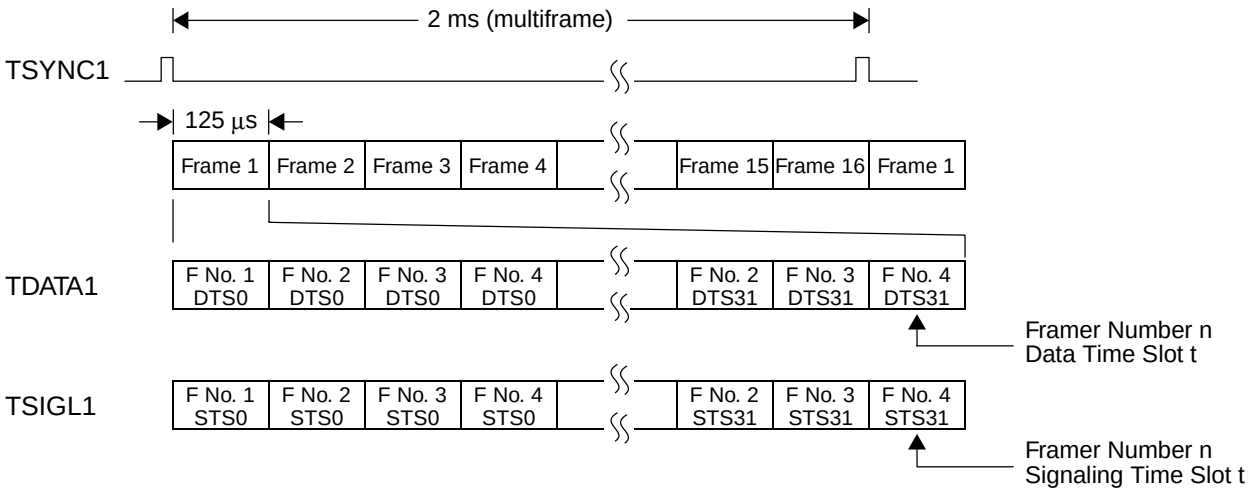
8 MBIT/S TRANSMISSION MODE

The 8 Mbit/s Transmission Mode is enabled when a low is placed on the CONFIG1 pin (pin 43), and a 1 is written to control bit HMVIP (bit 2) and a 0 is written to control bit MTP16M (bit 1) in register 006H.

Transmit Highway

When the 8 Mbit/s Transmission Mode is selected, a common transmit highway carries information for the four framers from the system to the QE1F-*Plus*. The single highway is subdivided into two time division multiplexed buses, one for data (TDATA1), and the other (TSIGL1) for signaling, alarms, and selected bits. The two buses are synchronous with respect to the single highway clock (TCLK1), which has a clock rate of 16.384 MHz (two cycles per bit time). The data bus is a single bit-serial bus organized into sixteen 1024-bit frames. Each frame contains byte-interleaved E1 frames of 32 time slots each for the four framers, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31, as shown in Figure 42. Each frame for each framer consists of thirty-two bytes, which represent the 32 time slots in an E1 frame. Also note that the beginning of the 16-frame multiframe is identified by an active high, two clock cycle (TCLK1) wide synchronization pulse (TSYNC1), which occurs every 2 ms, normally at the end of frame 16. The position of the TSYNC1 pulse is programmable using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned to bit 8 in Time Slot 31 of framer 4 in frame 16 when a value of 00H is written into this register.

The signaling bus (TSIGL1) is also divided into sixteen 1024-bit frames, each consisting of 32 byte-interleaved time slots for each framer. Each of the four framer's signaling time slots are interleaved on a byte (or time slot) boundary, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31. The format of the signaling frame is exactly the same as found in the 2 Mbit/s Transmission Mode.



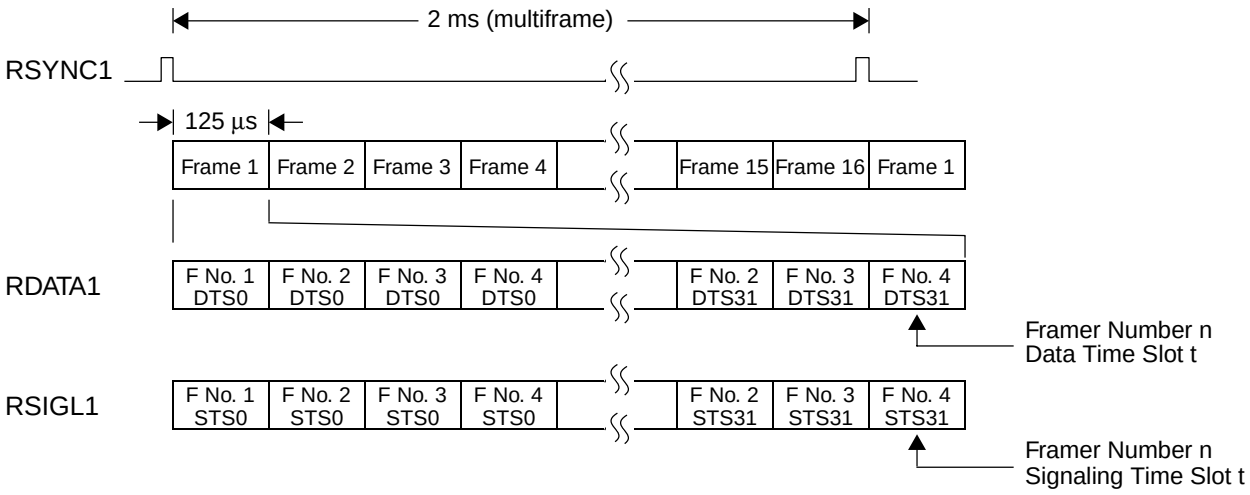
Note: The frame formats for a framer Data frame (F No. n, DTSt) and Signaling frame (F No. n, STSt) are the same as for the 2 Mbit/s Transmission format.

Figure 42. Transmit Highway - 8 Mbit/s Transmission Mode

Receive Highway

The receive highway has the same structure as the transmit highway. A common receive highway carries information for the four framers from the QE1F-*Plus* to the system. The single highway is subdivided into two time division multiplexed buses, one for data (RDATA1), and the other (RSIGL1) for signaling, alarms, and selected bits. The two buses are synchronous with respect to the single highway clock (RCLK1), which has a clock rate of 16.384 MHz. The data bus is a single bit-serial bus organized into sixteen 1024-bit frames. Each frame contains byte-interleaved E1 frames of 32 time slots each for the four framers, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31, as shown in Figure 43. The beginning of the 16-frame multiframe is identified by an active high, two clock cycle (RCLK1) wide synchronization pulse (RSYNC1), which occurs every 2 ms, normally at the end of frame 16. The position of the RSYNC1 pulse is programmable using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned to bit 8 in Time Slot 31 of framer 4 in frame 16 when a value of 00H is written into this register.

The signaling bus (RSIGL1) is also divided into sixteen 1024-bit frames. Each frame contains byte-interleaved E1 frames of 32 time slots each for the four framers, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31. The format of a signaling frame is exactly the same as found in the 2 Mbit/s Transmission Mode format.



Note: The frame formats for a framer Data frame (F No. n, DTSt) and Signaling frame (F No. n, STSt) are the same as for the 2 Mbit/s Transmission format.

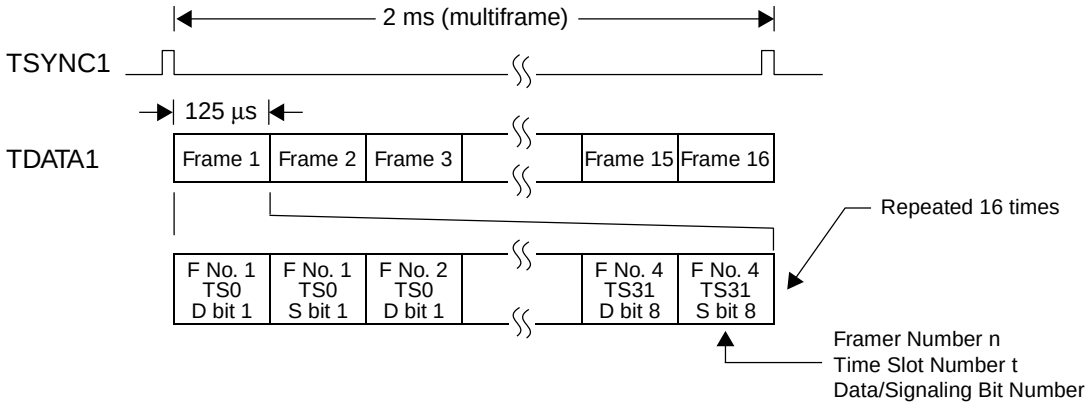
Figure 43. Receive Highway - 8 Mbit/s Transmission Mode

16 MBIT/S TRANSMISSION MODE

The 16 Mbit/s Transmission Mode is enabled when a low is placed on the CONFIG1 pin (pin 43), and a 0 is written to control bit HMVIP (bit 2) and a 1 is written to control bit MTP16M (bit 1) in register 006H.

Transmit Highway

When the 16 Mbit/s Transmission Mode is selected, a common time division multiplexed bus (TDATA1) carries data, signaling, alarms, and selected bits in a bit-interleaved format. The bus is synchronous with respect to the single highway clock (TCLK1), which has a clock rate of 16.384 MHz (one cycle per bit time). The data bus is a single bit-serial bus organized into sixteen 2048-bit frames. Each frame contains bit-interleaved data and signaling bit-pairs from the E1 frames (32 time slots) of the four framers, starting with framer 1 Time Slot 0 data bit 1, then framer 1 Time Slot 0 signaling bit 1, followed by framer 2 Time Slot 0 data bit 1, and ending with framer 4 Time Slot 31 signaling bit 8, as shown in Figure 44. Each 16-frame multiframe is identified by an active high, one clock cycle (TCLK1) wide synchronization pulse (TSYNC1), which occurs every 2 ms, normally at the end of frame 16. The position of the TSYNC1 pulse is programmable using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned to framer 4, Time Slot 31 signaling bit 8 in frame 16 when a value of 00H is written into this register. The formats for each of the framer's data frame and signaling frame are exactly the same as found in the 2 Mbit/s Transmission Mode format.



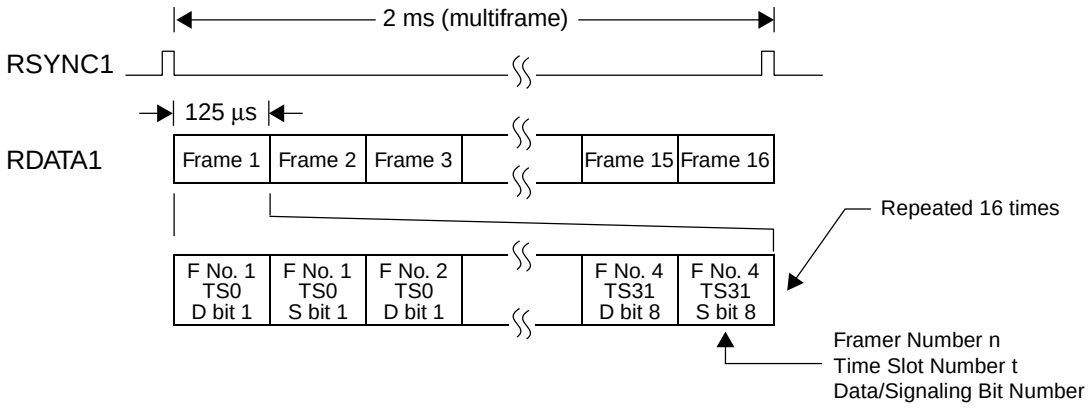
Note: The frame formats for a framer data frame and signaling frame are the same as for the 2 Mbit/s Transmission Mode.

Figure 44. Transmit Highway - 16 Mbit/s Transmission Mode

Receive Highway

The receive highway has the same structure as the transmit highway. When the 16 Mbit/s Transmission Mode is selected, a single time division multiplexed bus (RDATA1) carries data, signaling, alarms, and selected bits in a bit-interleaved format for each of the four framers. The bus is synchronous with respect to the single highway clock (RCLK1), which has a clock rate of 16.384 MHz. The data bus is a single bit-serial bus organized into sixteen 2048-bit frames. Each frame contains bit-interleaved data and signaling bit-pairs from the E1 frames (32 times slots) of the four framers, starting with framer 1 Time Slot 0 data bit 1, then framer 1 Time Slot 0 signaling bit 1, followed by framer 2 Time Slot 0 data bit 1 and ending with framer 4 Time Slot 31 signaling bit 8, as shown in Figure 45. The beginning of each 16-frame multiframe is identified by an active high, one clock cycle wide (RCLK1) synchronization pulse (RSYNC1), which occurs every 2 ms, normally at the end of frame 16. The position of the RSYNC1 pulse is programmable using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned to framer 4 Time Slot 31 signaling bit 8 in frame 16 when a value of 00H

is written into this register. The formats for each of the framer's data frame and signaling frame are exactly the same as found in the 2 Mbit/s Transmission Mode format.



Note: The frame formats for a framer data frame and signaling frame are the same as for the 2 Mbit/s Transmission Mode.

Figure 45. Receive Highway - 16 Mbit/s Transmission Mode

2 MBIT/S MVIP MODE

The 2 Mbit/s MVIP Mode is enabled when a high is placed on the CONFIG1 pin (pin 43) and control bits HMVIP (bit 2) and MTP16M (bit 1) in register 006H are both written with a 0.

Transmit Highway

In the 2 Mbit/s MVIP Mode, the transmit highway for each framer in the QE1F-*Plus* carries input information from the system. The highway for framer n is subdivided into two time division multiplexed buses, one for data (TDATAn), and one for signaling (TSIGLn). The two buses are synchronous with the highway clock (TCLKn), which has a clock rate of 2048 kHz. The data bus is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty-two bytes, which represent the 32 time slots, as shown in Figure 45. Time Slot 0 is used for frame alignment. Time Slot 16 carries either the Channel Associated Signaling multiframe, or a clear channel. The other time slots in the frame carry the 30 telephone data channels.

The frame start is identified by a synchronization pulse (TSYNCn), which is one (TCLKn) clock cycle wide and occurs every 125 microseconds. The position of the TSYNCn pulse is programmable to any bit position within the frame using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned to bit 1 in Time Slot 0 when a value of 00H is written into this register.

The signaling bus (TSIGLn) is also divided into 256-bit frames. Each signaling frame consists of 32 time slots, of which 30 time slots (1-15 and 17-31) carry the ABCD signaling bits associated with the 30 telephone channels. The signaling information in Time Slot t on the signaling bus corresponds to Time Slot t on the data bus. The signaling information (ABCD) is carried in the last four bits of a signaling bus time slot. The first four bits in each signaling bus time slot are 0000. For Time Slot 16 on the signaling bus, the spare bits (X0, X1, X2) from the signaling multiframe occupy the ACD bits. Bit position B, which corresponds to the multiframe alarm Y-bit, is ignored by the QE1F-*Plus*.

The signaling buffer is updated every other frame by the signaling information present in Time Slot 1 on the signaling bus. In alternating frames, Time Slot 0 must carry the frame alignment sequence (FAS), which is a

framing pattern in bits 2 through 8 (0011011) and an international bit in bit 1. The other alternating frames (NFAS) carry the second international bit in bit 1, a 1 in bit 2, an RAI bit (A-bit) in bit 3, and five national bits in bits 4 through 8. Bit 2 identifies the frame alternations for Time Slot 0. The state of the RAI bit in Time Slot 0 from the system is ignored. (Note: If the international, RAI and Sa bits are forced internally by the microprocessor or FDL, then the TS0 may be left unformatted). The framer will always generate the FAS and NFAS framing patterns. FAS and NFAS need to be inserted only if the Si, San, and/or R bits from the signaling highway are to be used.

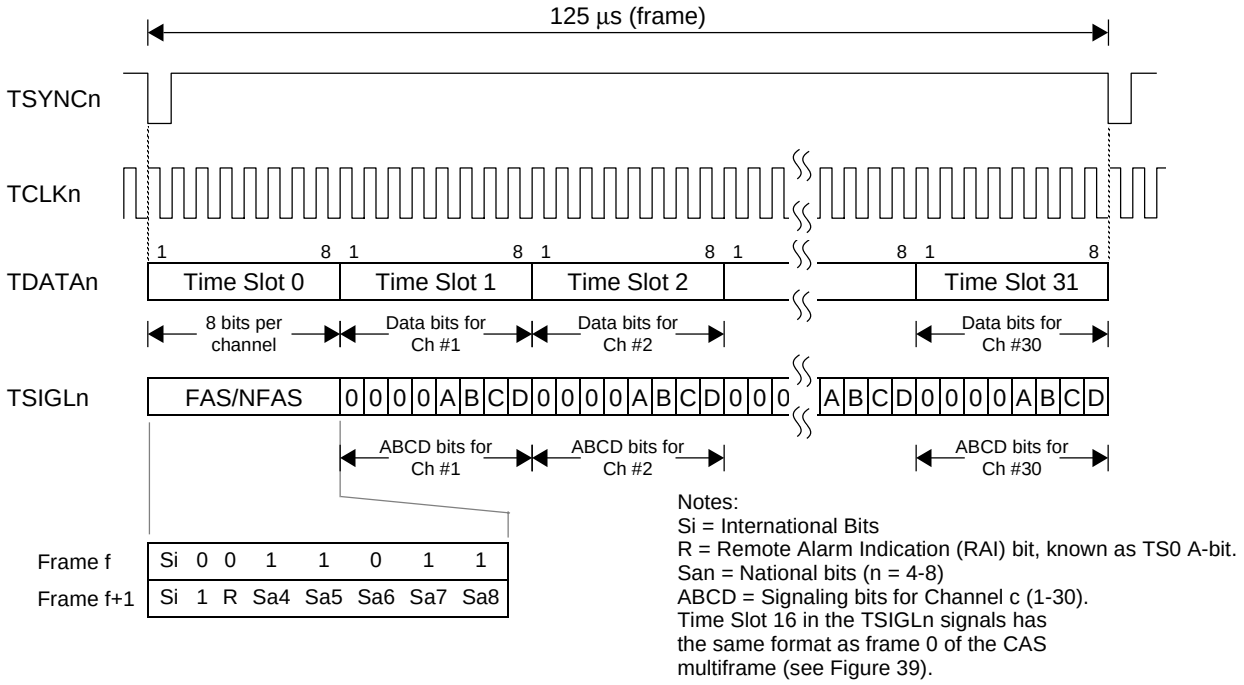


Figure 46. Transmit Highway - 2 Mbit/s MVIP Mode

Receive Highway

In the 2 Mbit/s MVIP Mode, the receive highway for each framer carries output information from the QE1F-*Plus* to the system. The highway for framer n is subdivided into two time division multiplexed buses, one for data (RDATAn), and one for signaling (RSIGLn). The two buses are synchronous with the highway clock (RCLKn), which has a clock rate of 2048 kHz. The data bus is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty-two bytes, which represent the 32 time slots, as shown in Figure 47. Time Slot 0 is used for frame alignment. Time Slot 16 carries either the Channel Associated Signaling multiframe, or a clear channel. The other time slots carry the 30 telephone data channels.

The frame start is identified by a synchronization pulse (RSYNCn), which is one (RCLKn) clock cycle wide and occurs every 125 microseconds. The position of the RSYNCn pulse is programmable to any bit position within the frame using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned to bit 1 in Time Slot 0 when a value of 00H is written into this register.

The signaling bus (RSIGLn) is also divided into 256-bit frames. Each signaling frame consists of 32 time slots, of which 30 time slots (1-15 and 17-31) carry the ABCD signaling bits associated with the 30 telephone channels. The signaling information in Time Slot t on the signaling bus corresponds to Time Slot t on the data bus. The signaling information (ABCD) is carried in the last four bits of a signaling bus time slot. The first four bits in each time slot are 0000. For Time Slot 16 on the signaling bus, the spare bits (X0, X1, X2) from the signaling multiframe occupy the ACD bits. The multiframe alarm Y-bit is carried in bit position B in Time Slot 16.

The signaling bus is updated from the signaling buffer every frame. In alternating frames, Time Slot 0 carries

the frame alignment sequence (FAS), which is a framing pattern in bits 2 through 8 (0011011) and an international bit in bit 1. The other alternating frames carry the second international bit in bit 1, a 1 in bit 2, an RAI bit (A-bit) in bit 3, and five national bits in bits 4 through 8. Bit 2 identifies the frame alternations for Time Slot 0.

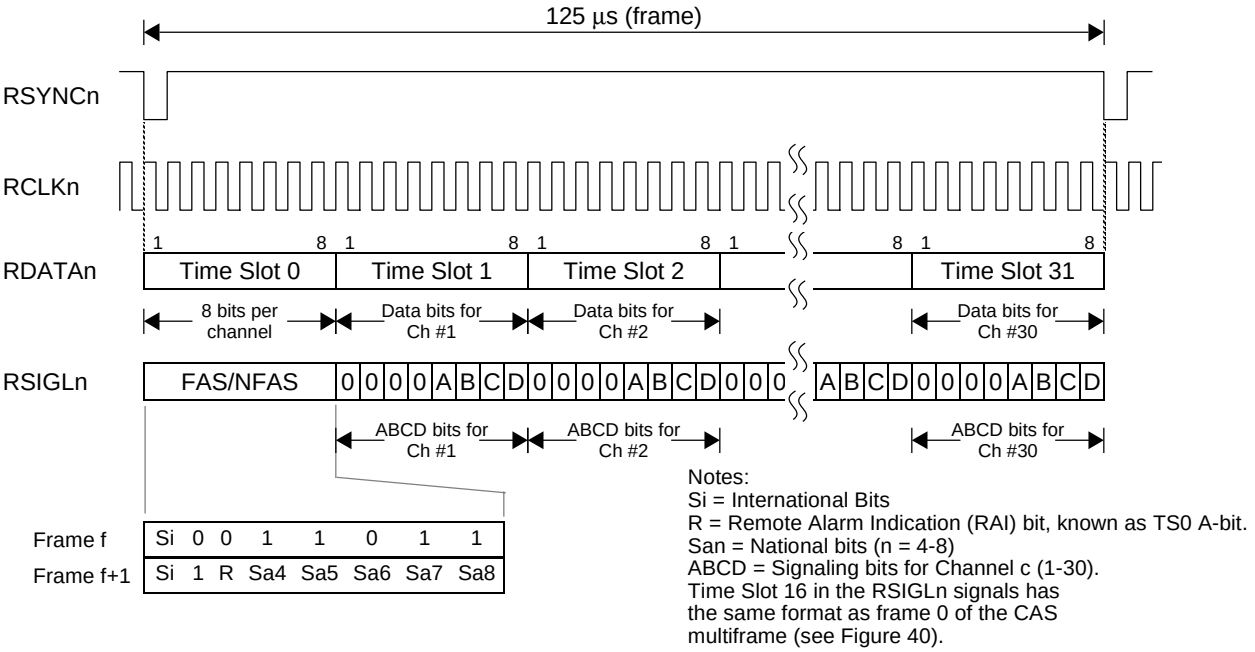


Figure 47. Receive Highway - 2 Mbit/s MVIP Mode

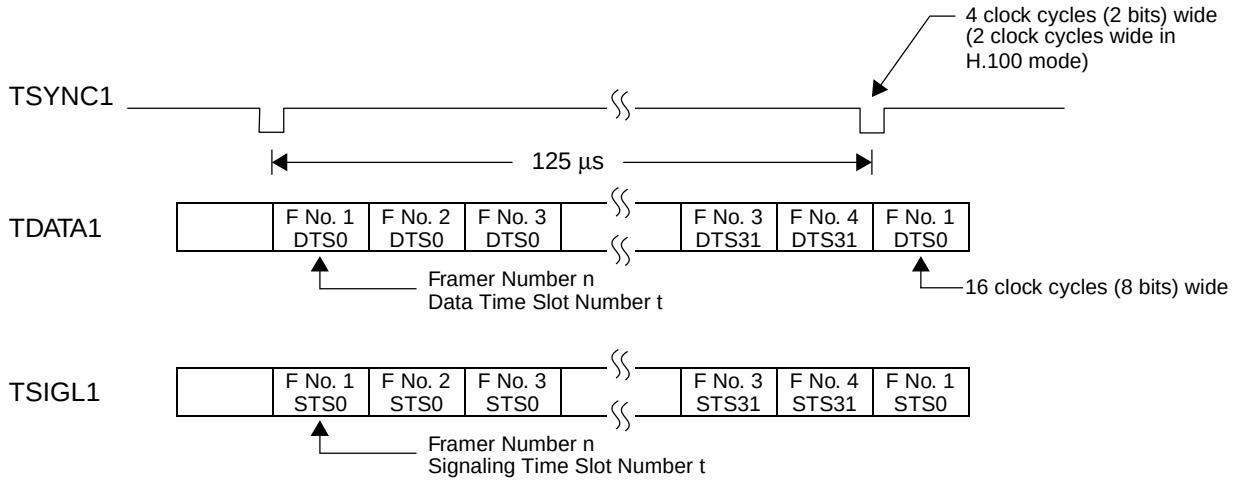
8 MBIT/S H-MVIP/H.100 MODE

The 8 Mbit/s H-MVIP/H.100 Mode is enabled when a high is placed on the CONFIG1 pin (pin 43) and a 1 is written to control bit HMVIP (bit 2) and a 0 to control bit MTP16M (bit 1) in register 006H. The H.100 option for the TSYNC1 and RSYNC1 pulse width is determined by control bit H100 (bit 2) in register 0FFH; if set to a 1, the frame pulse expected is two clock cycles of TCLK1 or RCLK1 wide; if set to a 0 a four clock cycle wide frame pulse is expected.

Transmit Highway

When the 8 Mbit/s H-MVIP/H.100 Transmission Mode is selected, a common transmit highway carries information for the four framers from the system to the QE1F-*Plus*. The single highway is subdivided into two time division multiplexed buses, one for data (TDATA1), and the other (TSIGL1) for signaling and selected bits. The two buses are synchronous with respect to the single highway clock (TCLK1), which has a clock rate of 16.384 MHz. The data bus is a single bit-serial bus organized into 1024-bit frames. Each frame contains byte-interleaved E1 frames of 32 time slots each for the four framers, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31, as shown in Figure 48. Each frame for each framer consists of thirty-two bytes, which represent the 32 time slots in an E1 frame. Also note that the frame is identified by an active low, four clock cycle (TCLK1) wide synchronization pulse (TSYNC1), which occurs every 125 microseconds for H-MVIP. For H.100 the synchronization pulse is active low, two clock cycles (TCLK1) wide. The position of the TSYNC1 pulse is programmable using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned with framer 4 Time Slot 31 bit 8 and framer 1 Time Slot 0 bit 1 in the next frame when a value of 00H is written into this register.

The signaling bus (TSIGL1) is also divided into 1024-bit frames, each consisting of 32 byte-interleaved time slots for each framer. Each of the four framer's signaling time slots are interleaved on a byte (time slot) boundary, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31. The format of the signaling frame is exactly the same as found in the 2 Mbit/s MVIP Mode. The framer will always generate the FAS and NFAS framing patterns. FAS and NFAS need to be insertedonly if the Si, San, and/or R bits from the signaling highway are to be used.



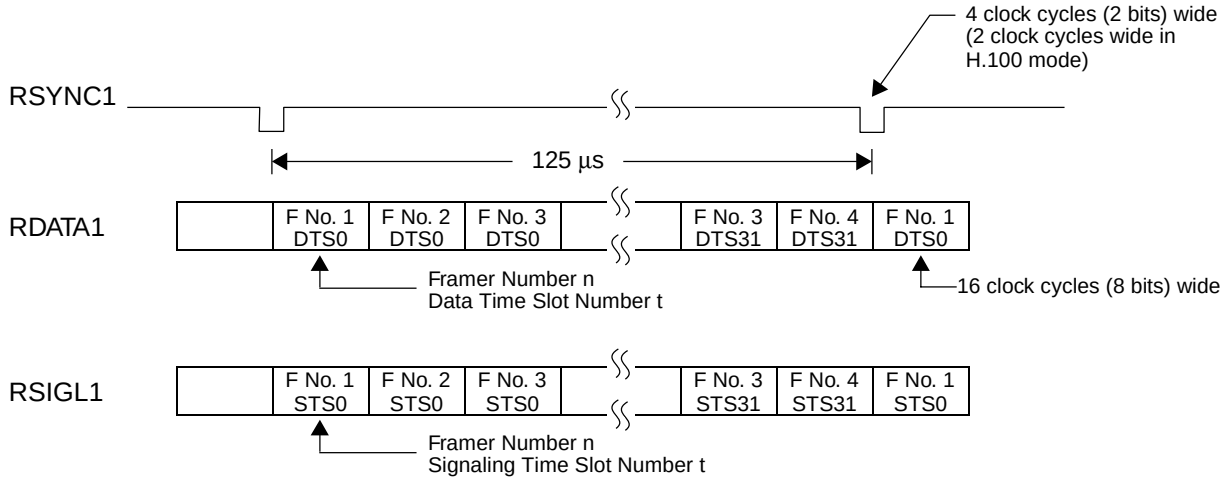
Note: The data and signaling frame formats for each framer are the same as found in the 2 Mbit/s MVIP Mode.

Figure 48. Transmit Highway - 8 Mbit/s H-MVIP/H.100 Mode

Receive Highway

The receive highway has the same structure as the transmit highway. A common receive highway carries information for the four framers from the QE1F-*Plus* to the system. The single highway is subdivided into two time division multiplexed buses, one for data (RDATA1), and the other (RSIGL1) for signaling and selected bits. The two buses are synchronous with respect to the single highway clock (RCLK1), which has a clock rate of 16.384 MHz. The data bus is a single bit-serial bus organized into 1024-bit frames. Each frame contains byte-interleaved E1 frames of 32 time slots each for the four framers, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31, as shown in Figure 49. The beginning of the 1024-bit frame is identified by an active low, four clock cycle (RCLK1) wide synchronization pulse (RSYNC1), which occurs every 125 microseconds for H-MVIP. For H.100 the synchronization pulse is active low, two clock cycles (RCLK1) wide. The position of the RSYNC1 pulse is programmable using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned with framer 4 Time Slot 31 bit 8 and framer 1 Time Slot 0 bit 1 in the next frame when a value of 00H is written into this register.

The signaling bus (RSIGL1) is also divided into 1024-bit frames, each consisting of 32 byte-interleaved time slots for each framer, starting with framer 1 Time Slot 0, followed by framer 2 Time Slot 0, and ending with framer 4 Time Slot 31. The format of a signaling frame is exactly the same as found in the 2 Mbit/s MVIP Mode format.



Note: The data and signaling frame formats for each framer are the same as found in the 2 Mbit/s MVIP Mode.

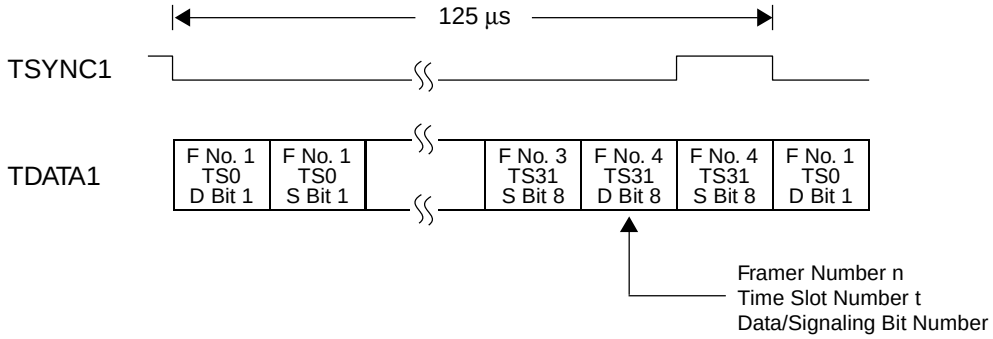
Figure 49. Receive Highway - 8 Mbit/s H-MVIP/H.100 Mode

16 MBIT/S PCM HIGHWAY MODE

The 16 Mbit/s PCM Highway Mode is enabled when a high is placed on the CONFIG1 pin (pin 43) and a 0 is written to control bit HMVIP (bit 2) and a 1 to control bit MTP16M (bit 1) in register 006H.

Transmit Highway

When the 16 Mbit/s PCM Highway Mode is selected, a common transmit highway carries information for the four framers from the system to the QE1F-*Plus*. The single highway is a single time division multiplexed bus (TDATA1) that is used to carry data, signaling, and selected bits. The bus is synchronous with respect to the single highway clock (TCLK1), which has a clock rate of 16.384 MHz (one cycle per bit time). The data bus is a single bit-serial bus organized into 2048-bit frames. Each frame contains bit-interleaved data and signaling bit-pairs from the E1 frames (32 time slots) of the four framers, starting with framer 1 Time Slot 0 data bit 1, then framer 1 Time Slot 0 signaling bit 1, followed by framer 2 Time Slot 0 data bit 1, and ending with framer 4 Time Slot 31 signaling bit 8, as shown in Figure 50. Each 2048-bit frame is identified by an active high, one (TCLK1) clock cycle wide synchronization pulse (TSYNC1), which occurs every 125 microseconds. The position of the TSYNC1 pulse is programmable using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned to framer 4 Time Slot 31 signaling bit 8 when a value of 00H written into this register. The formats for each of the framer's data frame and signaling frame are exactly as found in the 2 Mbit/s MVIP Mode format.



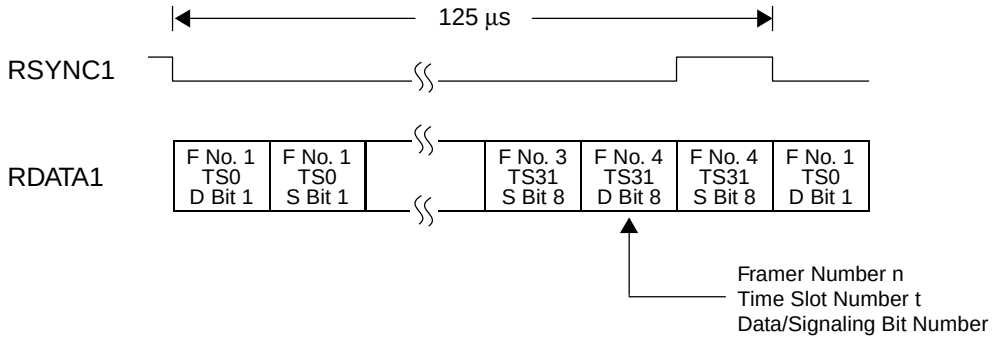
Note: The frame formats for a framer data frame and signaling frame are the same as for the 2 Mbit/s MVIP Mode.

Figure 50. Transmit Highway - 16 Mbit/s PCM Highway Mode

Receive Highway

The receive highway has the same structure as the transmit highway. When the 16 Mbit/s PCM Highway Mode is selected, a single time division multiplexed bus (RDATA1) carries data, signaling, and selected bits in a bit-interleaved format for each of the four framers. The bus is synchronous with respect to the single highway clock (RCLK1), which has a clock rate of 16.384 MHz. The data bus is a single bit-serial bus organized into 2048-bit frames. Each frame contains bit-interleaved data and signaling bit-pairs from the E1 frames (32 time slots) of the four framers, starting with framer 1 Time Slot 0 data bit 1, then framer 1 Time Slot 0 signaling bit 1, followed by framer 2 Time Slot 0 data bit 1 and ending with framer 4 Time Slot 31 signaling bit 8, as shown in Figure 51. The beginning of each 2048-bit frame period is identified by an active high, one (RCLK1) clock cycle wide synchronization pulse (RSYNC1), which occurs every 125 microseconds. The position of the RSYNC1 pulse is programmable using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned to framer 4 Time Slot 31 signaling bit 8 when a value of 00H written into this register. The formats for each of

the framer's data frame and signaling frame are exactly as found in the 2 Mbit/s MVIP Mode format.



Note: The frame formats for a framer data frame and signaling frame are the same as for the 2 Mbit/s MVIP Mode.

Figure 51. Receive Highway - 16 Mbit/s PCM Highway Mode

TRANSMIT AND RECEIVE SYNCHRONIZATION

Control bits TSD7-TSD0 in register 017H specify the number of transmit clock cycles (TCLKn) that the transmit sync input signal (TSYNCn) can be advanced with respect to the data and signaling signals TDATAn and TSIGLn. The programmability is common to all four framers. The default value is 00H. The following table lists the default position of the sync pulse in relationship to the TDATAn or TSIGLn signals. Control bits RSD7-RSD0 in register 018H have a corresponding function with respect to RCLKn, RSYNCn, RDATAn and RSIGLn.

System Interface	Synchronization
2 Mbit/s Transmission	Default Location (00H): Bit 8 in Time Slot 31 in frame 16. Each binary value allows the sync pulse to occur one bit earlier. For example, a count of 1 corrects for a sync pulse that occurs in bit 7 instead of 8 in Time Slot 31 in frame 16.
8 Mbit/s Transmission	Default Location (00H): Framer No.4 bit 8 in Time Slot 31 in frame 16. Each binary value in increments of 8 allows the sync pulse to occur one time slot earlier. For example, a count of 8 corrects for a sync pulse that occurs in framer No.4 bit 8 in Time Slot 30 in frame 16. Not valid for values which are not multiples of 8.
16 Mbit/s Transmission	Default Location (00H): Framer No.4 signaling bit 8 in Time Slot 31 in frame 16. Each binary value in increments of 8 allows the sync pulse to occur one time slot earlier. For example, a count of 8 corrects for a sync pulse that occurs in framer No.4 signaling bit 8 in Time Slot 30 in frame 16. Not valid for values which are not multiples of 8.
2 Mbit/s MVIP	Default Location (00H): Bit 1 in Time Slot 0. Each binary value allows the sync pulse to occur one bit earlier. For example, a count of 1 corrects for a sync pulse that occurs in bit 8 in Time Slot 31.
8 Mbit/s H-MVIP/H.100	Default Location (00H): Framer No.4 bit 8 in Time Slot 31, and framer No. 1 bit 1 in Time Slot 0 of next frame (4 clock cycles wide). Each binary value in increments of 8 allows the sync pulse to occur one time slot earlier. For example, a count of 8 corrects for a sync pulse that occurs in framer No.4 bit 8 in Time Slot 30 and framer No.1 bit 1 in Time Slot 31. Not valid for values which are not multiples of 8.
16 Mbit/s PCM Highway	Default Location (00H): Framer No.4 signaling bit 8 in Time Slot 31. Each binary value in increments of 8 allows the sync pulse to occur one time slot earlier. For example, a count of 8 corrects for a sync pulse that occurs in framer No.4 signaling bit 8 in Time Slot 30. Not valid for values which are not multiples of 8.

FRACTIONAL E1 CAPABILITY

When control bit FE1M (bit 0) in register X02H is set to a one, control bits HMVIP and MTP16M (bits 2 and 1) in register 06H are set to 0, and CONFIG1 (pin 43) is low (which place all the framers in 2 Mbit/s Transmission Mode) or high (which place all framers in 2 Mbit/s MVIP Mode) the receive and transmit signaling highway pins become gapped clock outputs. These pins are designated RFE1GCn and TFE1GCn. Individual per time slot control bits are provided for transmit and receive.

Control bits RFTS31-RFTS0 in registers X38H through X3BH, when set to one for E1 framer number n, generate a gapped clock on pin RFE1GCn with 8 clock pulses per selected time slot; the first falling edge of the gapped clock can be used to sample the first bit of the selected time slot. Figure 25 and Figure 26 show the timing details for both Receive Line Clock and System Clock options.

Control bits TFTS31-TFTS0 in registers X3CH through X3FH, when set to one for E1 framer number n, generate a gapped clock on pin TFE1GCn with 8 clock pulses per selected time slot; the first rising edge of the gapped clock occurs just before the first bit of the selected time slot. This permits a one clock cycle delay through an external device to prepare data to be sampled on the next rising edge of TCLKn. Figure 27 shows the timing details.

Control bit ENTSLB (bit 4) in register 0FFH must also be set to 0 since control bits TFTS31-TFTS0 are also used to control time slot loopbacks. The following table outlines the control options for fractional E1 and time slot loopbacks.

FE1M Bit 0, X02H	CONFIG1 Pin 43	HMVIP Bit 2, 006H	MTP16M Bit 1, 006H	ENTSLB Bit 1, 0FFH	System Interface	RSIGLn/ RFE1GCn	TSIGLn/ TFE1GCn	Mode
0	Low or high	0	0	0	2 Mbit/s Transmission or 2 Mbit/s MVIP	Signaling out	Signaling in	Normal
1	Low or high	0	0	0	2 Mbit/s Transmission or 2 Mbit/s MVIP	Gapped clock out	Gapped clock out	Fractional E1
0	Low or high	0	0	1	2 Mbit/s Transmission or 2 Mbit/s MVIP	Signaling out	Signaling in	Time Slot Loopback
1	Low or high	0	0	1	2 Mbit/s Transmission or 2 Mbit/s MVIP	Gapped clock out	Gapped clock out	Time Slot Loopback and Fractional E1

FRAMING

Frame Structure

The basic frame structure of the 2048 kbit/s E1 signal consists of thirty-two 8-bit time slots, or 256 bits, and has a duration of 125 microseconds (8,000 frames per second). Each time slot provides a 64 kbit/s channel. The thirty-two time slots are numbered 0 to 31, and the time slot bits are numbered 1 to 8. The first bit in a time slot to be received and transmitted is bit 1. Framing information is carried in Time Slot 0, and signaling information, if it is assigned for Channel Associated Signaling (CAS), is carried in Time Slot 16.

Framing information for aligning the E1 frame is carried in Time Slot 0, using a two-frame sequence that alternates for consecutive frames. Time Slot 0 in the first frame carries the frame alignment pattern of X0011011. The second frame carries the pattern of X1XXXXXX, so that bit 2 identifies the first and second frames. The other bits in Time Slot 0, which are designated as X and are not used for frame alignment, are assigned for national, alarm and international use. The following table illustrates the framing pattern and bit assignment for Time Slot 0 when assigned to carry the basic framing format.

Frame	Bit 1	2	3	4	5	6	7	8
1	Si (#1)	0	0	1	1	0	1	1
2	Si (#2)	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8

Where: Si is reserved for international use.
RAI is defined as a Remote Alarm Indication A-bit (true state is equal to 1).
Sa4-Sa8 bits are reserved for national use.

To provide additional framing protection against the emulation of a frame alignment pattern in the data stream, Time Slot 0 can be assigned to carry a 16-frame multiframe. The 16-frame multiframe carries a 001011 multiframe alignment pattern, CRC-4 check, and two E-bits in the bit 1 position of two sub-multiframes designated as SF I and SF II, as shown below:

Sub-F	Frame	Bit 1	2	3	4	5	6	7	8
SF I	0	C1	0	0	1	1	0	1	1
	1	0	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
SF II	8	C1	0	0	1	1	0	1	1
	9	1	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8

Where: C1-C4 are the CRC-4 bits.
RAI is defined as a Remote Alarm Indication A-bit (true state is equal to 1).
Sa4-Sa8 are reserved for national use.
E-bits are used for a CRC-4 error indication

Frame Alignment

The QE1F-*Plus* supports two frame alignment operating modes in each framer: basic frame alignment detection, and frame alignment detection with a CRC-4 validation. The receive framer circuit also employs an offline framing algorithm, where the payload is sent to the terminal side output even during loss of frame (together with RSYNC and RCLK, if these are framer outputs). This is advantageous, since re-framing usually occurs at the same frame position.

Basic frame alignment detection has two algorithms: Standard and Frame Hold-Off. The selection is determined by control bit BFAA (bit 5) in the Framer Configuration Register (X04H) for each framer. When control bit BFAA is written with a 0, the Standard algorithm is selected. When written with a 1, the Frame Hold-Off algorithm is selected. The Standard framing algorithm operates continuously according to the following steps:

- A valid frame alignment signal X0011011 is detected in Time Slot 0 of frame f (FAS frame).
- The absence of a frame alignment signal is verified by checking that bit 2 is a 1 in Time Slot 0 of frame f+1 (NFAS frame).
- A valid frame alignment signal X0011011 is detected in Time Slot 0 of frame f+2 (FAS frame).

If these criteria are met by three consecutive frames, then the framer is declared to be aligned. Thereafter, if any step fails at frame x, a new search for frame alignment is started in the next bit position of frame x. The Frame Hold-Off algorithm uses the same steps as found in the Standard frame alignment search, except that the new search is initiated in the next bit position in frame x+2.

The QE1F-*Plus* also supports frame alignment detection by validating a CRC-4 multiframe check sequence in addition to either of the basic frame alignment detection sequences. Each framer in the QE1F-*Plus* can be configured for two types of CRC-4 multiframe check: manual or an automatic mode. The manual mode is selected by writing a 0 to control bit CRCA (bit 3) in register X04H. In the manual mode, after frame alignment has been achieved, multiframe alignment occurs if two valid CRC multiframe signals are detected within 8 milliseconds (see table above). After CRC multiframe is established the QE1F-*Plus* begins checking the CRC bits. If multiframe cannot be achieved within the 8 millisecond period and control bit CRCA is set to a 1, a new search for frame alignment is initiated, and an Out Of CRC-4 Multiframe status indication (OOCRCM) is declared (bit 3 in register X1BH). When control bits CRCMD1 and CRCMD0 (bits 2 and 1) in register X04H are set to 10, an indication of CRC-4 multiframe alignment loss is sent to the distant end by setting the two E-bits in Time Slot 0 to zero.

The automatic mode is selected by writing a 1 to control bit CRCA (bit 3) in register X04H. If multiframe is not found by the process described above within a 400 millisecond search period, the framer assumes that the distant end is not configured for CRC multiframe pattern, and sets a status bit, NCRC4 (bit 7) in register X1BH. The QE1F-*Plus* then inhibits further CRC-4 processing. When control bits CRCMD1 and CRCMD0 (bits 2 and 1) in register X04H are set to 10, an indication of CRC-4 multiframe alignment loss is sent to the distant end by setting the two E-bits in Time Slot 0 to zero.

For ISDN applications (ITU-T I.431 or ETS 300 011), the automatic mode selected by writing a 1 to control bit CRCA (bit 3) in register X04H may be altered by setting control bit AAGS (bit 3) in global register 0FFH to a 1. The basic differences are that: 1) RAI in Time Slot 0 is set to a 1 if multiframe alignment is not found in the 8 millisecond period and then returned to 0 if basic frame alignment is still present and a new search is initiated; 2) The E-bits are set to a 1 and only reset to indicate CRC-4 errors once multiframe alignment has been achieved; and 3) The QE1F-*Plus* never stops searching for multiframe alignment. If multiframe alignment is not achieved in 100 to 500 milliseconds (status bit OOCRCM (bit 3) in register X1BH remains a 1) the control bit RAIE (bit 2) in register X07H should be set to a 1 until OOCRCM becomes a 0. For ETS 300 011 this sends a required remote alarm indication to the far end indicating failure to achieve multiframe alignment.

The CRC-4 pattern is checked, and an excessive CRC error indication ECRCE (bit 6) in register X1BH is set when 915 or more of the last 1000 CRCs were received in error. ECRCE is cleared after basic frame alignment is regained. The following table summarizes the control bits associated with selection of the frame alignment algorithm for one of the four framers

.

CRCMD1 X04H:2	CRCMD0 X04H:1	BFAA X04H:5	CRCA X04H:3	Action
0	0	X	X	Transparent (unframed mode). Frame alignment detector is bypassed. Please note that the slip buffers and signaling buffers are also disabled in this mode.
0	1	0	X	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are disabled.
0	1	1	X	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are disabled.
1	0	0	0	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zeros when the CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled, to count E-bit errors.
1	0	1	0	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zeros when the CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled, to count E-bit errors.
1	0	0	1	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. In addition, the receive 10-bit CRC counter is enabled. Transmit E-bits are sent as zero when CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled for counting E-bit errors.
1	0	1	1	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zero when CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled for counting E-bit errors.
1	1	0	0	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The E-bits are always transmitted as 1s, and the 10-bit E-bit performance counter is disabled.
1	1	1	0	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector is enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The E-bits are always transmitted as 1s, and the 10-bit E-bit performance counter is disabled.

CRCMD1 X04H:2	CRCMD0 X04H:1	BFAA X04H:5	CRCA X04H:3	Action
1	1	0	1	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. The E-bits are always transmitted as 1s. The CRC-4 counter is enabled.
1	1	1	1	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. The E-bits are always transmitted as 1s. The CRC-4 counter is enabled.

Loss Of Frame Alignment

An Out Of Frame (OOF) alarm is declared when a selected number of consecutive incorrect frame alignment patterns in Time Slot 0 is detected, or when 915 or more out of 1000 CRC-4 are received in error (ECRCE, bit 6 in register X1BH). The OOF alarm is indicated at bit 5 in register X10H. An incorrect frame alignment pattern is defined as an incorrect bit in at least one of the seven framing bits in an FAS Time Slot 0, or an error (i.e., a 0) in bit 2 in Time Slot 0 in the next (NFAS) frame. The number of incorrect frame alignment patterns in error is programmable using the OOF1 and OOF0 control bits (bits 7 and 6) in register X04H. The Out Of Frame alignment condition starts the resynchronization process for frame alignment. In addition, the software can also initiate a resynchronization of the frame alignment detector by writing a one to control bit RSYC (bit 0) in register X04H. The following table lists the selection options for declaring an Out Of Frame (OOF) alarm.

OOF1 X04H:7	OOF0 X04H:6	Action
0	0	Three consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0.
0	1	Four consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0.
1	0	Three consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0, or three consecutive incorrect bit 2 values of 0 in a NFAS Time Slot 0.
1	1	Four consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0, or four consecutive incorrect bit 2 values of 0 in a NFAS Time Slot 0.

Loss Of CRC-4 Multiframe Alignment

When the CRC-4 feature is enabled, a CRC-4 loss of multiframe indication OOCRCM (bit 3 in register X1BH) is generated when basic frame alignment is lost either by consecutive incorrect frame alignment patterns or by 915 or more out of 1000 CRC-4 received in error, as indicated by the OOF alarm, bit 5 in register X10H. The OOCRCM bit is cleared only when multiframe alignment is regained.

Transmit Framer

Each of the four transmit framers performs the following functions, unless the framer is configured for the transparent (unframed) mode of operation using the 2 Mbit/s Transmission Mode interface only:

- Generates the framing pattern (X0011011) in alternating (FAS) frames for Time Slot 0.

- Sets bit 2 to 1 in Time Slot 0 in (NFAS) frames not carrying the framing pattern.
- Inserts either the international bits for the basic format, or the CRC-4/E-bits into Time Slot 0.
- Inserts the national bits, and Remote Alarm Indication bit, into NFAS Time Slot 0.
- Inserts Time Slots 1-15 and 17-31 into the transmitted frame.
- Inserts Time Slot 16 as either a clear channel, or Channel Associated Signaling information.

The transparent mode is not valid for other system interface highway modes. These five modes require the slip buffers and framed mode to be enabled. Please note that when a framer is configured for the transparent mode, all the time slots in the frame are transmitted from the data bus transparently through the QE1F-*Plus*, bypassing the slip buffer.

Time Slot 0

The basic framed mode of operation is selected by writing control bits CRCMD1 (bit 2) and CRCMD0 (bit 1) in register X04H to 01. The selection is common to both the transmit and receive sides of a framer channel. The international bits from the transmit signaling highway are inserted into bit 1 of Time Slot 0, unless the CRC-4 feature is selected. The microprocessor can disable this path by writing a 0 to control bit TSIS (bit 7) in register X2CH, which freezes the values of the two international bits, located at bit 7 in registers X90H and XB0H, and allows them to be written by the microprocessor.

The CRC-4 framing mode is selected by writing control bits CRCMD1 (bit 2) and CRCMD0 (bit 1) in register X04H to 10 or 11. The insertion of the international bits from the signaling highway is disabled, and the transmit framer inserts the calculated CRC-4 value and the E-bits. The E-bit generation is internal to the framer within the QE1F-*Plus*, and is not accessible by the microprocessor in the transmit direction. When control bit AAGS (bit 3) in register 0FFH is set to a 1, one E-bit may be set to 0 immediately after the QE1F-*Plus* frames up even though the first CRC-4 is correct.

The CRC multiframe alignment pattern is generated by the framer. The Time Slot 16 (TS16) multiframe alignment pattern is generated only when either the CAS or CAS-inverted signaling types are selected (bits 7 and 6) in register X03H. TS16 multiframe alignment is meaningless in TS16 clear channel mode. TS16 multiframe alignment is independent of device mode.

The Remote Alarm Indication (RAI) A-bit is assigned to bit 3 in alternating frames in both the framed and CRC-4 mode of operation. When control bit AUTRAI (bit 6) in register X1AH is set to 1, a loss of frame alignment on the receive side sets the transmitted RAI bit to 1 for the duration of the alarm. The microprocessor can also write the state of the RAI bit, independent of automatic RAI insertion. When the microprocessor writes a 1 to control bit RAIE (bit 2) in register X07H, the RAI bit is transmitted as a 1. In addition, when control bit ENSRAI (bit 4) in register X00 is written with a 1, a 1 in bit RFI (bit 3) in Time Slot 0 from the signaling highway in the Transmission Mode only will also result in an RAI alarm being transmitted. The RAI alarm from the system highway is designated as a Remote Failure Indication (RFI).

The transmitted path for the individual national bits (Sa4 to Sa8) in Time Slot 0 in either framing mode can be assigned from the HDLC link or from the signaling highway. When control bit BNAL (bit 1) in register X01H is a 1, all the national bits are transmitted from the signaling highway via a buffer. The microprocessor can disable any of the national bits by writing a 0 to one more control bits TSA4S-TSA8S (bits 4-0) in register X2CH and insert the software values for Sa4-Sa8 into the transmitted bits by writing the values to bits 4-0 in register XB0H. This is the recommended method of fixing the Sa bits to a specific value per G.704. When control bit BNAL is written with a 0, the transmitted path will be either via the data link or via the signaling highway through the buffer. The bandwidth of the HDLC channel is controlled by control bits SA4-SA8 (bits 4-0) in register X0CH. A 1 written to one or more bits selects those bits as the HDLC channel. For example, if control bits SA4-SA7 are set with a 1, then bits Sa4 to Sa7 in Time Slot 0 will transmit the HDLC channel. The Sa8 bit Time Slot 0 path will be from the signaling highway via the buffer. When a 1 is written to control bits SA4-SA8 and control bit BNAL is set to a 0, HDLC flag characters are continuously sent in the national bits selected regardless of the setting of control bit EHT (bit 6) in register X08H.

The seven-bit framing pattern (X0011011) in alternating (FAS) frames for Time Slot 0, and the 1 value for bit 2

in Time Slot 0 in (NFAS) frames not carrying the framing pattern (X1XXXXXX), are generated by the framer.

Each framer also has the capability of generating framing pattern errors in FAS frames, Bit 2 errors in alternating (NFAS) frames, and CRC-4 errors. When control bit FASE (bit 3) in register X07H is set to 1, the transmitter sends the frame alignment pattern (in FAS Time Slot 0 in alternating frames) in error continuously. All the bits in the frame alignment sequence are inverted (X0011011 becomes X1100100). The frame alignment sequence error condition is transmitted until this bit is written with a 0. When control bit NFASE (bit 4) in X06H is set to 1, the transmit framer sends bit 2 (in NFAS Time Slot 0 in alternating frames) as a 0. Bit 2 in Time Slot 0 of the NFAS frames is transmitted in error as a 0 until this bit is written with a 0. When control bit CRC (bit 4) in register X07H is set to 1, the CRC-4 bits in Time Slot 0 are transmitted in the inverted state once. To send another CRC-4 error, this bit must be first written with a 0, and then a 1.

Time Slot 16

Time Slot 16 may be assigned for Channel Associated Signaling or as a clear channel. Different modes of Channel Associated Signaling are selected when control bits TYP1 and TYP0 (bits 7 and 6) in register X03H are equal to 01, 10, or 11. When control bits TYP1 and TYP0 are equal to 00, Time Slot 16 is designated as a clear channel, and the transmitted path is from the data bus. The selection is common for the receive side of the same framer (n = X).

Channel Associated Signaling is inserted into Time Slot 16 of the transmitted frame from the signaling highway via buffer locations when the buffer is enabled, or directly from the signaling highway when it is bypassed (2 Mbit/s Transmission Mode Option only). The buffer location for reading the multiframe pattern, spare bits, and multiframe alarm is register XD0H. The buffer locations for the ABCD bits of the signaling channels are registers XD1H through XDFH. The signaling channel (i.e., ABCD signaling bits) states can be frozen by writing a 1 to control bit TXF (bit 4) in register X03H. The contents of an individual signaling channel (C = 1-30) in buffer locations XD1H through XDFH can be frozen by writing a 0 to one or more of control bits SE1-SE30 in registers XE8-XEBH. When signaling channel c is frozen, the transmitted signaling state is the value sitting in the buffer at the time the SEc bit was set to 0. The microprocessor can write a new signaling state, or a service code, for the frozen channel.

Frame 0 in the 16-frame multiframe carries the 4-bit multiframe pattern, 3 spare bits, and the remote multiframe alarm. The QE1F-*Plus* regenerates the multiframe alignment pattern. These bits from the signaling highway can be read by the microprocessor in register XD0H. However, the value sitting in the transmit signaling buffer cannot be frozen, and a new value substituted for it. A loss of multiframe alignment will result in a remote multiframe alarm being transmitted when control bit AUTY (bit 7) in register X1AH is a 1. In addition, the microprocessor can also generate a remote multiframe alarm by writing a 1 to control bit TS16YE (bit 5) in register X06H.

Time Slots 1-15 and 17-31

The Time Slots 1-15 and 17-31 are inserted into the transmitted frame from the slip buffer when it is enabled, or directly from the data highway when it is bypassed (2 Mbit/s Transmission Mode only). The slip buffer locations are registers X91H - XAFH (frame 1) and XB1H - XCFH (frame 2). An individual time slot in the buffer can be frozen by writing a 0 to one or more control bits TDE1-TDE31 in registers XE4H - XE7H. This permits the microprocessor to write idle or service codes for one or more framers.

Fast Sync Mode

The QE1F-*Plus* provides a fast sync mode which may be used for testing purposes. The fast sync mode for the receiver side is selected when control bit RXFS (bit 1) in register X06H is written with a 1 in the NRZ mode. A pulse that is one clock cycle wide in bit position 256 of the last frame in the CRC-4 multiframe forces the framer into synchronization. It can occur repetitively at 2 ms intervals, or it can be pulsed once provided the received framing sequence is valid afterwards.

The fast sync mode for the transmitter side is selected when control bit TXFS (bit 0) in register X06H is written

with a 1 in the NRZ mode. The TFSn output in this mode is a one clock cycle wide pulse in bit position 256 of the last frame in the CRC-4 multiframe that occurs every 2 ms. This allows an external device to be synchronized to the QE1F-*Plus* framer.

Slip Buffers

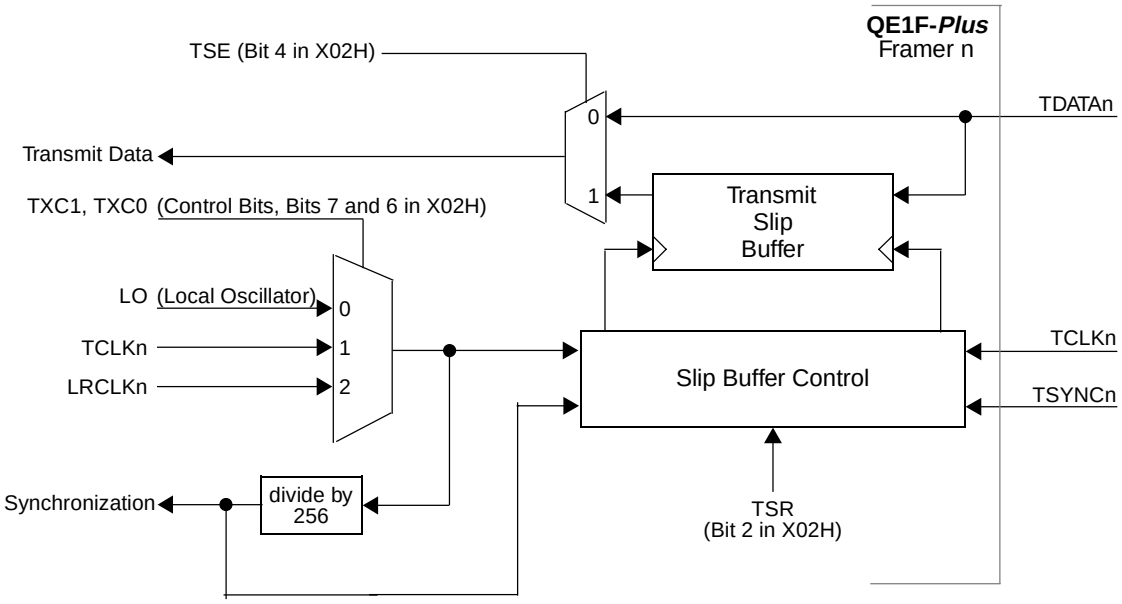
Each framer contains a two-frame slip buffer in both the transmit and receive data directions. Either of the slip buffers can be bypassed, if required, in the 2 Mbit/s Transmission Mode only. The slip buffers must be enabled in the 2 Mbit/s MVIP Mode, the 8 Mbit/s H-MVIP/H.100 Mode, the 16 Mbit/s PCM Highway Mode, and the 8 Mbit/s and 16 Mbit/s Transmission Modes. Only the transmit and receive data time slots (Time Slots 1-15 and 17-31) are passed through the slip buffers. Channel 16 may also be present in the slip buffer when it assigned as a clear channel. The signaling channel in Time Slot 16 and selected bits in Time Slot 0 are buffered in a separate memory location and are not subjected to slips. Each buffer is organized as a circular queue two frames in length. At this point, if data is arriving faster than it is being removed, the buffer will begin to fill.

Before the buffer becomes totally full, a controlled slip will occur and one frame of data will discarded. This is accomplished by moving the write pointer back one frame and overwriting the previous frame that was written. If, after recentering, the data is being removed faster than it is arriving, the buffer will begin to empty. Before the buffer becomes completely empty, a controlled slip occurs in the opposite direction, and a frame of data is added to the buffer. This is accomplished by moving the read pointer back one frame and repeating the last frame sent. Each buffer may be manually recentered by setting the TSR or RSR control bits (bit 2 and 1) in the Framer Clock Control register X02H.

The transmit slip buffer is used to absorb low speed jitter in the transmit direction. The transmit slip buffer is enabled by writing a 1 to control bit TSE (bit 4) in the Framer Clock Control register X02H. When enabled, time slots are written into the transmit slip buffer by the system clock (TCLKn), and read out by the recovered receive clock (LRCLKn) or the local oscillator (LO). Control bits TXC1 and TXC0 (bits 7 and 6) in X02H select the clock source. The time slots (t = 1-31) from the transmit data bus are written into the slip buffer when their respective enable bits (TDEt) in registers XE4H, XE5H, XE6H, and XE7H are written with a 1.

A phase shift between the two clocks is detected, and the deletion or repetition of one frame of data (31 time slots, or 30 time slots if Time Slot 16 signaling is enabled) occurs if the buffer reaches an almost full or almost empty threshold. A transmit slip error is indicated by status bit TXSLIP (bit 1) in register X10H, with a latched event LTXSLIP (bit 1) indicated in X11H. The transmit slip buffer status is indicated by reading status bits TXS1 and TXS0 (bits 7 and 6) in register X14H.

The individual time slots in both frames can be accessed by the microprocessor, as well as written by the microprocessor in place of data. When a time slot enable control bit in register location XE4-XE7H is written with a 0, the content of the two-frame slip buffer location is frozen. The microprocessor can write an idle or service code to be transmitted to the line. The transmit slip buffer data locations are X91H (Time Slot 1) to XAFH (Time Slot 31) for frame 1, and XB1H (Time Slot 1) to XCFH (Time Slot 31) for frame 2. Please note that both buffer locations (i.e., frame 1 and frame 2) must be written with the service or idle code. A simplified schematic of the transmit slip buffer is shown in Figure 52.



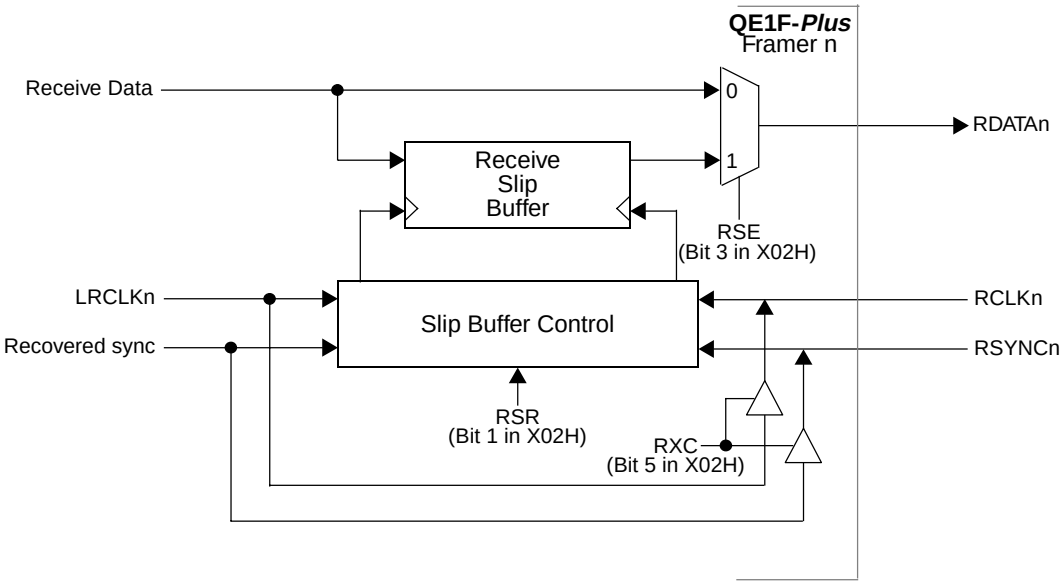
Note: n is the framer number (1, 2, 3, 4)

Figure 52. Transmit Slip Buffer

The receive buffer is used when the receive clock (RCLKn) is provided from an external source. The receive slip buffer controls the time slot access and retiming, providing a two-frame buffer that is optionally bypassable in the 2 Mbit/s Transmission Mode only. The slip buffer must be enabled in the other system highway modes. Time slots from the line interface are written into the slip buffer by the recovered receive clock (LRCLKn), and read out by the system clock (RCLKn). A phase shift between the two clocks is detected, and deletion or repetition of one frame of data (31 time slots, or 30 time slots if Time Slot 16 signaling is enabled) occurs if the buffer reaches an almost full or almost empty threshold. The time slots from the receive line signal are written into the slip buffer when their respective enable bits (RDEn) in registers XE0H, XE1H, XE2H, and XE3H are written with a 1.

Individual time slots can be accessed by the microprocessor, and they can be written by the microprocessor in place of data. When a time slot enable control bit in register location XE0-XE3H is written with a 0, the content of the two-frame slip buffer location is frozen. The microprocessor can write an idle or service code in the location that will be transmitted to the receive data highway. The receive slip buffer data locations are X41H (Time Slot 1) to X5FH (Time Slot 31) for frame 1, and X61H (Time Slot 1) to X7FH (Time Slot 31) for frame 2. Please note that both buffer locations (i.e., frame 1 and frame 2) must be written with the service or idle code. A simplified schematic of the receive slip buffer is shown in Figure 53.

A receive slip error is indicated by status bit RXSLIP (bit 0) in register X10H, with a latched event LRXSLIP (bit 0) indicated in X11H. The receive slip buffer status is indicated by reading status bits RXS1 and RXS0 (bits 5 and 4) in register X14H.



Note: n is the framer number (1, 2, 3, 4)

Figure 53. Receive Slip Buffer

THROUGHPUT DELAY

Delay through the QE1F-*Plus* is a function mainly of the slip buffers, though other factors also influence the amount of delay. The table below gives the typical delay for different elements of the framer from line to system and from system to line. All numbers are in bit times for a clock rate of 2048 kHz (i.e., 488 ns). To estimate the total delay through a framer, add the system interface delay to the slip buffer delay and the codec delay (choose NRZ, AMI or HDB3 value) and the framing mode delay, and then multiply by 488 ns.

Direction of Signal Flow	System Interface	Slip Buffer (select one)		Codec (select one)			Framing Mode (select one)	
		Disabled	Enabled	NRZ	AMI	HDB3	Framed Modes	Transparent Mode
Line to System RPOSn/RLDATn to RDATAn	0.5	1	8 to 504 (Note 1)	0	0	2	2.5	0
System to Line TDATAn to TPOSn/TLDATn	0.5	0	8 to 504 (Note 2)	0	0	2	6	0.5

Notes:

1. When the framer is reset, the nominal delay is 128 bits through the slip buffer. Recenter (control bit RSR toggled) will cause a slip if the delay exceeds 384 bits, to minimize the delay.
2. When the framer is reset, the nominal delay is 128 bits through the slip buffer. Recenter (control bit TSR toggled) will cause a slip if the delay exceeds 384 bits, to minimize the delay.

SIGNALING

There are two types of signaling schemes used for the E1 telephone channels: Common Channel Signaling (CCS), and Channel Associated Signaling (CAS). Common Channel Signaling, such as CCS No. 7, can be assigned to be carried in one or more of the time slots, including Time Slot 16. The QE1F-*Plus* does not process any part of the Common Channel Signaling format. Instead, it is passed transparently through the system to the data bus. The clear channel capability for Time Slot 16 is selected when control bits TYP1 and TYP0 (bits 7 and 6) in register X03H are written with 00.

Time Slot 16 may be used to carry Channel Associated Signaling. The Channel Associated Signaling feature is selected when control bits TYP1 and TYP0 (bits 7 and 6) in register X03H are written with a value other than 00. The signaling information is carried as ABCD signaling bits that are associated with Time Slots 1 through 15, and 17 through 31. A sixteen-frame format, referred to as a signaling multiframe, is used to carry the signaling information. Please note that the signaling multiframe is arbitrary with respect to the multiframe structure carried in Time Slot 0. The following table shows the signaling multiframe structure for Time Slot 16.

Frame	Bit 1	2	3	4	5	6	7	8
0	0	0	0	0	X0	Y	X1	X2
1	A1	B1	C1	D1	A16	B16	C16	D16
2	A2	B2	C2	D2	A17	B17	C17	D17
3	A3	B3	C3	D3	A18	B18	C18	D18
4	A4	B4	C4	D4	A19	B19	C19	D19
5	A5	B5	C5	D5	A20	B20	C20	D20

Frame	Bit 1	2	3	4	5	6	7	8
6	A6	B6	C6	D6	A21	B21	C21	D21
7	A7	B7	C7	D7	A22	B22	C22	D22
8	A8	B8	C8	D8	A23	B23	C23	D23
9	A9	B9	C9	D9	A24	B24	C24	D24
10	A10	B10	C10	D10	A25	B25	C25	D25
11	A11	B11	C11	D11	A26	B26	C26	D26
12	A12	B12	C12	D12	A27	B27	C27	D27
13	A13	B13	C13	D13	A28	B28	C28	D28
14	A14	B14	C14	D14	A29	B29	C29	D29
15	A15	B15	C15	D15	A30	B30	C30	D30

Where: Ac, Bc, Cc, Dc represent the signaling information associated with the telephone channel number (c = 1-30). Channel 1 corresponds to Time Slot 1, while channel 16 corresponds to Time Slot 17, since Time Slot 16 is assigned to carry the signaling information.

The Y-bit is used for a multiframe alarm indication. A 1 indicates an alarm.

The X0, X1 and X2 spare bits are not used, and are normally set to 1.

Channel Associated Signaling Multiframe Alignment

The QE1F-*Plus* supports two CAS multiframe alignment operating modes for each framer: Standard, or Enhanced. The Standard algorithm is selected by writing a 0 to control bit CASA (bit 4) in register X04H. The Enhanced algorithm is selected when a 1 is written to the control bit CASA. The Standard multiframe alignment algorithm is compatible with ITU-T Recommendation G.732. Standard Channel Associated Signaling multiframe alignment is declared when the QE1F-*Plus* detects a 0000 pattern in bits 1 to 4 in Time Slot 16 and this was preceded by a Time Slot 16 with a non-zero pattern in bits 1-4. For the Enhanced algorithm, multiframe alignment is declared only when the 0000 pattern is found after the previous 15 frames contained a Time Slot 16 that did not carry the 0000 pattern in bits 1-4.

The status bit TS16ME (bit 4) in register X1BH is assigned for a multiframe error indication for each framer. When a 1 is written to control bit ENOO16M (bit 2) in register X1AH, TS16ME is used to provide unlatched and latched status indications at OOMF (bit 2) in register X10H and LOOMF (bit 2) in register X11H. The TS16ME status indication is set when any of the following conditions occurs:

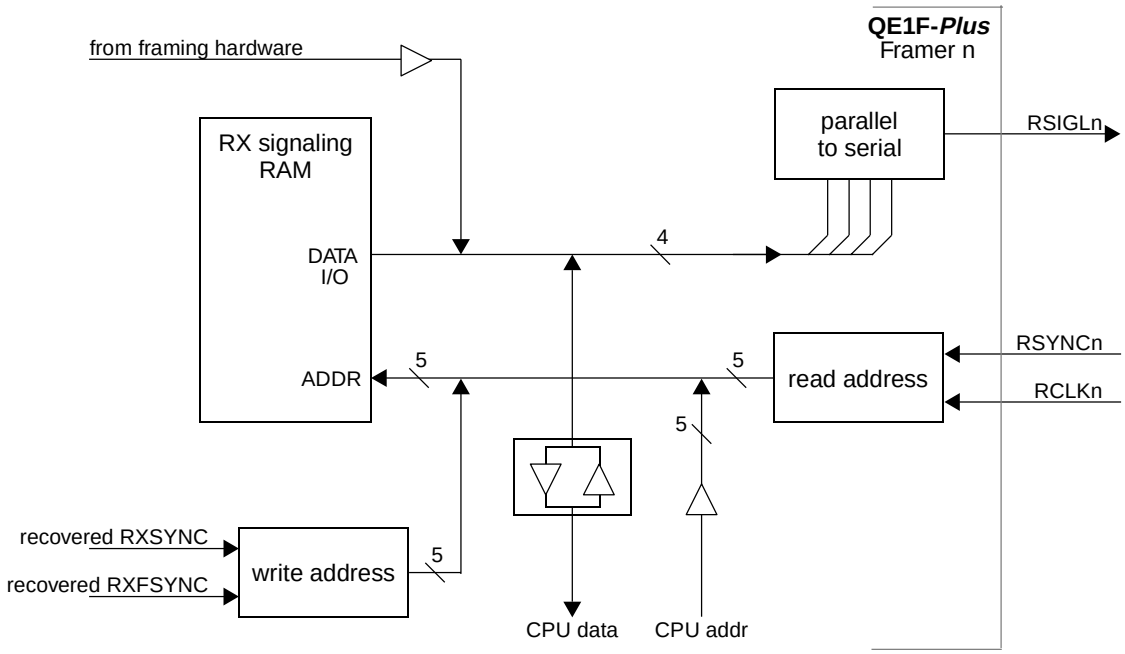
- The 4-bit all zero pattern (bits 1-4) in Time Slot 16 is lost for two consecutive multiframes.
- Time Slot 16 is all zeros for 16 consecutive frames.
- Frame alignment is lost (OOF alarm)

Control bits TYP1 and TYP0 (bits 7 and 6) in register X03H may be written to 01, to prevent the far end framer from falsely achieving CAS multiframe alignment if signaling bits Ac Bc Cc Dc = 0000. The QE1F-*Plus* will automatically replace the 0000 code with 1111 prior to insertion into Time Slot 16 for transmission.

Signaling Buffers

120-bit transmit and receive signaling buffers are used to interface the QE1F-*Plus* to the system. In the receive direction, the signaling bits are extracted from the data stream and placed in the receive signaling buffer after the multiframe sequence is detected in the receive framer block. A simplified schematic of the receive signal-

ing buffer is shown in Figure 54. In the 2 Mbit/s, 8 Mbit/s and 16 Mbit/s Transmission Modes, eight signaling bits are sent each frame. Receive signaling bits are clocked out by the system clock (RCLKn), which is sourced by either the system or the QE1F-*Plus*. The signaling bits on RSIGLn are sent such that they will meet the system requirements for formatting a Tributary Unit (TU) in an SDH format in the next multiframe. These bits can be extracted using the receive sync signal RSYNCn. In the 2 Mbit/s MVIP Mode, the 8 Mbit/s H-MVIP/ H.100 Mode and the 16 Mbit/s PCM Highway Mode, all the signaling bits are sent for every framer every frame (125 microseconds) from the receive signaling buffer by using the system clock (RCLKn) and sync pulse (RSYNCn).



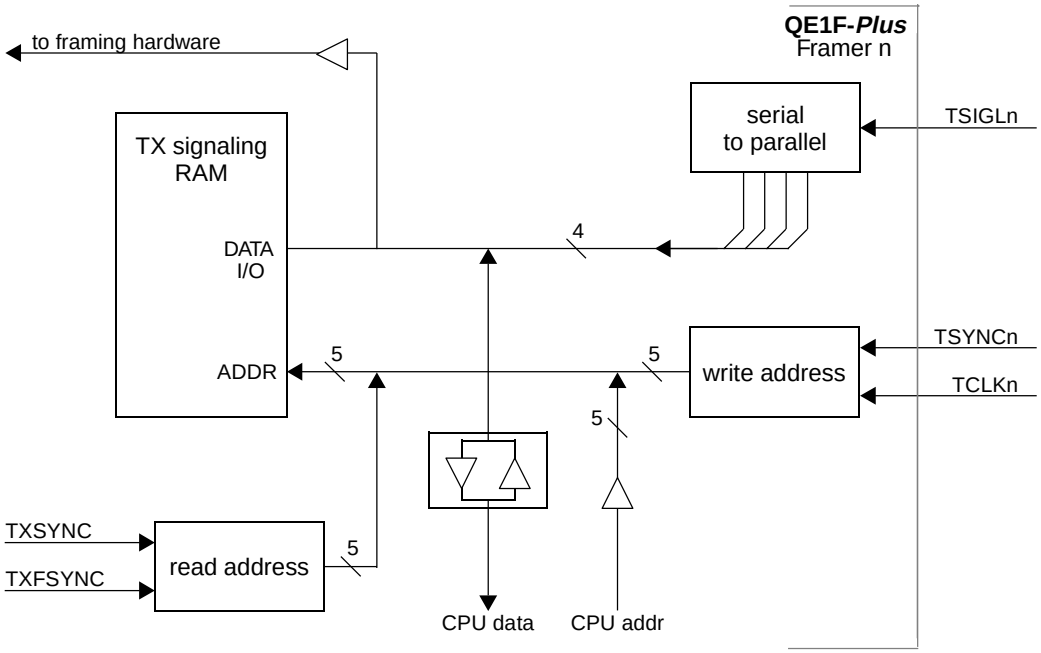
Note: n is the framer number (1, 2, 3, 4)

Figure 54. Receive Signaling Buffer

The received signaling bits are stored sequentially in the receive signaling buffer in the order they are received. The storage sequence starts with 0 0 0 0 X0 Y X1 X2 (in X80H), followed by A1 B1 C1 D1 A16 B16 C16 D16 (in X81H) and so on, ending with A15 B15 C15 D15 A30 B30 C30 D30 (in X8FH). The signaling bits in the receive signaling buffer (register locations X80H-X8FH) may be read at any time by the microprocessor in order to monitor the signaling states, or to modify the outgoing values. Since the buffer is accessed by multiple asynchronous processes, the read and write cycles for the signaling buffer are synchronous to the internal clocks. Simultaneous accesses are serviced sequentially. The priority of service depends on the amount of latency acceptable between when the request was received and when the data is required to be available. When the corresponding (receive and transmit) signaling enable bits (SE1-SE30 bits) in register locations XE8H (channels 1 - 8), XE9H (channels 9 - 16), XEAH (channels 17 - 24), and XEBH (channels 25 - 30) are written with a 1, the signaling bits are sent on the signaling highway (and data highway) in Time Slot 16. For example, a 1 written to control bit SE1 enables the signaling bits for channel 1 to be written into the signaling buffer. When a 0 is written into control bit SE1, the signaling buffer for channel 1 signaling is frozen. The frozen states will be sent on the signaling highway until the SE1 bit is written with a 1 or the microprocessor writes a new value into bits A1B1C1D1 (bits 7-4) in register location X81H. The hex value written into register X81H for bits 3-0 (signaling for A16 B16 C16 D16) will be ignored by the QE1F-*Plus* unless the SE16 bit is set to 1.

The signaling bits in the receive direction are automatically frozen in their present states when loss of signal or loss of synchronization occurs. A signaling freeze may also be initiated manually by writing a 1 to control bit RXF (bit 5) in register X03H. A receive signaling freeze indication is given by status bit RXSF (bit 7) in register X15H.

A simplified schematic of the transmit signaling buffer is shown in Figure 55. Transmit signaling bits on the signaling pin TSIGLn are clocked into the transmit signaling buffer using the transmit system clock TCLKn and sync pulse TSYNCn. In the 2 Mbit/s, 8 Mbit/s, and 16 Mbit/s Transmission Modes, eight signaling bits are provided each frame. In the 2 Mbit/s MVIP Mode, the 8 Mbit/s H-MVIP/H.100 Mode and the 16 Mbit/s PCM Highway Mode, all signaling bits are exchanged for every channel every frame (125 microseconds).



Note: n is the framer number (1, 2, 3, 4)

Figure 55. Transmit Signaling Buffer

The transmit signaling bits from the signaling highway are stored sequentially in the transmit signaling buffer in the order they are received. The storage sequence starts with 0 0 0 0 X0 Y X1 X2 (in XD0H), A1 B1 C1 D1 A16 B16 C16 D16 (in XD1H) and so on, ending with A15 B15 C15 D15 A30 B30 C30 D30 (in XDFH). The signaling bits in the transmit signaling buffer (register locations XD0H-XDFH) may be read at any time by the microprocessor in order to monitor the signaling states, or to modify the outgoing values. Since the buffer is accessed by multiple asynchronous processes, the read and write cycles for the signaling buffer are synchronous to the internal clocks. Simultaneous accesses are serviced sequentially. The priority of service depends on the amount of latency acceptable between when the request was received and when the data is required to be available. When the corresponding signaling enable bits (SE1-SE30 bits) in register locations XE8H (channels 1 - 8), XE9H (channels 9 - 16), XEAH (channels 17 - 24), and XEBH (channels 25 - 30) are written with a 1, the signaling bits are written into the transmit signaling buffer. For example, a 1 written to control bit SE1 enables the signaling bits from the signaling highway for channel 1 to be written into the signaling buffer. When a 0 is written into control bit SE1, the signaling buffer for channel 1 signaling is frozen. The frozen states will be transmitted until the SE1 bit is written with a 1 or the microprocessor writes a new value into bits A1B1C1D1 (bits 7-4) in register XD1H. The hex value written into register XD1H for bits 3-0 (signaling for A16 B16 C16 D16) is ignored by the QE1F-*Plus* unless the SE16 bit is set to 1. The actual generation of the Y-bit to the transmit line is activated by [TS16YE or (OOMF and AUTY)] where TS16YE is bit 5 of X06H, OOMF is the detection of loss of multiframe (bit 2 of register X10H) and AUTY is bit 7 of X1AH.

A transmit signaling freeze indication occurs when control bit TXF (bit 4) in register X03H is written with a 1 (manual freeze), or when AIS is detected on the signaling highway (2 Mbit/s, 8 Mbit/s, and 16 Mbit/s Transmission Modes only). A transmit signaling freeze indication is given by status bit TXSF (bit 6) in register X15H.

CLOCKING AND SYNCHRONIZATION

The clocking and synchronization portion of the QE1F-*Plus* includes the receive clock configuration, transmit clock synchronization, and the slip buffers for each of the framers. The following table provides a summary of the RCLKn clock operation in the receive direction (RCLK1 above 2 Mbit/s).

Interface Mode	Clock Rate	Sync Edge In	Data/Sig Edge Out	Comments
2 Mbit/s Trans.	2.048 MHz	Pos.	Neg.	Clock and sync pulse may be outputs. The RCLKn clock is derived from the recovered received clock (LRCLKn). See Note.
8 Mbit/s Trans.	16.384 MHz	Pos.	Neg.	System clock and sync pulse must be inputs.
16 Mbit/s Trans.	16.384 MHz	Pos.	Neg.	System clock and sync pulse must be inputs. Signaling highway is not used.
2 Mbit/s MVIP	2.048 MHz	Pos.	Pos.	System clock and sync pulse must be inputs.
8 Mbit/s H-MVIP/H.100	16.384 MHz	Pos.	Neg.	System clock and sync pulse must be inputs.
16 Mbit/s PCM	16.384 MHz	Pos.	Neg.	System clock and sync pulse must be inputs. Signaling highway is not used.

Note: Control bit RXC (bit 5) in the Framer Clock Control Register X02H configures RCLKn as an input or output for each of the framers. In the 8 Mbit/s and 16 Mbit/s Transmission Modes, the 2 Mbit/s MVIP Mode, the 8 Mbit/s H-MVIP/H.100 Mode and the 16 Mbit/s PCM Highway Mode, the system clock must be an input.

In the transmit direction, the system clock TCLKn and sync pulse TSYNCn are always inputs to the QE1F-*Plus*. The transmit data TDATAn is clocked out of the slip buffer by either the transmit system clock (TCLKn), the local oscillator input (LO), or the recovered receive clock (LRCLKn). The clock selection for each framer is controlled by TXC1 (bit 7), and TXC0 (bit 6) in Framer Clock Control Register X02H. The local oscillator input (LO) has a nominal frequency of 2.048 MHz.

The following table provides a summary of the TCLKn clock operation in the transmit direction (TCLK1 above 2 Mbit/s).

Interface Mode	Clock Rate	Sync Edge In	Data/Sig Edge In	Comments
2 Mbit/s Trans.	2.048 MHz	Pos.	Pos.	
8 Mbit/s Trans.	16.384 MHz	Pos.	Pos.	
16 Mbit/s Trans.	16.384 MHz	Pos.	Pos.	Signaling bus is not used.
2 Mbit/s MVIP	2.048 MHz	Pos.	Neg.	
8 Mbit/s H-MVIP/H.100	16.384 MHz	Neg.	Pos.	
16 Mbit/s PCM	16.384 MHz	Pos.	Pos.	Signaling bus is not used.

Clock Reference

For system applications that require the recovered receive clock, the QE1F-*Plus* can provide two reference clocks derived from any of the four clock inputs (LRCLKn), when enabled. The recovered receive clock input LRCLKn that is used to derive the reference clock CLKREF1 (pin 46) is determined by the value written to con-

trol bits CR1S1 and CR1S0 (bits 1 and 0) in the Clock Reference Selection Register (019H). The recovered receive clock that is used to derive the reference clock CLKREF2 (pin 2) is determined by the value written to control bits CR2S1 and CR2S0 (bits 7 and 6) in the Clock Reference Selection Register (019H).

The following table lists the various conditions for enabling/disabling the clock reference signal on the CLKREF1 pin. The ENREF1 and 2048KHZ control bits are located at bits 3 and 4 in the Clock Reference Selection Register (019H). The LIE control bit is located in the Frame Configuration Register (X00H). The LOS alarm status bit (bit 7) is located in the E1 Status Register (X10H).

ENREF1 (Control)	LOS(n) (Alarm)	LIE(n) (Control)	2048KHZ (Control)	Action
0	X	X	X	CLKREF1 pin tri-stated.
1	0	0	0	8 kHz Reference provided on CLKREF1. The 8 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	0	0	1	2048 kHz Reference provided on CLKREF1. The 2048 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	1	X	X	CLKREF1 pin is forced low.
1	X	1	X	CLKREF1 pin is forced low when LINTn is in the active true state.

Note: X can be either state.

The following table lists the various conditions for enabling/disabling the clock reference signal on the CLKREF2 pin. The ENREF2 and 2048KHZ control bits are located at bits 5 and 4 in the Clock Reference Selection Register (019H). The LIE control bit (bit 1) is located in the Frame Configuration Register (X00H). The LOS alarm status bit (bit 7) is located in the E1 Status Register (X10H).

ENREF2 (Control)	LOS(n) (Alarm)	LIE(n) (Control)	2048KHZ (Control)	Action
0	X	X	X	CLKREF2 pin tri-stated.
1	0	0	0	8 kHz Reference provided on CLKREF2. The 8 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	0	0	1	2048 kHz Reference provided on CLKREF2. The 2048 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	1	X	X	CLKREF2 pin is forced low.
1	X	1	X	CLKREF2 pin is forced low when LINTn is in the active true state

Note: X can be either state.

AIS DETECTION AND GENERATION

Both frame AIS and Time Slot 16 AIS are detected in the received E1 line signal. A line AIS is detected when the received line signal has two or less zeros in each of two consecutive double-frame periods (512 bits). Recovery occurs when each of two consecutive double-frame periods contains three or more zeros after frame alignment has been detected. The status of line AIS is given by the LINEAIS status bit (bit 0) in register X1BH.

An AIS in Time Slot 16 is detected when the received time slot has three or less zeros in each of two consecutive multiframe periods. Recovery occurs when each of two consecutive multiframe periods contains four or more zeros or when the multiframe alignment signal has been detected. The status of Time Slot 16 AIS is given by the TS16AIS status bit (bit 1) in register X1BH.

Two enable bits are provided for or-gating the line AIS and Time Slot 16 AIS status bits together to provide unlatched and latched AIS indications, and an interrupt when the associated mask bit is 0. Control bit ENLAIS (bit 0) in X1AH enables a line AIS alarm. Control bit E16AIS (bit 1) in X1AH enables a Received Time Slot 16 AIS alarm.

The QE1F-*Plus* also provides control bits and enable bits for alarms to generate AIS for the receive highway. When control bit STUAIS (bit 6) in register X07H is written with 1, the AIS, OOF and LOS alarms, if enabled by their respective ENAIS (bit 2), ENOOF (bit 1), and ENLOS (bit 0) control bits in the Signaling and Time Slot Control register X03H, cause the generation of AIS according to the following table. The table reflects the AIS actions taken on Out Of Frame (OOF) alarm when enabled by ENOOF and STUAIS. Control bits ENAIS for AIS and ENLOS for loss of signal function in the same manner. Please note that the microprocessor can force AIS to be generated for the receive data highway independent of the three control bits by writing a 1 to control bit SYSALL1 (bit 5) in register X07H.

Transmission Modes (2 Mbit/s, 8 Mbit/s and 16 Mbit/s)

ENOOF	STUAIS	Action
0	0	Normal operation. No AIS generated on signaling or data highway.
0	1	Normal operation. No AIS generated on signaling or data highway.
1	0	AIS generated only on signaling highway when OOF alarm is detected. A-bits are equal to 1.
1	1	AIS generated on signaling and data highways when OOF alarm is detected. A-bits on the signaling highway are equal to 1.

2 Mbit/s MVIP Mode, 8 Mbit/s H-MVIP/H.100 Mode and 16 Mbit/s PCM Highway Mode

ENOOF	STUAIS	Action
0	0	Normal operation. No AIS generated on data highway.
0	1	Normal operation. No AIS generated on data highway.
1	0	Normal operation. No AIS generated on data highway when OOF alarm is detected.
1	1	AIS generated on data highway when OOF alarm is detected.

In the transmit direction, from the transmit highway to the line, line AIS and Time Slot 16 AIS can be generated. When the microprocessor writes a 1 to control bit AIS16 (bit 7) in register X07H, the all ones AIS pattern is transmitted in Time Slot 16 continuously until the control bit is written with a 0. When the microprocessor writes a 1 to control bit AISE (bit 1) in register X07H, the all ones AIS pattern is transmitted in all the time slots of the frame continuously until the control bit is written with a 0. When the microprocessor writes a 1 to control bit ENSAIS (bit 2) in register X00H, in the Transmission Modes only, the all ones AIS pattern is transmitted in all time slots of the frame when the A-bits in the signaling highway are detected as ones. In addition, a status bit TUAIS (bit 3) in register X14H indicates when the A-bits are set to 1 in the Transmission Modes. The following table summarizes the various enable bits and actions for generating AIS in the transmit direction.

Transmit AIS Generation

ENSAIS	AIS16	AISE	Action
0	0	0	Normal operation.
X	X	1	AIS generated. All ones inserted into all time slots.
0	1	0	AIS generated for Time Slot 16. All ones inserted into Time Slot 16.
1	X	X	AIS generated when the A-bits in the transmit signaling highway are equal to ones in the Transmission Modes. All ones inserted into all time slots.

HDLC CHANNEL

A HDLC message frame is composed of four parts: an opening flag, the message (which consists of multiple bytes), a two-byte CRC-16 frame check sequence, and a closing flag, as shown in Figure 56 below.

Bit	8	7	6	5	4	3	2	1
Opening Flag	0	1	1	1	1	1	1	0
Message	Address and Control Information							
CRC-16								
Closing Flag	0	1	1	1	1	1	1	0

Figure 56. HDLC Format

The opening and closing flags are represented by a single, unique 8-bit character defined as 01111110, which contains six contiguous ones. To avoid the occurrence of a false flag within the data stream, a zero is inserted (stuffed) after each string of five contiguous ones in the message or CRC-16. Reception of more than six contiguous ones is interpreted as a frame abort sequence. When an abort sequence is received, the remainder of the current frame is ignored and the received portion is discarded as an invalid frame. A two-byte CRC-16 frame check sequence is computed across the contents of the message (after the opening flag), and appended to the end of the message. The time between consecutive frames is filled with one or more flags. When two or more flags occur in sequence, they may share the boundary zero between them (011111101111110).

A 16-byte FIFO is provided in each direction for each framer, which permits short messages to be transmitted and received without having the microprocessor service the FIFOs during message reception. For long messages, interrupts and status information are provided to facilitate FIFO servicing by the microprocessor. For both short and long messages, the HDLC controller performs the following functions:

- Zero bit stuffing/destuffing (11111 to 111110 / 111110 to 11111)
- ITU-T CRC-16 generation/checking (16-bit sequence)
- Flag generation/detection (01111110)
- Abort generation/detection (01111111...)
- Start of frame detection
- End of frame detection
- FIFO overflow and underflow

The bandwidth of the HDLC channel is determined by the spare bits in Time Slot 0. The five spare bits, labeled Sa4-Sa8, in bit positions 4-8 of Time Slot 0 in alternating (NFAS) frames that do not carry the frame alignment sequence, each have a bandwidth of 4 kbit/s. Any or all of the Sa bits (Sa4-Sa8) can be programmed to build up the bandwidth of the HDLC channel from 4 kbit/s to 20 kbit/s. Writing a 1 to an SA4-SA8 bit (bits 4-0) in HDLC Link Control Register X0CH enables the corresponding Sa bit to be used as part of the HDLC channel bandwidth for both the transmit and receive directions.

The HDLC receiver is enabled when a 1 is written to control bit EHR (bit 7) in the HDLC Link Control Register X08H. When enabled, the HDLC receiver will remove the stuffed zero bits, search for the opening flag and place the message contents in a 16-byte FIFO. The HDLC Controller will compute a CRC and compare it against the CRC that is received. The received CRC is not stored in the FIFO and is discarded after being received.

The receive FIFO is monitored for fill level, with maskable interrupts and latched indications provided. Bits RXFS1 and RXFS0 (bits 3 and 2) in the HDLC Link Status Register X16H indicate when the receive FIFO is less than half full, equal to or greater than half full, full or overflowed. An interrupt may also be set at the end of the message, or when the FIFO is half full, using the RHIE control bit (bit 3) in the HDLC Link Control Register X08H. Thus, when the messages are always expected to be shorter than the maximum FIFO depth of 16 bytes, the HDLC controller will generate an interrupt on the completion of the message. When the messages are expected to exceed the maximum FIFO depth of 16 bytes, the controller will generate an interrupt when the FIFO is half filled.

Bits C4-C0 (bits 4-0) in the HDLC Link Receive Data Register (X18H) provide the number of bytes presently stored in the receive FIFO. Bits RHIS2-RHIS0 (bits 7-5) in the HDLC Link Status Register (X16H) provide message status and error indications. The HDLC controller will generate a maskable interrupt for start of message detected, valid message received, CRC in error, and message aborted. The message bytes are read by the microprocessor at bits RHD7-RHD0 in register X17H for each framer. Bit 0 corresponds to the first bit received in a byte.

The HDLC transmitter is enabled when a 1 is written to control bit EHT (bit 6) in the HDLC Link Control Register X08H. When enabled, the HDLC controller will transmit flags until data is placed in the transmit FIFO. Up to 16 bytes can be placed in the 16-byte FIFO. The message bytes are written into bits THD7-THD0 in the HDLC Link Transmit Data Register X0AH. Bit 0 corresponds to the first bit transmitted. The transmit bytes are read from the transmit FIFO and a 16-bit CRC is computed until the end of message is detected. When the last byte of the message is written into the FIFO, the microprocessor will set the end of message status bit EOM (bit 4) in the HDLC Link Control Register X08H. The computed 16-bit CRC will be appended to the end of the message followed by at least one flag before another message is transmitted. When the transmit FIFO is emptied without setting the EOM bit, the FIFO will set an underflow indication, and an abort character will be transmitted, thereby terminating the message.

The transmit HDLC controller provides latched event bits and maskable interrupt bits related to the transmit FIFO status. Information such as underflow, overfill, and fill status is provided by reading status bits TXFS1-TXFS0 (bits 1-0) in the HDLC Link Status Register X16H.

Transmit HDLC FIFO service interrupts may be programmed to occur when the transmit FIFO is half empty, or when the last byte is sent, by setting control bit THIE (bit 2) in register X08H. For short messages, the entire message may be written into the FIFO, and the controller will generate an interrupt, indicated by status bit THIS (bit 4) in register X16H, when the message has been sent. For longer messages, the controller will generate an interrupt when the FIFO is ready to accept more data.

There are four general types of message transfers, which are described below: transmitting long and short messages, and receiving long and short messages. The difference between the long and short messages is primarily in how the 16-bit FIFOs are serviced. With short messages, the entire message will fit into the FIFOs and interrupts will be generated when the end of the message occurs. With long messages, the message will not fit into the FIFO, and the message will have to be transmitted or received in several segments. Since long and short received messages are similar, their processing is described under the same heading.

Transmit Short Message

To transmit a short message, first configure the transmitter to generate an interrupt at the end of message by writing a 0 to control bit THIE (bit 2) in the HDLC Link Control Register X08H. Then write a 1 to control bit EHT (bit 6) in register X08H to enable the transmitter. The HDLC controller will transmit flags until data is written into the transmit HDLC FIFO.

Write the message into the transmit FIFO by writing each byte in turn to THD7-THD0 in register X0AH. Bit 0 represents the first bit in the byte to be transmitted. The bytes written into THD7-THD0 are transferred automatically into the FIFO. After the last byte is written into the FIFO, the EOM (bit 4) in register X08H is written with a 1. The transmitter will then begin to send the message bytes until the FIFO is empty. Since the EOM bit was set, the completion of the message will generate an interrupt, if not masked, indicated by the latched THIS status bit ETHIS, (bit 4) in X0EH. This latched status indication indicates that the message is complete or the FIFO is half full. After the CRC-16 is sent, the HDLC controller will start to send flags.

Transmit Long Message

To transmit a long message, first configure the transmitter to generate an interrupt at the half full level of the FIFO by writing a 1 to control bit THIE (bit 2) in the HDLC Link Control Register X08H. Then write a 1 to control bit EHT (bit 6) in register X08H to enable the transmitter. The HDLC controller will transmit flags until data is written into the transmit HDLC FIFO.

Write the first 16-byte message segment into the transmit FIFO by writing each byte in turn to THD7-THD0 in register X0AH. Bit 0 represents the first bit in the byte to be transmitted. The bytes written into THD7-THD0 are transferred automatically into the FIFO. The HDLC controller will then start to send the message bytes. When the FIFO empties to the half full level, the ETHIS bit (bit 4) in register X0EH will be latched, and an interrupt generated, if the corresponding mask bit MTHIS (bit 4) in register X0FH is set to 0. This is an indication for the microprocessor to write another 8 bytes into the transmit HDLC FIFO. This process of sending and refilling is repeated, 8 bytes at a time, until the last byte in the message is written into the FIFO, when the EOM (bit 4) in register X08H is written with a 1. The transmitter continues to send the final message bytes until the FIFO is empty. When the last byte is transmitted and the FIFO is empty, the ETHIS bit will latch while EOM=1, indicating completion of the message. After the CRC-16 is sent, the HDLC controller will start to send flags. Status bits TXFS1-TXFS0 (bits 1-0) in register X16H indicate the fill level of the transmit FIFO.

Receive Message

To receive a message, first configure the receiver to generate an interrupt at the end of the message by writing a 0 to control bit RHIE (bit 3) in the HDLC link control register X08H. Enable interrupts from the FIFO being half full by setting mask bits MRXFS1-MRXFS0 (bits 3-2) in control register X0FH to 00 and mask bits MRHIS2-MRHIS0 (bits 7-5) in control register X0FH to 001. Finally, enable the receiver by writing a 1 to control bit EHR (bit 7) in register X08H.

The receiver will generate an interrupt when the FIFO is half full via status and event bits RXFS1-RXFS0 (bits

3-2) in register X16H and ERXFS1-ERXFS0 (bits 3-2) in register X0EH or when an end of message is detected via status and event bits RHIS2-RHIS1 (bits 7-5) in register X16H and ERHIS2-ERHIS1 (bits 7-5) in the latched register X0EH. The receive message is read from the FIFO by reading the bytes RHD7-RHD0 in register X17H. Bit 0 represents the first bit in the byte to be received. The bytes in RHD7-RHD0 are transferred automatically from the receive FIFO. When the interrupt occurs, the RHIS2-RHIS0 status bits (bits 7-5) in register X16H are also set in the ERHIS2-ERHIS0 bits (bits 7-5) in the latched register X0EH, indicating the message status. If the message in progress status is set, the microprocessor should read the message bytes from RHD7-RHD0 using the FIFO Depth bits C4-C0 in register X18H to detect the number of bytes stored in the receive FIFO. Please note that the FIFO depth count is updated when the event indication is latched and interrupt generated, and will not be modified until it is read and cleared by the microprocessor. During long messages, the count is allowed to change after the half full indication. If the microprocessor fails to read out the FIFO in time, a second interrupt indication is generated. The reason for interrupt is indicated by status bits RXFS1-RXFS0 (bits 3-2) in register X16H. These control bits provide status information about the fill level of the receive FIFO. An end of message is also indicated by the RHIS2-RHIS0 status bits.

ALARMS

The following line level alarms for each of the four framers are detected in the QE1F-*Plus*: Loss Of Signal (LOS), Alarm Indication Signal (AIS), Out Of Frame (OOF), Remote Alarm Indication (RAI), Change Of Frame Alignment (CFA), Out Of Multiframe (OOMF), transmit slip (TXSLIP) and receive slip (RXSLIP). These alarms are provided by the E1 Status and Mask Registers (registers X09H-X13H). In addition, the following HDLC link level alarms are supported by the QE1F-*Plus*: Receive HDLC event, Transmit HDLC event, Receive FIFO event, Transmit FIFO event (registers X0EH, X0FH, X16H). Each condition can cause an interrupt when the corresponding mask bit is set to 0.

The latched status event indication (which can also be referred to as a software interrupt indication) for an alarm or condition is latched on either positive transitions, negative transitions, or both transitions. Control bits RISE (bit 6), and FALL (bit 5) in the Global Configuration register 006H determine the transitions that cause an event bit to latch for all four framers, as shown in the following table:

RISE (bit 6)	FALL (bit 5)	Action
0	0	Latched status bit indications in all registers disabled. Hardware and software interrupt indications disabled.
1	0	Latched status indication sets on positive alarm transition, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt bit GIM (bit 7 in 006H) are both 0.
0	1	Latched status indication sets on negative alarm transition, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt bit GIM (bit 7 in 006H) are both 0.
1	1	Latched status indication sets on both positive and negative alarm transitions, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt bit GIM (bit 7 in 006H) are both 0.

The latched event is cleared by writing a 0 to the associated bit position in the latched status indication register. The QE1F-*Plus* also provides a Global Interrupt Mask (GIM) bit for the microprocessor interrupt pin (pin 125, INT/$\overline{IRQ}$). When a 1 is written to control bit GIM (bit 7) in the Global Configuration Register 006H, this hardware interrupt indication pin is tri-stated when a latched indication (event) bit is set. When a 0 is written into the GIM bit, the hardware interrupt pin is enabled. When enabled, the polarity of the interrupt pin can be inverted by writing a 1 to control bit IPOL (bit 4) in the Global Configuration Register 006H.

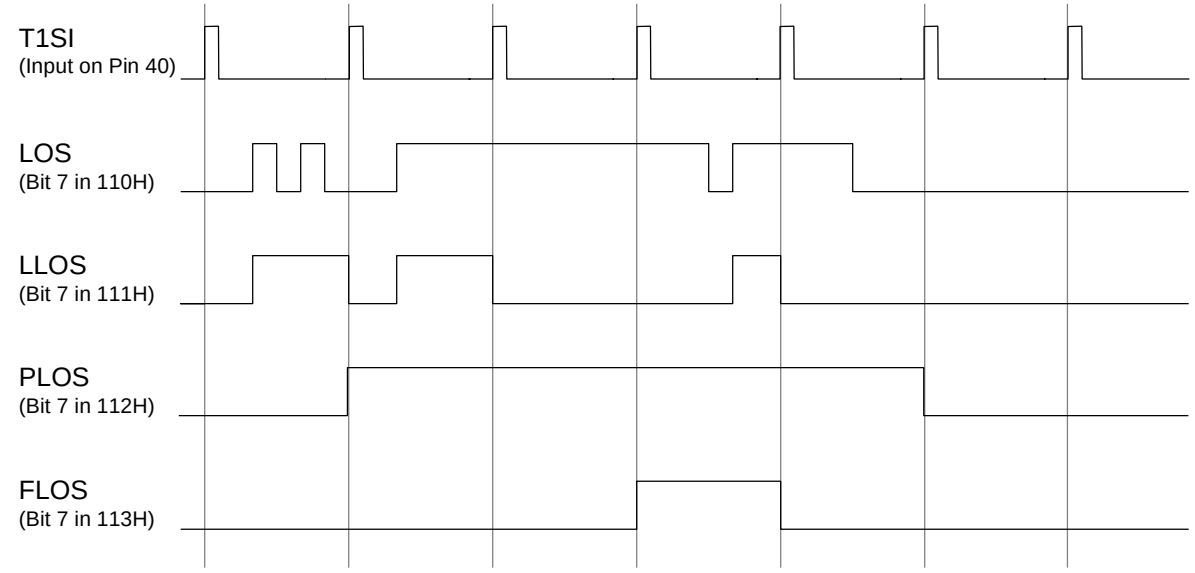
Besides providing individual unlatched and latched alarm status indications, and interrupt mask bits, on a per framer basis, the QE1F-*Plus* provides global interrupt status indication bits, as well as global interrupt mask bits and framer pointer bits in the Global Register segment (registers 00AH-00EH). An indication bit is set in register 00AH if the same type of alarm occurs in any of the four framers. Registers 00CH and 00EH provide pointers to the framer which caused the line event or HDLC link event that triggered the interrupt.

For example, assuming a loss of signal alarm occurred in framer 1 only, the LOS alarm will set the LOS bit (bit 7) in the unlatched register 110H. This alarm indication bit will be set to 1 for the duration of the alarm. Assuming that control bits RISE and FALL (bits 6 and 5) in the Global Configuration Register 006H are set to 10 (latched event set on a positive transition), the transition from 0 to 1 of the LOS alarm will cause the LLOS bit (bit 7) in register 111H to latch. A hardware interrupt will be generated on pin 125 if the interrupt mask bit MLOS (bit 7) in register 109H is a 0, and the global interrupt mask bit GIM (bit 7) in register 006H is a 0. If either of these bits is set to 1, the hardware interrupt will not occur. In addition, the latched LOS indication will also cause a Global LOS indication (bit 7) in register 00AH. The framer in which the loss of signal alarm was detected can be found by reading bits 3-0 in register 00CH. The interrupt will be reset by first reading the LLOS latched alarm bit position (bit 7) in 111H and then writing a 0 into the bit position. This will also clear the global LOS indication bit. Reading the register confirms that the loss of signal alarm occurred in framer 1. If the LOS alarm persists, it will not cause the latched bit position to relatch. The alarm status can be determined by now reading the unlatched status bit (bit 7) in register 110H, until it becomes 0, indicating that recovery has taken place.

Shadow Registers

The QE1F-*Plus* also provides shadow registers for the alarms of each of the four framers. By applying a pulse at one second intervals to T1SI (pin 40), an indication bit will be set in register X12H if the corresponding alarm occurred at any time in the last one second interval. In addition, an indication bit will be set in register X13H if the alarm is active, but the transition to the active state did not occur in the last one second interval (i.e., the alarm has persisted for longer than one second). The rising edge of the T1SI pulse will also reset a latched event bit position in register X11H independent of the microprocessor.

Figure 57 illustrates the operation of the shadow registers for a loss of signal (LOS) alarm for framer 1. The behavior shown in the diagram also applies to the other line signal alarms in the same registers (AIS, OOF, RAI, CFA, OOMF, TXSLIP, and RXSLIP). This figure assumes that control bits RISE and FALL (bits 6 and 5) in the Global Configuration Register 006H are set to 10 (latched event set on a positive transition). Please note that the LOS alarm causes a latched status indication LLOS (bit 7) in register 111H, and that the latched bit is reset by the rising edge of the T1SI pulse. The PLOS status bit (bit 7) in register 112H is a 1 whenever there is a transition to LOS during the last one second interval or a LOS is present at the end of the last one-second interval. The FLOS status bit (bit 7) in register 113H is a 1 if the LOS alarm is active but did not become active during the previous one-second interval.



Notes:
1. For this example, latched events are set only on positive event transitions.
2. PLOS = LOS + LLOS evaluated at one second boundaries (where '+' is a logical ' or').
3. FLOS = LOS & $\overline{\text{LLOS}}$ evaluated at one second boundaries (where '&' is a logical 'and' and $\overline{X}$ is a logical inversion).

Figure 57. Shadow Register Operation

In addition, shadow registers have been provided for monitoring the number of line errors that have occurred in one second intervals. When control bit ENPMFM (bit 3 in global configuration register 006H) is set to a 1, the following shadow registers are updated with the count from the previous one-second interval on the rising edges of the one-second pulse provided at the T1SI pin: a 10-bit register for a CRC-4 count, a 16-bit register for coding violations, a 10-bit register for E-bit errors, and a 13-bit register for frame errors. The rising edge of the one-second pulse also clears the counters that were holding the count for the transfer to the shadow registers. Control bit ENPMFM has no effect on the counters counting, just on the 1 second clearing.

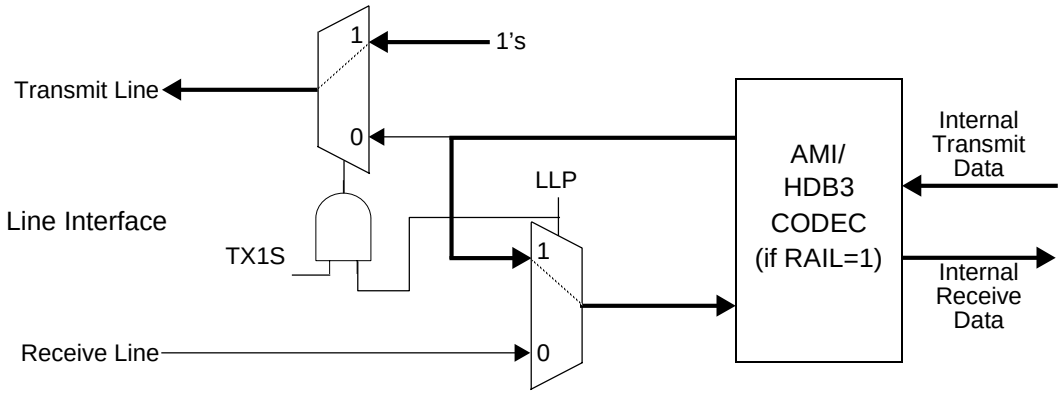
For example, the shadow registers for monitoring frame bit errors in framer 1 work in the following way. The 13-bit framing word error counter FBE12-FBE0 in registers 1FCH and 1FDH counts the number of frame word errors over a one-second interval, which is determined by the T1SI signal. At the rising edge of the pulse on the T1SI pin, the count in registers 1FCH and 1FDH is transferred to the shadow register LFBE12-LFBE0 in locations 1FAH and 1FBH. The frame word error counter in registers 1FCH and 1FDH is cleared at the same instant and it starts the error count for the next one-second interval. At the end of the next one-second interval, the shadow register is updated with the new count. A counter overflow bit FBEO is also provided (bit 7 in 1FDH), with a corresponding shadow overflow bit LFBEO (bit 7) in register 1FBH. The microprocessor can also clear the counter in registers 1FCH and 1FDH by writing 00H to these registers. The shadow register holds its count during a microprocessor read cycle.

MAINTENANCE

The QE1F-*Plus* provides two loopback modes. Local and remote line loopbacks are available for each of the four framers. In addition, a payload remote loopback is available. A per time slot loopback is also available in 2 Mbit/s Transmission and MVIP Modes when the system side clocks and frames are synchronous that loops any one or more received time slots and substitutes them for transmit time slots from the system side. These loopback modes allow the user to section a network path and isolate a specific failure. In addition, a pseudo-random test generator and analyzer are provided for board testing in 2 Mbit/s Transmission Mode.

Local Loopback

Local loopback for a framer is enabled when a 1 is written to control bit LLP (bit 0) in register X05H. Local loopback connects the transmit path with the receive path (via the CODEC) in the direction toward the line, as illustrated in Figure 58 below. The loopback is independent of the line interface selected, NRZ or dual unipolar (rail). When control bit TX1S (bit 2) in register X05H is written to 1, an AIS (all ones signal) is transmitted in either NRZ or rail mode to the line instead of data. Please note that the normal transmit line AIS can be enabled independently of the local loopback feature. When performing a local loopback, control bits RLP (bit 1) and PAYL (bit 3) in register X05H should be set to 0 to prevent errors in testing.

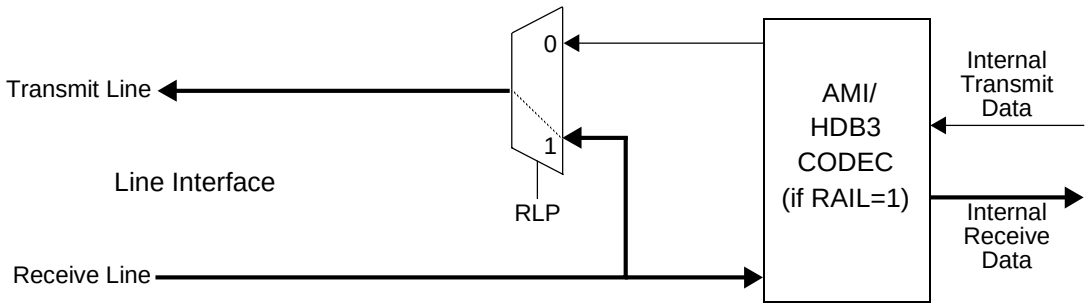


Note: Bold/dashed lines show paths used for TX1S=1 and LLP=1.

Figure 58. Local Loopback

Remote Line Loopback

Remote line loopback for a framer is enabled when a 1 is written to control bit RLP (bit 1) in register X05H. Remote line loopback connects the receive line data back to the transmitter, as illustrated in Figure 59 below. The loopback is performed before the AMI/HDB3 CODEC, allowing any coding violations to be passed through unaltered. The loopback is independent of the line interface selected, NRZ or dual unipolar (rail). Control bits PAYL (bit 3) and LLP (bit 0) in register X05H should be set to 0 to prevent errors in testing.

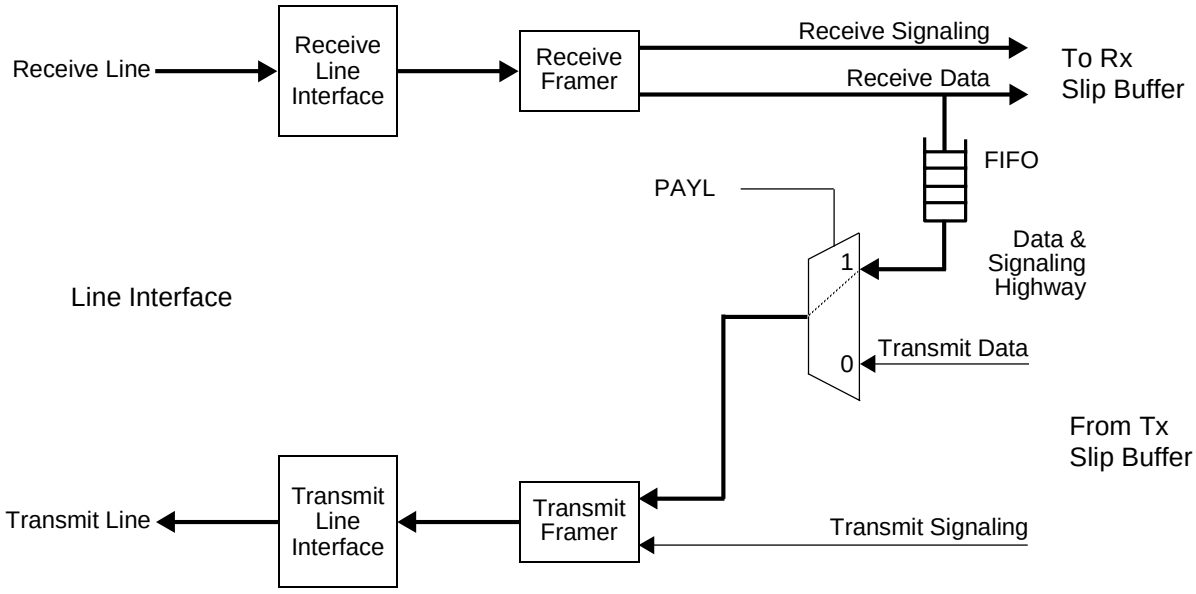


Note: Bold/dashed lines show paths used for RLP=1.

Figure 59. Remote Line Loopback

Payload Remote Loopback

Payload remote loopback for a framer is enabled when a 1 is written to control bit PAYL (bit 3) in register X05H. Payload remote loopback connects the receive data back as the transmit data for Time Slots 1 through 31, as illustrated in Figure 60 below. A small FIFO provides for the delay necessary to allow the received Time Slot 0 to be skipped and the transmit Time Slot 0 to be inserted. Time slot number and bit position within a time slot are not retained from receive to transmit, only the bit sequence is maintained.



Note: Bold/dashed lines show paths used for PAYL=1.

Figure 60. Payload Remote Loopback

Time Slot Remote Loopback

When control bit ENTSLB (bit 4) in register 0FFH is set to 1, control bits TFTS31 through TFTS0 in registers X3CH through X3FH, if set to a 1, cause the Framer to source the selected time slots from the receive data highway instead of TDATAn pin. Pins RCLKn and RSYNCn must be connected to pins TCLKn and TSYNCn respectively, and RCLKn and RSYNCn must be inputs (recovered receive clock cannot be selected) to prevent data errors in the looped back time slots. The loopback takes place after the slip buffer and is provided whether the receive slip buffer is enabled or disabled. Control bits ENTSLB and TFTS31 through TFTS0 are set to 0 upon a hardware reset. This function requires the presence of TCLKn to operate correctly and is supported in Transmission Mode and 2 Mbit/s MVIP Mode. Figure 61 shows the basic operation of the time slot loopback feature. ENTSLB when set to 1 over rides the transmit side gapped clock feature on pins TFE1GCn as selected by control bit FE1M (bit 0) in register X02H. Though a loopback can be applied to Time Slot 0, the QE1F-*Plus* regenerates Time Slot 0 and no change to the transmit framing pattern will occur.

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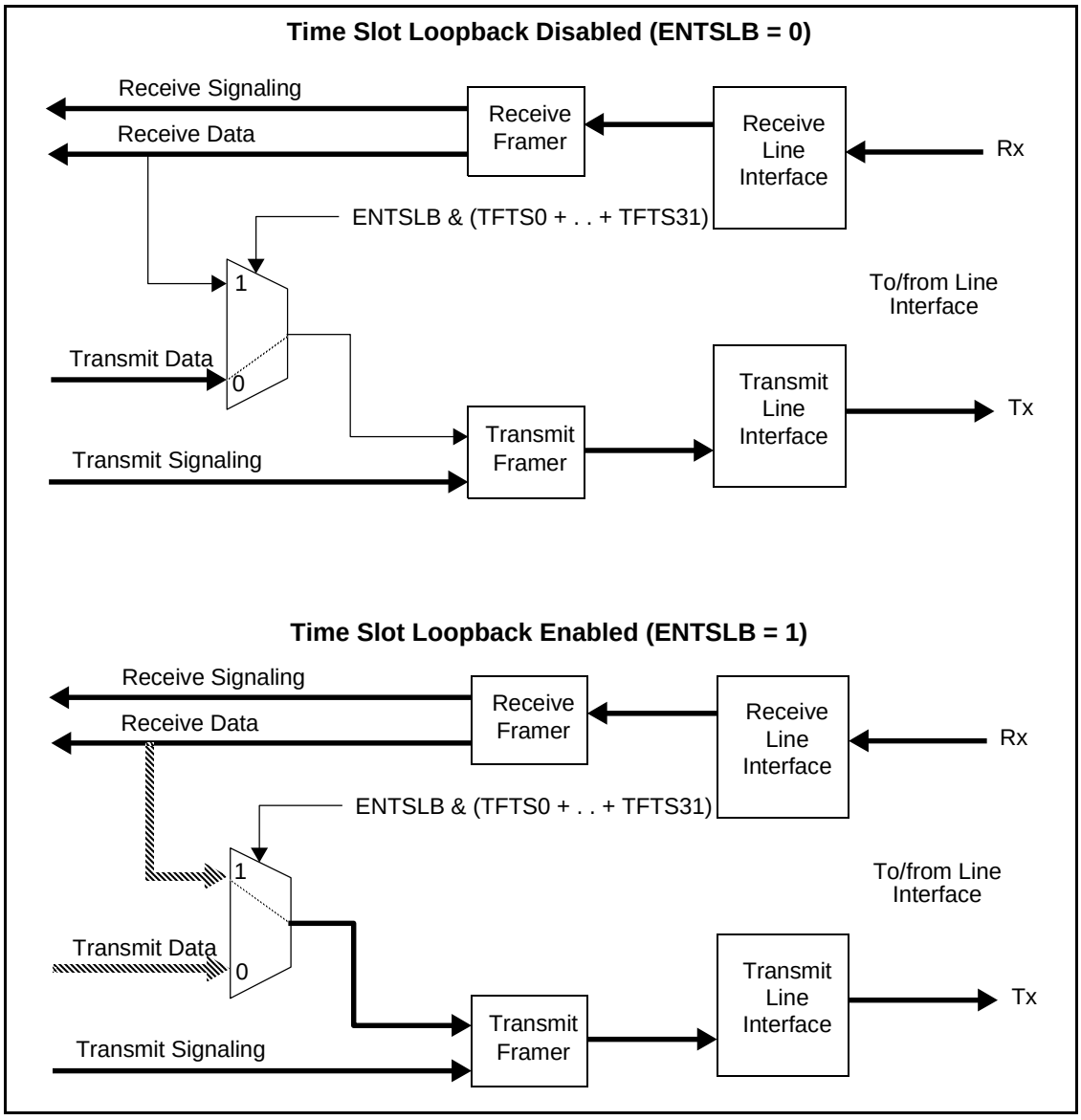


Figure 61. Time Slot Remote Loopback

BOUNDARY SCAN

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Figure 62. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the QE1F-*Plus* device's internal logic, as illustrated in Figure 62. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 29.

Boundary Scan Support

The maximum frequency the QE1F-*Plus* device will support for boundary scan is 10 MHz. The QE1F-*Plus* device performs the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS
- IDCODE

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the QE1F-*Plus* device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external QE1F-*Plus* input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the QE1F-*Plus* device remains fully operational. While in this test mode, QE1F-*Plus* input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the QE1F-*Plus* device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Test Instruction:

The format of the IDCODE test instruction is "10".

Boundary Scan Reset

Specific control of the $\overline{TRS}$ pin is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This pin must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-on of the QE1F-*Plus*. If boundary scan testing is to be performed and the pin is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this pin high, but still meet the V_{IL} requirements listed in the Input, Output and I/O Parameters section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

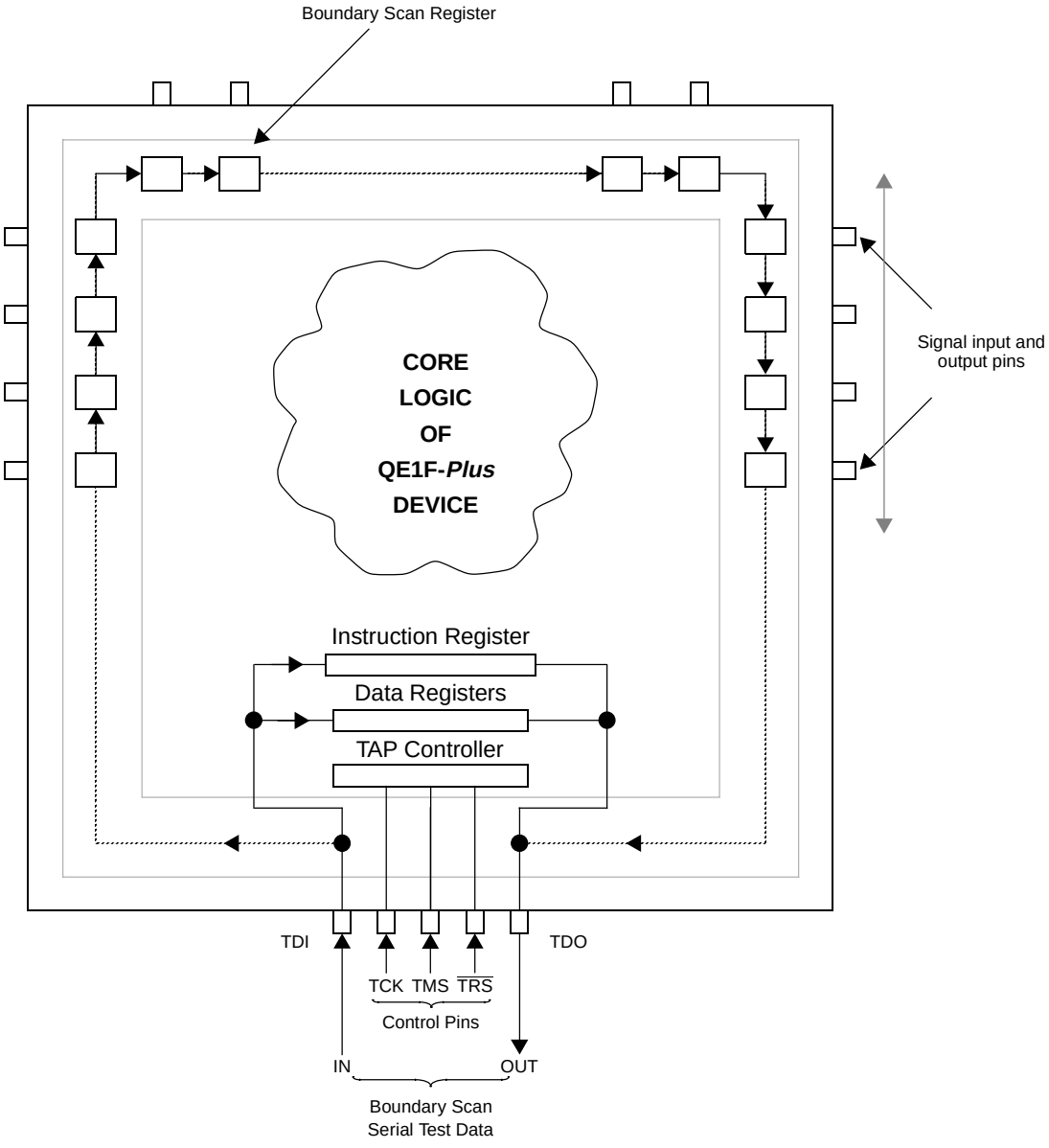


Figure 62. Boundary Scan Schematic

Boundary Scan Chain

There are 139 scan cells in the QE1F-*Plus* boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their function. A BSDL file is provided on the TranSwitch Web Site at www.transwitch.com.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
138	CONTROL	NA	XIOTRI_B	A 1 enables the outputs of I/O type OUTPUT3.
137	OUTPUT3	39	RDATA1_O39	
136	OUTPUT3	38	RSIGL1_O38	
135	CONTROL	NA	XRXC1_B	A 0 makes Pins 37, 36 to be OUTPUT.
134	BIDIR_IN	37	RCLK1_IO37	
133	BIDIR_OUT	37	RCLK1_IO37	
132	BIDIR_IN	36	RSYNC1_IO36	
131	BIDIR_OUT	36	RSYNC1_IO36	
130	INPUT	35	TDATA1_I35	
129	CONTROL	NA	XTSIGL1_B	A 0 makes Pin 34 to be OUTPUT.
128	BIDIR_IN	34	TSIGL1_IO34	
127	BIDIR_OUT	34	TSIGL1_IO34	
126	INPUT	33	TCLK1_I33	
125	INPUT	32	TSYNC1_I32	
124	OUTPUT3	31	RDATA2_O31	
123	OUTPUT3	29	RSIGL2_O29	
122	CONTROL	NA	XRXC2_B	A 0 makes Pins 28, 27 to be OUTPUT.
121	BIDIR_IN	28	RCLK2_IO28	
120	BIDIR_OUT	28	RCLK2_IO28	
119	BIDIR_IN	27	RSYNC2_IO27	
118	BIDIR_OUT	27	RSYNC2_IO27	
117	INPUT	26	TDATA2_I26	
116	CONTROL	NA	XTSIGL2_B	A 0 makes Pin 24 to be OUTPUT.
115	BIDIR_IN	24	TSIGL2_IO24	
114	BIDIR_OUT	24	TSIGL2_IO24	
113	INPUT	23	TCLK2_I23	
112	INPUT	22	TSYNC2_I22	
111	OUTPUT3	21	RDATA3_O21	
110	OUTPUT3	19	RSIGL3_O19	
109	CONTROL	NA	XRXC3_B	A 0 makes Pins 18, 17 to be OUTPUT.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
108	BIDIR_IN	18	RCLK3_IO18	
107	BIDIR_OUT	18	RCLK3_IO18	
106	BIDIR_IN	17	RSYNC3_IO17	
105	BIDIR_OUT	17	RSYNC3_IO17	
104	INPUT	16	TDATA3_I16	
103	CONTROL	NA	XTSIGL3_B	A 0 makes Pin 15 to be OUTPUT.
102	BIDIR_IN	15	TSIGL3_IO15	
101	BIDIR_OUT	15	TSIGL3_IO15	
100	INPUT	13	TCLK3_I13	
99	INPUT	12	TSYNC3-I12	
98	OUTPUT3	11	RDATA4_O11	
97	OUTPUT3	10	RSIGL4_O10	
96	CONTROL	NA	XRDY_ENB	A 0 makes Pin 9 to be OUTPUT, 1 to be tri-stated.
95	OUTPUT3	9	RDY_O9	
94	CONTROL	NA	XRXC4_B	A 0 makes Pins 8, 7 to be OUTPUT.
93	BIDIR_IN	8	RCLK4_IO8	
92	BIDIR_OUT	8	RCLK4_IO8	
91	BIDIR_IN	7	RSYNC4_IO7	
90	BIDIR_OUT	7	RSYNC4_IO7	
89	INPUT	6	TDATA4_I6	
88	CONTROL	NA	XTSIGL4_B	A 0 makes Pin 5 to be OUTPUT.
87	BIDIR_IN	5	TSIGL4_IO5	
86	BIDIR_OUT	5	TSIGL4_IO5	
85	INPUT	4	TCLK4_I4	
84	INPUT	3	TSYNC4_I3	
83	CONTROL	NA	XREF_CLK_EN2_B	A 0 makes Pin 2 to be OUTPUT enabled.
82	OUTPUT3	2	CLKREF2_O2	
81	INPUT	1	$\overline{\text{RESET}}$_I1	
80	INPUT	128	$\overline{\text{WR}}$_I128	
79	INPUT	127	$\overline{\text{SEL}}$_I127	
78	INPUT	126	$\overline{\text{RD}}$_I126	
77	OUTPUT3	125	INT_O125	
76	CONTROL	NA	XDT_EN	A 0 makes Pins 123-114 to be OUTPUT.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
75	BIDIR_IN	123	DAT7_IO123	
74	BIDIR_OUT	123	DAT7_IO123	
73	BIDIR_IN	122	DAT6_IO122	
72	BIDIR_OUT	122	DAT6_IO122	
71	BIDIR_IN	120	DAT5_IO120	
70	BIDIR_OUT	120	DAT5_IO120	
69	BIDIR_IN	119	DAT4_IO119	
68	BIDIR_OUT	119	DAT4_IO119	
67	BIDIR_IN	118	DAT3_IO118	
66	BIDIR_OUT	118	DAT3_IO118	
65	BIDIR_IN	117	DAT2_IO117	
64	BIDIR_OUT	117	DAT2_IO117	
63	BIDIR_IN	115	DAT1_IO115	
62	BIDIR_OUT	115	DAT1_IO115	
61	BIDIR_IN	114	DAT0_IO114	
60	BIDIR_OUT	114	DAT0_IO114	
59	INPUT	113	ADDR11_I113	
58	INPUT	112	ADDR10_I112	
57	INPUT	110	ADDR9_I110	
56	INPUT	109	ADDR8_I109	
55	INPUT	108	ADDR7_I108	
54	INPUT	107	ADDR6_I107	
53	INPUT	106	ADDR5_I106	
52	INPUT	105	ADDR4_I105	
51	INPUT	104	ADDR3_I104	
50	INPUT	103	ADDR2_I103	
49	INPUT	102	ADDR1_I102	
48	INPUT	101	ADDR0_I101	
47	INPUT	100	SYSCLK_I100	
46	INPUT	99	MOTO_I99	
45	OUTPUT3	98	$\overline{\text{LCS4}}$_O98	
44	OUTPUT3	97	LTCLK4_O97	
43	OUTPUT3	96	TNEG4_O96	
42	OUTPUT3	95	TPOS4_O95	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
41	INPUT	93	LRCLK4_I93	
40	INPUT	92	RNEG4_I92	
39	INPUT	91	RPOS4_I91	
38	INPUT	90	LINT4_I90	
37	OUTPUT3	88	$\overline{\text{LCS3}}$_O88	
36	OUTPUT3	87	LTCLK3_O87	
35	OUTPUT3	86	TNEG3_O86	
34	OUTPUT3	85	TPOS3_O85	
33	INPUT	83	LRCLK3_I83	
32	INPUT	82	RNEG3_I82	
31	INPUT	81	RPOS3_I81	
30	INPUT	80	LINT3_I80	
29	OUTPUT3	79	$\overline{\text{LCS2}}$_O79	
28	OUTPUT3	77	LTCLK2_O77	
27	OUTPUT3	76	TNEG2_O76	
26	OUTPUT3	75	TPOS2_O75	
25	INPUT	74	LRCLK2_I74	
24	INPUT	72	RNEG2_I72	
23	INPUT	71	RPOS2_I71	
22	INPUT	70	LINT2_I70	
21	OUTPUT3	69	$\overline{\text{LCS1}}$_O69	
20	OUTPUT3	68	LTCLK1_O68	
19	OUTPUT3	67	TNEG1_O67	
18	OUTPUT3	66	TPOS1_O66	
17	INPUT	65	LRCLK1_I65	
16	INPUT	64	RNEG1_I64	
15	INPUT	63	RPOS1_I63	
14	INPUT	62	LINT1_I62	
13	CONTROL	NA	XMON_ENB	A 0 enables Pins 61, 60.
12	OUTPUT3	61	LSCLK_O61	
11	OUTPUT3	60	LSDO_O60	
10	INPUT	59	LSDI_I59	
9	INPUT	51	SCAN_ENB_I51	
8	INPUT	50	$\overline{\text{IOTRI}}$_I50	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
7	INPUT	49	$\overline{\text{CSO}}$_I49	
6	OUTPUT3	48	PRBSOOL_O48	
5	CONTROL	NA	XREF_CLK_EN1_B	A 0 enables Pin 46.
4	OUTPUT3	46	CLKREF1_O46	
3	INPUT	43	CONFIG1_I43	
2	INPUT	42	CONFIG2_I42	
1	INPUT	41	LO_I41	
0	INPUT	40	T1SI_I40	

RESET PROCEDURE

After power-up the QE1F-*Plus* requires a hardware reset. This reset will reset all the per channel registers in the memory map below address X40H. It will also reset all of the global registers at addresses 004H through 0FFH. A low placed on the $\overline{\text{RESET}}$ pin for at least 10 cycles of SYSCLK after all clocks become stable will accomplish the hardware reset.

A global software reset is also available and should be applied at least 40 ms after power-up. This resets the internal state machines. It does not change the state of any of the control registers, performance counters and latched shadow registers. Writing a 91H to control byte RESET in register 005H places the QE1F-*Plus* in a reset state. Writing a value other than 91H to control byte RESET will take the QE1F-*Plus* out of the reset state. The RESET register can be read to determine the reset state of the QE1F-*Plus*. A value of 01H in the RESET register indicates the QE1F-*Plus* is in a reset state; a value of 00H indicates the QE1F-*Plus* is not in reset. A per channel version of this function is available by writing a 1 to control bit SRST (bit 7) in register X05H followed by writing a 0 to control bit SRST. Note that all the memory locations at addresses X40H through XFFH are located in a per channel internal RAM and are not reset by either a hardware reset or a software reset.

Changing the mode of operation of a framer should be followed by a per channel software reset (SRST). The mode bits can be found in framer per channel registers X00H through X04H (RAIL, BE, ENSRAI, LIE, LPOL, TXCP, RXCP, TXNRZP, RXNRZP, PWRD, FDAT, FPOL, BNAL, TXC1, TXC0, RXC, TSE, RSE, TSR, RSR, TYP1, TYP0, RX_SIG_INV, ENAIS, ENOOF, ENLOS, OOF1, OOF0, BFAA, CRCA, CASA, CRCMD1, and CRCMD0). Not resetting the framer after changing most mode control bits will have minimal effect.

If all 4 channels of the QE1F-*Plus* are not implemented in an application, the channels that are not used should be powered down (control bit PWRD, bit 4 in register X01H is set to a 0) and all interrupts masked (register X09H set to FFH).

MEMORY MAP

The QE1F-*Plus* memory map contains registers and counters which may be accessed by the microprocessor. Addresses which are shown as spare, or are not listed in the memory map, must not be accessed by the microprocessor. The status designation R stands for a read-only unlatched register location, R(L) a read-only latched register location, W a write-only register location and RW a read/write register location. R and R(L) register bit positions designated as Reserved (R) will read out an indeterminate value unless a 0 or 1 read value is indicated. RW Reserved (R) bit positions must be set to 0 unless otherwise noted.

COMMON REGISTERS

Device ID Registers (See descriptions on page 128)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	0	0	0	1	0	0	0	0
002	R	1	1	0	0	0	0	1	0
003	R	Revision Level (currently 0000)				0	0	0	0

Customer Notebook Register (See descriptions on page 128)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004	RW	Customer Defined Byte							

Global Software Register (See descriptions on page 128)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
005	RW	QE1F-*Plus* Chip Reset (RESET byte)							

Global Configuration Registers (See descriptions on page 129)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
006	RW	GIM	RISE	FALL	IPOL	ENPMFM	HMVIP	MTP16M	ENHWM
007		Spare							
008		Spare							
009		Spare							
01A	RW	LOSI7 - LOSI0 (Loss Of Signal Detection Interval)							
01B	RW	R (0)	R (0)	OND5 - OND0 (Ones Density Loss Of Signal Recovery Interval)					
01C-0FE		Spare							
0FF	RW	WGDEC	R (0)	R (0)	ENTSLB	AAGS	H100	R (0)	R (0)

Global Status Indication, Interrupt Mask and Pointer Registers (See descriptions on page 132)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00A	R	GLOS	GAIS	GOOF	GRAI	GCFA	GOOMF	GTXSLIP	GRXSLIP
00B	RW	GMLOS	GMAIS	GMOOF	GMRAI	GMCFA	GMOOMF	GMTXSLIP	GMRXSLIP
00C	R	Reserved				CHA4	CHA3	CHA2	CHA1
00D		Spare							
00E	R	Reserved				CHDL4	CHDL3	CHDL2	CHDL1
00F		Spare							

Line Interface Control and Monitoring Registers (See descriptions on page 134)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010	RW	LCB7 - LCB0 (Command Byte)							
011	RW	LDO7 - LDO0 (Line Interface Data Output)							
012	R	LDI7 - LDI0 (Line Interface Data Input)							
013	RW	BDCST	PRBSFR	PRBSEN	ESP/ EMON	RXTX	R (0)	E1CHCS1	E1CHCS0
014	RW	Reserved (Set to 0)							
015	RW	Reserved (Set to 0)							
016	RW	Reserved (Set to 0)							

Transmit and Receive Sync Delay Registers (See descriptions on page 136)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
017	RW	TSD7 - TSD0 (Transmit Sync Delay)							
018	RW	RSD7 - RSD0 (Receive Sync Delay)							

Clock Reference Selection Register (See descriptions on page 136)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
019	RW	CR2S1	CR2S0	ENREF2	2048KHZ	ENREF1	R (0)	CR1S1	CR1S0

PER CHANNEL CONTROL AND STATUS INDICATION REGISTERS

The following registers configure, control or provide status information on a per channel basis. When an address location is written as XXXH, the first X indicates 1, 2, 3, or 4 to identify the associated channel, which corresponds to the like-numbered framer (n=1, 2, 3 or 4).

Framer Configuration and Control Registers (See descriptions on page 138)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100 200 300 400	RW	RAIL	BE	R (0)	ENSRAI	R (0)	ENSAIS	LIE	LPOL
101 201 301 401	RW	TXCP	RXCP	TXNRZP	PWRD	FDAT	FPOL	BNAL	RXNRZP
102 202 302 402	RW	TXC1	TXC0	RXC	TSE	RSE	TSR	RSR	FE1M
103 203 303 403	RW	TYP1	TYP0	RXF	TXF	RX_SIG_INV	ENAIS	ENOOF	ENLOS
104 204 304 404	RW	OOF1	OOF0	BFAA	CASA	CRCA	CRCMD1	CRCMD0	RSYC
11A 21A 31A 41A	RW	AUTY	AUTRAI	ENRAIA	ENRAIY	EOOCRC	EOO16M	E16AIS	ENLAIS
138 238 338 438	RW	RFTS7	RFTS6	RFTS5	RFTS4	RFTS3	RFTS2	RFTS1	RFTS0
139 239 339 439	RW	RFTS15	RFTS14	RFTS13	RFTS12	RFTS11	RFTS10	RFTS9	RFTS8
13A 23A 33A 43A	RW	RFTS23	RFTS22	RFTS21	RFTS20	RFTS19	RFTS18	RFTS17	RFTS16
13B 23B 33B 43B	RW	RFTS31	RFTS30	RFTS29	RFTS28	RFTS27	RFTS26	RFTS25	RFTS24
13C 23C 33C 43C	RW	TFTS7	TFTS6	TFTS5	TFTS4	TFTS3	TFTS2	TFTS1	TFTS0
13D 23D 33D 43D	RW	TFTS15	TFTS14	TFTS13	TFTS12	TFTS11	TFTS10	TFTS9	TFTS8
13E 23E 33E 43E	RW	TFTS23	TFTS22	TFTS21	TFTS20	TFTS19	TFTS18	TFTS17	TFTS16
13F 23F 33F 43F	RW	TFTS31	TFTS30	TFTS29	TFTS28	TFTS27	TFTS26	TFTS25	TFTS24

Software Reset and Loopback Control Register (See descriptions on page 146)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
105 205 305 405	RW	SRST	Reserved (Set to 0)			PAYL	TX1S	RLP	LLP

System AIS and Test Registers (See descriptions on page 147)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
106 206 306 406	RW	Reserved (Set to 0)		TS16YE	NFASE	INSPRBS	SFZ	RXFS	TXFS
107 207 307 407	RW	AIS16	STUAIS	SYSALL1	CRC	FASE	RAIE	AISE	BPV

E1 Status and Mask Registers (See descriptions on page 149)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
109 209 309 409	RW	MLOS	MAIS	MOOF	MRAI	MCFA	MOOMF	MTXSLIP	MRXSLIP
110 210 310 410	R	LOS	AIS	OOF	RAI	CFA	OOMF	TXSLIP	RXSLIP
111 211 311 411	RW	LLOS	LAIS	LOOF	LRAI	LCFA	LOOMF	LTXSLIP	LRXSLIP
112 212 312 412	RW	PLOS	PAIS	POOF	PRAI	PCFA	POOMF	PTXSLIP	PRXSLIP
113 213 313 413	RW	FLOS	FAIS	FOOF	FRAI	FCFA	FOOMF	FTXSLIP	FRXSLIP

Counters and Counter Shadow Registers (See descriptions on page 154)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1EC 2EC 3EC 4EC	RW	LEBE7 - LEBE0 (Latched E-bit Error Counter Shadow Register, 10 bits)							
1ED 2ED 3ED 4ED	RW	LEBEO	Reserved (Set to 0)					LEBE9 - LEBE8	
1EE 2EE 3EE 4EE	RW	EBE7 - EBE0 (E-Bit Error Counter, 10 bits)							
1EF 2EF 3EF 4EF	RW	EBEO	Reserved (Set to 0)					EBE9 - EBE8	
1F0 2F0 3F0 4F0	RW	LCRC7 - LCRC0 (Latched CRC-4 Error Counter Shadow Register, 10 bits)							
1F1 2F1 3F1 4F1	RW	LCRCO	Reserved (Set to 0)					LCRC9 - LCRC8	
1F2 2F2 3F2 4F2	RW	CRC7 - CRC0 (CRC-4 Error Counter, 10 bits)							
1F3 2F3 3F3 4F3	RW	CRCO	Reserved (Set to 0)					CRC9 - CRC8	
1F4 2F4 3F4 4F4	RW	LCV7 - LCV0 (Latched Coding Violation Counter Shadow Register, 16 bits)							
1F5 2F5 3F5 4F5	RW	LCV15 - LCV8 (Latched Coding Violation Counter Shadow Register, 16 bits)							
1F6 2F6 3F6 4F6	RW	LCVO	Reserved (Set to 0)						
1F7 2F7 3F7 4F7	RW	CV7 - CV0 (Coding Violation Counter, 16 bits)							
1F8 2F8 3F8 4F8	RW	CV15 - CV8 (Coding Violation Counter, 16 bits)							
1F9 2F9 3F9 4F9	RW	CVO	Reserved (Set to 0)						
1FA 2FA 3FA 4FA	RW	LFBE7 - LFBE0 (Latched Framing Word Error Counter Shadow Register, 13 bits)							
1FB 2FB 3FB 4FB	RW	LFBEO	Reserved (Set to 0)		LFBE12-LFBE8				
1FC 2FC 3FC 4FC	RW	FBE7 - FBE0 (Framing Word Error Counter, 13 bits)							
1FD 2FD 3FD 4FD	RW	FBEO	Reserved (Set to 0)		FBE12-FBE8				
1FE 2FE 3FE 4FE	RW	Reserved (Set to 0)							
1FF 2FF 3FF 4FF	RW	Reserved (Set to 0)							

Operational Status Registers (See descriptions on page 158)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
114 214 314 414	R	TXS1	TXS0	RXS1	RXS0	TUAIS	TURAI	Reserved	
115 215 315 415	R	RXSF	TXSF	Reserved					LINT
11B 21B 31B 41B	R	NCRC4	ECRCE	RAIA	TS16ME	OOCRCM	OOTS16M	TS16AIS	LINEAIS

Slip Buffer Pointer Status Registers (See descriptions on page 160)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
120 220 320 420	RW	TWP7 - TWP0 (Transmit Slip Buffer Write Pointer)							
121 221 321 421	RW	TRP7 - TRP0 (Transmit Slip Buffer Read Pointer)							
122 222 322 422	RW	TWSBS	Reserved			TWPF3 - TWPF0 (Tx Write Pointer Frame)			
123 223 323 423	RW	TRSBS	Reserved			TRPF3 - TRPF0 (Tx Read Pointer Frame)			
124 224 324 424	RW	RWP7 - RWP0 (Receive Slip Buffer Write Pointer)							
125 225 325 425	RW	RRP7 - RRP0 (Receive Slip Buffer Read Pointer)							
126 226 326 426	RW	RWSBS	Reserved			RWPF3 - RWPF0 (Rx Write Pointer Frame)			
127 227 327 427	RW	RRSBS	Reserved			RRPF3 - RRPF0 (Rx Read Pointer Frame)			
128 228 328 428	RW	Reserved							
129 229 329 429	RW	Reserved							

Receive Time Slot Control Registers (See descriptions on page 161)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12A 22A 32A 42A	RW	RSIS	Reserved (Set to 0)		RSA4S - RSA8S (Rx National Bit Selection)				
12B 22B 32B 42B	RW	Reserved (Set to 0)					RX2S - RX0S		
1E0 2E0 3E0 4E0	RW	RDE7 - RDE1 (Rx Time Slots 7-1 Selection)							R (0)
1E1 2E1 3E1 4E1	RW	RDE15 - RDE8 (Rx Time Slots 15-8 Selection)							
1E2 2E2 3E2 4E2	RW	RDE23 - RDE16 (Rx Time Slots 23-16 Selection)							
1E3 2E3 3E3 4E3	RW	RDE31 - RDE24 (Rx Time Slots 31-24 Selection)							

Receive Time Slot Registers (See descriptions on page 163)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
140 240 340 440	RW	RFAS - Receive Frame Alignment Pattern FAS (Time Slot 0 - Frame 1)							
141 - 15F Ch 1 241 - 25F Ch 2 341 - 35F Ch 3 441 - 45F Ch 4	RW	Frame 1 RTS1-RTS31 (Receive Time Slots TS1 - TS31) X41 - Time Slot 1 X5F - Time Slot 31							
160 260 360 460	RW	RNFAS - Receive No Frame Alignment Pattern NFAS (Time Slot 0 - Frame 2)							
161 - 17F Ch 1 261 - 27F Ch 2 361 - 37F Ch 3 461 - 47F Ch 4	RW	Frame 2 RTS1-RTS31 (Receive Time Slots TS1 - TS31) X61 - Time Slot 1 X7F - Time Slot 31							

Transmit Time Slot Control Registers (See descriptions on page 164)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12C 22C 32C 42C	RW	TSIS	Reserved		TSA4S - TSA8S (Tx National Bit Selection)				
12D 22D 32D 42D	RW	Reserved (Set to 0)					TX2S - TX0S		
12E 22E 32E 42E	RW	Reserved (Set to 0)							
12F 22F 32F 42F	RW	Reserved (Set to 0)							
1E4 2E4 3E4 4E4	RW	TDE7 - TDE1 (Tx Time Slots 7-1 Selection)							R (0)
1E5 2E5 3E5 4E5	RW	TDE15 - TDE8 (Tx Time Slots 15-8 Selection)							
1E6 2E6 3E6 4E6	RW	TDE23 - TDE16 (Tx Time Slots 23-16 Selection)							
1E7 2E7 3E7 4E7	RW	TDE31 - TDE24 (Tx Time Slots 31-24 Selection)							

Transmit Time Slot Registers (See descriptions on page 166)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
190 290 390 490	RW	TFAS - Transmit Frame Alignment Pattern FAS (Time Slot 0 - Frame 1)							
191 - 1AF Ch 1 291 - 2AF Ch 2 391 - 3AF Ch 3 491 - 4AF Ch 4	RW	Frame 1 TTS1-TTS31 (Transmit Time Slots TS1 - TS31) X91 - Time Slot 1 XAF - Time Slot 31							
1B0 2B0 3B0 4B0	RW	TNFAS - Transmit No Frame Alignment Pattern NFAS (Time Slot 0 - Frame 2)							
1B1 - 1CF Ch 1 2B1 - 2CF Ch 2 3B1 - 3CF Ch 3 4B1 - 4CF Ch 4	RW	Frame 2 TTS1-TTS31 (Transmit Time Slots TS1 - TS31) XB1 - Time Slot 1 XCF - Time Slot 31							

Signaling Control Registers (See descriptions on page 167)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1E8 2E8 3E8 4E8	RW	SE8 - SE1 (Signaling Enable for Channels 8-1 Selection)							
1E9 2E9 3E9 4E9	RW	SE16 - SE9 (Signaling Enable for Channels 16-9 Selection)							
1EA 2EA 3EA 4EA	RW	SE24 - SE17 (Signaling Enable for Channels 24-17 Selection)							
1EB 2EB 3EB 4EB	RW	Reserved		SE30 - SE25 (Signaling Enable for Channels 30-25 Selection)					

Receive and Transmit Signaling Registers (See descriptions on page 168)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
180 280 380 480	RW	Receive Multiframe Pattern RSIGMAS (0000)				RX0	RY	RX1	RX2
181 - 18F Ch 1 281 - 28F Ch 2 381 - 38F Ch 3 481 - 48F Ch 4	RW	Receive Signaling Bits RA1-RD1 (A1 B1 C1 D1) to RA15-RD15 (A15 B15 C15 D15)				Receive Signaling Bits RA16-RD16 (A16 B16 C16 D16) to RA30-RD30 (A30 B30 C30 D30)			
1D0 2D0 3D0 4D0	RW	Transmit Multiframe Pattern TSIGMAS (0000)				TX0	TY	TX1	TX2
1D1 - 1DF Ch 1 2D1 - 2DF Ch 2 3D1 - 3DF Ch 3 4D1 - 4DF Ch 4	RW	Transmit Signaling Bits TA1-TD1 (A1 B1 C1 D1) to TA15-TD15 (A15 B15 C15 D15)				Transmit Signaling Bits TA16-TD16 (A16 B16 C16 D16) to TA30-TD30 (A30 B30 C30 D30)			

HDLC Link Control Registers (See descriptions on page 176)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
108 208 308 408	RW	EHR	EHT	TAB	EOM	RHIE	THIE	Reserved	
10B 20B 30B 40B	RW	Reserved (Set to 0)							
10C 20C 30C 40C	RW	Reserved (Set to 0)			SA4	SA5	SA6	SA7	SA8

HDLC Link Transmit and Receive Data Registers (See descriptions on page 177)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10A 20A 30A 40A	W	THD7-THD0 (HDLC Transmit Data)							
117 217 317 417	R	RHD7-RHD0 (HDLC Receive Data)							
118 218 318 418	RW	Reserved (Set to 0)			C4 - C0 (HDLC Receive FIFO Depth)				

HDLC Link Status Registers (See descriptions on page 178)

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10E 20E 30E 40E	RW	ERHIS2 - ERHIS0			ETHIS	ERXFS1 - ERXFS0		ETXFS1 - ETXFS0	
10F 20F 30F 40F	RW	MRHIS2 - MRHIS0			MTHIS	MRXFS1 - MRXFS0		MTXFS1 - MTXFS0	
116 216 316 416	R	RHIS2 - RHIS0			THIS	RXFS1 - RXFS0		TXFS1 - TXFS0	
119 219 319 419	RW	Reserved (Set to 0)							

Spare Registers

The following registers are designated as spare. They must not be accessed for read or write operations by the microprocessor.

007H, 008H, 009H, 00DH, 00FH, 01CH to 0FEH, X0DH, X1CH and X1DH.

Reserved Registers

The following read/write registers and bit locations in read/write registers are designated as reserved and require zeros to be written into them. Some of these bits are designated as internal test bits, etc.

Global Registers

Register	Bits	Comments
013	2	Write a 0 to this bit location
014	7 - 0	Write a 0 to these bit locations
015	7 - 0	Write a 0 to these bit locations
016	7 - 0	Write a 0 to these bit locations
019	2	Write a 0 to this bit location
01B	7, 6	Write a 0 to these bit locations
0FF	6, 5	Write a 0 to these bit locations
0FF	1, 0	Write a 0 to these bit locations

Per Framer Registers (X = 1, 2, 3, 4)

Register	Bits	Comments
X00	5, 3	Write a 0 to these bit locations
X05	6 - 4	Write a 0 to these bit locations
X06	7, 6	Write a 0 to these bit locations
X08	1, 0	Write a 0 to these bit locations
X0B	7 - 0	Write a 0 to these bit locations
X0C	7 - 5	Write a 0 to these bit locations

Register	Bits	Comments
X18	7 - 5	Write a 0 to these bit locations
X19	7 - 0	Write a 0 to these bit locations
X2A	6, 5	Write a 0 to these bit locations
X2B	7 - 3	Write a 0 to these bit locations
X2C	6, 5	Write a 0 to these bit locations
X2D	7 - 3	Write a 0 to these bit locations
X2E	7 - 0	Write a 0 to these bit locations
X2F	7 - 0	Write a 0 to these bit locations
XE0	0	Write a 0 to this bit location
XE4	0	Write a 0 to this bit location
XEB	7, 6	Write a 0 to these bit locations
XED	6 - 2	Write a 0 to these bit locations
XEF	6 - 2	Write a 0 to these bit locations
XF1	6 - 2	Write a 0 to these bit locations
XF3	6 - 2	Write a 0 to these bit locations
XF6	6 - 0	Write a 0 to these bit locations
XF9	6 - 0	Write a 0 to these bit locations
XFB	6 - 5	Write a 0 to these bit locations
XFD	6 - 5	Write a 0 to these bit locations
XFE	7 - 0	Write a 0 to these bit locations
XFF	7 - 0	Write a 0 to these bit locations

MEMORY MAP DESCRIPTIONS

COMMON REGISTERS

Device ID Registers

The manufacturer ID, part number and version of the QE1F-*Plus* are implemented in registers 000H - 003H with read-only capability. The manufacturer ID is 107 (decimal), and has been assigned for TranSwitch by the Joint Electron Device Engineering Council (JEDEC) of the Solid State Products Engineering Council. This field is 12 bits in length (06BH), and is assigned to bits 3 through 0 in register 001H, and bits 7 through 1 (LSB) in register 000H and a fixed 1 bit in bit 0 of register 000H, (i.e., 0000 11010111 or 0D7H.), as shown above in the Memory Map section. The part number is 16 bits long. The internal part number for the QE1F-*Plus* is 03105 (decimal). The binary value (0C21H) is assigned to bits 3-0 in register 003H, bits 7-0 in register 002H, and bits 7-4 (LSB) in register 001H. The Revision Level in bits 7-4 of register 003H represents the version number of the device and will vary as the device evolves. The current value is 0H.

Customer Notebook Register

The read/write bits in this register location are provided for use by the customer's application software.

Address	Bit	Symbol	Description
004	7-0	Notebook	**User Defined Register:** The bits in this read/write register are provided for use by the application software. The contents of this register will have no direct effect on the operation of the QE1F-*Plus*.

Global Software Register

The control bits in this read/write register location are used for resetting the QE1F-*Plus*.

Address	Bit	Symbol	Description
005	7-0	RESET	**Software Reset:** Writing a 91H into this location will reset the QE1F-*Plus*. Writing a value other than 91H will remove the QE1F-*Plus* from the reset state. Reading this location provides a value of 00H if the QE1F-*Plus* is not in reset, and 01H if the QE1F-*Plus* is reset. The QE1F-*Plus* defaults to reset deactivation on an external hardware reset (e.g., power-up). At least 40 ms after power-up, a software reset should be applied to this register location in order to clear the QE1F-*Plus* prior to programming the register positions. The software reset resets the internal state machines. The control registers, performance counters and the latched/shadow registers are not affected by this reset. In addition to this global reset byte, each of the four framers has an individual software reset bit, which is assigned to bit 7 (SRST) in register location X05H (where X corresponds to the framer's number, n).

Global Configuration Registers

The bits in these read/write registers control QE1F-*Plus* operations on a global basis for all four framers.

Address	Bit	Symbol	Description
006	7	GIM	**Global Interrupt Mask Bit:** A 1 disables (masks) the hardware interrupt pin (pin 125). When not masked (0), any latched status event (if not masked by the corresponding event mask bit) causes a hardware interrupt to occur.
	6	RISE	**Rising Edge Latched Status Event Bits Enable:** This bit works in conjunction with the FALL control bit (bit 5) to provide the following states for controlling the setting of the latched status event indication bits for the four framers. RISE / FALL / Action 0 / 0 / Latched status bit indications for all framers disabled. Hardware interrupt indication disabled. 0 / 1 / Latched status indication bits for all framers set on a negative status event bit indication transition. 1 / 0 / Latched status indication bits for all framers set on a positive status event bit indication transition. 1 / 1 / Latched status indication bits for all framers set on both a positive and a negative status event bit indication transition.
	5	FALL	**Falling Edge Latched Status Event Bits Enable:** Works in conjunction with the RISE control bit according to the table given above.
	4	IPOL	**Hardware Interrupt Polarity Sense:** When set to 1, the polarity of the hardware interrupt pin (pin 125) is inverted from active high to active low for the Intel microprocessor bus. When the Motorola microprocessor bus is selected, the polarity of the hardware interrupt pin (pin 125) is inverted from active low to active high.
	3	ENPMFM	**Enable Performance Monitoring and Fault Monitoring Feature:** When set to 1, the monitoring feature for the shadow registers (X12H and X13H) and latched counters (XECH, XEDH, XF0H, XF1H, XF4H, XF5H, XF6H, XFAH, and XFBH) is enabled. The register bits set on the rising edges of the one second pulse, which must be present on the T1SI pin (pin 40). When set to 0, the monitoring feature is disabled.
	2	HMVIP	**Multi-Vendor Integration Protocol:** This control bit works in conjunction with the MTP16M control bit (bit 1) and the CONFIG1 lead (pin 43) to provide the following system highway modes of operation. CONFIG1 / HMVIP / MTP16M / System Interface Low / 0 / 0 / 2 Mbit/s Transmission Mode Low / 1 / 0 / 8 Mbit/s Transmission Mode Low / 0 / 1 / 16 Mbit/s Transmission Mode High / 0 / 0 / 2 Mbit/s MVIP Mode High / 1 / 0 / 8 Mbit/s H-MVIP/H.100 Mode High / 0 / 1 / 16 Mbit/s PCM Highway Mode X / 1 / 1 / Not valid, do not use

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>006
(cont.)</td><td>1</td><td>MTP16M</td><td>Multiplexed 16 Mbit/s Format: This control bit works in conjunction with the HMVIP control bit (bit 2) and the CONFIG1 lead (pin 43) to provide the system highway modes of operation, as listed in the table above.</td></tr>
<tr><td></td><td>0</td><td>ENHWM</td><td>Enable Hardware Mask Hierarchy: When this bit is set to 1, the masking hierarchy for the alarms is enabled according to the table below:
Alarm Suppression Table (Shaded Columns indicate suppressed alarms)
<table>
<tr><th>Direction</th><th>LOS</th><th>Line AIS</th><th>OOF</th><th>RAI</th><th>CRC OOMF</th><th>TS16 OOMF</th><th>TS16 AIS</th><th>SLIPS</th></tr>
<tr><td rowspan="3">Line Port to System</td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>01A</td><td>7-0</td><td>LOSI7-LOSI0</td><td>Loss of Signal Detection and Recovery Interval Select: The binary value written to this register selects the number of consecutive missing pulses used to declare loss of signal. The normal range is between 10 and 255. Bit 0 is the LSB. This value is also used to set the duration of the recovery interval (see register 01BH).</td></tr>
<tr><td>01B</td><td>7-6</td><td>Reserved</td><td>Reserved: Set to 0.</td></tr>
<tr><td></td><td>5-0</td><td>OND5-OND0</td><td>Ones Density Loss of Signal Recovery Threshold Select: The binary value written to this register selects the minimum number of ones that must occur in the recovery interval set up by register 01AH to recover loss of signal. This value must be less than the value written in register 01AH. For a loss of signal recovery interval value of 255, the recovery threshold value is normally set to 32. Bit 0 is the LSB.</td></tr>
<tr><td>0FF</td><td>7</td><td>WGDEC</td><td>Test Equipment BPV Selection: A 1 enables the decoder to detect coding violations as found in certain test equipment (e.g., Wandel & Golterman™). A 0 enables the decoder to detect coding violations as found in other types of test equipment (e.g., Tberd™). The following table summarizes the two decoding procedures of coding violations:
<table>
<tr><th>BPV HDB3</th><th>1 (W & G)</th><th>0 (Tberd)</th></tr>
<tr><td>+ + or - -</td><td>000 (preceding bit changed)</td><td>11</td></tr>
<tr><td>0BV or 000V</td><td>0000</td><td>1010 or 0001</td></tr>
<tr><td>BB00V after odd</td><td>1000</td><td>1101</td></tr>
<tr><td>BB00V after even</td><td>1000</td><td>1001</td></tr>
</table></td></tr>
<tr><td></td><td>6-5</td><td>Reserved</td><td>Reserved: Set to 0.</td></tr>
<tr><td></td><td>4</td><td>ENTSLB</td><td>Enable Time Slot Loopback Feature: A 1 enables the time slot loopback feature for the four framers. Time slot loopbacks occur when the corresponding control bits TFTS31-TFTS0 are written with a 1. Pins RCLKn and RSYNCn must be connected to pins TCLKn and TSYNCn respectively to prevent data errors in the looped back time slots.</td></tr>
</table>

Address	Bit	Symbol	Description
0FF (cont.)	3	AAGS	**Alternative Alarm Generation Selection:** When set to a 1, A-bit and E-bit alarm generation with respect to out of frame and out of multiframe behave as specified in ETS 300 011 (also see ITU-T G.704, G.706, 1988). A bit (RAI) will be set to a 1 for at least one NFAS frame pattern each time a search for multiframe alignment is performed (which is every 8 ms until multiframe alignment is achieved). E-bits will be set to 1 unless CRC-4 errors are detected after multiframe alignment is achieved. Note: CRCA must be set to 1 for normal operation. See control bit CRCA description (bit 3 in register X04H) for operation when CRCA is set to 1. One E-bit may be set to 0 immediately after the QE1F-*Plus* frames up, even though the first CRC-4 is correct. When set to a 0, A-bit and E-bit alarm generation with respect to out of frame and out of multiframe should behave as specified in ITU-T G.704, G.706, 1991. In this case the E-bits are set to 0 and the A-bit is set to 1 initially. When basic frame alignment is reached the A-bit is set to 0. The A-bit is only set to 1 again if basic frame alignment is lost due to loss of the Time Slot 0 FAS and NFAS codes or excessive CRC-4 errors after multiframe alignment is reached (not if an alternate frame position is chosen or if multiframe alignment can not be reached). The E-bits are set to 1 once multiframe alignment is reached, one E-bit toggling to 0 for each sub-multiframe error detected in a multiframe using the CRC-4 check.
	2	H100	**H.100/H-MVIP Selection:** A 1 enables the H.100 synchronization pulse option when CONFIG1 (pin 43) is high, and control bits HMVIP and MTP16M are set to 10 respectively (bits 2 and 1 of register 006H). In this mode the nominal pulse widths of RSYNC1 and TSYNC1 are two clock periods of RCLK1 and TCLK1 respectively. The active low RSYNC1 and TSYNC1 signals straddle the transition between bit 8 of Time Slot 31 of framer number 4 and bit 1 of Time Slot 0 of framer number 1. A 0 enables the H-MVIP synchronization pulse option when CONFIG1 (pin 43) is high, and control bits HMVIP and MTP16M are set to 10 respectively (bits 2 and 1 of register 006H). In this mode the nominal pulse widths of RSYNC1 and TSYNC1 are four clock periods of RCLK1 and TCLK1 respectively. The active low RSYNC1 and TSYNC1 signals straddle bit 8 of Time Slot 31 of framer number 4 and bit 1 of Time Slot 0 of framer number 1.
	1-0	Reserved	**Reserved:** Set to 0.

Global Status Indication, Mask and Pointer Registers

These registers are read-only, except for the mask register 00BH, which is read/write. The bits in the Global Status Indication Register 00AH indicate an alarm caused by a line event on a global basis (i.e., in any framer). If the corresponding mask bit is written with a 1 in the E1 Mask Register (X09H) it prevents an interrupt generation, but the global indication will be present in register 00AH. Each event bit is formed by or-gating the corresponding event bits in each of the four framer channels (registers X10H) to provide the individual status indication in register 00AH. A 1 written into a bit position in the Global Mask Register 00BH will mask the interrupt indication for the corresponding bit position in register 00AH. The bits in register locations 00CH and 00EH provide a pointer to the framer which caused the line or HDLC link latched event.

Global Status Indication Register

Address	Bit	Symbol	Description
00A	7	GLOS	**Global Loss of Signal (LOS) Indication:** This bit is a 1 when any of the four framer channels has detected a loss of signal alarm.
	6	GAIS	**Global AIS Indication:** This bit is a 1 when any of the four framer channels has detected an AIS alarm.
	5	GOOF	**Global Out of Frame (OOF) Indication:** This bit is a 1 when any of the four framer channels has detected an Out Of Frame alarm.
	4	GRAI	**Global Remote Alarm Indication (RAI):** This bit is a 1 when any of the four framers has detected an RAI alarm.
	3	GCFA	**Global Change In Frame Alignment (CFA) Indication:** This bit is a 1 when any of the four framer channels has detected a change in frame alignment.
	2	GOOMF	**Global Out Of Multiframe Alignment (OOMF) Indication:** This bit is a 1 when any of the framer channels has detected an out of multiframe alignment alarm.
	1	GTXSLIP	**Global Transmit Slip Indication:** This bit is a 1 when any of the four framer channels has detected a transmit slip.
	0	GRXSLIP	**Global Receive Slip Indication:** This bit is a 1 when any of the four framer channels has detected a receive slip.

Global Interrupt Mask Register

Address	Bit	Symbol	Description
00B	7	GMLOS	**Global Loss of Signal (LOS) Mask Bit:** When set to 1, a loss of signal alarm detected in any framer channel (LLOS, registers X11H) is masked from providing an interrupt indication.
	6	GMAIS	**Global AIS Mask Bit:** When set to 1, an AIS condition detected in any framer channel (LAIS, registers X11H) is masked from providing an interrupt indication.
	5	GMOOF	**Global Out of Frame (OOF) Mask Bit:** When set to 1, an Out Of Frame alarm detected in any framer channel (LOOF, registers X11H) is masked from providing an interrupt indication.
	4	GMRAI	**Global Remote Alarm Indication (RAI) Mask Bit:** When set to 1, an RAI in any framer channel (LRAI, registers X11H) is masked from providing an interrupt indication.
	3	GMCFA	**Global Change In Frame Alignment (CFA) Mask Bit:** When set to 1, a change in frame alignment indication in any framer channel (LCFA, registers X11H) is masked from providing an interrupt indication.
	2	GMOOMF	**Global Out of Multiframe Alignment (OOMF) Mask Bit:** When set to 1, an out of multiframe alarm detected in any framer channel (LOOMF, registers X11H) is masked from providing an interrupt indication.
	1	GMTXSLIP	**Global Transmit Slip Indication Mask Bit:** When set to 1, a transmit slip detected in any framer channel (LTXSLIP, registers X11H) is masked from providing an interrupt indication.
	0	GMRXSLIP	**Global Receive Slip Indication Mask Bit:** When set to 1, a receive slip detected in any framer channel (LRXSLIP, registers X11H) is masked from providing an interrupt indication.

Global Pointer Registers

Address	Bit	Symbol	Description
00C	7-4	Reserved	**Reserved:** Disregard these bits.
	3-0	CHA4-CHA1	**Channel Activity Line Events for Channels 4-1:** A 1 in a bit position points to (indicates) the framer channel that caused the global status indication because of a line event (e.g., loss of signal). For example, 0011 indicates that channels 2 and 1 have a latched line event.
00E	7-4	Reserved	**Reserved**: Disregard these bits.
	3-0	CHDL4-CHDL1	**Channel Activity HDLC Link Event for Channels 4-1:** A 1 in a bit position points to (indicates) the framer channel that caused the global status indication because of a HDLC link event (e.g., receive FIFO event). For example, 1000 indicates that channel 4 has a latched data link event.

Line Interface Control and Monitoring Registers

These registers are read/write, except for register 012H, which is read-only unlatched. The control bits in these registers determine the Line Interface Control information flow between the QE1F-*Plus* and the external line interface transceivers, enable the pseudo-random generator and analyzer, and enable the monitor mode for the QE1F-*Plus*. The Line Interface Control feature is enabled by placing a low on the CONFIG2 pin (pin 42).

Address	Bit	Symbol	Description
010	7-0	LCB7-LCB0	**Line Interface Control Command Byte:** The bits in this register contain the command byte for the external line interface transceiver. The contents of the command byte written into this location depend on the transceiver selected. Please consult the transceiver data sheet for the appropriate codes. The command byte is transmitted via the Line Interface Control serial port output (LSDO). This byte is shifted out of this register starting with bit LCB0 first, and represents the first byte transmitted on the LSDO pin (pin 60).
011	7-0	LDO7-LDO0	**Line Interface Control Serial Data Output Byte:** The bits in this register contain the data byte which is written to the selected external line interface transceiver. The data byte is transmitted via the Line Interface Control serial port output (LSDO). This byte is shifted out of this register starting with bit LDO0 first, and represents the second byte transmitted on the LSDO pin.
012	7-0	LDI7-LDI0	**Line Interface Control Serial Data Input Byte:** The bits in this register contain the data byte which is read from the selected external line interface transceiver. The data byte is received via the Line Interface Control serial port input (LSDI). This byte is shifted into this register starting with bit LDI0 first.
013	7	BDCST	**Broadcast Command:** When this bit is set to 1, the two bytes in the Line Interface Control Command and Serial Data Output Byte registers are broadcasted to all external line interface transceivers. This is accomplished by forcing all line interface chip select signals ($\overline{\text{LCSn}}$) active low. This feature is disabled in the Internal E1 Monitor Mode (CONFIG2 pin is low).
	6	PRBSFR	**PRBS Framed Mode**: When this bit is set to 1, the internal 2^{15}-1 PRBS generator and analyzer are configured to operate in the framed mode, which means that the channel's Transmit Framer block generates framing. When set to 0 for unframed mode, the internal 2^{15}-1 PRBS generator and analyzer are configured to operate on all of the bits in the transmit and receive data highways. Both the framer and the PRBS generator and analyzer must be set to the same mode. If PRBSFR = 1, then CRCMD1-CRCMD0 $\neq$ 00 (bits 2-1 in register X04H). If PRBSFR = 0, then CRCMD1-CRCMD0 = 00.

Address	Bit	Symbol	Description
013 (cont.)	5	PRBSEN	**PRBS Enable:** When this bit is set to 1, the internal 2^{15}-1 PRBS analyzer is enabled in the 2 Mbit/s Transmission Mode only. The E1 Channel Selection bits (bits 1 and 0) in this register select which channel's receive data highway is connected to the analyzer. The state of the analyzer is provided on pin PRBSOOL. A low on this pin indicates that the analyzer is locked, while a high indicates the unlocked state. The recovered line clock is the clock source for the analyzer. If the receive slip buffer is enabled, its read clock source is the LRCLKn input pin. The LO input pin is the clock source for the generator. If the transmit slip buffer is enabled, then the input LO must be synchronous and in phase with TCLKn.
	4	ESP/EMON	**Enable Serial Port:** This feature is enabled when a low is placed on the CONFIG2 pin. When set to 1, a single transfer takes place between the external line interface transceiver and its associated QE1F-*Plus* framer via the Line Interface Control serial port. The external transceiver is accessed by an active low chip select signal ($\overline{\text{LCSn}}$) for the transceiver selected by the E1 selection bits, bits 1 and 0 in this register. This bit must be first set to 0 and then to 1 before another transfer is enabled. **Enable Monitor Port:** When the Internal E1 Monitor mode is selected by placing a high on the CONFIG2 pin, a 1 enables the NRZ data stream via the MONCLK and MONDTO pins. A 0 causes the MONCLK and MONDTO pins to be tri-stated.
	3	RXTX	**RX or TX Monitor Selection:** When the internal E1 Monitor Mode is selected (a high is placed on the CONFIG2 pin), a 0 enables the transmit side to be monitored. A 1 enables the receive side to be monitored.
	2	Reserved	**Reserved:** Set to 0.
	1-0	E1CHCS1-E1CHCS0	**E1 Channel Selection:** Selects the external line interface transceiver, the internal E1 channel (framer) for monitoring and the receive data highway channel for the internal 2^{15}-1 PRBS analyzer, according to the table given below: Bit 1 / Bit 0 / Transceiver/E1 Monitored/Analyzer 0 0 Channel 1 0 1 Channel 2 1 0 Channel 3 1 1 Channel 4

Transmit and Receive Sync Delay Registers

The value written in register 017H controls the number of clock cycles the transmit sync pulse (TSYNCn) will be delayed relative to the transmit system clock (TCLKn). The value written in register 018H controls the number of clock cycles the receive system sync pulse (RSYNCn) will be delayed relative to the receive system clock (RCLKn), when RSYNCn and RCLKn are set to be inputs (RXC=0).

Address	Bit	Symbol	Description
017	7-0	TSD7-TSD0	**Transmit Sync Delay:** The value written into this register location specifies the number of transmit clock cycles (TCLKn) that the transmit Sync signal (TSYNCn) is delayed internal to the QE1F-*Plus*. If no delay is required then 00 hex must be written into this register. For H-MVIP/ H.100, 8 Mbit/s and 16 Mbit/s transmission, and 16 Mbit/s PCM highway modes, the number of clock cycles delay is obtained by multiplying this value by 8.
018	7-0	RSD7-RSD0	**Receive Sync Delay:** The value written into this register location specifies the number of receive clock cycles (RCLKn) that the receive Sync signal (RSYNCn) is delayed internal to the QE1F-*Plus*. If no delay is required then 00 hex must be written into this register. For H-MVIP/ H.100, 8 Mbit/s and 16 Mbit/s transmission, and 16 Mbit/s PCM highway modes, the number of clock cycles delay is obtained by multiplying this value by 8.

Clock Reference Selection Register

The control bits in this read/write register are used to control the clock references for the QE1F-*Plus*.

Address	Bit	Symbol	Description
019	7-6	CR2S1-CR2S0	**Reference Channel Clock 2 Selection:** Selects the channel from which the reference clock CLKREF2 (pin 2) is derived, according to the table given below: Bit 7 / Bit 6 / Reference clock derived from 0 / 0 / Channel 1 0 / 1 / Channel 2 1 / 0 / Channel 3 1 / 1 / Channel 4
	5	ENREF2	**Enable Reference Clock 2:** When set to 1, the reference clock on CLKREF2 (pin 2) is enabled. The reference clock is selected by the Reference Channel Clock 2 Selection control bits (bits 7 and 6), and is derived from receive clock (LRCLKn) for the selected channel. When set to 0, CLKREF2 (pin 2) is tri-stated. Note: When set to 1, CLKREF2 will be forced low when a loss of signal is detected either locally (LOS), or from the external line interface transceiver when control bit LIE in Framer Configuration register X00H is a 1.
	4	2048KHZ	**2048 kHz Reference Clock Enable:** When set to one, the 2048 kHz reference clock selected by the Reference Channel Clock 2 Selection control bits is provided on the pins CLKREF2 and/or CLKREF1, when enabled. When set to zero, a divide by 256 circuit is placed between the receive line clock (LRCLKn) and pins CLKREF2 and/or CLKREF1, when enabled. The output will be 8 kHz reference signals.

Address	Bit	Symbol	Description
019 (cont.)	3	ENREF1	**Enable Reference Clock 1:** When set to 1, the reference clock on CLKREF1 (pin 46) is enabled. The reference clock is selected by the Reference Channel Clock 1 Selection control bits (bits 1 and 0), and is derived from receive clock (LRCLKn) for the selected channel. When set to 0, CLKREF1 (pin 46) is tri-stated. Note: When set to 1, CLKREF1 will be forced low when a loss of signal is detected either locally (LOS), or from the external line interface transceiver when control bit LIE in bit 1 of Framer Configuration register X00H is a 1.
	2	Reserved	**Reserved:** Set to 0.
	1-0	CR1S1-CR1S0	**Reference Channel Clock 1 Selection:** Selects the channel from which the reference clock CLKREF1 (pin 46) is derived, according to the table given below: Bit 1 / Bit 0 / Reference clock derived from 0 / 0 / Channel 1 0 / 1 / Channel 2 1 / 0 / Channel 3 1 / 1 / Channel 4

PER CHANNEL CONTROL AND STATUS INDICATION REGISTERS

Framer Configuration and Control Registers

The control bits in the following read/write registers are used to configure the QE1F-*Plus* for the various modes of operation on a per channel basis. In the following table, n indicates the channel (framer) number 1-4.

Address	Bit	Symbol	Description
100 - Ch 1 200 - Ch 2 300 - Ch 3 400 - Ch 4	7	RAIL	**Dual Unipolar/NRZ Mode Selection:** When set to 1, the line interface for channel n is configured to operate in the dual unipolar mode (rail interface). When set to 0, the line interface for channel n is configured to operate in the NRZ mode.
	6	BE	**HDB3 Enable:** When set to 1 in the dual unipolar mode, the HDB3 CODEC is enabled. When set to 0, the interface CODEC is configured for AMI. In the NRZ mode, the state of this bit sets the TMODEn output bit value (e.g., to enable an external HDB3 CODEC) when the Fast Sync feature is not selected.
	5	Reserved	**Reserved:** Set to 0.
	4	ENSRAI	**Enable Signaling Highway Remote Alarm:** Enabled in the Transmission Mode. When set to 1, a remote alarm indication (bit 3 in Time Slot 0 of alternating frames) in the transmit signaling highway (TSIGLn) causes the Remote Alarm Indication to be propagated to the line for channel n.
	3	Reserved	**Reserved:** Set to 0.
	2	ENSAIS	**Enable Signaling Highway AIS:** Enabled in the Transmission Mode. When set to 1, an AIS alarm detected in the transmit signaling highway (TSIGLn) causes the AIS condition to be propagated to the line for channel n.
	1	LIE	**General Purpose Interrupt Input Port (LINT) Enable:** When set to 1, the active true state present on the General Purpose Interrupt Input Port (LINTn pin) is logically or-gated with the internal LOS signal to form the LOS event and interrupt for channel n. Control bit LPOL (bit 0 in this register) determines the active true sense. An active true signal also causes the clock reference pins CLKREF1 (pin 46) and/or CLKREF2 (pin 2), when enabled, to be forced low.
	0	LPOL	**General Purpose Interrupt Input Port (LINT) Polarity Selection:** When set to 1, a low present on the General Purpose Interrupt Input Port for channel n (LINTn pin) is the active true state. When set to 0, a high present on the General Purpose Interrupt Input Port is the active true state.

Address	Bit	Symbol	Description
101 - Ch 1 201 - Ch 2 301 - Ch 3 401 - Ch 4	7	TXCP	**Transmit Clock Polarity Selection:** When set to 1, data for channel n is clocked out to the line on the rising edges of the transmit clock (LTCLKn). When set to 0, data is clocked out on the falling edges of the transmit clock (LTCLKn). Set to 0 for local loopback operation.
	6	RXCP	**Receive Clock Polarity Selection:** When set to 1, data for channel n is clocked in from the line on the rising edges of the receive clock (LRCLKn). When set to 0, data is clocked in on the falling edges of the receive clock (LRCLKn).
	5	TXNRZP	**Transmit NRZ Data Polarity Selection:** When set to 1, the polarity of the transmit NRZ data for channel n (TLDATn) is inverted.
	4	PWRD	**Power-Down Selection:** When set to 0, the channel enters the inactivated low power state in both the transmit and receive directions. The transmit data value is determined by control bit FPOL when forcing is enabled by control bit FDAT. Note: Control bit FDAT must be set to 1 in the power-down mode, otherwise the transmit data output state will be indeterminate.
	3	FDAT	**Force Transmit Data:** When set to 1, the transmit data state is forced to the state specified by control bit FPOL.
	2	FPOL	**Force Transmit Data Polarity:** This control bit is enabled when the FDAT control bit is set to 1. When set to 1, transmit data output for channel n is set to 1 (AIS). When set to 0, transmit data is set to 0. Note: The forcing function occurs prior to the selected line encoding function. The following table is a summary of the actions taken by control bits FDAT and FPOL. FDAT / FPOL / Action 0 / X / Normal Operation. 1 / 0 / Transmit data set to 0. 1 / 1 / Transmit data set to 1.
	1	BNAL	**Bypass National Bits:** Enabled in the Transmission Mode. When set to 1, the national bits from the signaling highway (TSIGLn) or microprocessor-written bits are used in place of the HDLC data link in the transmit direction.
	0	RXNRZP	**Receive NRZ Data Polarity Selection:** When set to 1, the polarity of the received NRZ data for channel n (RLDATn) is inverted.

Address	Bit	Symbol	Description
102 - Ch 1 202 - Ch 2 302 - Ch 3 402 - Ch 4	7-6	TXC1-TXC0	**Transmit Clock Selection:** These two bits select the clock source for clocking out data from the transmit slip buffer to the line interface according to the following table: TXC1 / TXC0 / Transmit clock source 0 / 0 / Local Oscillator (LO). 0 / 1 / System Transmit Clock (TCLKn). Only valid for 2 Mbit/s MVIP mode and Transmission Modes. 1 / 0 / Recovered Receive Line Clock (LRCLKn). 1 / 1 / Invalid combination (do not use).
	5	RXC	**Receive Clock Select:** This bit works in conjunction with control bit RSE for selecting the clock (and sync) source for shifting data out of the receive slip buffer to the system. See bit 3 below.
	4	TSE	**Transmit Slip Buffer Enable:** When set to 1, the transmit slip buffer is enabled. When set to 0, the transmit slip buffer is disabled, and data bypasses the slip buffer. This bit position must be written with a 1 in all operating modes, except the 2 Mbit/s Transmission Mode.
	3	RSE	**Receive Slip Buffer Enable:** This bit works in conjunction with the RXC bit for enabling and disabling the receive slip buffer according to the following table. This bit position must be written with a 1 in all operating modes, except the 2 Mbit/s Transmission Mode. RXC / RSE / Receive clock source/slip buffer 0 / 0 / System Receive Clock (RCLKn) and Sync Pulse (RSYNCn); Slip buffer disabled. Use of this setting is not recommended. 0 / 1 / System Receive Clock (RCLKn) and Sync Pulse (RSYNCn); Slip buffer enabled. Valid for all modes. 1 / 0 / Recovered Receive Clock (LRCLKn) and internal sync pulse; Slip buffer disabled. Valid for 2 Mbit/s Transmission Mode only. 1 / 1 / Recovered Receive Clock (LRCLKn) and internal sync pulse; Slip buffer enabled. Valid for 2 Mbit/s Transmission Mode only. Note**:** RSYNCn and RCLKn pins are outputs when RXC is set to 1.
	2	TSR	**Transmit Slip Buffer Recenter:** When set to 1, this bit forces the transmit slip buffer to recenter. Afterwards this bit should be written with a 0. While set to 0, the transmit slip buffer will recenter automatically to avoid the loss of data (programmed slip).
	1	RSR	**Receive Slip Buffer Recenter:** When set to 1, this bit forces the receive slip buffer to recenter. Afterwards this bit should be written with a 0. While set to 0, the receive slip buffer will recenter automatically to avoid the loss of data (programmed slip).
	0	FE1M	**Fractional E1 Mode:** A 1 written to this bit position enables the transmit and receive fractional E1 feature for the channel. A gapped clock for the time slot(s) selected is provided on the RFE1GCn and TFE1GCn leads. Receive time slots are selected by writing a 1 to or more control bits RFTS0-RFTS31 (X38H-X3BH). Transmit time slots are selected by writing a 1 to one or more control bits TFTS0-TFTS31 (X3CH-X3FH).

Address	Bit	Symbol	Description
103 - Ch 1 203 - Ch 2 303 - Ch 3 403 - Ch 4	7-6	TYP1-TYP0	**Signaling Type Selection:** The following table lists the signaling selection formats in the transmit and receive directions that are controlled by bits TYP1 and TYP0. TYP1 TYP0 Signaling type 0 0 Time Slot 16 assigned as a clear channel. 0 1 Time Slot 16 assigned for CAS. ABCD bits carried. ABCD = 0000 from the transmit signaling highway (TSIGLn pins) or transmit signaling RAM is transmitted as 1111. 1 0 Time Slot 16 assigned for CAS. ABCD bits carried. 1 1 Time Slot 16 CAS invert mode. The ABCD bits will be inverted from their present values. This option is effective only for the transmit direction. The Time Slot 16 (TS16) multiframe alignment pattern is generated only when the CAS or CAS-inverted signaling types are selected. TS16 multiframe alignment is meaningless in TS16 clear channel mode. TS16 multiframe alignment is independent of device mode.
	5	RXF	**Receive Signaling Freeze:** When set to 1, the received line signaling bits are disabled from being written into the receive signaling registers. The contents present in the receive signaling registers before this bit was set will be used for the receive signaling highway. While frozen, the contents of the receive signaling registers (X80H through X8FH) may be altered by the microprocessor and these altered values will be repeated on the receive signaling highways.
	4	TXF	**Transmit Signaling Freeze:** When set to 1, the transmit signaling highway bits are disabled from being written into the transmit signaling registers. The contents present in the transmit signaling registers before this bit was set will be used for the transmit line. While frozen, the contents of the transmit signaling registers (XD0H through XDFH) may be altered by the microprocessor and these altered values will be repeated in Time Slot 16. This allows for trunk conditioning or signaling control to be accomplished.
	3	RX_SIG_INV	**Time Slot 16 CAS Receive Signaling Invert:** When set to 1, same as for TYP1, TYP0 = 11 above, except that it is effective for the receive direction only.
	2	ENAIS	**Enable AIS:** When set to 1, detection of a line AIS causes the A-bits in the receive signaling highway RSIGLn to be set to 1 in the Transmission Modes. The A-bits are present in Time Slots 2 through 31 in the signaling highway format. When ENAIS=1, AIS will also be inserted on the receive data highway when control bit STUAIS (bit 6) in register X07H is a 1 in any of the Transmission, MVIP, H-MVIP/H.100 or 16 Mbit/s PCM Highway Modes.
	1	ENOOF	**Enable OOF:** When set to 1, detection of an Out Of Frame Alarm will cause the A-bits in the receive signal highway bit RSIGLn to be set to 1. The A-bits are present in Time Slots 2 through 31 in the signaling highway format. When ENOOF=1, AIS will also be inserted on the receive data highway when control bit STUAIS (bit 6) in register X07H is a 1 in any system interface mode.

Address	Bit	Symbol	Description
103 - Ch 1 203 - Ch 2 303 - Ch 3 403 - Ch 4 (cont.)	0	ENLOS	**Enable LOS:** When set to 1, detection of a Loss Of Signal will cause the A-bits in the receive signal highway bit RSIGLn to be set to 1. The A-bits are present in Time Slots 2 through 31 in the signaling highway format. When ENLOS=1, AIS will also be inserted on the receive data highway when control bit STUAIS (bit 6) in register X07H is a 1 in any system interface mode.
104 - Ch 1 204 - Ch 2 304 - Ch 3 404 - Ch 4	7-6	OOF1-OOF0	**Out Of Frame Detection Criteria:** The OOF bits determine the Out Of Frame detection criteria according to the following table: OOF1 OOF0 Out Of Frame detection criteria 0 0 Three consecutive FAS patterns in error. 0 1 Four consecutive FAS patterns in error. 1 0 Three consecutive FAS patterns in error or three consecutive NFAS patterns in error. 1 1 Four consecutive FAS patterns in error or four consecutive NFAS patterns in error. The FAS pattern is defined as X0011011, and the NFAS pattern is defined as X1XXXXXX. These two patterns occur in alternating frames.
	5	BFAA	**Basic Frame Alignment Algorithm**: When set to 0, the Standard algorithm is selected. When set to 1, the Frame Hold-Off algorithm is selected. Note: When in a particular mode, a change in state of this bit will trigger a realignment procedure. The Operations section describes the differences between the two modes (algorithms).
	4	CASA	**Channel Associated Signaling Alignment:** When set to 0, the Standard G.732 algorithm is selected. When set to 1, an Enhanced algorithm is selected. Note: When in a particular mode, a change in state of this bit will trigger a realignment procedure. The Operations section describes the differences between the two modes (algorithms).
	3	CRCA	**Automatic CRC-4/Non-CRC-4 Mode Selection:** When set to 0, the non-CRC-4 mode is selected. A search for the multiframe frame alignment is started in consecutive 8 ms periods. If alignment is not established in the 8 ms period, a new search is started. When set to 1 and control bit AAGS (bit 3 in register 0FFH) is set to 0, the automatic mode is selected for multiframe alignment. If alignment is not achieved in 400 ms, a non-CRC-4 Interworking (NCRC4) alarm indication (bit 7 in register X1BH) is set. The alarm inhibits further CRC-4 processing and causes the E-bits in Time Slot 0 to be transmitted as zeros. Note: When in a particular mode, a change in state of this bit will trigger a realignment procedure. See control bit AAGS description (bit 3 in register 0FFH) for operation when AAGS is set to 1.

Address	Bit	Symbol	Description
104 - Ch 1 204 - Ch 2 304 - Ch 3 404 - Ch 4 (cont.)	2-1	CRCMD1- CRCMD0	**CRC Framing Mode:** The CRCMD1 and CRCMD0 control bits determine the CRC framing mode, according to the table given below: CRCMD1 / CRCMD0 / CRC framing mode 0 / 0 / Transparent (Unframed) Mode. 0 / 1 / Framed mode. CRC-4 disabled. Si bit used. 1 / 0 / Framed mode. CRC-4 enabled. When in sync the E-bits carry the results to the distant end. When out of sync, the E-bits are 0. 1 / 1 / Framed mode. CRC-4 enabled. The E-bits are always set to 1.
	0	RSYC	**Resync Enable:** A 1 causes the framer to reset the frame alignment circuit, and start the search for a new frame alignment pattern.
11A - Ch 1 21A - Ch 2 31A - Ch 3 41A - Ch 4	7	AUTY	**Automatic Y-Bit Response Enable:** The Y-bit is defined as a Remote Multiframe Alarm Indication in Time Slot 16. A 1 enables a loss of multiframe alignment, as selected by the EOO16M (bit 2) and EOOCRC (bit 3) bits, on the receive side to cause the Y-bit (bit 6) in Time Slot 16 in frame 0 of the multiframe to be transmitted as a 1. A 0 disables this automatic feature. Note: The microprocessor can generate a Remote Multiframe Alarm Indication independent of this feature by writing a 1 to control bit TS16YE (bit 5) in register X06H.
	6	AUTRAI	**Automatic RAI Bit Response Enable:** The RAI bit is defined as a Remote Alarm Indication, and it is carried in bit 3 in Time Slot 0 in the (NFAS) frames which are not carrying the frame alignment pattern. A 1 enables a loss of basic frame alignment on the receive side to be transmitted as an RAI on the transmit side. Note: The microprocessor can generate a Remote Alarm Indication independent of this feature by writing a 1 to control bit RAIE (bit 2) in register X07H.
	5	ENRAIA	**Enable RAI Status from A-Bit:** A 1 enables the detection of the A-bit in the TS0 of odd-numbered frames to produce RAI status (bit 4 in register X10H).
	4	ENRAIY	**Enable RAI Status from Y-Bit:** A 1 enables the detection of the Y-bit in TS16 to produce RAI status (bit 4 in register X10H).

Address	Bit	Symbol	Description
11A - Ch 1 21A - Ch 2 31A - Ch 3 41A - Ch 4 (cont.)	3	EOOCRC	**Enable Out Of Multiframe Alarm on Loss of CRC Multiframe:** A 1 enables a Time Slot 0 loss of CRC multiframe to cause an Out Of Multiframe alarm. When enabled, an Out of Multiframe Alarm may also be caused by a Time Slot 0 loss of multiframe alignment. The following table summarizes the enable bits associated with the Out Of Multiframe alarm. EOOCRC / EOO16M / Action 0 / 0 / Out Of Multiframe alarm disabled. 0 / 1 / A Time Slot 16 Loss Of Multiframe causes an Out Of Multiframe alarm. 1 / 0 / A Time Slot 0 Loss Of CRC multiframe causes an Out Of Multiframe alarm. 1 / 1 / A Time Slot 16 Loss Of Multiframe or a Time Slot 0 Loss Of CRC multiframe causes an Out Of Multiframe alarm.
	2	EOO16M	**Enable Out Of Multiframe Alarm on Time Slot 16 Loss of Multiframe:** A 1 enables a Time Slot 16 loss of multiframe to cause an Out Of Multiframe alarm. When enabled, a Out of Multiframe Alarm may also be caused by Time Slot 0 loss of CRC multiframe alignment. The table given above summarizes the operation of this bit.
	1	E16AIS	**Enable AIS Indication on AIS Detected in Time Slot 16:** A 1 enables an AIS detected in Time Slot 16 to cause an AIS alarm. When enabled, detection of a line AIS may be enabled to cause an AIS alarm by setting bit ENLAIS to 1. The following table summarizes the enable bits associated with the AIS alarm. E16AIS / ENLAIS / Action 0 / 0 / AIS Alarm Disabled. 0 / 1 / Line AIS detected causes an AIS alarm. 1 / 0 / Time Slot 16 AIS detected causes an AIS alarm. 1 / 1 / Time Slot 16 AIS detected or line AIS detected causes an AIS alarm.
	0	ENLAIS	**Enable AIS Indication on Line AIS Detected:** A 1 enables detection of a line AIS to cause an AIS alarm, as shown in the above table.
138 - Ch 1 238 - Ch 2 338 - Ch 3 438 - Ch 4	7-0	RFTS7- RFTS0	**Receive Enable Fractional Time Slots 7-0:** The receive fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode). A 1 written to one or more bits enable a gapped clock (RISGL/RFE1GC) to be generated for the corresponding Time Slots (7-0).
139 - Ch 1 239 - Ch 2 339 - Ch 3 439 - Ch 4	7-0	RFTS15- RFTS8	**Receive Enable Fractional Time Slots 15-8:** The receive fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode). A 1 written to one or more bits enable a gapped clock (RISGL/ RFE1GC) to be generated for the corresponding Time Slots (15-8).

Address	Bit	Symbol	Description
13A - Ch 1 23A - Ch 2 33A - Ch 3 43A - Ch 4	7-0	RFTS23-RFTS16	**Receive Enable Fractional Time Slots 23-16:** The receive fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low/high, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode or 2 Mbit/s MVIP Mode). A 1 written to one or more bits enable a gapped clock (RISGL/RFE1GC) to be generated for the corresponding Time Slots (23-16).
13B - Ch 1 23B - Ch 2 33B - Ch 3 43B - Ch 4	7-0	RFTS31-RFTS24	**Receive Enable Fractional Time Slots 31-24:** The receive fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low/high, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode or 2 Mbit/s MVIP Mode). A 1 written to one or more bits enable a gapped clock (RISGL/RFE1GC) to be generated for the corresponding Time Slots (31-24).
13C - Ch 1 23C - Ch 2 33C - Ch 3 43C - Ch 4	7-0	TFTS7-TFTS0	**Transmit Enable Fractional Time Slots 7-0:** The transmit fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low/high, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode or 2 Mbit/s MVIP Mode). A 1 written to one or more bits enables a gapped clock (TISGL/TFE1GC) to be generated for the corresponding Time Slots (7-0). When control bit ENTSLB is 1, these bits if set to 1 source Time Slots 7-1 from the receive data highway instead of TDATAn pin. Pins RCLKn and RSYNCn must be connected to pins TCLKn and TSYNCn respectively to prevent data errors in the looped back time slots. Note: Time Slot 0 is generated by the framer and not taken from TDATAn.
13D - Ch 1 23D - Ch 2 33D - Ch 3 43D - Ch 4	7-0	TFTS15-TFTS8	**Transmit Enable Fractional Time Slots 15-8:** The transmit fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low/high, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode or 2 Mbit/s MVIP Mode). A 1 written to one or more bits enable a gapped clock (TISGL/TFE1GC) to be generated for the corresponding Time Slots (15-8). When control bit ENTSLB is 1, these bits if set to 1 source Time Slots 15-8 from the receive data highway instead of TDATAn pin. Pins RCLKn and RSYNCn must be connected to pins TCLKn and TSYNCn respectively to prevent data errors in the looped back time slots.
13E - Ch 1 23E - Ch 2 33E - Ch 3 43E - Ch 4	7-0	TFTS23-TFTS16	**Transmit Enable Fractional Time Slots 23-16:** The transmit fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low/high, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode or 2 Mbit/s MVIP Mode). A 1 written to one or more bits enable a gapped clock (TISGL/TFE1GC) to be generated for the corresponding Time Slots (23-16). When control bit ENTSLB is 1, these bits if set to 1 source Time Slots 23-16 from the receive data highway instead of TDATAn pin. Pins RCLKn and RSYNCn must be connected to pins TCLKn and TSYNCn respectively to prevent data errors in the looped back time slots.

Address	Bit	Symbol	Description
13F - Ch 1 23F - Ch 2 33F - Ch 3 43F - Ch 4	7-0	TFTS31- TFTS24	**Transmit Enable Fractional Time Slots 31-24:** The transmit fractional E1 mode is enabled when control bit FE1M is a 1, the CONFIG1 pin is low/high, and control bits HMVIP and MTP16M are both set to 0 (2 Mbit/s Transmission Mode or 2 Mbit/s MVIP Mode). A 1 written to one or more bits enable a gapped clock (TISGL/TFE1GC) to be generated for the corresponding Time Slots (31-24). When control bit ENTSLB is 1, these bits if set to 1 source Time Slots 31-24 from the receive data highway instead of TDATAn pin. Pins RCLKn and RSYNCn must be connected to pins TCLKn and TSYNCn respectively to prevent data errors in the looped back time slots.

Software Reset and Loopback Control Register

The control bits in the following read/write register are used to reset each of the channels, and to configure each of the channels within the QE1F-*Plus* for the various loopback modes of operation. Note that only one loopback is to be selected at any one time.

Address	Bit	Symbol	Description
105 - Ch 1 205 - Ch 2 305 - Ch 3 405 - Ch 4	7	SRST	**Software Reset Channel n:** When set to 1, the channel is initialized and held in the reset state until a 0 is written into this bit position to permit commencement of channel operation.
	6-4	Reserved	**Reserved:** Set to 0.
	3	PAYL	**Payload Remote Loopback Enable:** When set to 1, the payload remote loopback feature is enabled until this bit position is written with a 0. The receive data is looped back as the transmit data for Time Slots 1 through 31 prior to the receive slip buffer input and in place of the transmit slip buffer output when this loopback feature is enabled.
	2	TX1S	**Transmit AIS (all ones):** When set to 1 and control bit LLP is set to 1, an AIS (all ones) is transmitted instead of data. When set to 0, data is transmitted.
	1	RLP	**Remote Line Loopback Enable:** When set to 1, the remote line loopback feature is enabled until this bit position is written with a 0. Receive line data (prior to the AMI/HDB3 CODEC) is looped back as transmit line data when this loopback feature is enabled.
	0	LLP	**Local Loopback Enable:** When set to 1, the local loopback feature is enabled until this bit position is written with a 0. Transmit data (after the AMI/HDB3 CODEC) is looped back as received data when this loopback feature is enabled. When control bit TX1S (bit 2) is a 0 in X05H, data is transmitted. When TX1S is a 1, AIS is transmitted. The AIS signal is defined as an all ones signal.

System AIS and Test Registers

The control bits in the following read/write registers are used to generate test conditions and to configure the system interface for AIS in channel (framer) n.

Address	Bit	Symbol	Description
106 - Ch 1 206 - Ch 2 306 - Ch 3 406 - Ch 4	7-6	Reserved	**Reserved:** Set to 0.
	5	TS16YE	**Generate Time Slot 16 Remote Alarm Indication:** When set to 1, the Remote Alarm Indication, which is carried in bit 6 (Y-bit) in Time Slot 16 in frame 0 of the multiframe, is transmitted as a 1 until the microprocessor writes a 0 into this bit position.
	4	NFASE	**Generate Bit 2 Error In Frames Not Carrying the Frame Alignment Sequence:** When set to 1, the transmit framer sends bit 2 in Time Slot 0 in alternating (NFAS) frames as a 0, instead of the normal 1 value. To send a second NFAS error, this bit has to be reset to 0 and then set to 1 again.
	3	INSPRBS	**Insert Pseudo-Random Bit Sequence Enable:** When set to 1, PRBS is inserted for the terminal data on the transmit data highway. This feature is only available for 2 Mbit/s Transmission Mode. To resume normal operation, this bit position must be written with a 0.
	2	SFZ	**System Freeze:** When set to 1, the output clocks LTCLKn and RCLKn are forced to zero. The input clocks LRCLKn and TCLKn are gated off. To resume normal operation, this bit position must be written with a 0.
	1	RXFS	**Receive Fast Sync Enable:** When set to 1, and the NRZ mode is selected, a pulse received on the RNEGn lead will force the synchronization of this pulse to be interpreted as bit position 256 of the last frame (16) of a multiframe. When set to 0, coding violations indicated on the RNEGn lead are counted.
	0	TXFS	**Transmit Fast Sync Enable:** When set to 1, and the NRZ mode is selected, a synchronization pulse will be transmitted on the TNEGn lead every two milliseconds in bit position 256 of frame 16.
107 - Ch 1 207 - Ch 2 307 - Ch 3 407 - Ch 4	7	AIS16	**Transmit Time Slot 16 AIS Enable:** When set to 1, AIS (all ones) is transmitted in Time Slot 16, including the multiframe alignment pattern in frame 0. AIS is defined as all ones. AIS is transmitted in Time Slot 16 until this bit is written with a 0.

Address	Bit	Symbol	Description
107 - Ch 1 207 - Ch 2 307 - Ch 3 407 - Ch 4 (cont.)	6	STUAIS	**System TUAIS:** When set to 1, the AIS, OOF and LOS alarms, if enabled by setting to 1 their respective ENAIS (bit 2), ENOOF (bit 1), and ENLOS (bit 0) control bits in the Signaling and Time Slot Control register X03H, cause the generation of AIS on the data highway for all six system interface modes of operation. The AIS is sent until the alarm has recovered, or the enable bit (e.g., ENAIS) is set to 0. The following table lists the operation of control bit ENOOF and this bit. Control bits ENAIS and ENLOS function in similar fashion. 2 Mbit/s, 8 Mbit/s and 16 Mbit/s Transmission Modes ENOOF STUAIS Action 0 0 No AIS generated on signaling or data highway. 0 1 No AIS generated on signaling or data highway. 1 0 AIS generated only on signaling highway when OOF alarm is detected. 1 1 AIS generated on signaling and data highways when OOF alarm is detected. 2 Mbit/s MVIP Mode, 8 Mbit/s H-MVIP/H.100 Mode and 16 PCM Highway Mode ENOOF STUAIS Action 0 0 No AIS generated on data highway. 0 1 No AIS generated on data highway. 1 0 No AIS generated on data highway even when OOF alarm is detected. 1 1 AIS generated on data highway when OOF alarm is detected. Note: The microprocessor can cause AIS to be generated for the receive data highway independently of the two control bits by writing a 1 to control bit SYSALL1 (bit 5) in this register.
	5	SYSALL1	**Send System AIS:** When set to 1, AIS (all ones) is sent on the receive data highway. AIS will be transmitted on the receive data highway until this bit is written with a 0.
	4	CRC	**Generate a CRC-4 Error:** This feature is enabled when control bits CRCMD1 and CRCMD0 (bits 2 and 1) in register X04H are equal to 10, or 11 (i.e., this enables the CRC-4 feature). When CRC is set to 1, the CRC-4 bits in Time Slot 0 are transmitted in the inverted state once. To send another CRC-4 error, this bit must be first written with a 0, and then a 1.
	3	FASE	**Generate a Frame Alignment Sequence Error:** When set to 1, the transmitter will send the 7-bit frame alignment pattern in Time Slot 0 in alternating (FAS) frames in error once. All the bits in the frame alignment sequence are inverted once (X0011011 becomes X1100100). To send another frame alignment sequence error, this bit must be first written with a 0, and then a 1.

Address	Bit	Symbol	Description
107 - Ch 1 207 - Ch 2 307 - Ch 3 407 - Ch 4 (cont.)	2	RAIE	**Generate Remote Alarm Indication:** When set to 1, the Remote Alarm Indication, which is carried in bit 3 in Time Slot 0 of those (NFAS) frames not carrying the frame alignment sequence, is transmitted as a 1 until the microprocessor writes a 0 into this bit position.
	1	AISE	**Transmit Line AIS Enable:** When set to 1, a line AIS is transmitted. A line AIS is defined as all ones transmitted in the frame. Line AIS is transmitted until this bit is written with a 0.
	0	BPV	**Generate Bipolar Violation (BPV) Error:** When the dual unipolar mode is selected by bit 7 in register X00H, a 1 in this bit position causes a single BPV error to be sent. The microprocessor must write a 0 to this bit before another BPV error can be transmitted by setting it to 1. In random data the BPV may mimic a valid zero substitution code in HDB3 mode and may not be detected as an error.

E1 Status and Mask Registers

These registers are read/write, except for registers X10H, which are read-only unlatched. The status bits in the X11H register represent the latched status indications generated by the channel alarms. The bits latch on either the rising edge, the falling edge, or both edges of the current status or interrupt request event bits as defined by the RISE/FALL control bits (bits 6 and 5) in the Global Configuration Register 006H. A latched bit will cause a hardware interrupt indication when the global interrupt mask bit GIM (bit 7) in register 006H and the corresponding masks bit in the mask registers X09H and 00B are both written with a 0. The bits in register X10H represent the current (unlatched) alarm status. A latched status bit is reset by writing a 0 into the latched bit position, or by the rising edge of the T1SI pulse when the performance monitoring/fault monitoring feature is enabled. This feature activates the shadow registers X12H and X13H, and it is enabled by writing a 1 to control bit ENPMFM (bit 3) in the Global Configuration register 006H.

Address	Bit	Symbol	Description
109 - Ch 1 209 - Ch 2 309 - Ch 3 409 - Ch 4	7	MLOS	**Loss Of Signal (LOS) Mask Bit:** When set to 1, detection of a loss of signal alarm is masked from providing a hardware interrupt.
	6	MAIS	**AIS Mask Bit:** When set to 1, detection of an AIS condition is masked from providing a hardware interrupt.
	5	MOOF	**Out Of Frame (OOF) Mask Bit:** When set to 1, detection of an Out Of Frame alarm is masked from providing a hardware interrupt.
	4	MRAI	**Remote Alarm Indication (RAI) Mask Bit:** When set to 1, detection of a remote alarm indication is masked from providing a hardware interrupt.
	3	MCFA	**Change In Frame Alignment (CFA) Mask Bit:** When set to 1, detection of a change in frame alignment indication is masked from providing a hardware interrupt.
	2	MOOMF	**Out Of Multiframe Alignment (OOMF) Mask Bit:** When set to 1, detection of an out of multiframe alarm is masked from providing a hardware interrupt.
	1	MTXSLIP	**Transmit Slip Indication Mask Bit:** When set to 1, detection of a transmit slip is masked from providing a hardware interrupt.
	0	MRXSLIP	**Receive Slip Indication Mask Bit:** When set to 1, detection of a receive slip is masked from providing a hardware interrupt.

Address	Bit	Symbol	Description
110 - Ch 1 210 - Ch 2 310 - Ch 3 410 - Ch 4	7	LOS	**Loss Of Signal (LOS) Alarm (Unlatched):** A 1 indicates a loss of signal has been detected. A loss of signal alarm is detected when the incoming signal for the rail interface only has no transitions for N consecutive pulse positions, where the value of N is programmable between 10 and 255. The binary value written to LOSI7-LOSI0 (bits 7-0) in register 01AH selects the value of N. The LOS alarm is cleared when at least M ones are detected in an interval of N pulse positions, where M is the value written to OND5-OND0 in bits 5-0 of register 01BH. In addition, an external LOS indication from the external line transceiver (using the LINTn pin) can be or-gated with this alarm by setting control bit LIE (bit 1) in register X00H to 1.
	6	AIS	**AIS Indication (Unlatched):** A 1 indicates that a line Alarm Indication Signal (AIS) and/or an AIS in Time Slot 16 has been detected. Control bit ENLAIS (bit 0) in register X1AH enables a line AIS alarm. Control bit E16AIS (bit 1) in register X1AH enables a Receive Time Slot 16 AIS alarm. A line AIS is detected when the received line signal has two or less zeros in each of two consecutive double-frame periods (512 bits). Recovery occurs when each of two consecutive double-frame periods contain three or more zeros after frame alignment has been detected. An AIS in Time Slot 16 is detected when the received time slot has detected three or less zeros in each of two consecutive multiframe periods. Recovery occurs when each of two consecutive multiframe periods contains four or more zeros or when the multiframe alignment signal has been detected.
	5	OOF	**Out Of Frame (OOF) Alarm (Unlatched):** A 1 indicates that an Out Of Frame alarm has been detected. The alarm is programmed using the OOF1 and OOF0 control bits (bits 7 and 6) in register X04H. The QE1F-*Plus* supports two recovery schemes, with or without the CRC-4 check. This is controlled by control bit BFAA (bit 5) in the register X04H.
	4	RAI	**Remote Alarm Indication (RAI) (Unlatched):** A 1 indicates that the received RAI bit is a 1 for four or more consecutive frames in which it is carried. The RAI bit is bit 3 in Time Slot 0, in those alternate (NFAS) frames that are not carrying the frame alignment pattern, or the Y-bit of TS16. Recovery occurs when the RAI bit is 0 for four (NFAS) or three (Y-bit) or more consecutive frames in which it is carried. Control bit ENRAIY (bit 4 of register X1AH) enables this alarm if the Y-bit in Time Slot 16 is set. Control bit ENRAIA (bit 5 of register X1AH) enables this alarm if the A-bit in Time Slot 0 is set.
	3	CFA	**Change In Frame Alignment (CFA) Indication (Unlatched):** A 1 indicates that the frame alignment circuit has detected a change in the frame alignment pattern only after frame alignment has been detected.
	2	OOMF	**Out Of Multiframe Alignment (OOMF) Alarm (Unlatched):** A 1 indicates that Time Slot 16 multiframe alignment has been lost and/or a CRC-4 multiframe alignment has been also lost. Control bit EOOCRC (bit 3) in register X1AH enables a loss of CRC-4 multiframe alignment alarm. Control bit EOO16M (bit 2) in X1AH enables a TS16 multiframe alarm.
	1	TXSLIP	**Transmit Slip Indication (Unlatched):** This bit reflects the current status of the transmit slip buffer with respect to a slip being executed in the previous 125 microseconds.

Address	Bit	Symbol	Description
110 - Ch 1 210 - Ch 2 310 - Ch 3 410 - Ch 4 (cont.)	0	RXSLIP	**Receive Slip Indication (Unlatched):** This bit reflects the current status of the receive slip buffer with respect to a slip being executed in the previous 125 microseconds.
111 - Ch 1 211 - Ch 2 311 - Ch 3 411 - Ch 4	7	LLOS	**Latched Loss Of Signal (LOS):** This bit is set to 1 on an active edge of LOS which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	6	LAIS	**Latched AIS:** This bit is set to 1 on an active edge of AIS which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	5	LOOF	**Latched Out Of Frame (OOF):** This bit is set to 1 on an active edge of OOF which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	4	LRAI	**Latched Remote Alarm Indication (RAI):** This bit is set to 1 on an active edge of RAI which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	3	LCFA	**Latched Change In Frame Alignment (CFA) Mask Bit:** This bit is set to 1 on an active edge of CFA which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	2	LOOMF	**Latched Out Of Multiframe Alignment (OOMF):** This bit is set to 1 on an active edge of OOMF which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	1	LTXSLIP	**Latched Transmit Slip Indication:** This bit is set to 1 on an active edge of TXSLIP which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register, location 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	0	LRXSLIP	**Latched Receive Slip Indication:** This bit is set to 1 on an active edge of RXSLIP which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.

Address	Bit	Symbol	Description
112 - Ch 1 212 - Ch 2 312 - Ch 3 412 - Ch 4	7	PLOS	**Loss Of Signal (LOS) One Second Error:** This bit is set to 1 if the LOS alarm occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	6	PAIS	**AIS One Second Error:** This bit is set to 1 if the AIS indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	5	POOF	**Out Of Frame (OOF) One Second Error:** This bit is set to 1 if the OOF alarm occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	4	PRAI	**Remote Alarm Indication (RAI) One Second Error:** This bit is set to 1 if the RAI indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	3	PCFA	**Change In Frame Alignment (CFA) One Second Error:** This bit is set to 1 if the CFA indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	2	POOMF	**Out Of Multiframe Alignment (OOMF) One Second Error:** This bit is set to 1 if the OOMF alarm occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	1	PTXSLIP	**Transmit Slip Indication One Second Error:** This bit is set to 1 if the TXSLIP indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	0	PRXSLIP	**Receive Slip Indication One Second Error:** This bit is set to 1 if the RXSLIP indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.

Address	Bit	Symbol	Description
113 - Ch 1 213 - Ch 2 313 - Ch 3 413 - Ch 4	7	FLOS	**Loss Of Signal (LOS) Persistent Error:** This bit is set to 1 if the LOS alarm is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	6	FAIS	**AIS Persistent Error:** This bit is set to 1 if the AIS indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	5	FOOF	**Out Of Frame (OOF) Persistent Error:** This bit is set to 1 if the OOF alarm is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	4	FRAI	**Remote Alarm Indication (RAI) Persistent Error:** This bit is set to 1 if the RAI indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	3	FCFA	**Change In Frame Alignment (CFA) Persistent Error:** This bit is set to 1 if the CFA indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	2	FOOMF	**Out Of Multiframe Alignment (OOMF) Persistent Error:** This bit is set to 1 if the OOMF alarm is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	1	FTXSLIP	**Transmit Slip Indication Persistent Error:** This bit is set to 1 if the TXSLIP indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	0	FRXSLIP	**Receive Slip Indication Persistent Error:** This bit is set to 1 if the RXSLIP indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.

Counters and Counter Shadow Registers

The QE1F-*Plus* provides counter and counter shadow read/write registers for E-bit errors, CRC-4 bit errors, coding violations, and framing bit errors. The counter shadow registers provide the microprocessor with an error count for the previous one second interval. A counter and the corresponding counter shadow register (and their overflow bits) are cleared when the microprocessor writes 0 to their bits. The rising edges of a one second interval pulse clear the counters (and the overflow bits, if set). The shadow registers for the various counters are also updated at one second intervals by the rising edge of the pulse applied to the T1SI pin (pin 40).

Address	Bit	Symbol	Description
1EC - Ch 1 2EC - Ch 2 3EC - Ch 3 4EC - Ch 4	7-0	LEBE7-LEBE0	**Latched E-Bit Error Counter Shadow Register:** This register contains the lower 8 bits of the 10-bit shadow register assigned for holding the E-bit error count that occurred in the previous one second interval. This location is updated from EBE7-EBE0 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 0 is the LSB of the 10-bit count.
1ED - Ch 1 2ED - Ch 2 3ED - Ch 3 4ED - Ch 4	7	LEBEO	**Latched E-Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit shadow register LEBE9-LEBE0 assigned for holding the E-bit error count that occurred in the previous one second interval. This location is updated from EBEO at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-2	Reserved	**Reserved**: Set to 0.
	1-0	LEBE9-LEBE8	**Latched E-Bit Error Counter Shadow Register:** This register contains the upper two bits of the 10-bit shadow register assigned for holding the E-bit error count that occurred in the previous one second interval. This location is updated from EBE9-EBE8 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 1 is the MSB of the 10-bit count.
1EE - Ch 1 2EE - Ch 2 3EE - Ch 3 4EE - Ch 4	7-0	EBE7-EBE0	**E-Bit Error Counter:** This register contains the lower 8 bits of the 10-bit E-bit error counter. When enabled (control bits CRCMD1,0 bits 2 and 1 in register X04H = 10), this counter increments for every received E-bit which is 0, after CRC-4 multiframe alignment is achieved and OOF or AIS is not detected. This location is cleared at one second intervals between the rising and falling edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 0 is the LSB of the 10-bit count.
1EF - Ch 1 2EF - Ch 2 3EF - Ch 3 4EF - Ch 4	7	EBEO	**E-Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit E-bit counter EBE9-EBE0. This bit sets when the 10-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-2	Reserved	**Reserved**: Set to 0.

Address	Bit	Symbol	Description
1EF - Ch 1 2EF - Ch 2 3EF - Ch 3 4EF - Ch 4 (cont.)	1-0	EBE9-EBE8	**E-Bit Error Counter:** This register contains the upper 2 bits of the 10-bit E-bit error counter. When enabled (control bits CRCMD1,0 bits 2 and 1 in register X04H = 10), this counter increments for every received E-bit which is 0, after CRC-4 multiframe alignment is achieved and OOF or AIS is not detected. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 1 is the MSB of the 10-bit count.
1F0 - Ch 1 2F0 - Ch 2 3F0 - Ch 3 4F0 - Ch 4	7-0	LCRC7-LCRC0	**Latched CRC-4 Error Counter Shadow Register:** This register contains the lower 8 bits of the 10-bit shadow register assigned for holding the CRC-4 error count that occurred in the previous one second interval. This location is updated from CRC7-CRC0 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 0 is the LSB of the 10-bit count.
1F1 - Ch 1 2F1 - Ch 2 3F1 - Ch 3 4F1 - Ch 4	7	LCRCO	**Latched CRC-4 Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit shadow register LCRC9-LCRC0 assigned for holding the CRC-4 error count that occurred in the previous one second interval. This location is updated from CRCO at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-2	Reserved	**Reserved**: Set to 0.
	1-0	LCRC9-LCRC8	**Latched CRC-4 Error Counter Shadow Register:** This register contains the upper two bits of the 10-bit shadow register assigned for holding the CRC-4 error count that occurred in the previous one second interval. This location is updated from CRC9-CRC8 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 1 is the MSB of the 10-bit count.
1F2 - Ch 1 2F2 - Ch 2 3F2 - Ch 3 4F2 - Ch 4	7-0	CRC7-CRC0	**CRC-4 Error Counter:** This register contains the lower 8 bits of the 10-bit CRC-4 error counter. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 0 is the LSB of the 10-bit count.
1F3 - Ch 1 2F3 - Ch 2 3F3 - Ch 3 4F3 - Ch 4	7	CRCO	**CRC-4 Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit CRC-4 counter CRC9-CRC0. This bit sets when the 10-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-2	Reserved	**Reserved**: Set to 0.
	1-0	CRC9-CRC8	**CRC-4 Error Counter:** This register contains the upper 2 bits of the 10-bit CRC-4 error counter. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 1 is the MSB of the 10-bit count.

Address	Bit	Symbol	Description
1F4 - Ch 1 2F4 - Ch 2 3F4 - Ch 3 4F4 - Ch 4	7-0	LCV7-LCV0	**Latched Coding Violation Counter Shadow Register:** This register contains the lower 8 bits of the 16-bit shadow register assigned for holding the HDB3 coding violation count that occurred in the previous one second interval. This location is updated from CV7-CV0 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 0 is the LSB of the 16-bit count.
1F5 - Ch 1 2F5 - Ch 2 3F5 - Ch 3 4F5 - Ch 4	7-0	LCV15-LCV8	**Latched Coding Violation Counter Shadow Register:** This register contains the upper 8 bits of the 16-bit shadow register assigned for holding the HDB3 coding violation count that occurred in the previous one second interval. This location is updated from CV15-CV8 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 7 is the MSB of the 16-bit count.
1F6 - Ch 1 2F6 - Ch 2 3F6 - Ch 3 4F6 - Ch 4	7	LCVO	**Latched Coding Violation Counter Overflow Bit:** This bit contains the overflow indication associated with the 16-bit shadow register LCV15-LCV0 assigned for holding the Coding Violation count that occurred in the previous one second interval. This location is updated from CVO at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-0	Reserved	**Reserved**: Set to 0.
1F7 - Ch 1 2F7 - Ch 2 3F7 - Ch 3 4F7 - Ch 4	7-0	CV7-CV0	**Coding Violation Counter:** This register contains the lower 8 bits of the 16-bit HDB3 coding violation counter. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 0 is the LSB of the 16-bit count.
1F8 - Ch 1 2F8 - Ch 2 3F8 - Ch 3 4F8 - Ch 4	7-0	CV15-CV8	**Coding Violation Counter:** This register contains the upper 8 bits of the 16-bit HDB3 coding violation counter. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 7 is the MSB of the 16-bit count.
1F9 - Ch 1 2F9 - Ch 2 3F9 - Ch 3 4F9 - Ch 4	7	CVO	**Coding Violation Counter Overflow Bit:** This bit contains the overflow indication associated with the 16-bit coding violation counter CV15-CV0. This bit sets when the 16-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-0	Reserved	**Reserved**: Set to 0.
1FA - Ch 1 2FA - Ch 2 3FA - Ch 3 4FA - Ch 4	7-0	LFBE7-LFBE0	**Latched Framing Error Counter Shadow Register:** This register contains the lower 8 bits of the 13-bit shadow register assigned for holding the framing word errors that occurred in the previous one second interval. This location is updated from FBE7-FBE0 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.

Address	Bit	Symbol	Description
1FB - Ch 1 2FB - Ch 2 3FB - Ch 3 4FB - Ch 4	7	LFBEO	**Latched Framing Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 13-bit shadow register LFBE12-LFBE0 assigned for holding the framing word error count that occurred in the previous one second interval. This location is updated from FBEO at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-5	Reserved	**Reserved**: Set to 0.
	4-0	LFBE12-LFBE8	**Latched Framing Error Counter Shadow Register:** This register contains the upper 5 bits of the shadow register assigned for holding the framing word errors that occurred in the previous one second interval. This location is updated from FBE12-FBE8 with a new count at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 4 is the MSB of the 13-bit count.
1FC - Ch 1 2FC - Ch 2 3FC - Ch 3 4FC - Ch 4	7-0	FBE7-FBE0	**Framing Error Counter:** This register contains the lower 8 bits of the 13-bit framing word error counter. An incorrectly received FAS word in Time Slot 0 is counted as one frame word error. A frame word error is also counted if bit 2 of the NFAS pattern in Time Slot 0 is not a 1. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
1FD - Ch 1 2FD - Ch 2 3FD - Ch 3 4FD - Ch 4	7	FBEO	**Framing Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 13-bit framing word error counter FBE12-FBE0. This bit sets when the 13-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1.
	6-5	Reserved	**Reserved**: Set to 0.
	4-0	FBE12-FBE8	**Framing Error Counter:** This register contains the upper 5 bits of the 13-bit framing word error counter. An incorrectly received FAS word in Time Slot 0 is counted as one frame word error. A frame word error is also counted if bit 2 of the NFAS pattern in Time Slot 0 is not a 1. This location is cleared at one second intervals on the rising edges of the T1SI signal if control bit ENPMFM is set to a 1. Bit 4 is the MSB of the 13-bit count.

Operational Status Registers

The status bits in the following read-only unlatched registers indicate various status information associated with the transmit and receive two-frame slip buffers. The slip buffers are always enabled in the MVIP, H-MVIP/ H.100 and 16 Mbit/s PCM Highway Modes (CONFIG1 pin is high - pin 43). The slip buffers are optional in the Transmission Modes (CONFIG1 pin is low - pin 43). The transmit slip buffer is enabled when a 1 is written into control bit TSE (bit 4) in register X02H. The receive slip buffer is enabled when a 1 is written into control bit RSE (bit 3) in register X02H.

Address	Bit	Symbol	Description
114 - Ch 1 214 - Ch 2 314 - Ch 3 414 - Ch 4	7-6	TXS1-TSX0	**Transmit Slip Buffer Status:** The following table indicates the direction of a transmit slip. A transmit slip indication (unlatched) is provided by status bit TXSLIP (bit 1) set to 1 in register X10H. A latched indication is given by LTXSLIP (bit 1) set to 1 in register X11H. TXS1 TXSO Buffer Status 0 0 No slips have occurred. 0 1 Slip overflow. One frame dropped. 1 0 Slip underflow. One frame repeated. 1 1 Slip buffer error. Two slips in a row.
	5-4	RXS1-RXS0	**Receive Slip Buffer Status:** The following table indicates the direction of a receive slip. A receive slip indication (unlatched) is provided by status bit RXSLIP (bit 0) set to 1 in register X10H. A latched indication is given by LRXSLIP (bit 0) set to 1 in register X11H. RXS1 RXSO Buffer Status 0 0 No slips have occurred. 0 1 Slip overflow. One frame dropped. 1 0 Slip underflow. One frame repeated. 1 1 Slip buffer error. Two slips in a row.
	3	TUAIS	**TU AIS Received:** This status bit is enabled in the Transmission Modes only. A 1 indicates that the (AIS) A-bits on the transmit signaling highway (TSIGLn) are set to 1. The response time and recovery times are immediate.
	2	TURAI	**TU RAI Received:** This status bit is enabled in the Transmission Modes only. A 1 indicates that the Remote Alarm Indication (RAI) bit (bit 3 in Time Slot 0 in alternating NFAS frames) on the transmit signaling highway (TSIGLn) is set to 1. The response time and recovery times are immediate.
	1-0	Reserved	**Reserved**: Disregard these bits.

Address	Bit	Symbol	Description
115 - Ch 1 215 - Ch 2 315 - Ch 3 415 - Ch 4	7	RXSF	**Receive Signaling Freeze Indication:** When set to 1, this status bit indicates that the receive signaling bits in the signaling buffer are frozen as a result of a loss of signal, an out of frame alarm, or control bit RXF (bit 5) in register X03H being set to a 1.
	6	TXSF	**Transmit Signaling Freeze Indication:** When set to 1, this status bit indicates that the transmit signaling bits in the signaling buffer are frozen as a result of receiving an AIS indication on the signaling highway in the Transmission Mode, or control bit TXF (bit 4) in register X03H is a 1.
	5-1	Reserved	**Reserved**: Disregard these bits.
	0	LINT	**General Purpose Input Status Indication:** The status of this bit reflects the state of the external input pin LINTn. The input polarity (i.e., active true state) of this pin is determined by control bit LPOL (bit 0) in register X00H.
11B - Ch 1 21B - Ch 2 31B - Ch 3 41B - Ch 4	7	NCRC4	**Non-CRC4 Interworking:** A 1 indicates that a CRC-4 to non-CRC-4 interworking has been established. When 0, this bit indicates that a CRC-4 interworking has been established. The status becomes valid after a one second interval when control bit CRCA (bit 3) in register X04H is 1. The status of this bit should be disregarded when control bit CRCA is 0.
	6	ECRCE	**Receive Excessive CRC-4 Errors:** A 1 indicates that 915 or more of the last 1000 CRC-4 received were in error. A 0 indicates that the number of CRC-4 errors was below this level. If set to a 1, this bit will clear several frames after basic frame alignment is regained.
	5	RAIA	**Remote Alarm Indication (RAI) from A-Bit:** This bit is set to 1 when RAI status occurs due to detection of the A-bit in the TS0 of even-numbered frames.
	4	TS16ME	**Time Slot 16 Multiframe Error:** This bit is set to 1 when a multiframe error is detected in the Time Slot 16 multiframe.
	3	OOCRCM	**CRC-4 Multiframe Out Of Frame:** This bit reflects the status of the CRC-4 multiframe out of frame detector. A 1 indicates out of CRC-4 multiframe detection.
	2	OOTS16M	**Time Slot 16 Multiframe Out Of Frame:** This bit reflects the status of the Channel Associated Signaling multiframe detector. A 1 indicates out of Time Slot 16 multiframe detection.
	1	TS16AIS	**Time Slot 16 AIS Detection:** This bit reflects the status of the AIS detector for Time Slot 16. A 1 indicates Time Slot 16 AIS detection.
	0	LINEAIS	**Line AIS Detection:** This bit reflects the status of the line AIS detector for the E1 frame format. A 1 indicates Line AIS detection.

Slip Buffer Pointer Status Registers

The following unlatched register locations provide receive read and write pointer information, and transmit read and write pointer information, from the receive and transmit slip buffers respectively. Although these registers are writable, writing to these registers will cause a slip to occur.

Address	Bit	Symbol	Description
120 - Ch 1 220 - Ch 2 320 - Ch 3 420 - Ch 4	7-0	TWP7-TWP0	**Transmit Slip Buffer Write Pointer:** Bit 0 is the LSB. The value (between 0 and 255) is the current value of the transmit slip buffer write pointer.
121 - Ch 1 221 - Ch 2 321 - Ch 3 421 - Ch 4	7-0	TRP7-TRP0	**Transmit Slip Buffer Read Pointer:** Bit 0 is the LSB. The value (between 0 and 255) is the current value of the transmit slip buffer read pointer.
122 - Ch 1 222 - Ch 2 322 - Ch 3 422 - Ch 4	7	TWSBS	**Transmit Slip Buffer Write Side:** A 1 indicates that the upper side of the transmit buffer is currently being written, A 0 indicates that the lower side of the transmit buffer is being written.
	6-4	Reserved	**Reserved**: Disregard these bits.
	3-0	TWPF3-TWPF0	**Transmit Slip Buffer Write Pointer Frame:** The bits in these locations indicate for which frame the transmit slip buffer write pointer is being written. For the basic frame format, there are two values (0000 = frame 0 and 0001 = frame 1). For the CRC-4 multiframe format the value will range between 0 and 15. Bit 0 is the LSB.
123 - Ch 1 223 - Ch 2 323 - Ch 3 423 - Ch 4	7	TRSBS	**Transmit Slip Buffer Read Side:** A 1 indicates that the upper side of the transmit buffer is currently being read, A 0 indicates that the lower side of the transmit buffer is being read.
	6-4	Reserved	**Reserved**: Disregard these bits.
	3-0	TRPF3-TRPF0	**Transmit Slip Buffer Read Pointer Frame:** The bits in these locations indicate for which frame the transmit slip buffer read pointer is being read. For the basic frame format, there are two values (0000 = frame 0 and 0001 = frame 1). For the CRC-4 multiframe format the value will range between 0 and 15. Bit 0 is the LSB.
124 - Ch 1 224 - Ch 2 324 - Ch 3 424 - Ch 4	7-0	RWP7-RWP0	**Receive Slip Buffer Write Pointer:** Bit 0 is the LSB. The value (between 0 and 255) is the current value of the receive slip buffer write pointer.
125 - Ch 1 225 - Ch 2 325 - Ch 3 425 - Ch 4	7-0	RRP7-RRP0	**Receive Slip Buffer Read Pointer:** Bit 0 is the LSB. The value (between 0 and 255) is the current value of the receive slip buffer read pointer.

Address	Bit	Symbol	Description
126 - Ch 1 226 - Ch 2 326 - Ch 3 426 - Ch 4	7	RWSBS	**Receive Slip Buffer Write Side:** A 1 indicates that the upper side of the receive buffer is currently being written. A 0 indicates that the lower side of the receive buffer is being written.
	6-4	Reserved	**Reserved**: Disregard these bits.
	3-0	RWPF3-RWPF0	**Receive Slip Buffer Write Pointer Frame:** The bits in these locations indicate for which frame the receive slip buffer write pointer is being written. For the basic frame format, there are two values (0000 = frame 0 and 0001 = frame 1). For the CRC-4 multiframe format the value will range between 0 and 15. Bit 0 is the LSB.
127 - Ch 1 227 - Ch 2 327 - Ch 3 427 - Ch 4	7	RRSBS	**Receive Slip Buffer Read Side:** A 1 indicates that the upper side of the receive buffer is currently being read, A 0 indicates that the lower side of the receive buffer is being read.
	6-4	Reserved	**Reserved**: Disregard these bits.
	3-0	RRPF3-RRPF0	**Receive Slip Buffer Read Pointer Frame:** The bits in these locations indicate for which frame the receive slip buffer read pointer is being read. For the basic frame format, there are two values (0000 = frame 0 and 0001 = frame 1). For the CRC-4 multiframe format the value will range between 0 and 15. Bit 0 is the LSB.

Receive Time Slot Control Registers

The control bits in the following read/write registers are used to enable or disable (freeze) the receive buffer locations for the system highway, and to allow the microprocessor to write in service codes and idle codes.

Address	Bit	Symbol	Description
12A - Ch 1 22A - Ch 2 32A - Ch 3 42A - Ch 4	7	RSIS	**Receive International Bits (Si) Select:** When set to 1, the two international bits received from the line (in bit 1 of Time Slot 0 in alternating FAS and NFAS frames) are sent to the receive signaling highway and to the data highway, via a buffer. When set to 0, the received international bits are disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of these bits in the buffer may now be rewritten by the microprocessor. The buffer location of Time Slot 0 is register X40H for (FAS) frames carrying the frame alignment pattern, and X60H for (NFAS) frames not carrying the frame alignment pattern.
	6-5	Reserved	**Reserved:** Set to 0.
	4-0	RSA4S-RSA8S	**Receive National Bits (Sa4-Sa8) Select:** Bit 4 corresponds to the received Sa4 bit in Time Slot 0 of NFAS frames. When a bit is set to 1, the corresponding national bit received in Time Slot 0 is sent to the receive signaling highway and to the data highway, via a buffer. When set to 0, the received national bit is disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of the bit in the buffer may be rewritten by the microprocessor. The buffer location is register X60H.

Address	Bit	Symbol	Description
12B - Ch 1 22B - Ch 2 32B - Ch 3 42B - Ch 4	7-3	Reserved	**Reserved:** Set to 0.
	2-0	RX2S-RX0S	**Receive Time Slot 16 Spare Bits Select:** Bits RX2S-RX0S correspond to the spare bits X2-X0 in bit positions 8, 7 and 5 in Time Slot 16 of frame 0 in the multiframe (see table following Figure 53). When a bit is set to 1, the corresponding spare bit received in Time Slot 16 is sent to the receive signaling highway via a buffer. When set to 0, the receive spare bit in the multiframe is disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of the bit in the buffer may be rewritten by the microprocessor for sending to the receive signaling highway. The buffer location is X80H.
1E0 - Ch 1 2E0 - Ch 2 3E0 - Ch 3 4E0 - Ch 4	7-1	RDE7-RDE1	**Receive Time Slot Enable for Time Slots 7-1:** When a bit in this register is set to 1, the corresponding received time slot is written into the slip buffer. The time slot is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 7. The slip buffers are located in registers X47H-X41H (frame 1) and X67H-X61H (frame 2).
	0	Reserved	**Reserved**: Set to 0.
1E1 - Ch 1 2E1 - Ch 2 3E1 - Ch 3 4E1 - Ch 4	7-0	RDE15-RDE8	**Receive Time Slot Enable for Time Slots 15-8:** When a bit in this register is set to 1, the corresponding received time slot is written into the slip buffer. The time slot is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 15. The slip buffers are located in registers X4FH-X48H (frame 1) and X6FH-X68H (frame 2).
1E2 - Ch 1 2E2 - Ch 2 3E2 - Ch 3 4E2 - Ch 4	7-0	RDE23-RDE16	**Receive Time Slot Enable for Time Slots 23-16:** When a bit in this register is set to 1, the corresponding received time slot is written into the slip buffer. The time slot is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 23. The slip buffers are located in registers X57H-X50H (frame 1) and X77H-X70H (frame 2).
1E3 - Ch 1 2E3 - Ch 2 3E3 - Ch 3 4E3 - Ch 4	7-0	RDE31-RDE24	**Receive Time Slot Enable for Time Slots 31-24:** When a bit in this register is set to 1, the corresponding received time slot is written into the slip buffer. The time slot is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 31. The slip buffers are located in registers X5FH-X58H (frame 1) and X7FH-X78H (frame 2).

Receive Time Slot Registers

The bits in these read/write registers are the receive time slots from the E1 frame format that are present in the two-frame slip buffer, when enabled. Please note that, on loss of frame alignment, the states present in the slip buffer will be frozen to the states existing prior to the loss of frame alignment.

Address	Bit	Symbol	Description
140 - Ch 1 240 - Ch 2 340 - Ch 3 440 - Ch 4	7-0	RFAS	**Receive Time Slot 0 FAS Buffer:** The time slot bits for Time Slot 0 in frames carrying the frame alignment pattern (FAS, frame 1) are written into this location from the line. When control bit RSIS (bit 7) in register X2AH, is written with a 0, the state of the international bit from the line cannot be written into the buffer, and the buffer value is frozen. The microprocessor can now write the value of the international bit for receive Time Slot 0 to the system. The other bits represent the frame alignment sequence in Time Slot 0.
141-15F - Ch 1 241-25F - Ch 2 341-35F - Ch 3 441-45F - Ch 4	7-0	RTS1-RTS31	**Receive Time Slots 1-31:** Register locations X41H-X5FH represent frame 1 in the two-frame slip buffer for the data highway. The register locations for a time slot are enabled when the corresponding receive time slot enable bits (RDE1-RDE31) in registers XE0H, XE1H, XE2H and XE3H are written with 1. When one or more control bits in XE1H-XE3H are written with a 0, the corresponding receive time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Note: Both frame locations in the slip buffer must be written for a time slot (see X61H to X7FH below).
160 - Ch 1 260 - Ch 2 360 - Ch 3 460 - Ch 4	7-0	RNFAS	**Receive Time Slot 0 NFAS Buffer:** The Time Slot 0 bits for frames not carrying the frame alignment pattern (NFAS, frame 2) are written into this location from the line. When control bit RSIS (bit 7) and RSA4S-RSA8S (bits 4-0) in register X2AH are set to 0, the states of the corresponding international bit and national bits from the line cannot be written into the buffer, and the corresponding buffer value is frozen. The microprocessor can now write the value of the corresponding international bit and national bits for receive Time Slot 0 to the system.
161-17F - Ch 1 261-27F - Ch 2 361-37F - Ch 3 461-47F - Ch 4	7-0	RTS1-RTS31	**Receive Time Slots 1-31:** Register locations X61H-X7FH represent frame 2 in the two-frame slip buffer for the data highway. The register locations for a time slot are enabled when the corresponding receive time slot enable bits (RDE1-RDE31) in registers XE0H, XE1H, XE2H and XE3H are written with 1. When one or more control bits in XE1H-XE3H are written with a 0, the corresponding receive time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Note: Both frame locations in the slip buffer must be written for a time slot (see X41H-X5FH above).

Transmit Time Slot Control Registers

The control bits in the following read/write registers are used to enable or disable (freeze) the transmit slip buffer locations for receiving input from the system highway, and to allow the microprocessor to write in service codes and idle codes.

Address	Bit	Symbol	Description
12C - Ch 1 22C - Ch 2 32C - Ch 3 42C - Ch 4	7	TSIS	**Transmit International Bits (Si) Select:** This bit is enabled when the CRC framing mode bits CRCMD1 and CRCMD0 (bits 2 and 1) in register X04H are equal to 01. When set to 1, the two international bits for frames 1 and 2 in Time Slot 0 from the signaling highway are sent as the transmit bits via a buffer. When set to 0, the transmit international bits are disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of these bits in the buffer may be rewritten by the microprocessor for sending to the line. The buffer locations are registers X90H (FAS, frame 1) and XB0H (NFAS, frame 2).
	6-5	Reserved	**Reserved:** Set to 0.
	4-0	TSA4S-TSA8S	**Transmit National Bits (Sa4-Sa8) Select:** Bit 4 corresponds to the transmit Sa4 bit in Time Slot 0 of NFAS frames. When a bit is set to 1, the corresponding transmit national bit of frame 2 received in Time Slot 0 on the transmit signaling highway is transmitted via a buffer when control bit BNAL (bit 1) in the Framer Configuration register X01H is a 1. When a bit is set to 0, the corresponding transmit national bit from the signaling highway is disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of the bit in the buffer may be rewritten by the microprocessor for sending to the line. The buffer location is register XB0H.
12D - Ch 1 22D - Ch 2 32D - Ch 3 42D - Ch 4	7-3	Reserved	**Reserved:** Set to 0.
	2-0	TX2S-TX0S	**Transmit Time Slot 16 Spare Bits Select:** Bits TX2S-TX0S correspond to the spare bits X2-X0 in bit positions 8, 7 and 5 in Time Slot 16 of frame 0 in the multiframe (see table following Figure 53). When a bit is set to 1, the corresponding spare bit in Time Slot 16 from the transmit signaling highway is transmitted via a buffer. When set to 0, the transmit spare bit is disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of the bit in the buffer may be rewritten by the microprocessor for sending to the line. The buffer location is XD0H. This function operates only in Transmission Mode.
1E4 - Ch 1 2E4 - Ch 2 3E4 - Ch 3 4E4 - Ch 4	7-1	TDE7-TDE1	**Transmit Time Slot Enable for Time Slots 7-1:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the slip buffer. The time slot is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 7. The slip buffers are located in registers X97H-X91H (frame 1) and XB7H-XB1H (frame 2).
	0	Reserved	**Reserved**: Set to 0.

Address	Bit	Symbol	Description
1E5 - Ch 1 2E5 - Ch 2 3E5 - Ch 3 4E5 - Ch 4	7-0	TDE15-TDE8	**Transmit Time Slot Enable for Time Slots 15-8:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the slip buffer. The time slot is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 15. The slip buffers are located in registers X9FH-X98H (frame 1) and XBFH-XB8H (frame 2).
1E6 - Ch 1 2E6 - Ch 2 3E6 - Ch 3 4E6 - Ch 4	7-0	TDE23-TDE16	**Transmit Time Slot Enable for Time Slots 23-16:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the slip buffer. The time slot is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 23. The slip buffers are located in registers XA7H-XA0H (frame 1) and XC7H-XC0H (frame 2).
1E7 - Ch 1 2E7 - Ch 2 3E7 - Ch 3 4E7 - Ch 4	7-0	TDE31-TDE24	**Transmit Time Slot Enable for Time Slots 31-24:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the slip buffer. The time slot is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the time slot into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 31. The slip buffers are located in registers XAFH-XA8H (frame 1) and XCFH-XC8H (frame 2).

Transmit Time Slot Registers

The bits in these read/write registers are the transmit time slots from the E1 frame format that are present in the two-frame slip buffer, when enabled.

Address	Bit	Symbol	Description
190 - Ch 1 290 - Ch 2 390 - Ch 3 490 - Ch 4	7-0	TFAS	**Transmit Time Slot 0 FAS Buffer:** The time slot bits for Time Slot 0 in frames carrying the frame alignment pattern (FAS, frame 1) are written into this location from the signaling highway in any mode. When control bit TSIS (bit 7) in register X2CH is written with a 0, the state of the international bit from the system interface (signaling highway) cannot be written into the buffer and the buffer value is frozen. The microprocessor can now write the value of the international bit for transmit Time Slot 0 that will be sent to the line.
191-1AF - Ch 1 291-2AF - Ch 2 391-3AF - Ch 3 491-4AF - Ch 4	7-0	TTS1-TTS31	**Transmit Time Slots 1-31:** Register locations X91H-XAFH represent frame 1 in the two-frame slip buffer from the data highway. The register locations for a time slot are enabled when the corresponding transmit time slot enable bits (TDE1-TDE31) in registers XE4H, XE5H, XE6H and XE7H are written with 1. When one or more control bits in XE4H-XE7H are written with a 0, the corresponding transmit time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Note: Both frame locations in the slip buffer must be written for a time slot (see XB1H-XCFH below).
1B0 - Ch 1 2B0 - Ch 2 3B0 - Ch 3 4B0 - Ch 4	7-0	TNFAS	**Transmit Time Slot 0 NFAS Buffer:** The time slot bits for Time Slot 0 in frames not carrying the frame alignment pattern (NFAS, frame 2) are written into this location from the signaling highway in any mode. When control bit TSIS (bit 7) and TSA4S-TSA8S (bits 4-0) in register X2CH are set to 0, the states of the corresponding international bit and national bits from the system interface (signaling highway) cannot be written into the buffer, and the corresponding buffer value is frozen. The microprocessor can now write the values of the corresponding international bit and national bits for transmit Time Slot 0 that will be sent to the line. This write operation must be verified by reading the location after more than 10 microseconds has elapsed. If this value is not the same as written, then repeat write/read operation until it is correct.
1B1-1CF - Ch 1 2B1-2CF - Ch 2 3B1-3CF - Ch 3 4B1-4CF - Ch 4	7-0	TTS1-TTS31	**Transmit Time Slots 1-31:** Register locations XB1H-XCFH represent frame 2 in the two-frame slip buffer from the data highway. The register locations for a time slot are enabled when the corresponding transmit time slot enable bits (TDE1-TDE31) in registers XE4H, XE5H, XE6H, and XE7H are written with 1. When one or more control bits in XE4H-XE7H are written with a 0, the corresponding transmit time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Note: Both locations in the slip buffer must be written for a time slot (see X91H-XAFH above).

Signaling Control Registers

The bits in the following read/write registers control both the receive and transmit signaling buffer locations for telephone channels 1 through 30. Please note that the signaling information for telephone channel 1 is carried in Time Slot 1, and for telephone channel 30 in Time Slot 31. Time Slot 16 is used for a signaling channel, not a telephone channel.

Address	Bit	Symbol	Description
1E8 - Ch 1 2E8 - Ch 2 3E8 - Ch 3 4E8 - Ch 4	7-0	SE8-SE1	**Signaling Enable for Channels 8-1:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When set to 0, the signaling states in both the transmit and receive signaling buffers are frozen. The ability to internally write the signaling bits from the signaling highway and line into the transmit and receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit and receive signaling registers. Bit 7 is the enable bit for channel 8. Signaling information for telephone channel c is carried in Time Slot c.
1E9 - Ch 1 2E9 - Ch 2 3E9 - Ch 3 4E9 - Ch 4	7-0	SE16-SE9	**Signaling Enable for Channels 16-9:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When set to 0, the signaling states in both the transmit and receive signaling buffers are frozen. The ability to internally write the signaling bits from the signaling highway and line into the transmit and receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit and receive signaling registers. Bit 7 is the enable bit for channel 16. Signaling information for telephone channel c is carried in Time Slot c, except for channel 16, which is carried in Time Slot 17.
1EA - Ch 1 2EA - Ch 2 3EA - Ch 3 4EA - Ch 4	7-0	SE24-SE17	**Signaling Enable for Channels 24-17:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When set to 0, the signaling states in both the transmit and receive signaling buffers are frozen. The ability to internally write the signaling bits from the signaling highway and line into the transmit and receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit and receive signaling registers. Bit 7 is the enable bit for channel 24. Signaling information for telephone channel c is carried in Time Slot c+1.

Address	Bit	Symbol	Description
1EB - Ch 1 2EB - Ch 2 3EB - Ch 3 4EB - Ch 4	7-6	Reserved	**Reserved:** Set to 0.
	5-0	SE30-SE25	**Signaling Enable for Channels 30-25:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When set to 0, the signaling states in both the transmit and receive signaling buffers are frozen. The ability to internally write the signaling bits from the signaling highway and line into the transmit and receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit and receive signaling registers. Bit 5 is the enable bit for channel 30. Signaling information for telephone channel c is carried in Time Slot c+1.

Receive and Transmit Signaling Registers

The following read/write register locations contain the ABCD signaling states associated with each of the telephone channels carried in Time Slots 1 through 31. When the signaling states for a channel are frozen, the microprocessor can write a new signaling state using the following registers.

Address	Bit	Symbol	Description
180 - Ch 1 280 - Ch 2 380 - Ch 3 480 - Ch 4	7-4	RSIGMAS	**Received Signaling Multiframe Alignment Signal:** The bits in this register contain the states of the received multiframe alignment pattern (Time Slot 16 bits 1-4 in frame 0) in the receive signaling buffer. This pattern is normally 0000. Bit 7 is received bit 1.
	3-0	RX0, RY, RX1, RX2	**Received Signaling Spare Bits and Remote Alarm Bit:** Bits 3, 1 and 0 in this register contain the states of the received X0, X1, X2 bits (spare bits) in Time Slot 16, which correspond to bits 5, 7, and 8 in frame 0 of the multiframe. The RY bit (bit 2) is defined as the loss of multiframe indication bit and is carried in bit 6 in frame 0 of the multiframe.
181 - Ch 1 281 - Ch 2 381 - Ch 3 481 - Ch 4	7-4 3-0	RA1-RD1 RA16-RD16	**Receive A1-D1 and A16-D16 Signaling Bits:** The signaling bits in this register are the states of the received A1 to D1 bits and the A16 to D16 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 1 (Time Slot 1) and 16 (Time Slot 17). Bit 7 is the A1 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1 (where c is the channel number, from 1 to 30). When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 1 and 16 in this register.

Address	Bit	Symbol	Description
182 - Ch 1 282 - Ch 2 382 - Ch 3 482 - Ch 4	7-4 3-0	RA2-RD2 RA17-RD17	**Receive A2-D2 and A17-D17 Signaling Bits:** The signaling bits in this register are the states of the received A2 to D2 bits and the A17 to D17 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 2 (Time Slot 2) and 17 (Time Slot 18). Bit 7 is the A2 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 2 and 17 in this register.
183 - Ch 1 283 - Ch 2 383 - Ch 3 483 - Ch 4	7-4 3-0	RA3-RD3 RA18-RD18	**Receive A3-D3 and A18-D18 Signaling Bits:** The signaling bits in this register are the states of the received A3 to D3 bits and the A18 to D18 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 3 (Time Slot 3) and 18 (Time Slot 19). Bit 7 is the A3 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 3 and 18 in this register.
184 - Ch 1 284 - Ch 2 384 - Ch 3 484 - Ch 4	7-4 3-0	RA4-RD4 RA19-RD19	**Receive A4-D4 and A19-D19 Signaling Bits:** The signaling bits in this register are the states of the received A4 to D4 bits and the A19 to D19 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 4 (Time Slot 4) and 19 (Time Slot 20). Bit 7 is the A4 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 4 and 19 in this register.
185 - Ch 1 285 - Ch 2 385 - Ch 3 485 - Ch 4	7-4 3-0	RA5-RD5 RA20-RD20	**Receive A5-D5 and A20-D20 Signaling Bits:** The signaling bits in this register are the states of the received A5 to D5 bits and the A20 to D20 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 5 (Time Slot 5) and 20 (Time Slot 21). Bit 7 is the A5 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 5 and 20 in this register.

Address	Bit	Symbol	Description
186 - Ch 1 286 - Ch 2 386 - Ch 3 486 - Ch 4	7-4 3-0	RA6-RD6 RA21-RD21	**Receive A6-D6 and A21-D21 Signaling Bits:** The signaling bits in this register are the states of the received A6 to D6 bits and the A21 to D21 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 6 (Time Slot 6) and 21 (Time Slot 22). Bit 7 is the A6 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding enable bit SEc is written with a 1. When the corresponding channel enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 6 and 21 in this register.
187 - Ch 1 287 - Ch 2 387 - Ch 3 487 - Ch 4	7-4 3-0	RA7-RD7 RA22-RD22	**Receive A7-D7 and A22-D22 Signaling Bits:** The signaling bits in this register are the states of the received A7 to D7 bits and the A22 to D22 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 7 (Time Slot 7) and 22 (Time Slot 23). Bit 7 is the A7 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding enable bit SEc is written with a 1. When the corresponding channel enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 7 and 22 in this register.
188 - Ch 1 288 - Ch 2 388 - Ch 3 488 - Ch 4	7-4 3-0	RA8-RD8 RA23-RD23	**Receive A8-D8 and A23-D23 Signaling Bits:** The signaling bits in this register are the states of the received A8 to D8 bits and the A23 to D23 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 8 (Time Slot 8) and 23 (Time Slot 24). Bit 7 is the A8 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding enable bit SEc is written with a 1. When the corresponding channel enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 8 and 23 in this register.
189 - Ch 1 289 - Ch 2 389 - Ch 3 489 - Ch 4	7-4 3-0	RA9-RD9 RA24-RD24	**Receive A9-D9 and A24-D24 Signaling Bits:** The signaling bits in this register are the states of the received A9 to D9 bits and the A24 to D24 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 9 (Time Slot 9) and 24 (Time Slot 25). Bit 7 is the A9 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding enable bit SEc is written with a 1. When the corresponding channel enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 9 and 24 in this register.

Address	Bit	Symbol	Description
18A - Ch 1 28A - Ch 2 38A - Ch 3 48A - Ch 4	7-4 3-0	RA10-RD10 RA25-RD25	**Receive A10-D10 and A25-D25 Signaling Bits:** The signaling bits in this register are the states of the received A10 to D10 bits and the A25 to D25 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 10 (Time Slot 10) and 25 (Time Slot 26). Bit 7 is the A10 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 10 and 25 in this register.
18B - Ch 1 28B - Ch 2 38B - Ch 3 48B - Ch 4	7-4 3-0	RA11-RD11 RA26-RD26	**Receive A11-D11 and A26-D26 Signaling Bits:** The signaling bits in this register are the states of the received A11 to D11 bits and the A26 to D26 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 11 (Time Slot 11) and 26 (Time Slot 27). Bit 7 is the A11 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 11 and 26 in this register.
18C - Ch 1 28C - Ch 2 38C - Ch 3 48C - Ch 4	7-4 3-0	RA12-RD12 RA27-RD27	**Receive A12-D12 and A27-D27 Signaling Bits:** The signaling bits in this register are the states of the received A12 to D12 bits and the A27 to D27 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 12 (Time Slot 12) and 27 (Time Slot 28). Bit 7 is the A12 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 12 and 27 in this register.
18D - Ch 1 28D - Ch 2 38D - Ch 3 48D - Ch 4	7-4 3-0	RA13-RD13 RA28-RD28	**Receive A13-D13 and A28-D28 Signaling Bits:** The signaling bits in this register are the states of the received A13 to D13 bits and the A28 to D28 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 13 (Time Slot 13) and 28 (Time Slot 29). Bit 7 is the A13 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 13 and 28 in this register.

Address	Bit	Symbol	Description
18E - Ch 1 28E - Ch 2 38E - Ch 3 48E - Ch 4	7-4 3-0	RA14-RD14 RA29-RD29	**Receive A14-D14 and A29-D29 Signaling Bits:** The signaling bits in this register are the states of the received A14 to D14 bits and the A29 to D29 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 14 (Time Slot 14) and 29 (Time Slot 30). Bit 7 is the A14 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 14 and 29 in this register.
18F - Ch 1 28F - Ch 2 38F - Ch 3 48F - Ch 4	7-4 3-0	RA15-RD15 RA30-RD30	**Receive A15-D15 and A30-D30 Signaling Bits:** The signaling bits in this register are the states of the received A15 to D15 bits and the A30 to D30 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 15 (Time Slot 15) and 30 (Time Slot 31). Bit 7 is the A15 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits for channels 15 and 30 in this register.
1D0 - Ch 1 2D0 - Ch 2 3D0 - Ch 3 4D0 - Ch 4	7-4	TSIGMAS	**Transmit Signaling Multiframe Alignment Signal:** The bits in this register contain the states of the transmit multiframe alignment pattern (Time Slot 16 bits 1-4 in frame 0) in the transmit signaling buffer. This pattern is normally 0000. Bit 7 is transmitted bit 1.
	3-0	TX0, TY, TX1, TX2	**Transmit Signaling Spare Bits:** Bits 3, 1 and 0 in this register contain the states of the transmit X0, X1, X2 bits (spare bits) in Time Slot 16, which are carried in bits 5, 7, and 8 of frame 0 in the multiframe. The TY bit (bit 2) is defined as the loss of multiframe indication bit and is carried in bit 6 in frame 0 of the multiframe. The TY bit is not propagated from the signaling highway to the line in any modes. The TX bits are not propagated from the signaling highway to the line except when the framer is in any of the Transmission Modes (2 Mbit/s, 8 Mbit/s or 16 Mbit/s).
1D1 - Ch 1 2D1 - Ch 2 3D1 - Ch 3 4D1 - Ch 4	7-4 3-0	TA1-TD1 TA16-TD16	**Transmit A1-D1 and A16-D16 Signaling Bits:** The signaling bits in this register are the A1 to D1 and A16 to D16 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 1 (Time Slot 1) and 16 (Time Slot 17). Bit 7 is the A1 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 1 and 16 in this register.

Address	Bit	Symbol	Description
1D2 - Ch 1 2D2 - Ch 2 3D2 - Ch 3 4D2 - Ch 4	7-4 3-0	TA2-TD2 TA17-TD17	**Transmit A2-D2 and A17-D17 Signaling Bits:** The signaling bits in this register are the A2 to D2 and A17 to D17 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 2 (Time Slot 2) and 17 (Time Slot 18). Bit 7 is the A2 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding enable bit SEc is written with a 1. When the corresponding channel enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 2 and 17 in this register.
1D3 - Ch 1 2D3 - Ch 2 3D3 - Ch 3 4D3 - Ch 4	7-4 3-0	TA3-TD3 TA18-TD18	**Transmit A3-D3 and A18-D18 Signaling Bits:** The signaling bits in this register are the A3 to D3 and A18 to D18 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 3 (Time Slot 3) and 18 (Time Slot 19). Bit 7 is the A3 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 3 and 18 in this register.
1D4 - Ch 1 2D4 - Ch 2 3D4 - Ch 3 4D4 - Ch 4	7-4 3-0	TA4-TD4 TA19-TD19	**Transmit A4-D4 and A19-D19 Signaling Bits:** The signaling bits in this register are the A4 to D4 and A19 to D19 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 4 (Time Slot 4) and 19 (Time Slot 20). Bit 7 is the A4 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 4 and 19 in this register.
1D5 - Ch 1 2D5 - Ch 2 3D5 - Ch 3 4D5 - Ch 4	7-4 3-0	TA5-TD5 TA20-TD20	**Transmit A5-D5 and A20-D20 Signaling Bits:** The signaling bits in this register are the A5 to D5 and A20 to D20 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 5 (Time Slot 5) and 20 (Time Slot 21). Bit 7 is the A5 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 5 and 20 in this register.

Address	Bit	Symbol	Description
1D6 - Ch 1 2D6 - Ch 2 3D6 - Ch 3 4D6 - Ch 4	7-4 3-0	TA6-TD6 TA21-TD21	**Transmit A6-D6 and A21-D21 Signaling Bits:** The signaling bits in this register are the A6 to D6 and A21 to D21 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 6 (Time Slot 6) and 21 (Time Slot 22). Bit 7 is the A6 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 6 and 21 in this register.
1D7 - Ch 1 2D7 - Ch 2 3D7 - Ch 3 4D7 - Ch 4	7-4 3-0	TA7-TD7 TA22-TD22	**Transmit A7-D7 and A22-D22 Signaling Bits:** The signaling bits in this register are the A7 to D7 and A22 to D22 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 7 (Time Slot 7) and 22 (Time Slot 23). Bit 7 is the A7 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 7 and 22 in this register.
1D8 - Ch 1 2D8 - Ch 2 3D8 - Ch 3 4D8 - Ch 4	7-4 3-0	TA8-TD8 TA23-TD23	**Transmit A8-D8 and A23-D23 Signaling Bits:** The signaling bits in this register are the A8 to D8 and A23 to D23 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 8 (Time Slot 8) and 23 (Time Slot 24). Bit 7 is the A8 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 8 and 23 in this register.
1D9 - Ch 1 2D9 - Ch 2 3D9 - Ch 3 4D9 - Ch 4	7-4 3-0	TA9-TD9 TA24-TD24	**Transmit A9-D9 and A24-D24 Signaling Bits:** The signaling bits in this register are the A9 to D9 and A24 to D24 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 9 (Time Slot 9) and 24 (Time Slot 25). Bit 7 is the A9 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 9 and 24 in this register.

Address	Bit	Symbol	Description
1DA - Ch 1 2DA - Ch 2 3DA - Ch 3 4DA - Ch 4	7-4 3-0	TA10-TD10 TA25-TD25	**Transmit A10-D10 and A25-D25 Signaling Bits:** The signaling bits in this register are the A10 to D10 and A25 to D25 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 10 (Time Slot 10) and 25 (Time Slot 26). Bit 7 is the A10 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 10 and 25 in this register.
1DB - Ch 1 2DB - Ch 2 3DB - Ch 3 4DB - Ch 4	7-4 3-0	TA11-TD11 TA26-TD26	**Transmit A11-D11 and A26-D26 Signaling Bits:** The signaling bits in this register are the A11 to D11 and A26 to D26 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 11 (Time Slot 11) and 26 (Time Slot 27). Bit 7 is the A11 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 11 and 26 in this register.
1DC - Ch 1 2DC - Ch 2 3DC - Ch 3 4DC - Ch 4	7-4 3-0	TA12-TD12 TA27-TD27	**Transmit A12-D12 and A27-D27 Signaling Bits:** The signaling bits in this register are the A12 to D12 and A27 to D27 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 12 (Time Slot 12) and 27 (Time Slot 28). Bit 7 is the A12 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 12 and 27 in this register.
1DD - Ch 1 2DD - Ch 2 3DD - Ch 3 4DD - Ch 4	7-4 3-0	TA13-TD13 TA28-TD28	**Transmit A13-D13 and A28-D28 Signaling Bits:** The signaling bits in this register are the A13 to D13 and A28 to D28 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 13 (Time Slot 13) and 28 (Time Slot 29). Bit 7 is the A13 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 13 and 28 in this register.

Address	Bit	Symbol	Description
1DE - Ch 1 2DE - Ch 2 3DE - Ch 3 4DE - Ch 4	7-4 3-0	TA14-TD14 TA29-TD29	**Transmit A14-D14 and A29-D29 Signaling Bits:** The signaling bits in this register are the A14 to D14 and A29 to D29 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 14 (Time Slot 14) and 29 (Time Slot 30). Bit 7 is the A14 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 14 and 29 in this register.
1DF - Ch 1 2DF - Ch 2 3DF - Ch 3 4DF - Ch 4	7-4 3-0	TA15-TD15 TA30-TD30	**Transmit A15-D15 and A30-D30 Signaling Bits:** The signaling bits in this register are the A15 to D15 and A30 to D30 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 15 (Time Slot 15) and 30 (Time Slot 31). Bit 7 is the A15 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit SEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 15 and 30 in this register.

HDLC Link Control Registers

The bits in the following read/write registers control the transmit and receive HDLC link that is carried in the Sa bits (bits 4-8) of Time Slot 0 in NFAS frames (frame 2).

Address	Bit	Symbol	Description
108 - Ch 1 208 - Ch 2 308 - Ch 3 408 - Ch 4	7	EHR	**Enable HDLC Receiver:** A 1 enables the HDLC receiver. After flag detection and zero bit destuffing the bytes are written into the receive HDLC FIFO. A 0 disables the HDLC controller, clears the FIFO, and disables the HDLC receive interrupts.
	6	EHT	**Enable HDLC Transmitter:** A 1 enables the HDLC transmitter. The transmitter will send flags when the transmit HDLC FIFO is empty. The bytes are formatted into the message when the FIFO has bytes present. A 0 disables the HDLC controller, clears the FIFO, disables the HDLC transmit interrupts, but will continue to send flags as a fill in selected national bits if control bits SA4-SA8 (bit 4-0) in register X0CH are set to a 1 unless bypassed by control bit BNAL (bit 1) in register X01H is set to a1.
	5	TAB	**Transmit Abort:** When set to 1, the transmit HDLC controller will transmit the abort sequence (a zero followed by seven ones) after the next data byte. This is followed by clearing the transmit HDLC FIFO, and sending continuous flags.
	4	EOM	**Transmit End Of Message Flag:** When set to 1, the transmit HDLC FIFO contains the last byte in the message. When the FIFO has emptied, the 16-bit CRC is transmitted, and this followed by an interrupt.

Address	Bit	Symbol	Description
108 - Ch 1 208 - Ch 2 308 - Ch 3 408 - Ch 4 (cont.)	3	RHIE	**Receiver Half Full Interrupt Enable:** RHIE defines the function of the Receive HDLC Interrupt Status bits RHIS2-RHIS0 (bits 7-5 of register X16H). When set to 1, the Receive HDLC controller generates an interrupt when the receive HDLC FIFO is half full, or at the end of the message. When set to 0, the HDLC controller generates an interrupt request only at the end of the message or when the FIFO has overflowed.
	2	THIE	**Transmit Half Full Interrupt Enable:** THIE defines the function of the Transmit HDLC Interrupt Status bit THIS (bit 4 of register X16H). When set to 1, the Transmit HDLC controller generates an interrupt when the transmit HDLC FIFO is half full, or at the end of the message. When set to 0, the HDLC controller generates an interrupt request only at the end of the message or when the FIFO has underflowed.
	1-0	Reserved	**Reserved:** Set to 0.
10C - Ch 1 20C - Ch 2 30C - Ch 3 40C - Ch 4	7-5	Reserved	**Reserved:** Set to 0.
	4-0	SA4-SA8	**Enable Sa Bits:** A 1 written to one or more bits selects the corresponding Sa bit in Time Slot 0 of NFAS frames (frame 2) to be included as part of the HDLC link. For example, a value of 11111 selects all five of the national bits Sa4 through Sa8 as the data link and provides a bandwidth of 5 x 4 = 20 kbit/s.

HDLC Link Transmit and Receive Data Registers

The first two registers are used for writing the transmit bytes into the 16-byte transmit FIFO, and for reading the receive bytes from the receive FIFO, for the HDLC message. Register X18H indicates the number of bytes in the receive FIFO. All registers are read/write. These registers are either read or written, not both, for normal operation. For these registers, a write operation may not be followed by a read operation unless at least 7 cycles of SYSCLK occur following the end of the last write cycle.

Address	Bit	Symbol	Description
10A - Ch 1 20A - Ch 2 30A - Ch 3 40A - Ch 4	7-0	THD7-THD0	**HDLC Transmit Data:** The byte written to this location is written to the transmit FIFO. Bit 0 corresponds to the first bit transmitted in the HDLC message byte.
117 - Ch 1 217 - Ch 2 317 - Ch 3 417 - Ch 4	7-0	RHD7-RHD0	**HDLC Receive Data:** A read cycle transfers one byte from the receive FIFO into this location. Bit 0 corresponds to the first bit received in the HDLC message byte.
118 - Ch 1 218 - Ch 2 318 - Ch 3 418 - Ch 4	7-5	Reserved	**Reserved:** Set to 0.
	4-0	C4-C0	**HDLC Receive FIFO Depth**: This register indicates the number of data bytes currently present in the HDLC receive FIFO. The value read is in binary. Bit 0 is the LSB value. For example, the value 00000 indicates that the FIFO is empty, and the value 01111 indicates that there are 15 bytes present in the receive FIFO.

HDLC Link Status Registers

These registers are all read/write. The status bits in the X0E registers represent the latched status and interrupt request indications generated by the receive and transmit HDLC controllers and the FIFOs. The latched event bits are a result of a receive or transmit status indication or interrupt request in the HDLC Link Status register X16H. The bits latch on either the rising edge, the falling edge, or both edges of the current status or interrupt request event bits as defined by the RISE/FALL control bits (bits 6 and 5) in the Global Configuration Register 006H. A latched bit causes a hardware interrupt indication when the corresponding mask bit in the HDLC Link Mask Register X0FH is written with a 0. The status bits in register X16H represent the current (unlatched) status and interrupt request indications generated by the receive and transmit HDLC controllers and FIFOs.

Address	Bit	Symbol	Description
10E - Ch 1 20E - Ch 2 30E - Ch 3 40E - Ch 4	7-5	ERHIS2- ERHIS0	**Latched Receive HDLC Interrupt Events:** The latched bits in this location correspond to a receive HDLC interrupt status indication in bits 7-5 in register X16H. These bits are cleared by writing a 0 to any bit position that is set. A hardware interrupt is generated when any of these bits latches and the corresponding mask bit position in register X0FH is written with a 0. During normal message reception ERHIS0 does not get set at the start of message reception (RHIS2 - RHIS0 = 001).
	4	ETHIS	**Latched Transmit HDLC Interrupt Event:** The latched bit in this location corresponds to a transmit HDLC interrupt status indication in bit 4 in register X16H. This bit is cleared by writing a 0 to it. A hardware interrupt is generated when this bit latches and the corresponding mask bit position in register X0FH is written with a 0.
	3-2	ERXFS1- ERXFS0	**Latched Receive HDLC FIFO Status Events:** The latched bits in this location correspond to receive HDLC FIFO status indications in bits 3-2 in X16H. These bits are cleared by writing a 0 to any bit position that is set. If not masked by the corresponding mask bit position in register X0FH, a hardware interrupt is generated when any of these bits latches.
	1-0	ETXFS1- ETXFS0	**Latched Transmit HDLC FIFO Status Events:** The latched bits in this location correspond to transmit HDLC FIFO status indications in bits 1-0 in register X16H. These bits are cleared by writing a 0 to any bit position that is set. A hardware interrupt is generated when this bit latches and the corresponding mask bit position in register X0FH is written with a 0.
10F - Ch 1 20F - Ch 2 30F - Ch 3 40F - Ch 4	7-5	MRHIS2- MRHIS0	**Receive HDLC Interrupt Mask:** When one or more bits are set to a 1, the latched receive HDLC interrupt event indications in corresponding bits 7-5 in register X0EH are masked from causing a hardware interrupt. For example, if 001 is written into this location, a start of message indication is masked from causing a hardware interrupt (see RHIS2-RHIS0).
	4	MTHIS	**Transmit HDLC Interrupt Mask:** When set to 1, the latched transmit HDLC interrupt event indication corresponding to bit 4 in register X0EH is masked from causing a hardware interrupt (see THIS).
	3-2	MRXFS1- MRXFS0	**Receive HDLC FIFO Status Interrupt Mask:** When one or more bits are set to a 1, a latched receive HDLC FIFO event indication in corresponding bits 3-2 in register X0EH is masked from causing a hardware interrupt. For example, if a 01 is written into this location, a half or more than half full indication is masked from causing a hardware interrupt (see RXFS1-RXFS0).

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>10F - Ch 1
20F - Ch 2
30F - Ch 3
40F - Ch 4
(cont.)</td><td>1-0</td><td>MTXFS1-MTXFS0</td><td>Transmit HDLC FIFO Status Interrupt Mask: When one or more bits are set to a 1, a latched transmit HDLC FIFO status event that has taken place in corresponding bits 1-0 in register X0EH is masked from causing a hardware interrupt. For example, if a 01 is written into this location, a less than half full indication is masked from causing a hardware interrupt (see TXFS1-TXFS0).</td></tr>
<tr><td rowspan="4">116 - Ch 1
216 - Ch 2
316 - Ch 3
416 - Ch 4</td><td>7-5</td><td>RHIS2-RHIS0</td><td>Receive HDLC Interrupt Status: The following table lists the various interrupt status indications for the receive HDLC message. Condition 010 is additionally defined by control bit RHIE (bit 3 of register X08H).

<table>
<tr><th>RHIS2</th><th>RHIS1</th><th>RHIS0</th><th>RHIE</th><th>Condition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td><td>Idle Condition.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X</td><td>Start of message indication.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Valid message received (CRC checked OK) or FIFO overflow.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Valid message received (CRC checked OK) or FIFO needs servicing (e.g., half full).</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X</td><td>Message received with a CRC error.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>X</td><td>Abort detected.</td></tr>
</table>
X represents either value may be indicated.</td></tr>
<tr><td>4</td><td>THIS</td><td>Transmit HDLC Interrupt Status: A 1 indicates that the transmit FIFO needs servicing, either because the message is completed, or because the FIFO is less than half full, as determined by control bit THIE (bit 2 of register X08).</td></tr>
<tr><td>3-2</td><td>RXFS1-RXFS0</td><td>Receive FIFO Status: The following table lists the various receive FIFO status indications for the receive HDLC message.

<table>
<tr><th>RXFS1</th><th>RXFS0</th><th>Condition</th></tr>
<tr><td>0</td><td>0</td><td>Normal. FIFO less than half full.</td></tr>
<tr><td>0</td><td>1</td><td>FIFO equal to or greater than half full.</td></tr>
<tr><td>1</td><td>0</td><td>FIFO full.</td></tr>
<tr><td>1</td><td>1</td><td>FIFO overflowed (attempt to write to a full FIFO).</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>TXFS1-TXFS0</td><td>Transmit FIFO Status: The following table lists the various transmit FIFO status indications for the transmit HDLC message.

<table>
<tr><th>TXFS1</th><th>TXFS0</th><th>Condition</th></tr>
<tr><td>0</td><td>0</td><td>Normal. FIFO equal to or greater than half full.</td></tr>
<tr><td>0</td><td>1</td><td>FIFO less than half full.</td></tr>
<tr><td>1</td><td>0</td><td>FIFO overflowed (attempt to write to a full FIFO).</td></tr>
<tr><td>1</td><td>1</td><td>FIFO underflowed (attempt to read an empty FIFO).</td></tr>
</table></td></tr>
</table>

APPLICATION DIAGRAM

The diagram in Figure 63 illustrates the use of the QE1F-*Plus* device to provide framing and time slot access for a variety of E1 sources. Direct control of most commercial line interface unit devices (LIUs) is provided. Note that these applications require operating the QE1F-*Plus* at V_{DD} = +5.0 volt to comply with the +5.0 volt parts connected to the QE1F-*Plus*.

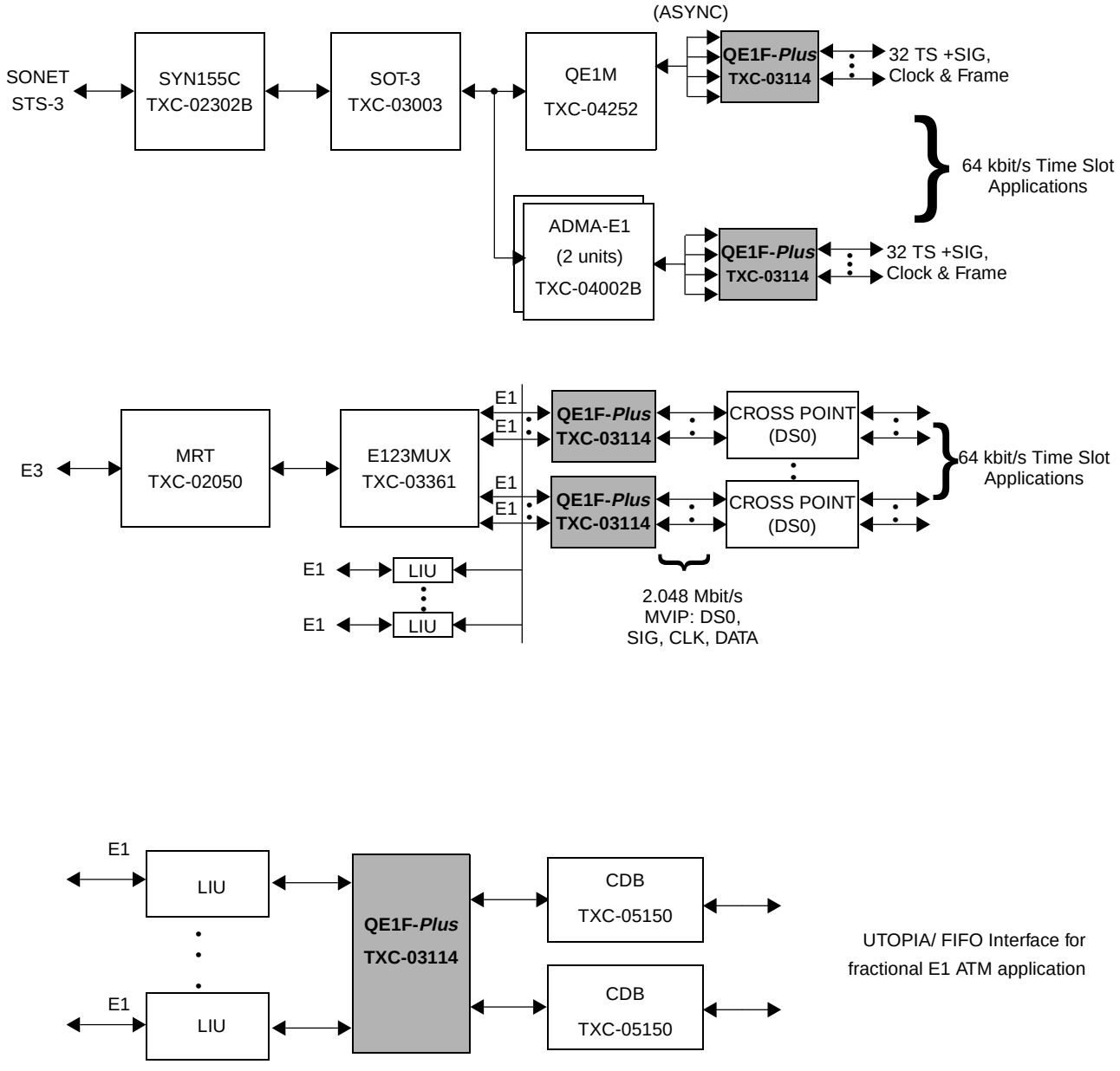
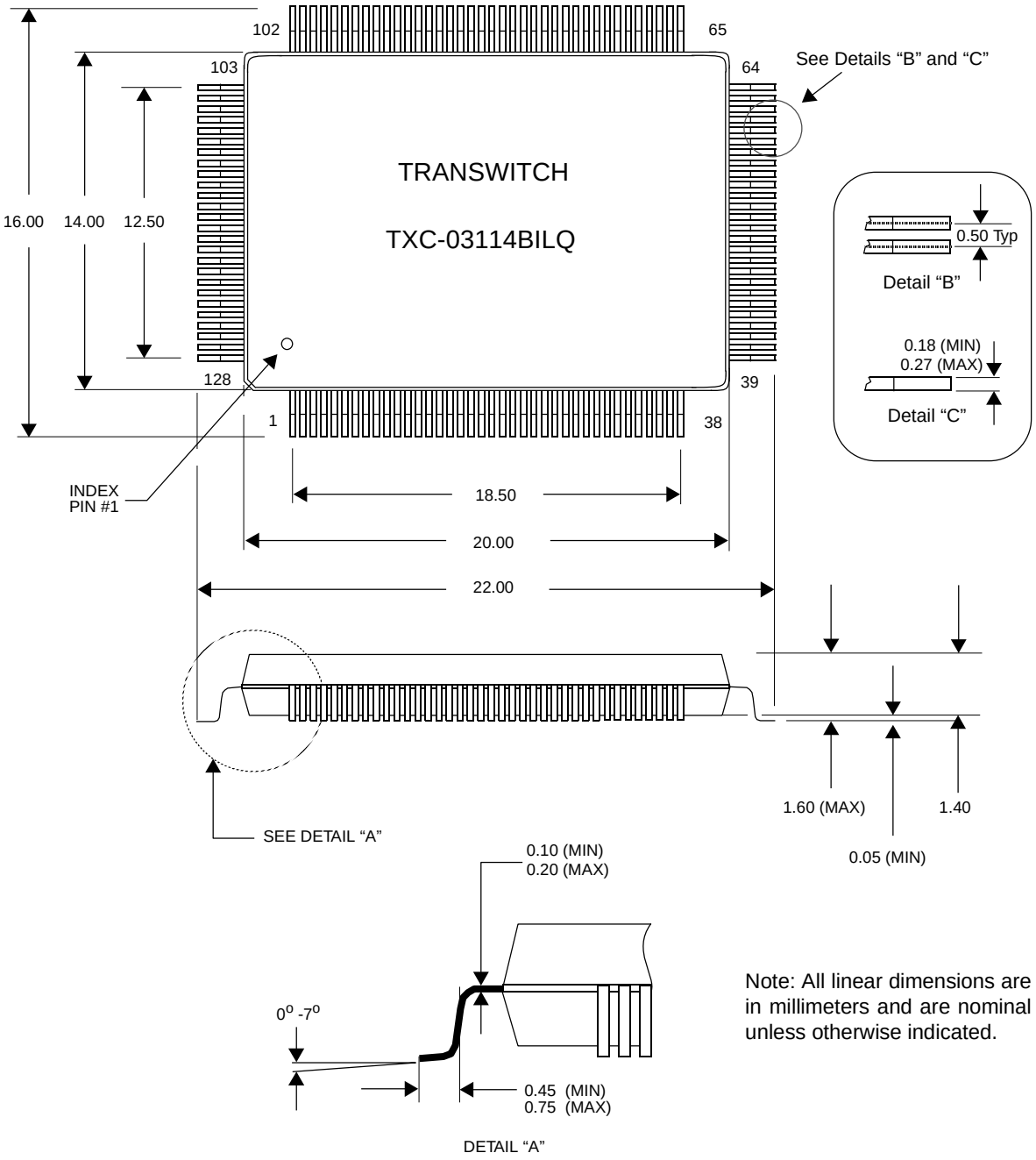


Figure 63. Some QE1F-*Plus* TXC-03114 Applications

PACKAGE INFORMATION

The QE1F-*Plus* device is packaged in a 128-pin low profile plastic quad flat package suitable for surface mounting, as illustrated in Figure 64.



Note: This 128-pin low profile plastic quad flat package conforms to the JEDEC MS-026-BHB Standard Outline.

Figure 64. QE1F-*Plus* TXC-03114 128-Pin Low Profile Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-03114BILQ 128-pin Low Profile Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02020/21, ART/ARTE VLSI Devices (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface. ARTE has the same functionality as ART, plus expanded features.

TXC-02050, MRT Multi-Rate Line Interface device. The MRT directly interfaces with the E123MUX device and provides the functions for terminating ITU-T-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU-T line rates.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single low-power unit. It has both clock and data outputs on the line side.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-T standards.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). This device provides extended features relative to the 84-pin TXC-03001B SOT-1 devices, and it has a 144-pin package.

TXC-03109, E1Fx8 VLSI Device (8-Channel E1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to E1 lines and operates from a power supply of 3.3 volt.

TXC-03361, E123MUX VLSI Device (E1/E2/E3 Mux/Demux). The E123MUX is a CMOS VLSI device that provides the E13 functions needed to multiplex and demultiplex 16 independent E1 signals to and from an E3 signal that conforms to the ITU-T G.751 Recommendation. The E123MUX can also be configured to operate as an E12 or E23 multiplexer and demultiplexer.

TXC-04002B, ADMA-E1 VLSI Device (Dual E1 to TU-12 Async Mapper-Desync). Interconnects two E1 signals with any two asynchronous mode TU-12 tributaries carried in SDH AU-3 rate payload interface.

TXC-04216, E1Mx16 VLSI Device (E1 Mapper 16-Channel). Sixteen E1 2.048 Mbit/s signals are mapped to and from asynchronous Tributary Unit-12s (TU-12s) or Virtual Tributary 2s (VT2s).

TXC-04252, QE1M VLSI Device (Quad E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects four E1 signals with any four asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-05101C, HDLC VLSI Device (HDLC Controller, 36-Bit Terminal I/O). High Speed High Level Data Link Controller that sends and receives packets at line rates up to 51.84 Mbit/s using either a nibble-parallel, byte-parallel, or serial interface.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble-parallel, or byte-parallel interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: 650-949-6700
Fax: 650-949-6705
Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79
Web: www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698
Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: 800-854-7179 (within U.S.A.)
Tel: 314-726-0444 (outside U.S.A.)
Fax: 314-726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: 800-669-6857 (within U.S.A.)
Tel: 903-769-3717 (outside U.S.A.)
Fax: 508-650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: 215-697-2179
Fax: 215-697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: 800-433-5177 (within U.S.A.)
Tel: 503-693-6232 (outside U.S.A.)
Fax: 503-693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (within U.S.A.)
Tel: 908-699-5800 (outside U.S.A.)
Fax: 908-336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated QE1F-*Plus* Data Sheet that have significant differences relative to the previous and now superseded QE1F-*Plus* Data Sheet:

Updated QE1F-*Plus* Data Sheet: *PRELIMINARY* Ed. 2, July 1999

Previous QE1F-*Plus* Data Sheet: *PRODUCT PREVIEW* Ed. 1, September 1998

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date. Changed *PRODUCT PREVIEW* to *PRELIMINARY.*
1	Added last line to System Interfaces under Features. Changed "thin" to "low profile" in last line of Features. Changed *PRODUCT PREVIEW* text to *PRELIMINARY* text in right margin.
2-4	Updated Table of Contents and List of Figures.
5	Reduced two power dissipation values in first paragraph. Changed "April 1992" to "Nov. 1996 Draft" in line prETS 300 011. Added one new line item under "TS0/CRC-4 Multiframe" and changed another.
7	Changed third line item under second bullet to indicate that PRBS testing is available only in 2 Mbit/s Transmission Mode.
8	Reduced power dissipation values on three lines in last two paragraphs.
21	Changed "T1" to "E1" three times for Receive Fractional E1 Gapped Clock Output in Name/Function column.
22	For Symbol PRBSOOL, changed Name/Function column to indicate that pin is enabled only in 2 Mbit/s Transmission Mode.
24	For Symbol SYSCLK, modified Name/Function column to reduce permitted frequency range and inserted new table.
25	Made extensive changes to both Power Requirements tables and deleted their notes.
27	Changed Test Conditions for Parameters V_{OH} and V_{OL} in last two tables.
28	Changed Test Conditions for Parameters V_{OH} and V_{OL} in second table.
30	Changed Test Conditions for Parameters V_{OH} and V_{OL} in last two tables.
31	Changed Test Conditions for Parameters V_{OH} and V_{OL} in last table.
32, 34	Modified Note 2 to change definition of minimum frequency of SYSCLK.
43-46, 52, 53	Changed Max for Symbol t_{PW} and added Note 2.
48-51	Changed Max for Symbols t_{PW}, $t_{PW(1)}$ and $t_{PW(2)}$, and added Notes 2 and 3.
51, 52	Increased Min for Symbols $t_{SU(1)}$ and t_{SU}.
54, 56	Changed "T1" to "E1" in Figure titles and increased Max for Symbols $t_{D(1)}$ and t_D in tables.
55	Changed "T1" to "E1" and added "and 2 Mbit/s MVIP" in Figure title. Added descriptive information for 2 Mbit/s MVIP Mode in diagram, table and note.
56, 57	Added 2 Mbit/s MVIP Mode information to Figure 27. Changed all Min. values for Transmission Mode.
58	Increased Max for Symbol t_D.

Page Number of Updated Data Sheet	Summary of the Change
59	Modified waveform diagram and table. Deleted Symbol $t_{SU(3)}$. Changed Symbol $t_{H(3)}$ to $t_{H(2)}$. Changed Min value of $t_{D(2)}$. Changed Parameter, Min and Typ for Symbol $t_{D(3)}$. Changed 18 MHz to 19 MHz in Note 2. Added Note 3.
60	Changed waveform diagram and table. Deleted Symbol $t_{SU(3)}$. Increased Min for Symbol $t_{PW(1)}$. Inserted new table rows for Symbols $t_{H(3)}$, $t_{SU(4)}$ and $t_{H(4)}$. Changed Min, Typ and Parameter for Symbol $t_{D(3)}$. Changed Parameters for some table rows to include references to Note 4.
61	Changed 18 MHz to 19 MHz in Note 2. Added Notes 4, 5 and 6.
62	Changed frequency value in Note 2.
63	Modified waveform diagram. Inserted new parameters for Symbols $t_{SU(5)}$ and $t_{H(4)}$ in table. Changed frequency value in Note 2. Added Notes 4 and 5 for Symbols $t_{PW(1)}$ and $t_{H(4)}$.
63	Added Figure 34.
71	Changed text in Transmit Highway section to agree with frame numbering change in Figure 40.
72	Changed frame numbering to "0 to 15" from "1 to 16" in Figure 40.
73	Changed text in Receive Highway section to agree with frame numbering change in Figure 41. Inserted "a regenerated" in fifth line of last paragraph.
74	Changed frame numbering to "0 to 15" from "1 to 16" in Figure 41.
86	Inserted third line of first paragraph under Fractional E1 Capability to add 2 Mbit/s MVIP Mode. Modified columns that are headed CONFIG1 pin 43 and System Interface in table.
88	Added to seventh line of paragraph that begins with "The QE1F-*Plus*". Added last two sentences to penultimate paragraph that begins with "For ISDN applications".
91	Added last sentence of fourth paragraph, "When control bit AAGS...".
96	Made extensive changes to numeric values in throughput delay table.
109	Added "and MVIP" to third line and changed last sentence of first paragraph. Clarified local loopback path description and Figure 58 (to show AMI codec capability). Added last sentence of second paragraph.
110	Clarified Figure 59 to show AMI codec capability. Modified third sentence and added last sentence of first paragraph.
111	Modified second and fifth sentences of first paragraph.
114	Added reference to availability of BSDL file on TranSwitch Web Site.
118	Modified second and third sentences of second paragraph to indicate action of software reset. Added last paragraph.
123	Changed slip buffer pointer status registers from read-only (R) status to read/write (RW).
128	Changed Description column for global software register to redefine its action.
131	Added last sentence of Note in first paragraph of Description column.
132	Modified third sentence of first paragraph.
135	Changed first sentence of Description for Symbol PRBSEN to indicate PRBS is enabled only in the 2 Mbit/s Transmission Mode.
141	Modified Description column for Symbols RXF and TXF.
145, 146	Inserted "high" and "or 2 Mbit/s MVIP Mode" in Description column for Addresses 13A to 13F.
146	Added last sentence to text paragraph. Changed HDB3 to AMI/HDB3 in Description column for Symbols RLP and LLP.
147	Changed Description column for Symbol INSPRBS to indicate that PRBS test feature is limited to 2 Mbit/s Transmission Mode.

Page Number of Updated Data Sheet	Summary of the Change
149	Added last sentence to Description column for Symbol BPV. Modified fourth sentence of first paragraph.
159	Modified last sentence of Description column for Symbol ECRCE.
160, 177	Added last sentence to text paragraph.
178	Added last sentence to Description column for Symbols ERHIS2-ERHIS0.
179	Clarified Description column for Symbols RHIS2-RHIS0, 0101 condition in the table.
182-185	Made extensive changes to update Related Products and Standards Documentation Sources sections.
186-188	Added List of Data Sheet Changes section.
189	Changed *PRODUCT PREVIEW* paragraph to *PRELIMINARY* paragraph at lower right.

-NOTES-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