256K x 16 Bit CMOS Video RAM

FEATURES

- Dual port Architecture
  256K x 16 bits RAM port
  512 x 16 bits SAM port
- Performance range :

Parameter \ Speed		-6	-7	-8
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page cycle (t_{HPC})		24ns	28ns	33ns
SAM access time (t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	20ns	25ns
RAM active current	KM4216C256	120mA	110mA	100mA
	KM4216V256	110mA	100mA	90mA
SAM active current	KM4216C256	50mA	45mA	40mA
	KM4216V256	40mA	35mA	30mA

- Fast Page Mode with Extended data out
- RAM Read, Write, Read-Modify-Write
- Serial Read (SR)
- Read / Real time read transfer (RT, RRT)
- Split Read Transfer with Stop Operation (SRT)
- Byte / Word Write Operation
- 8 Column Block Write (BW) and Write-per-Bit with Masking Operation (New and Old Mask)
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh
- Common Data I/O Using three state RAM Output Control
- All Inputs and Outputs TTL Compatible
- Refresh : 512 Cycle/8ms
- Single +5V ± 10% Supply Voltage (KM4216C256)
- Single +3.3 ± 10% Supply Voltage (KM4216V256)
- Plastic 64-Pin 525mil SSOP (0.8mm pin pitch)

GENERAL DESCRIPTION

The Samsung KM4216C/V256 is a CMOS 256K x 16 bit Dual Port DRAM. It consists of a 256K x 16 dynamic random access memory (RAM) port and 512 x 16 static serial access memory (SRAM) port. The RAM and SRAM port operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits.
It operates like a conventional 256K x 16 CMOS DRAM.
The RAM port has a write per bit mask capability.
Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, Byte/Word write operation and Block Write capabilities.

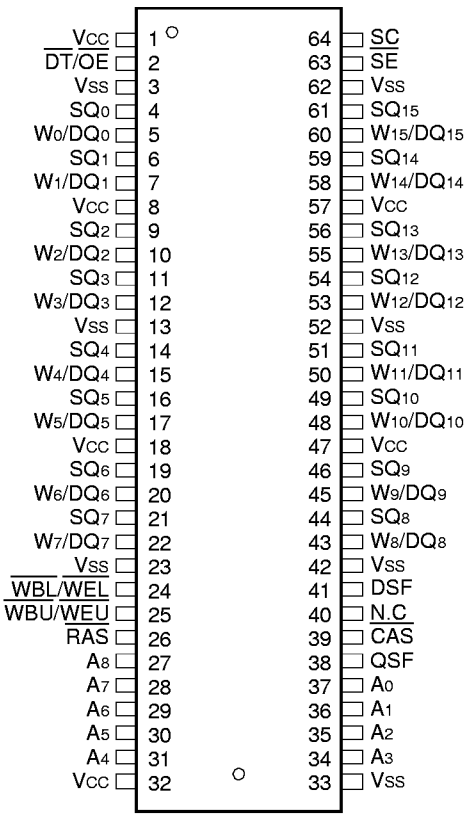
The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate. The SAM port has serial read capability.

Data may be internally transferred from the RAM to SAM port using read, and programmable (Stop Register) Split Transfers.
Refresh is accomplished by familiar DRAM refresh modes.
The KM4216C/V256 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (TOP VIEWS)

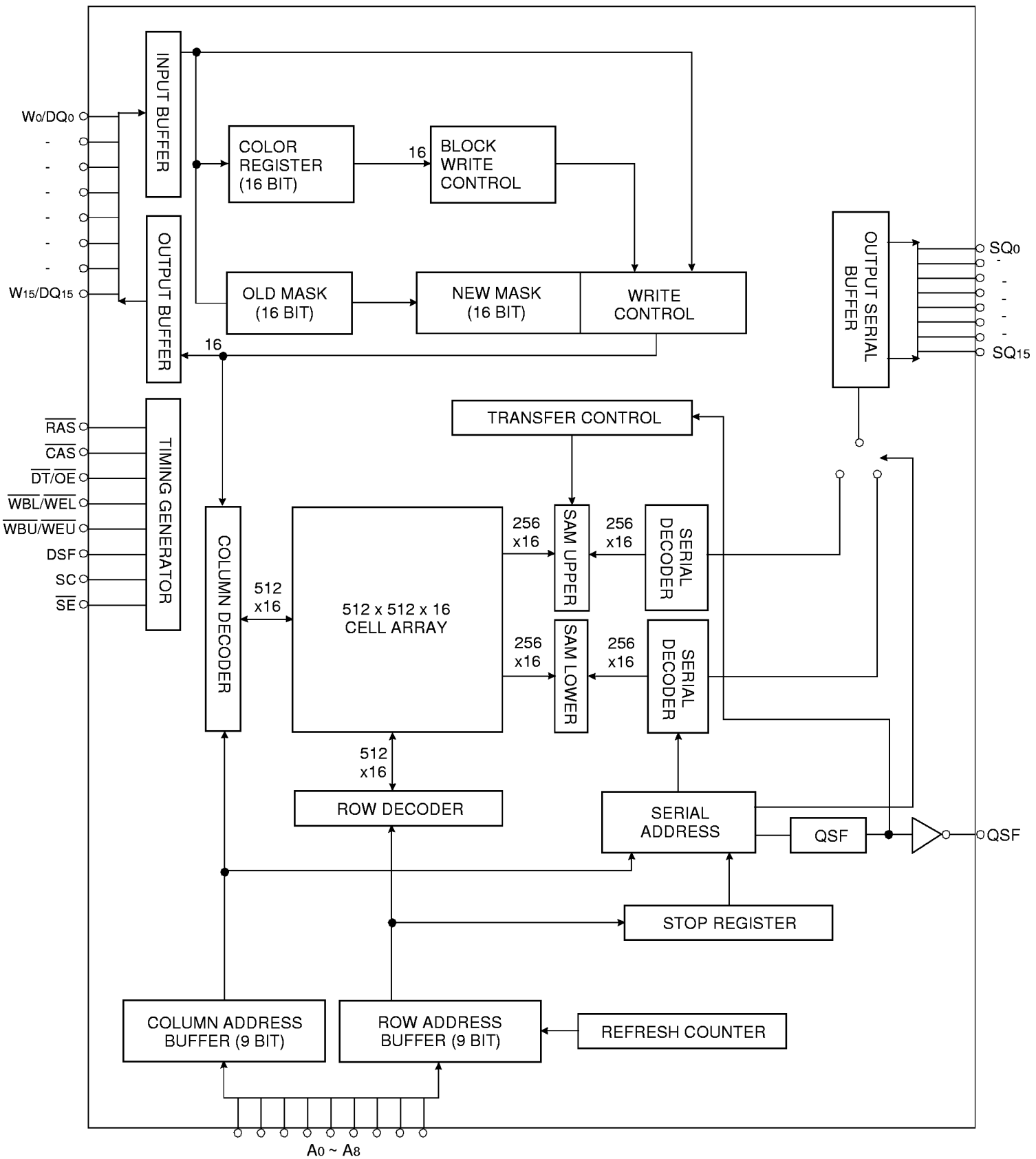
64-Pin 525 mil SSOP



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
$\overline{RAS}$	IN	Row address strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high"
$\overline{CAS}$	IN	Column address strobe. $\overline{CAS}$ is used to clock in the 9 column address bits as a strobe for the DSF inputs.
Address	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following 9 column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).
$\overline{WBL}/\overline{WEL}$ $\overline{WBU}/\overline{WEU}$ (Lower, Upper)	IN	The $\overline{WBX}/\overline{WEX}$ input is a multi-function pin. When $\overline{WBX}/\overline{WEX}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same as a standard DRAM. When $\overline{WBX}/\overline{WEX}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multi-function pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions (BW, FW, Split Transfer, etc.) are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register.
SQi	OUT	Serial output pin for serial read.(Serial write is not supported)
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0~255, High if address is 256~511.
$\overline{SE}$	IN	In a serial read cycle, $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
V_{CC}	SUPPLY	Power supply (+5.0V & +3.3V)
V_{SS}	SUPPLY	Ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	RAS ↓				CAS ↓	Address		DQi Input		Register		Function
	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE	Mask	Color	
CBRS (Note 1,3)	0	X	0	1	-	Stop (Note4)	-	X	-	-	-	CBR Refresh/Stop (No reset)
CBRN (Note 1)	0	X	1	1	-	X	-	X	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	X	X	0	-	X	-	X	-	-	-	CBR Refresh (Option reset)
ROR	1	1	X	0	-	Row	-	X	-	-	-	RAS - only Refresh
RT	1	0	1	0	X	Row	Tap	X	X	-	-	Read Transfer
SRT	1	0	1	1	X	Row	Tap	X	X	-	-	Split Read Transfer
RWM	1	1	0	0	0	Row	Col.	WMi	Data	Use	-	Masked Write (New / Old Mask)
BWM	1	1	0	0	1	Row	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New / Old Mask)
RW	1	1	1	0	0 (Note6)	Row	Col.	X	Data	-	-	Read or Write
BW	1	1	1	0	1	Row	Col.	X	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	Row (Note7)	X	X	WMi	Load (Note5)	-	Load(Old) Mask Register set Cycle
LCR	1	1	1	1	1	Row (Note7)	X	X	Color	-	Load	Load Color Register set Cycle

X : Don't Care, - : Not Applicable, Tap : SAM Start (Column) Address, WMi : Write Mask Data (i=0 ~15)
RAS only refresh does not reset Stop or LMR functions.

Notes :

(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask. (Use CBRR reset to new mask, use CBRS or CBRN to perform CAS-before-RAS refresh while using Old mask)
(3) After CBRS cycle, SRT use Stop Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don't care
(7) The Row that is addressed will be refreshed, but a Row address is not required.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM4216C256	KM4216V256	
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC} + 0.5	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	-0.5 to + 4.6	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power dissipation	P_D	1	0.6	W
Short circuit output current	I_{OS}	50	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage Reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	KM4216C256			KM4216V256			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	- 0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current { Any Input 0 ≤ V_{IN} ≤ V_{CC} +0.5V (0.3)*1, all other pins not under test = 0 volts.}	I_{IL}	-10	10	uA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OL}	-10	10	uA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}= 2mA, SAM I_{OL}= 2mA)	V_{OL}	-	0.4	V

Note) *1 : KM4216V256

CAPACITANCE (V_{CC} = 5V, f=1MHz, T_A=25 °C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0 ~ A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0 ~ W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C256			KM4216V256			Unit
			-6	-7	-8	-6	-7	-8	
Operating Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Standby *2	I_{CC1}	120	110	100	110	100	90	mA
	Active	I_{CC1} A	160	145	130	140	125	110	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ = V_{IH}, DSF=V_{IL})	Standby *2	I_{CC2}	10	10	10	10	10	10	mA
	Active	I_{CC2} A	50	45	40	40	35	30	mA
$\overline{RAS}$ Only Refresh Current *1 ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	Standby *2	I_{CC3}	120	110	100	110	100	90	mA
	Active	I_{CC3} A	160	145	130	140	125	110	mA
Extended Fast Page Mode Current *1 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min)	Standby *2	I_{CC4}	120	110	100	110	100	90	mA
	Active	I_{CC4} A	160	145	130	140	125	110	mA
$\overline{CAS}$- Before-$\overline{RAS}$ Refresh Current *1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Standby *2	I_{CC5}	120	110	100	110	100	90	mA
	Active	I_{CC5} A	160	145	130	140	125	110	mA
Data Transfer Current *1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Standby *2	I_{CC6}	140	130	120	130	120	110	mA
	Active	I_{CC6} A	180	165	150	160	145	130	mA
Block Write Cycle Current *1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Standby *2	I_{CC7}	120	110	100	110	100	90	mA
	Active	I_{CC7} A	160	145	130	140	125	110	mA
Color Register Load Current *1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Standby *2	I_{CC8}	110	90	80	90	80	70	mA
	Active	I_{CC8} A	140	125	110	120	105	90	mA

Note *1. Real values dependent on output loading and cycle rates. Specified values are obtained with the output open.
Icc is specified as average current.
In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, address transition should be changed only once while $\overline{RAS}$ = V_{IL}
In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$ = V_{IH}
*2. SAM standby condition : $\overline{SE}$ ≥ V_{IH}, SC ≤ V_{IL} or ≥ V_{IH}

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, KM4216C256 : V_{CC}=5.0V±10%, KM4216V256 : 3.3V±10%)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	104		124		144		ns	
Read-modify-write cycle time	t_{RWC}	140		170		190		ns	
Hyper page mode cycle time	t_{HPC}	25		30		35		ns	15
		30		35		40		ns	16
Hyper page read-modify-write cycle time	t_{HPRWC}	70		74		79		ns	15
		76		81		91		ns	16
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,6
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ Precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	3	15	3	15	3	15	ns	7
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		55		65		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	10	10K	12	10K	ns	15
		15		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	15	50	15	60	ns	5
$\overline{RAS}$ to column addr. delay time	t_{RAD}	12	30	12	35	12	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR Counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	10		10		10		ns	
Output hold time from $\overline{CAS}$	t_{DOH}	3		3		3		ns	
Row addr. set-up time	t_{ASR}	0		0		0		ns	
Row addr. hold time	t_{RAH}	10		10		10		ns	
Column addr. set-up time	t_{ASC}	0		0		0		ns	
Column addr. hold time	t_{CAH}	10		12		15		ns	
Column addr. to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Output buffer turn off delay from $\overline{WB}$/$\overline{WE}$	t_{WEZ}	3	15	3	15	3	15	ns	7
Write command pulse width	t_{WPZ}	10		10		10		ns	7
Write command hold time	t_{WCH}	10		10		15		ns	
Write command pulse width	t_{WP}	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		12		15		ns	10
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	35		40		40		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		100		ns	8
Column addr. to $\overline{WE}$ delay time	t_{AWD}	50		55		60		ns	8
$\overline{CAS}$ set-up time (CBR refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time (CBR refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
Access time from output enable	t_{OEA}		15		20		20	ns	
Output enable to data input delay	t_{OED}	15		15		15		ns	
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	3	15	3	15	3	15	ns	7
Output enable command hold time	t_{OEH}	15		15		15		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period (512 cycle)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	t_{FSR}	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	t_{RFH}	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	t_{FSC}	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	10		15		15		ns	
Write per bit mask data set-up time	t_{MS}	0		0		0		ns	
Write per bit mask data hold time	t_{MH}	10		10		15		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	10		10		15		ns	
$\overline{DT}$ low set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	10		10		15		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (RRT)	t_{RTH}	50		60		65		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (RRT)	t_{CTH}	15		20		25		ns	
$\overline{DT}$ low hold refer. to column address (RRT)	t_{ATH}	20		25		30		ns	
$\overline{DT}$ precharge time	t_{TP}	20		20		20		ns	
$\overline{RAS}$ to first SC delay (Read Transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay (Read Transfer)	t_{CSD}	25		30		35		ns	
Col. Addr. to first SC delay (Read Transfer)	t_{ASD}	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

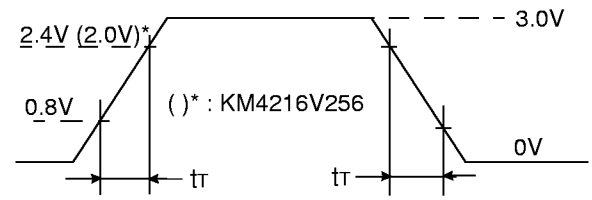
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to first SC delay time (Read Transfer)	t_{TSD}	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time	t_{SRS}	20		20		20		ns	
SC cycle time	t_{SCC}	18		20		25		ns	14
SC pulse width (SC high time)	t_{SC}	5		7		7		ns	
SC precharge (SC low time)	t_{SCP}	5		7		7		ns	
Access time from SC	t_{SCA}		15		17		20	ns	4
Serial output hold time from SC	t_{SOH}	3		5		5		ns	
Access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Split transfer set-up time	t_{STS}	20		25		25		ns	
Split transfer hold time	t_{STH}	20		25		25		ns	
SC-QSF delay time	t_{SQD}		20		25		25	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		20		25		25	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		70		75		80	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		35		35		40	ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	t_{TRP}	40		50		60		ns	
$\overline{DT}$ high pulse width	t_{OEP}	5		5		5		ns	
$\overline{DT}$ high hold time from $\overline{CAS}$ high	t_{OEHC}	5		5		5		ns	
$\overline{OE}$ to high set-up time	t_{OCH}	5		5		5		ns	

NOTES

1. An initial pause of 200uS is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT}/\overline{OE}$ = High) If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), and are assumed to be 2ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   DOUT comparator level : V_{OH}/V_{OL} = 2.0V / 0.8V.
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   DOUT comparator level : V_{OH}/V_{OL} = 2.0V / 0.8V.
5. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. The t_{RCD} (max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$(min), $t_{CPWD} \geq t_{CPWD}$(min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insured that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signal to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below.

Pin or Register	Status
QSF	Hi-Z
Color Register	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SQi	Hi-Z

13. Recommended operating input condition :



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 2ns
14. Assume t_T = 3ns.
15. $t_{ASC} \geq t_{CP}$(min), at Normal sycle, Assum t_T=2.0ns
16. $t_{ASC} < t_{CP}$ (min), Normal cycle or any condition at Block write cycle, Assume t_T=2ns

DEVICE OPERATIONS

The KM4216C/V256 contains 4,194,304 memory locations. Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C/V256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM4216C/V256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address, and are strobed by $\overline{CAS}$.

This is the beginning of any KM4216C/V256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C/V256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WBX}/\overline{WEX}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC}. However, If $\overline{CAS}$ goes low after t_{RCD}(max) or the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}.

The KM4216C/V256 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Extended Data Out

In the conventional RAM Read cycle, Dout buffer is designed to make turn-off by the rising edge of $\overline{CAS}$. the KM4216C/V256 offers an accelerated Fast Page Mode cycle by eliminating output disable from $\overline{CAS}$ high. This is called "Extended Data Output (or Hyper Page) mode". Data outputs are disabled at $\overline{WB}/\overline{WE}$ = Low, $\overline{DT}/\overline{OE}$ = High and t_{OFF} time after $\overline{RAS}$ and $\overline{CAS}$ are high the t_{OFF} time is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs later (see Figure 1). What the output buffer is disabling during $\overline{DT}/\overline{OE}$ = high is to use bank selection in the frame buffer memory using common I/O line, Read, Write and Read-modify-write cycles are available during the extended data out mode.

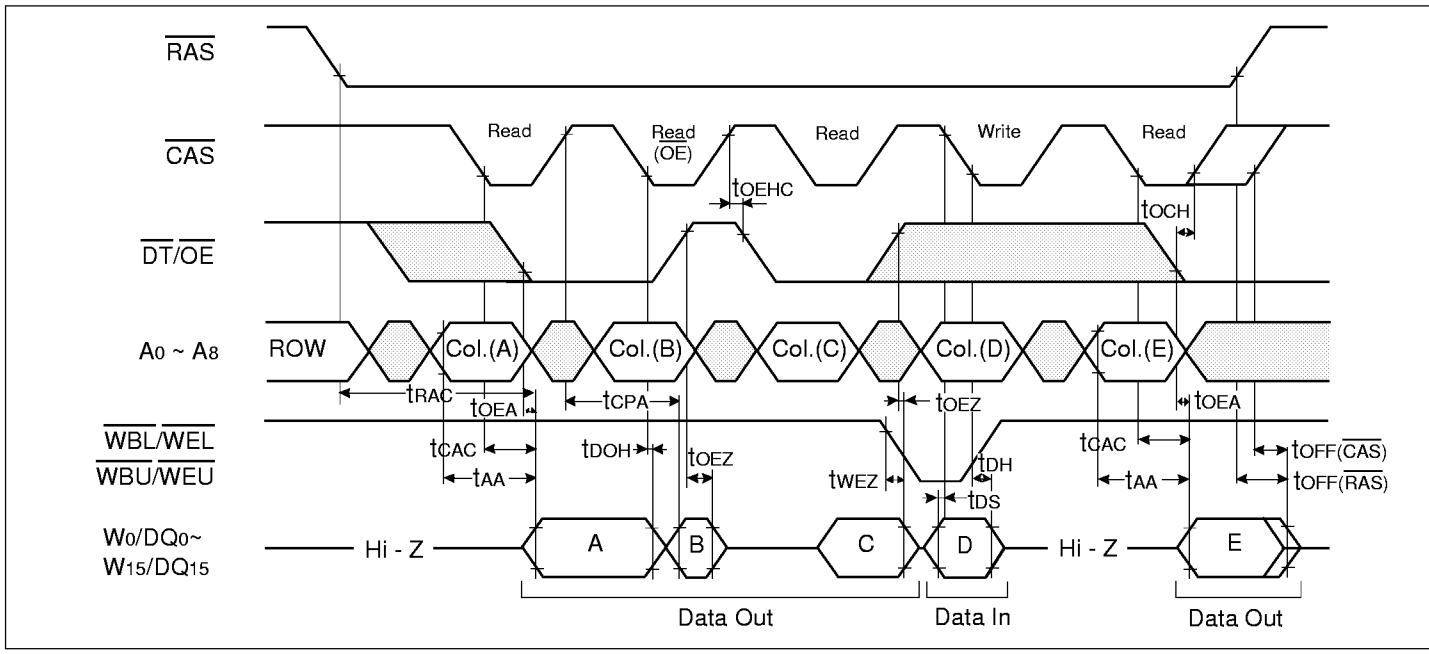


Figure 1. Extended Data Output Example

DEVICE OPERATIONS(Continued)

Byte Write Operation

The KM4216C/V256 has 2 Write control pin, WBL/WEL and WBU/WEU, and offers asynchronous write operation with lower byte (W_0/DQ_0 ~ W_7/DQ_7) and upper byte (W_8/DQ_8 ~ W_{15}/DQ_{15}). This is called Byte Write operation. This operation can be performed in any RAM Write, Block Write, Load Mask Register, and Load Color Register.

New Masked Write Per Bit

The New Masked Write per Bit cycle is achieved by maintaining CAS high and WB/WE and DSF low at the falling edge of RAS. The mask data on the W_0/DQ_0 ~ W_{15}/DQ_{15} pins are latched into the write mask register at the falling edge of RAS. When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM. The mask data is valid for only one cycle. Mask Data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by WBX/WEX low before CAS falling and the Late Write cycle is achieved by WB/WE low after CAS falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~ W_{15}/DQ_{15} must keep the set-up and hold time at the falling edge of CAS or WB/WE .

If WBL/WEL and WBU/WEU is high at the falling edge of RAS, no masking operation is performed (see Figure 2,3).

And if WBL/WEL is high during CAS low, write operation of lower byte does not perform and if WBU/WEU is high, also write operation of upper byte does not execute.

Load Mask Register (LMR)

The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of CAS or WB/WE. The LMR cycle is performed if DSF high, WB/WE high at the RAS falling edge and DSF low at the CAS falling edge. If an LMR is done, the KM4216C/V256 are set to Old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR) cycle. If an LMR is done, all Masked Write are Old masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register (see Figure 4).

The mask data is applied in the same manner as in New Masked Write Per Bit mode. Mask Data Register's content is changed by the another LMR, To reset the device back to the New Masked Write Mode, CBRR(CBR Refresh with option reset) cycle must be performed. After power-up, the KM4216C/V256 initializes in the New Masked Write Mode.

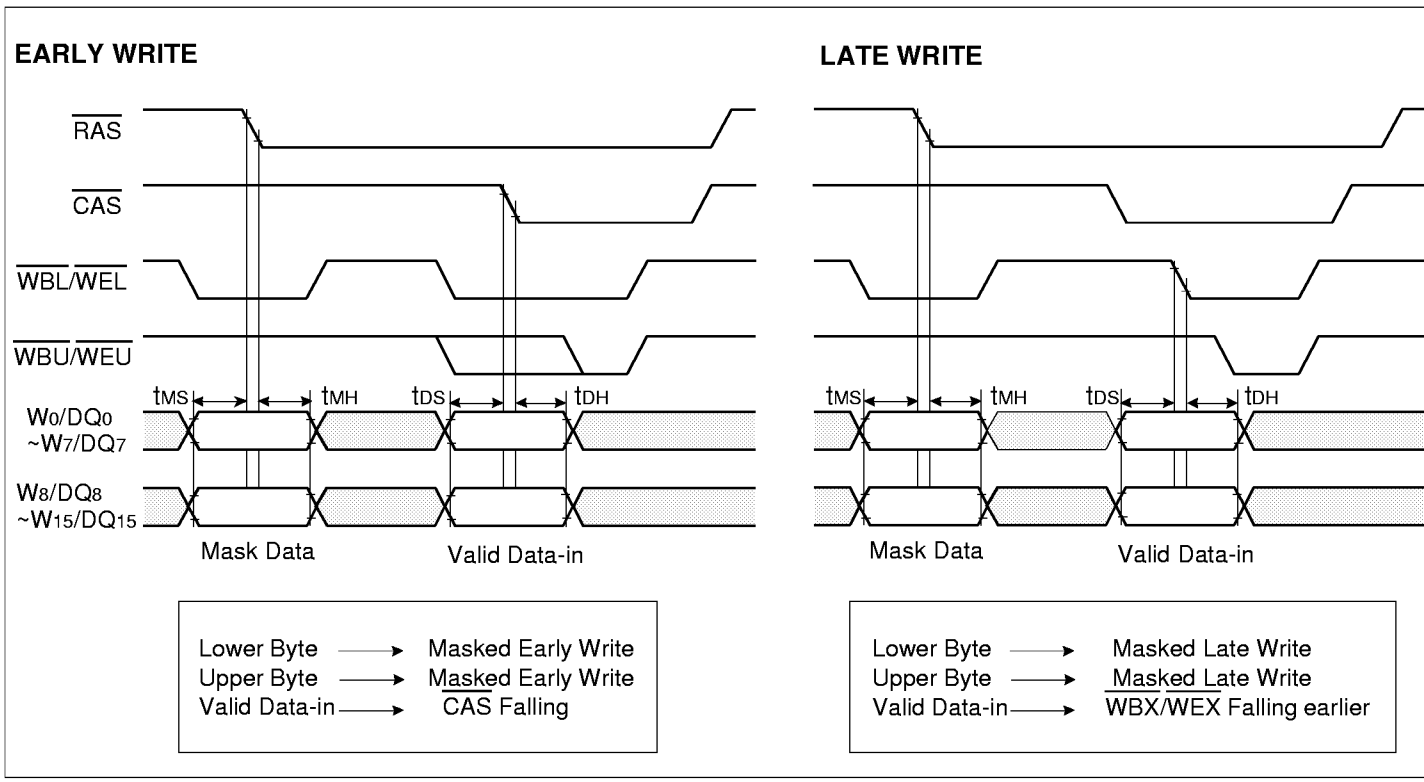


Figure 2. Byte Write and New Masked Write Cycle Example1. (Early Write & Late Write)

DEVICE OPERATIONS(Continued)

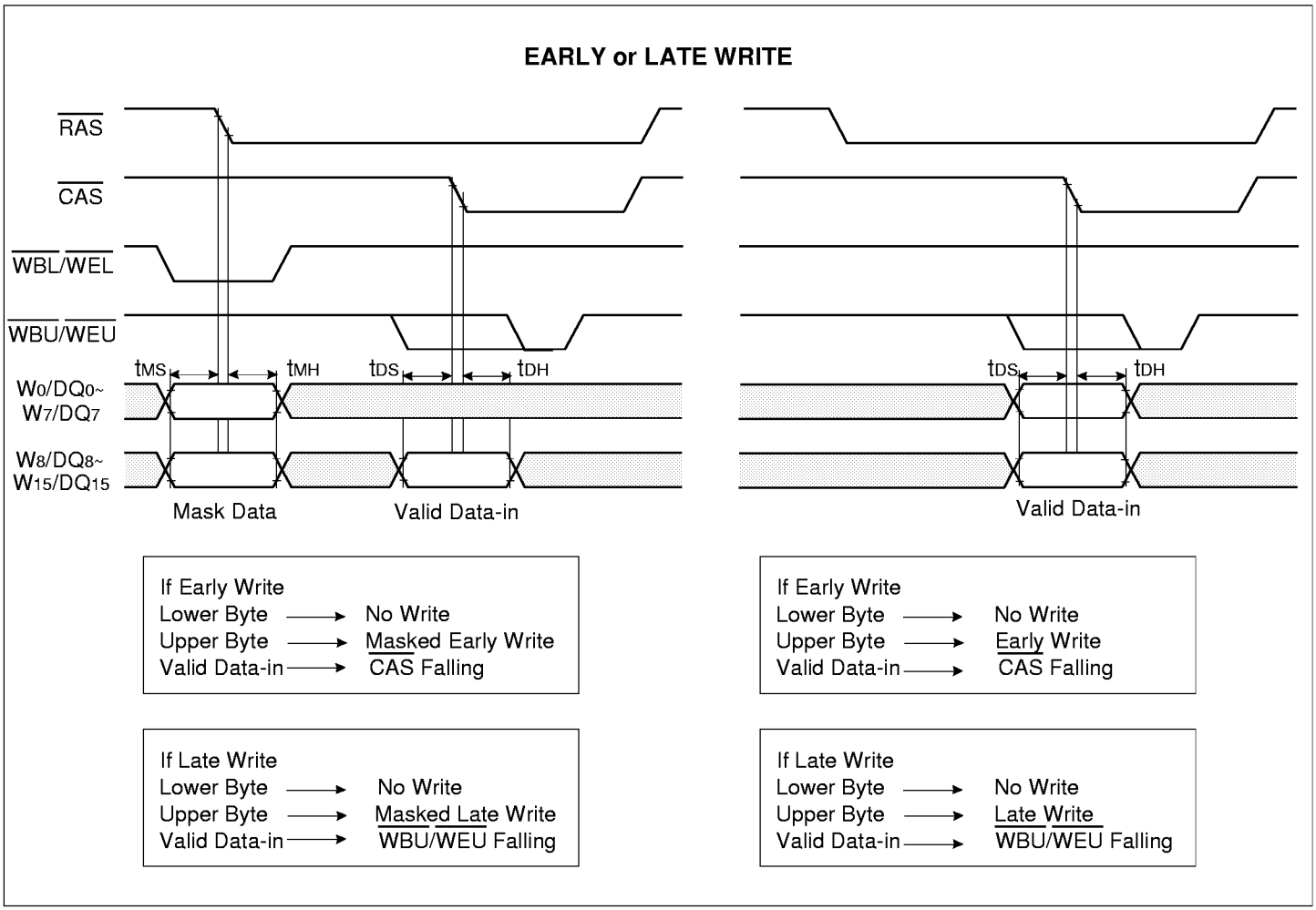


Figure 3. Byte Write and New Masked Write Cycle Example2.

Fast Page Mode

The KM4216C/V256 has Fast Page Mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. In this cycle, read, write, read-modify-write, and block write cycles can be mixed in any order.

In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Load Color Register (LCR)

A Load Color Register cycle is performed by keeping DSF high on the both the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded on the falling edge of $\overline{CAS}$ (early write) or $\overline{WE}$ (late write) via the W_0/DQ_0 ~ W_7/DQ_7 (lower byte), W_8/DQ_8 ~ W_{15}/DQ_{15} (upper byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register cycle.

DEVICE OPERATIONS(Continued)

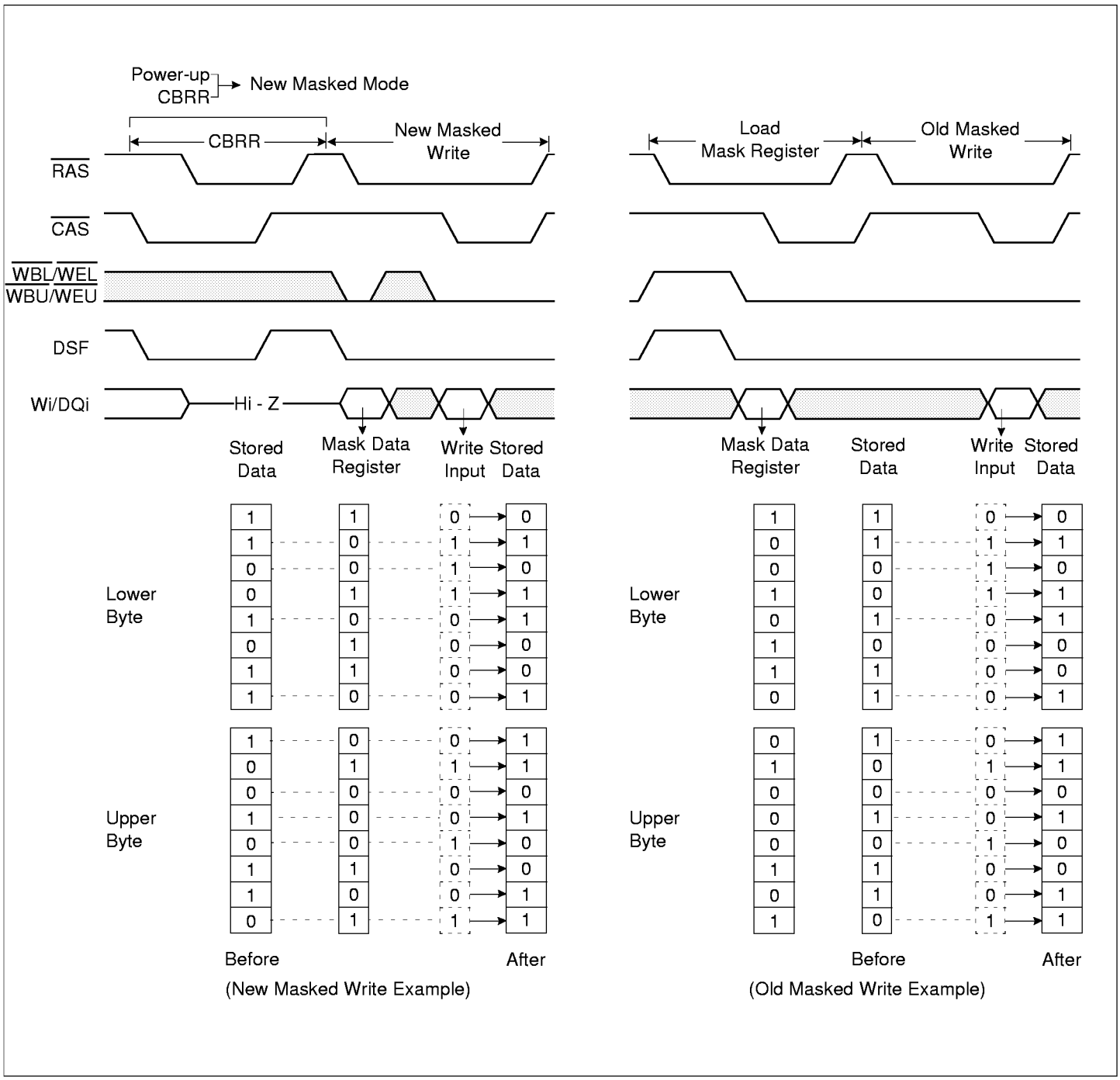


Figure 4. New Masked Write Cycle and Old Masked Write Cycle Example

DEVICE OPERATIONS(Continued)

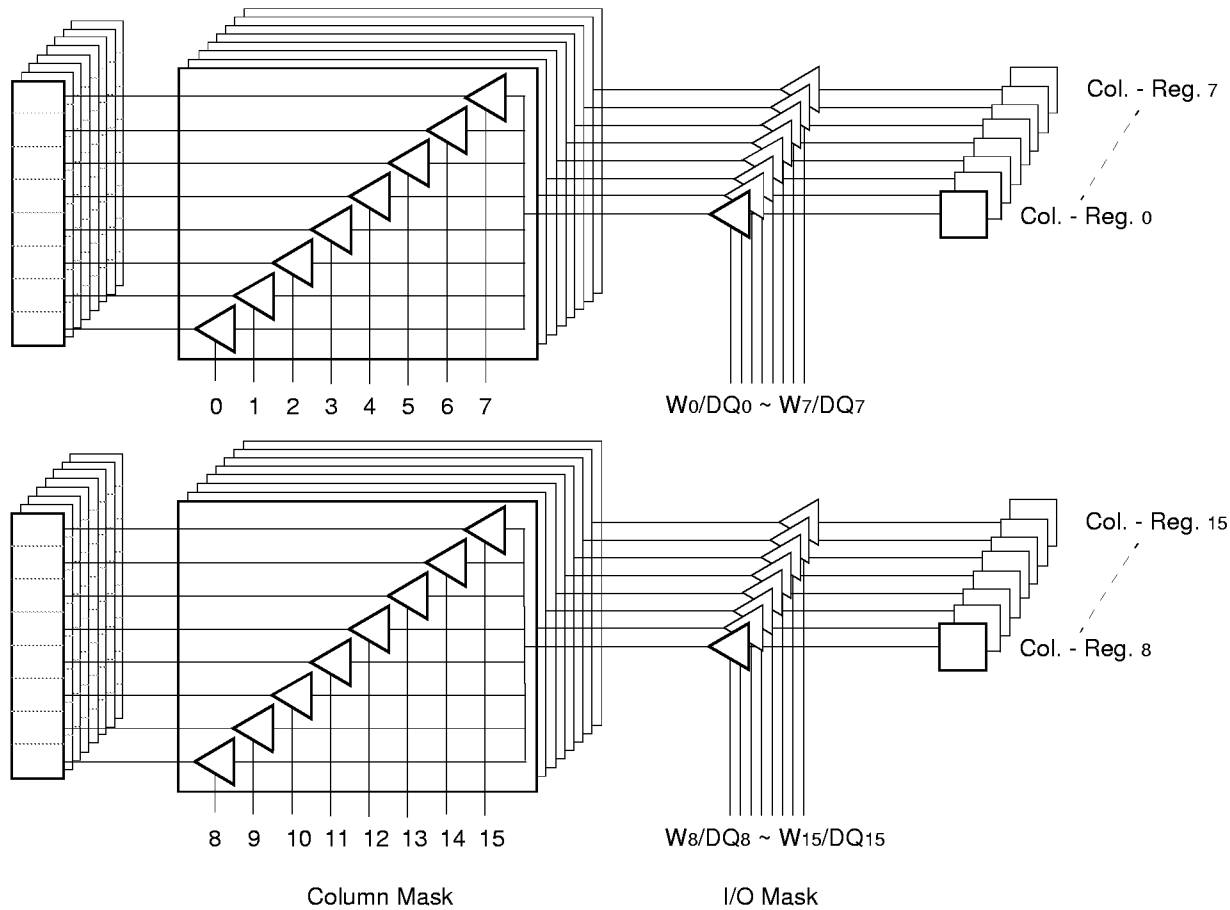
Block Write

In a Block Write cycle 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16 bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle.

When a Block write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each corresponding bit plane(16). This results in a total of 128bits being written in a single Block Write cycle compared to 16-bits in a normal Write cycle.

The Block Write cycle is performed if DSF is low at the falling edge of the $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.



1 Row of 512

	$\overline{RAS}$
W0/DQ0 ~ 7	Lower Block I/O Mask
W8/DQ8 ~ 15	Upper Block I/O Mask

	$\overline{CAS}$
A0 ~ A2	Don't Care
W0/DQ0 ~ 7	Lower Block Column Select
W8/DQ8 ~ 15	Upper Block Column Select

A2 ~ A0	Lower	Upper	Column Mask	
0 0 0	W0/DQ0	W8/DQ8	DQi = 1	Column Enable
0 0 1	W1/DQ1	W9/DQ9		
0 1 0	W2/DQ2	W10/DQ10		
0 1 1	W3/DQ3	W11/DQ11		
1 0 0	W4/DQ4	W12/DQ12	DQi = 0	Column Disable
1 0 1	W5/DQ5	W13/DQ13		
1 1 0	W6/DQ6	W14/DQ14		
1 1 1	W7/DQ7	W15/DQ15		

Figure 5. Block Write Scheme

DEVICE OPERATIONS(Continued)

Address Lines : The row address is latched on the falling edge of $\overline{RAS}$. Since 8 columns are being written at a time, the minimum increment required for the column address is eight.

Therefore, when the column address is latched at the falling edge of $\overline{CAS}$, the 3 LSBs, A_0 ~ A_2 are ignored and only bits(A_3~A_8) are used to define the location of the first bit out of the eight to be written.

Data Lines : On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0 ~ W_{15}/DQ_{15} pins provide column mask data. That is, for each of the eight bits in all 16-bit planes, writing of Color Register contents can be inhibited. For example, If W_0/DQ_0 = 1 and W_1/DQ_1 = 0, then the Color Register contents will be written into the first bit out of the 8, but the second remains unchanged.

Fig. 5 shows the correspondence of each data line to the column mask bits.

A masked Block Write cycle identical to a New/Old Masked Write-per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.

To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high at the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the W_0/DQ_0 ~ W_{15}/DQ_{15} pins at the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. And $\overline{WB}/\overline{WE}$ must be low, DSF must be high on the falling edge of $\overline{CAS}$. In Old Mask Mode, I/O mask data will be provided by the Mask Data Register.

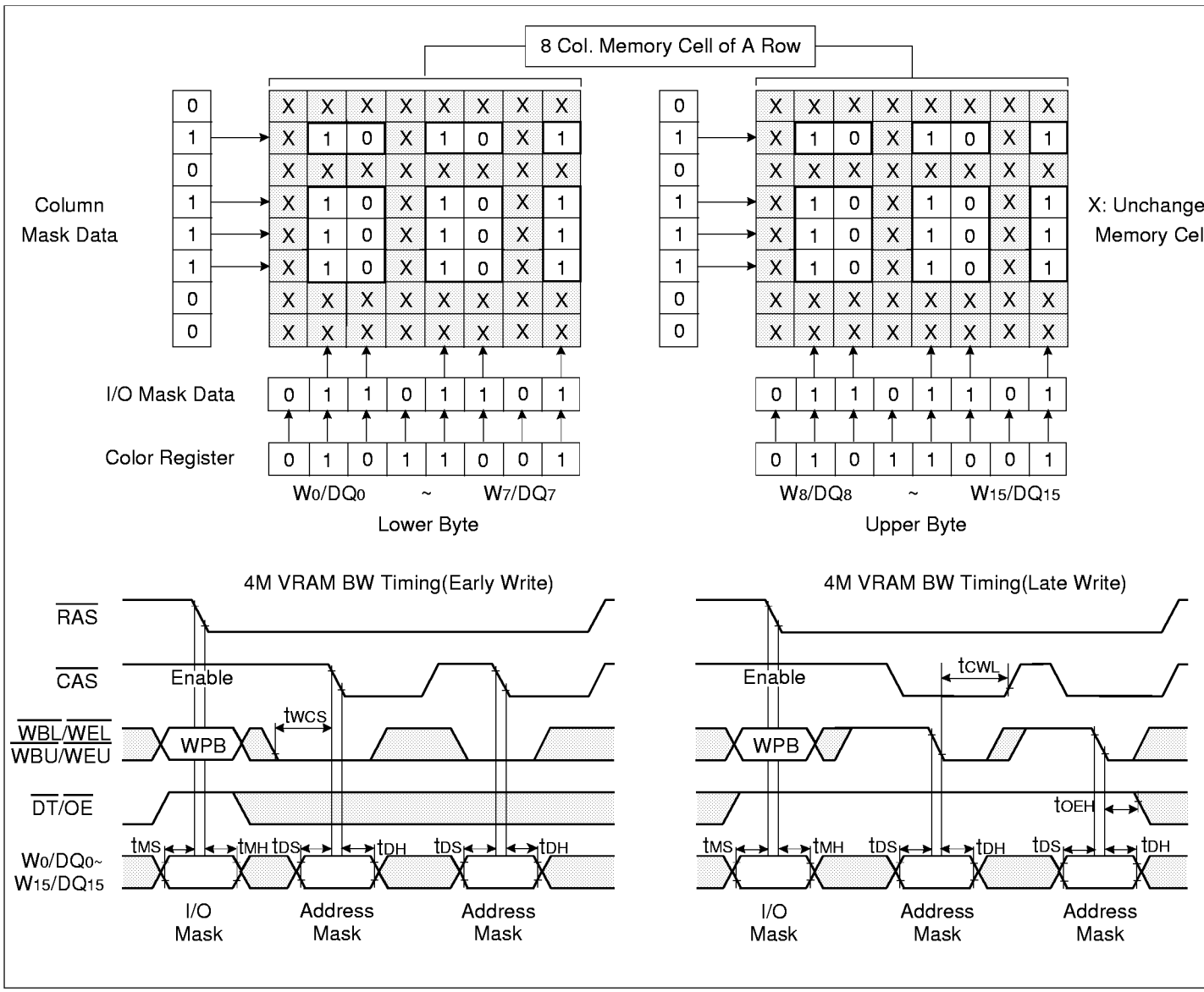


Figure 6. Block Write Example and Timing

DEVICE OPERATIONS(Continued)

Data Output

The KM4216C/V256 has three state output buffer controlled by $\overline{DT}/\overline{OE}$ and $\overline{CAS}/\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is high impedance (High-z). In any cycle, the output goes low impedance state after t_{CLZ} of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output during the time after t_{CLZ} and the valid data appears at the output. The timing parameter t_{RAC}, t_{CAC} and t_{AA} specify when the valid data will be present at the output.

Refresh

The data in the KM4216C/V256 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh

This is the most common method for performing refresh. it is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address, (A_0 ~ A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh

The KM4216C/V256 has $\overline{CAS}$-before-$\overline{RAS}$ on chip refresh capability that eliminates the need for external refresh address. If $\overline{CAS}$ is held low for the specified set up time(t_{CSR}) before $\overline{RAS}$ goes low, the on chip refresh circuitry is enabled.

An internal refresh operation occurs automatically. The refresh address is supplied by the on chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

The KM4216C/V256 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operations CBRR, CBRN, CBRS

CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default values.

CBRN (CBR refresh without reset) is set if DSF high when $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$ is high at the falling edge of $\overline{RAS}$ and simply does only refresh operation.

CBRS (CBR refresh with stop register set) cycle is set if DSF high when $\overline{WBL}/\overline{WEL}$ or $\overline{WBU}/\overline{WEU}$ is low and this mode is to set stop register's value.

Hidden Refresh :

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C/V256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle.

The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods :

It is also possible to refresh the KM4216C/V256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS(Continued)

Table.1 Truth Table for Transfer Operation

* : Don't care

RAS Falling Edge					Function	Transfer Direction	Transfer Data Bit
CAS	DT/OE	WB/WE	DSF	SE			
H	L	H	L	*	Read Transfer	RAM → SAM	512 x 16
H	L	H	H	*	Split Read Transfer	RAM → SAM	256 x 16

Transfer Operation

Transfer operation is initiated when DT/OE is low at the falling edge of RAS. The state of DSF when RAS goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if DT/OE is low, WB/WE is high and DSF low at the falling edge of RAS. The row address bits in the read transfer cycle indicate which sixteen 512bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operation, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A_8 is high, QSF will be high and means the start address is in upper half) Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC. DT/OE is taken high after CAS goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of DT/OE must be synchronized with the rising edge of SC(t_{TSL}/t_{TSD}) to retain the continuity of serial read data output. If the transfer does not have to be synchronized with SC, DT/OE may go high before CAS goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is performed by a Real Time Read Transfer cycle. However, this cycle has many critical timing restriction (between SC, DT/OE, RAS and CAS) because the transfer has to occur at the first rising edge of DT/OE

The split read transfer(SRT) cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM Register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between DT/OE and RAS, CAS, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and WB/WE high and DT/OE low at the falling edge of RAS.

Address : The row address is latched on the falling edge of RAS. The column address defined by (A_0 ~ A_7) defines the starting address of the SAM port from which data will begin shifting out. Column address pin A_8 is a "Don't Care."

The QSF pin indicates which SAM half is shifting out serial data (0 = Lower, 1 = Upper). A Split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g. 255th or 511th bit).

Examples of SRT application are shown in Fig. 7 through Fig.10. The normal usage of Split Read Transfer cycle is described in Fig.7. When Read Transfer is executed, data from X1 row address is fully transferred to the SAM port and serial Read is started from 0 (Tap address).

If SRT is performed while data is being serially read from lower half SAM, data from X2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM (255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y0" Tap address instead of "Y0" is loaded.

The another example of SRT cycle is described in Fig.8.

When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the starting address given by RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 9 and 10 are the example of abnormal SRT cycle.

DEVICE OPERATIONS(Continued)

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig. 9, the data transferred by SRT2 overwrites the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 10 indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511.

In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during $t_{STH} + t_{STS}$ (see Fig. 11)
A Split Read Transfer does not change the direction of the SAM I/O port.

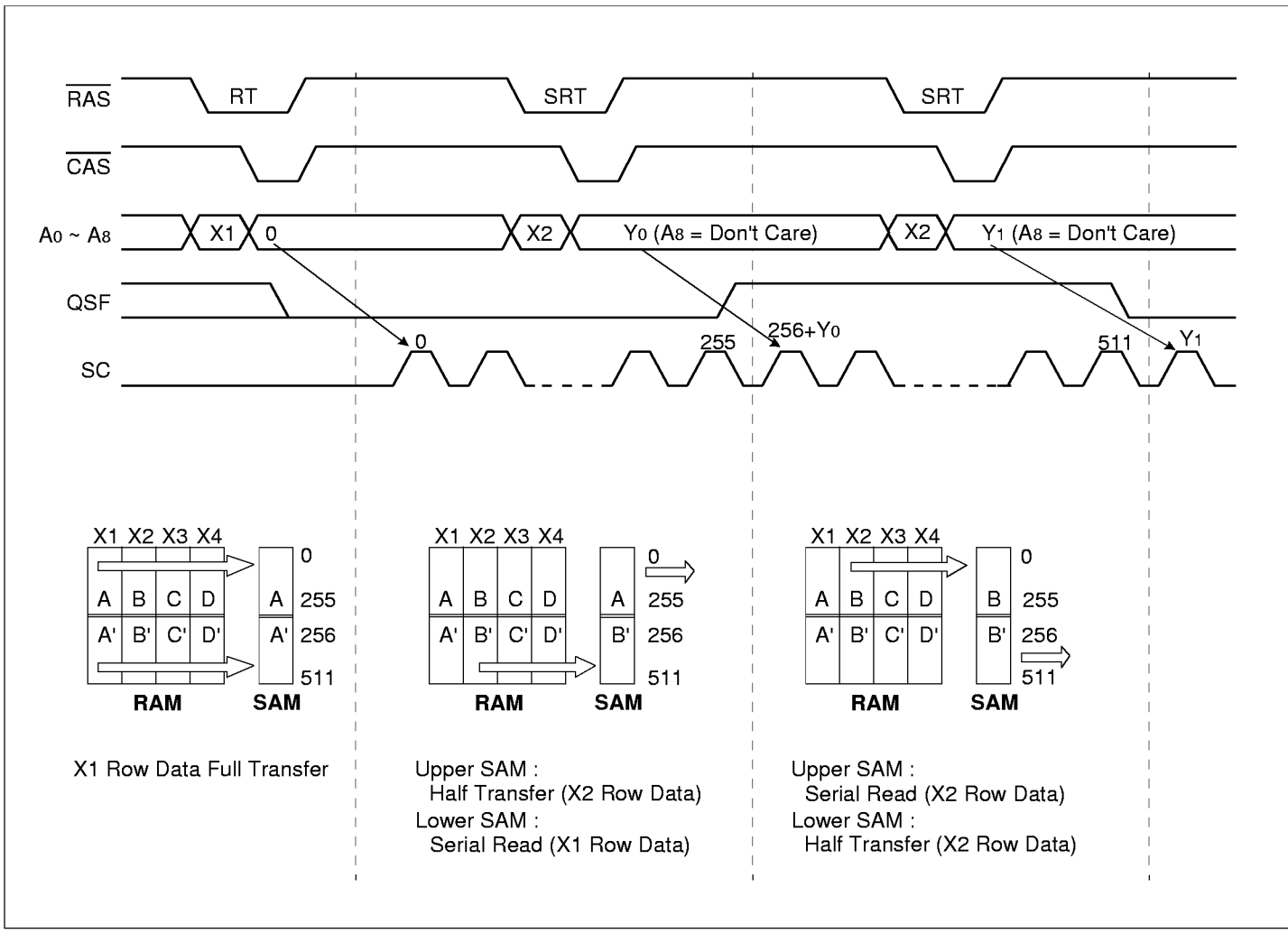


Figure 7. Split Read Transfer Normal Usage

DEVICE OPERATIONS(Continued)

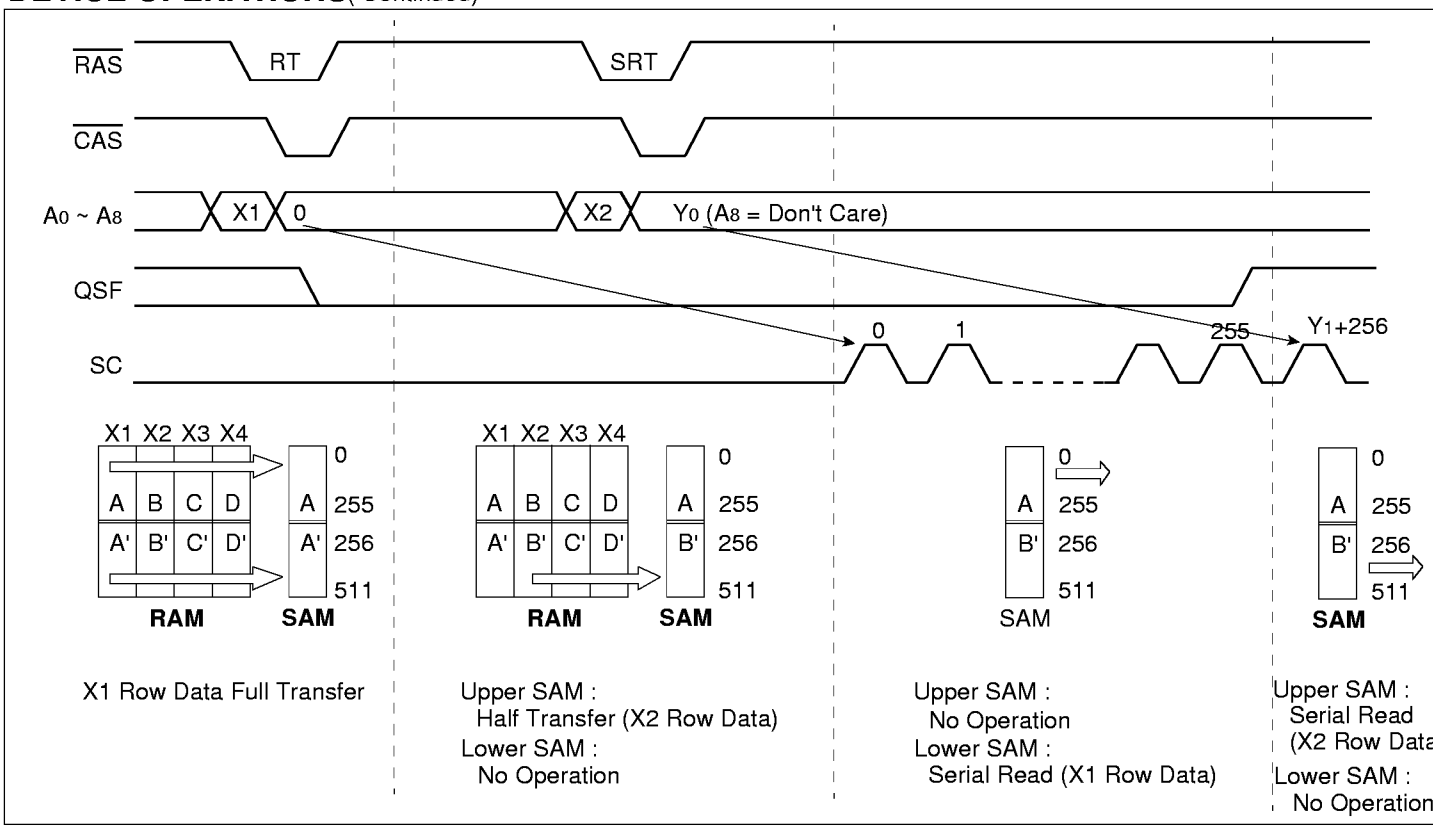


Figure 8. Split Read Transfer Normal Usage

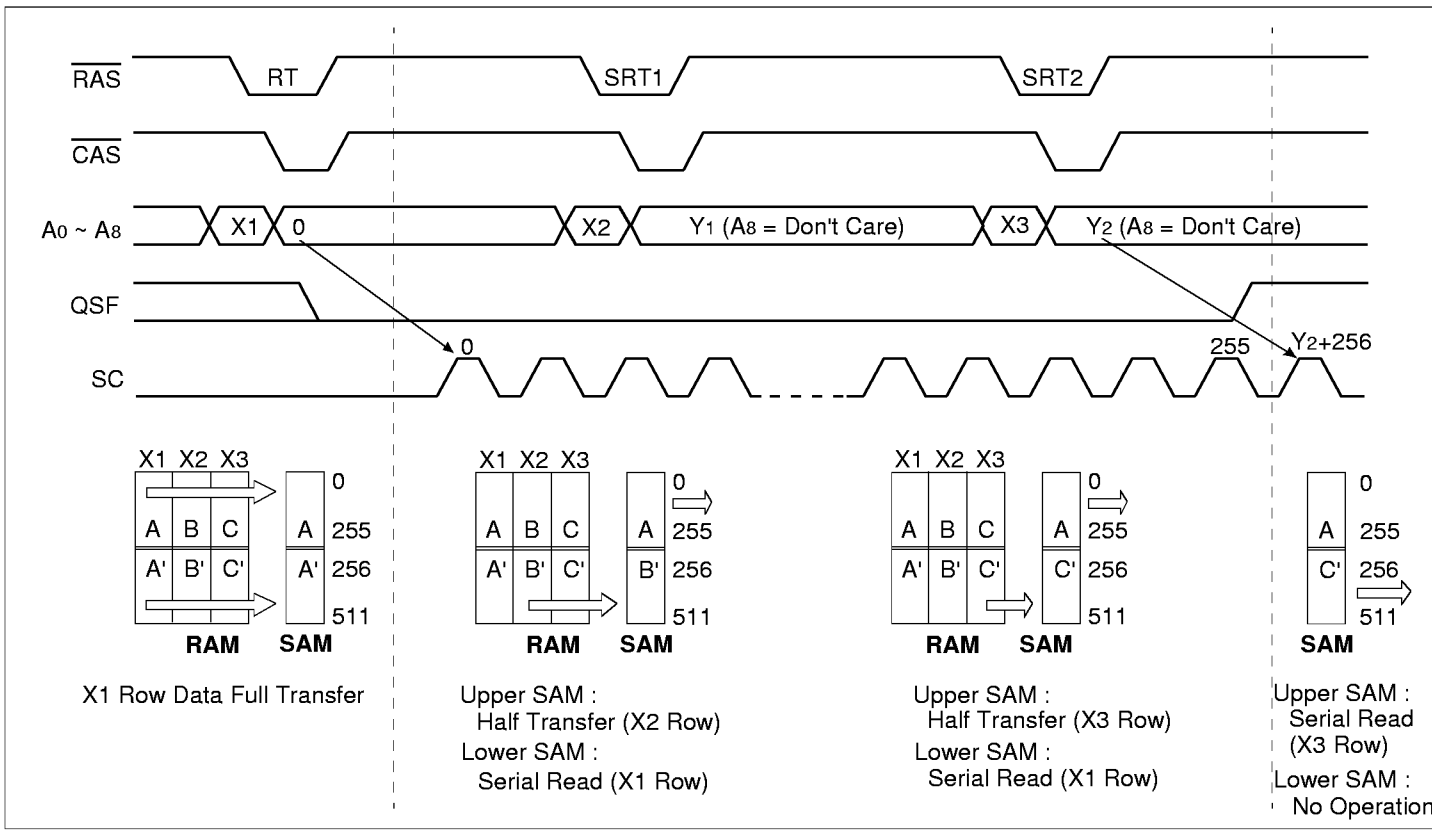


Figure 9. Split Read Transfer Abnormal Usage (Case 1)

DEVICE OPERATIONS(Continued)

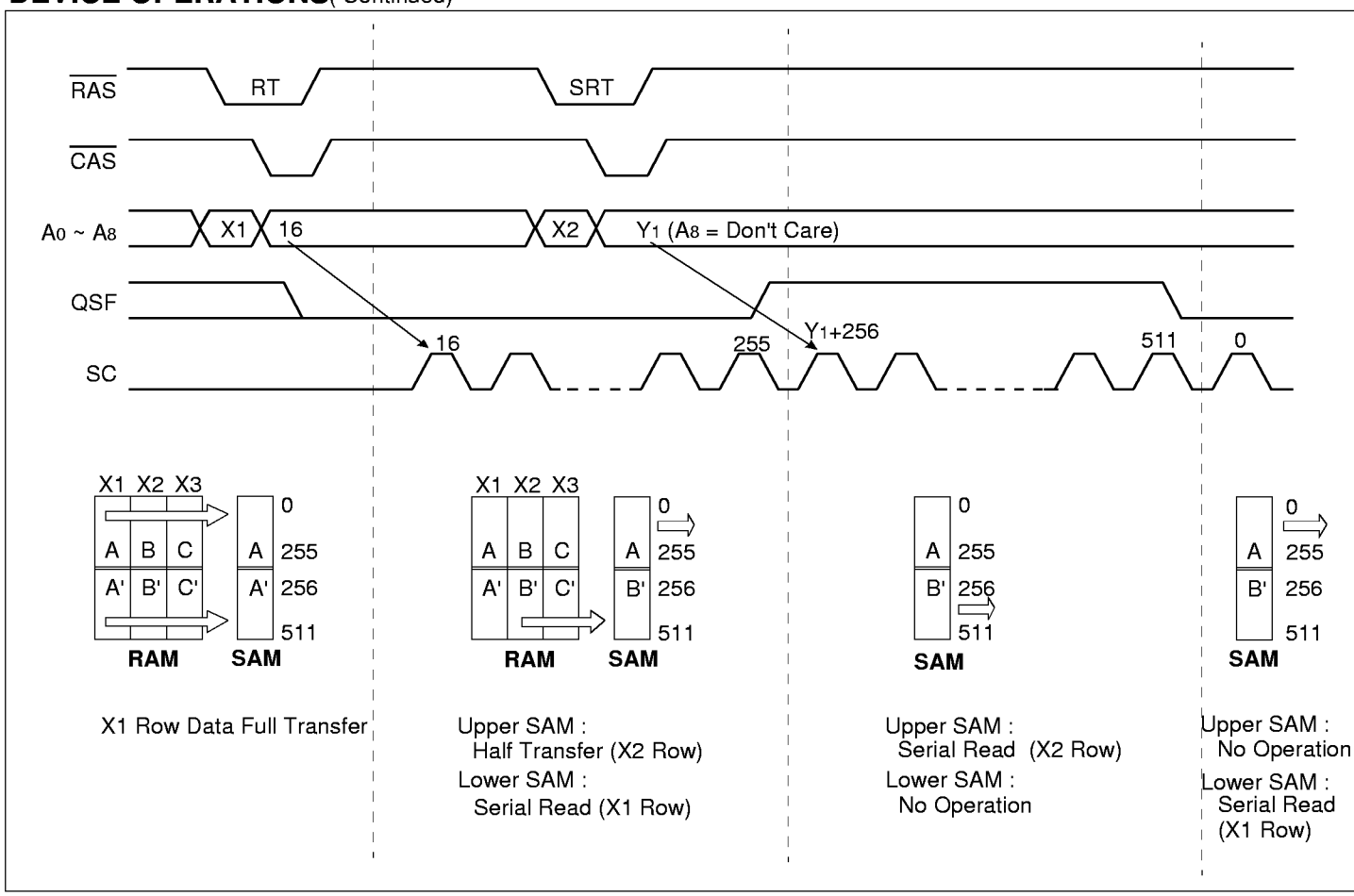


Figure 10. Split Read Transfer Abnormal Usage (Case 2)

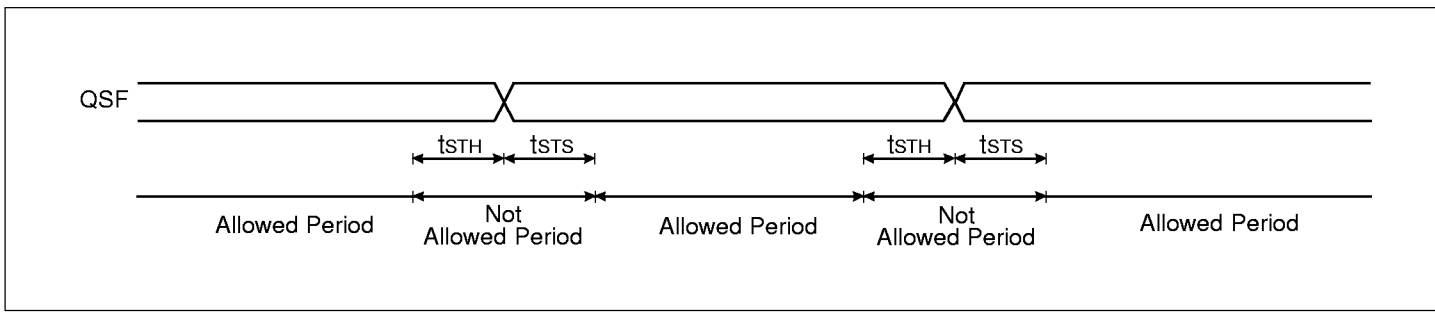


Figure 11. Split Transfer Cycle Limitation Period

DEVICE OPERATIONS(Continued)

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half, After the last address of each half SAM (255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded Tap address). This last address is called stop point.

The KM4216C/V256 offers user-programmable Stop Points. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Point is set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WBL}/\overline{WEL}$ or $\overline{WBU}/\overline{WEU}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.

The Stop Point will not become valid until a SRT cycle is done. The Stop Point does not effect to SAM in normal RT, RRT cycle. In Figure 12. programmable split SAM operation is shown. if a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address (70) of the next half. Otherwise, the access will continue in the same half until a SRT occurs at the SAM half boundary (255, 511). Note that the Stop Point may be changed at any time by performing another CBRS, and New Stop Point will not be valid until a SRT is performed.

To reset Stop Point, CBRR cycle must be performed. CBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$

The CBRR will take effect immediately ; it does not require a SRT to become active valid.

Table. 2 Stop Point Setting Address

Stop Register = Store The Address of Serial Access
Use on the Split Transfer Cycle
Stop Pointer Set ⟶ CBRS Cycle

Number Stop Points /Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	A_3~A_0
1	(1x256)x2	X	1	1	1	1	X
2	(2x128)x2	X	0	1	1	1	X
4	(4x64)x2	X	0	0	1	1	X
8	(8x32)x2	X	0	0	0	1	X
16	(16x16)x2	X	0	0	0	0	X

*Other Case = Inhibit, X =don't care.

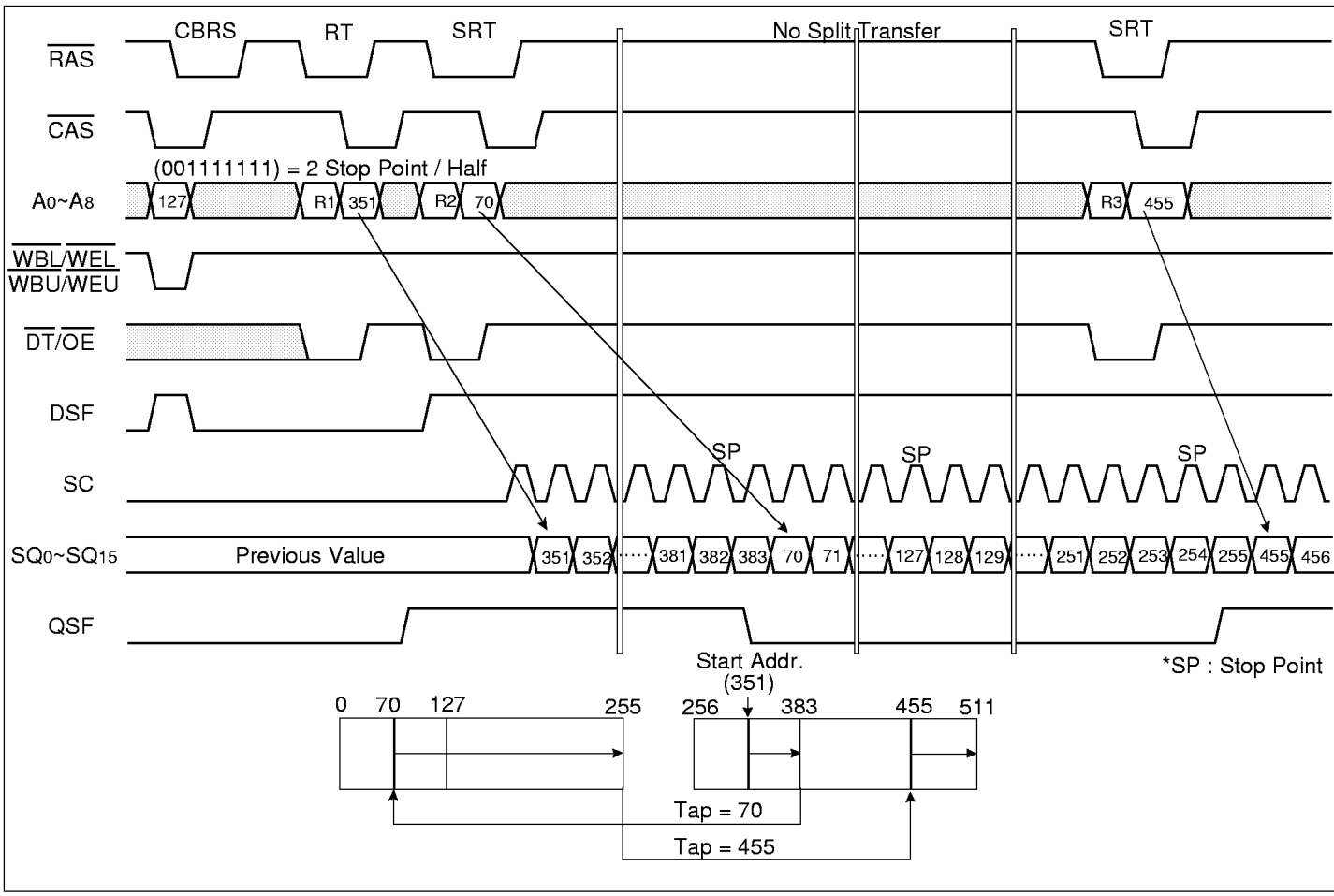
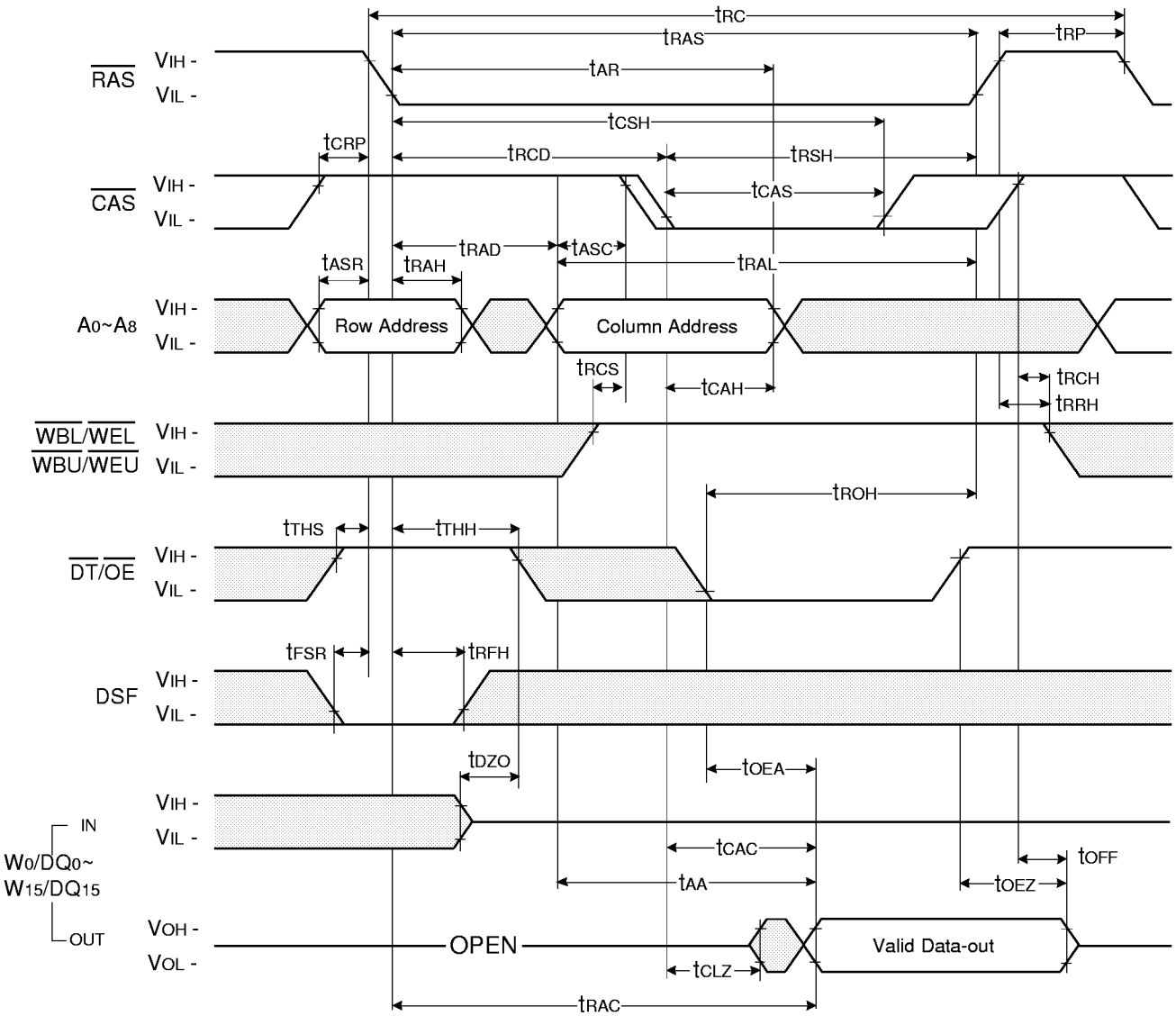


Figure 12. Programmable Split SAM Operation

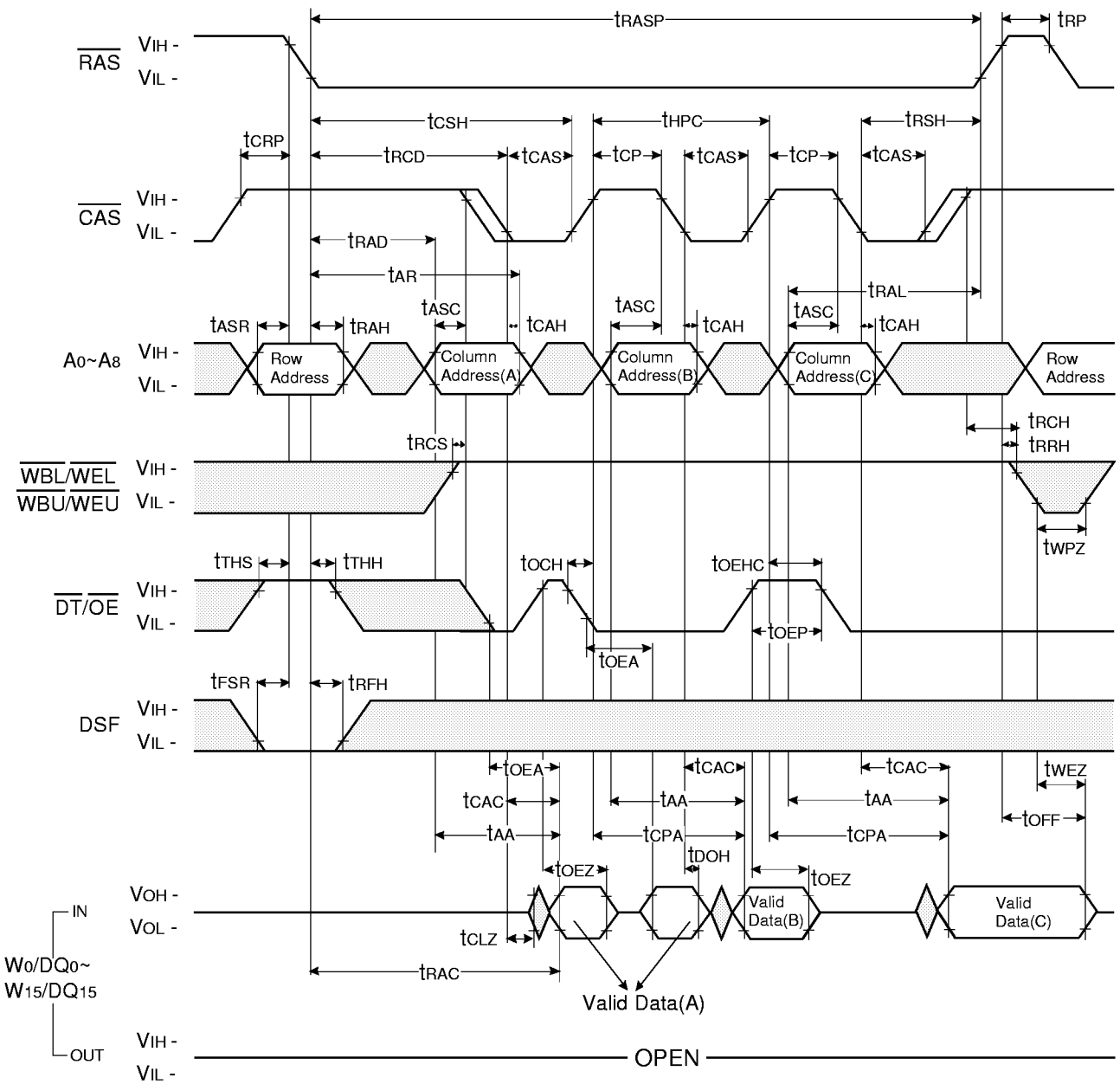
TIMING DIAGRAMS

READ CYCLE



Don't care

FAST PAGE MODE READ CYCLE (Extended Data Out)



TURTH TABLE FOR WRITE CYCLE (1)

FUNCTION	RAS ↘			CAS ↘	CAS ↘ or WBX/WEX ↘
	*1 WBX/WEX	*2 DSF	*3 Wi/DQi(4) (New Mask)	*4 DSF	*5 Wi/DQi
Normal Write	1	0	X	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)(4)	1	0	X	1	Column Mask
Masked Block Write(4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register(2)	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

Note :

1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram, on the following page.
2) Old Mask data load
3) Function table for Old Mask and New Mask

IF		*1		*3	Note
		WBL/WEL	WBU/WEU	Wi/DQi	
LMR Cycle Executed	YES	0 0 1	0 1 0	X X X	Write using mask register data (Old Mask Data)
		1	1	X	Non Masked Write
	NO	0 0 1	0 1 0	Write Mask	Write using New Mask Data Wi/DQi=0 Write Disable Wi/DQi=1 Write Enable
		1	1	X	Non Masked Write

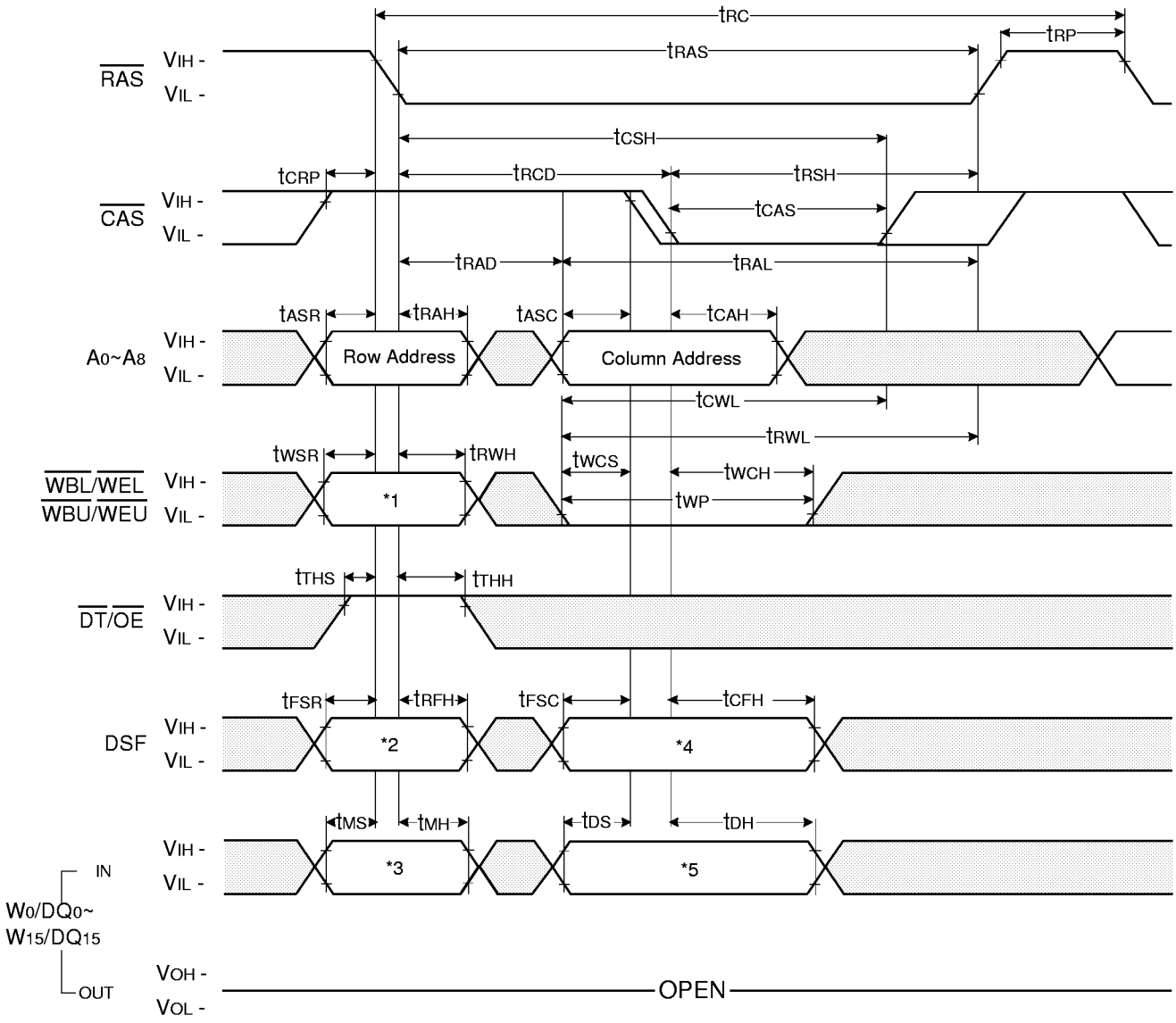
X : Don't care

4) Function Table for Block Write Column Mask

Column Address		
A_2	A_1	A_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

*5		IF	
Lower Byte	Upper Byte	Wi/DQi=0	Wi/DQi=1
W_0/DQ_0 W_1/DQ_1 W_2/DQ_2 W_3/DQ_3 W_4/DQ_4 W_5/DQ_5 W_6/DQ_6 W_7/DQ_7	W_8/DQ_8 W_9/DQ_9 W_{10}/DQ_{10} W_{11}/DQ_{11} W_{12}/DQ_{12} W_{13}/DQ_{13} W_{14}/DQ_{14} W_{15}/DQ_{15}	No Change the Internal Data	Color Register Data is Written to the Corresponding Column Address Location

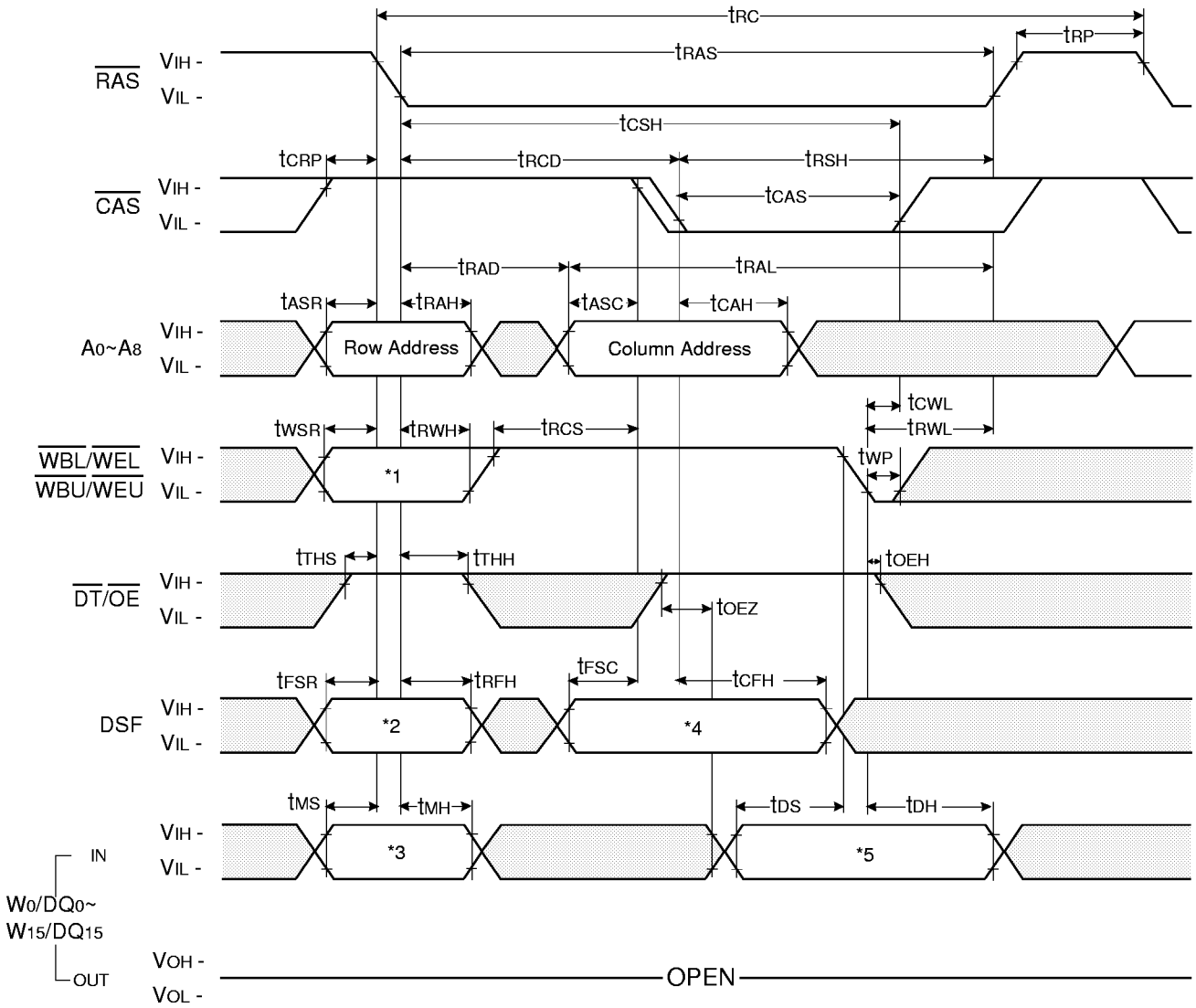
EARLY WRITE CYCLE



Note : In Block Write cycle, only Column Address A_3 ~ A_8 are used.

Don't care

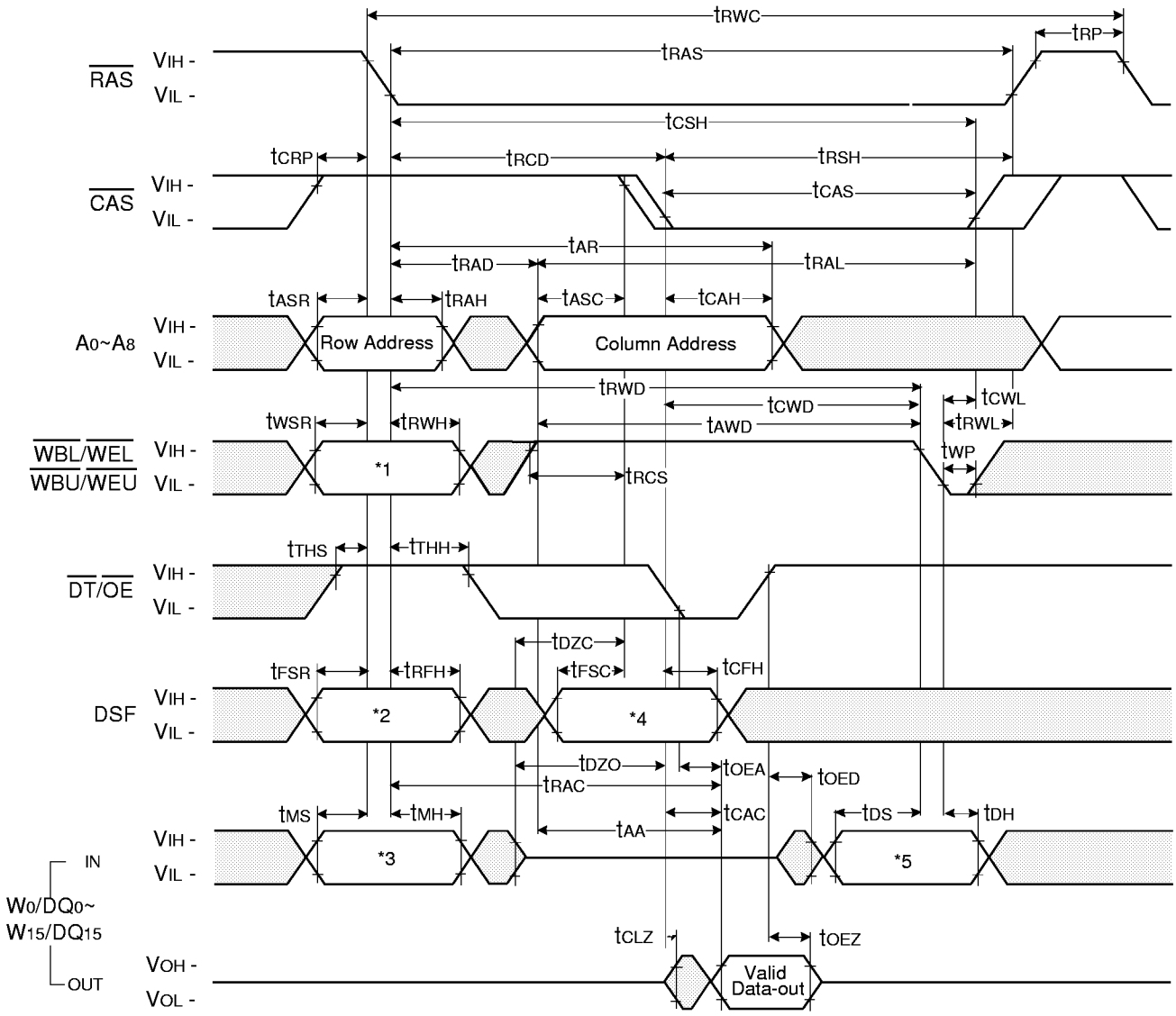
LATE WRITE CYCLE



Note : In Block Write cycle, only Column Address A_3 ~ A_8 are used.

Don't care

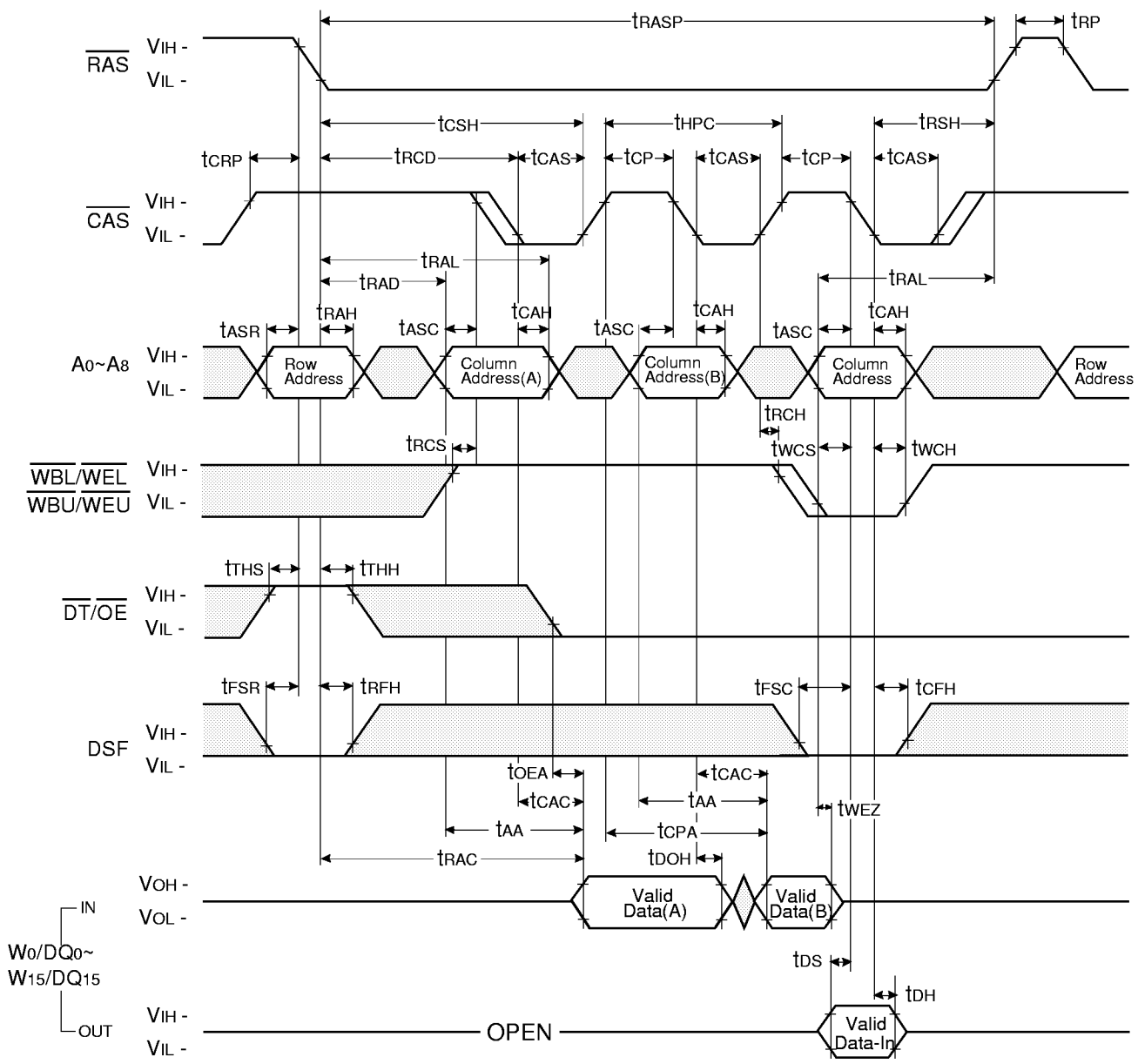
READ-WRITE/READ-MODIFY-WRITE CYCLE



Note : In Block Write cycle, only Column Address A_3 ~ A_8 are used.

Don't care

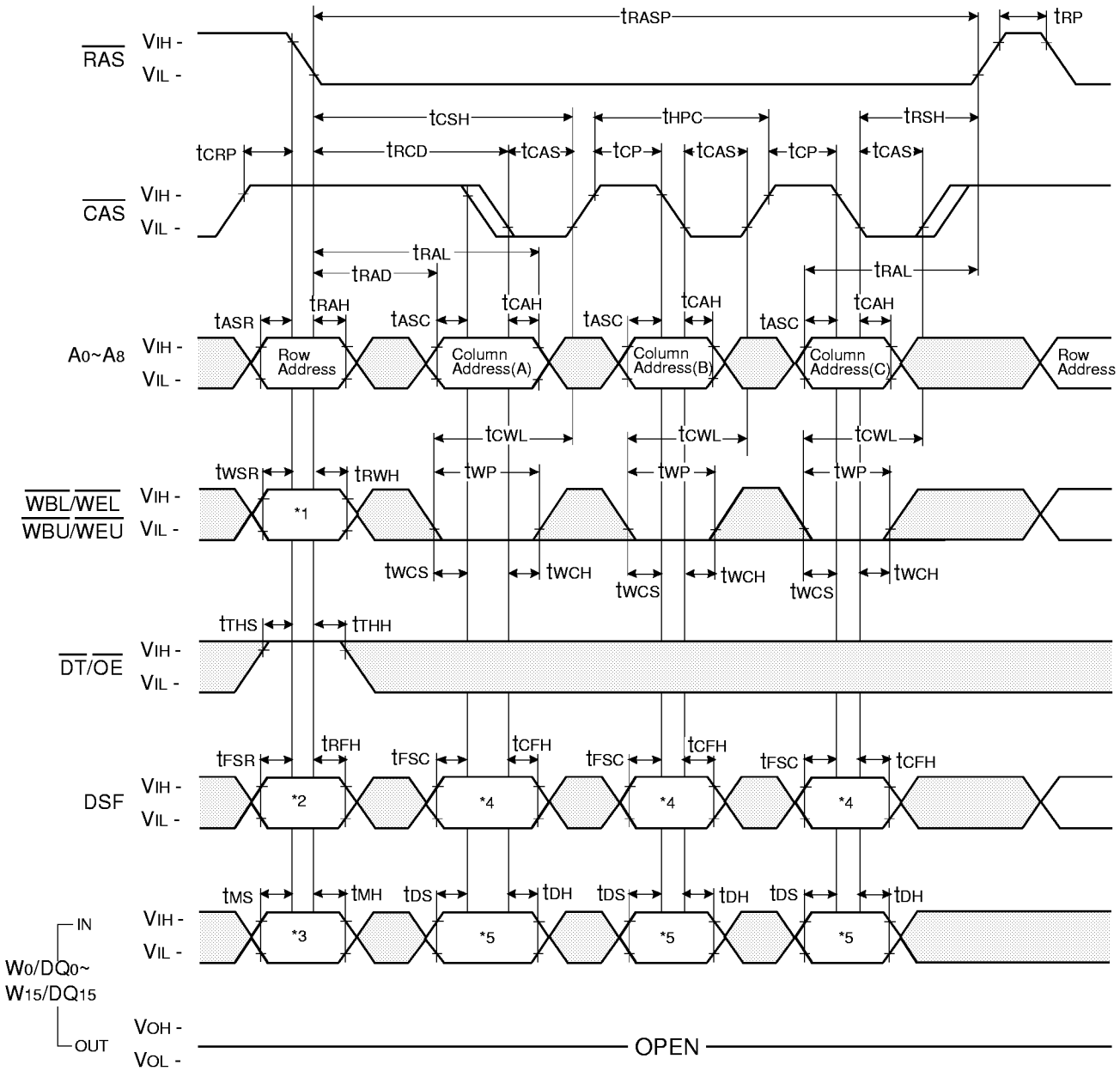
FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)



Note : In Block Write cycle, only Column Address A_3 ~ A_8 are used.

Don't care

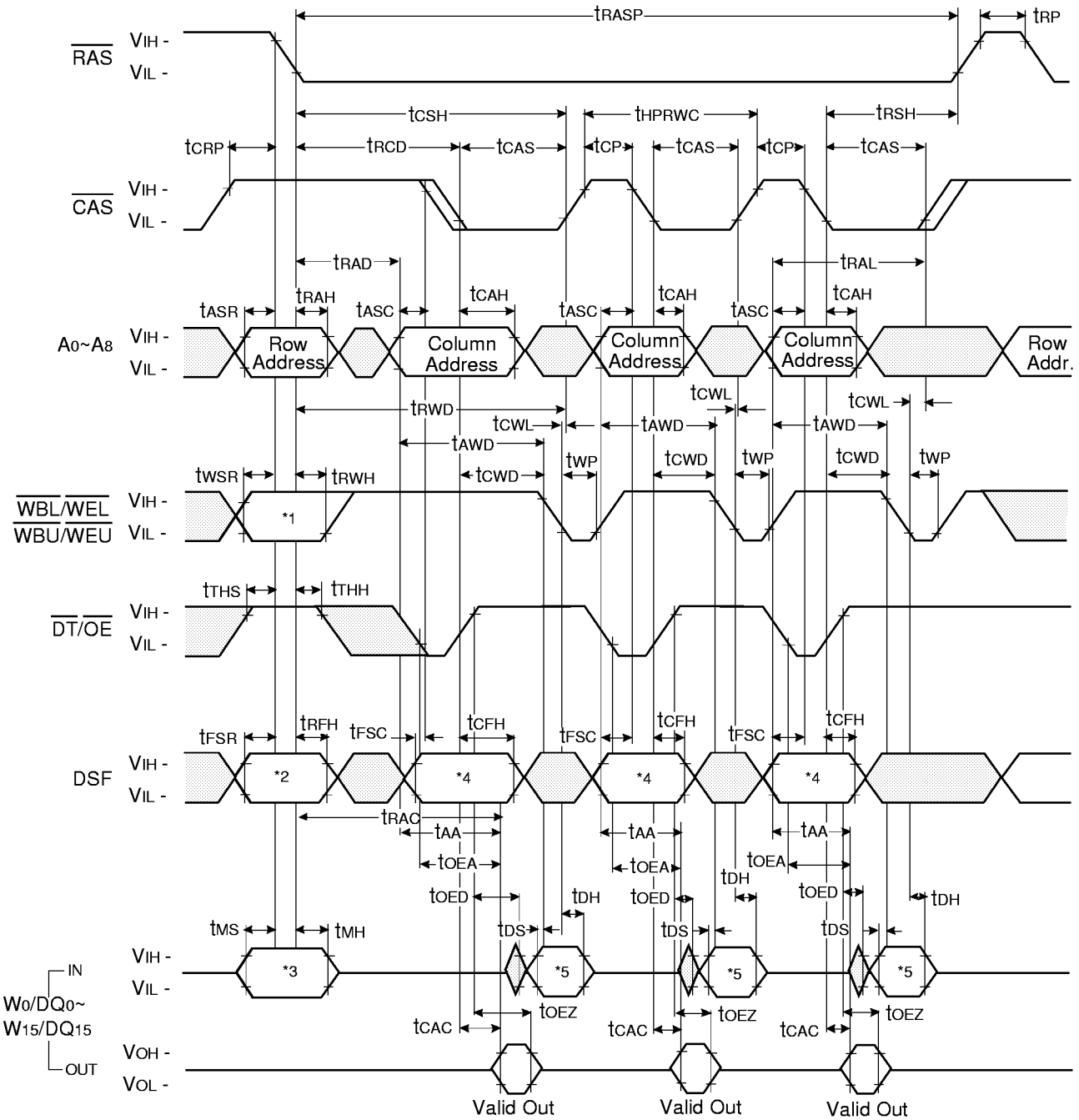
FAST PAGE MODE EARLY WRITE CYCLE



Note : In Block Write cycle, only Column Address A_3 ~ A_8 are used.

Don't care

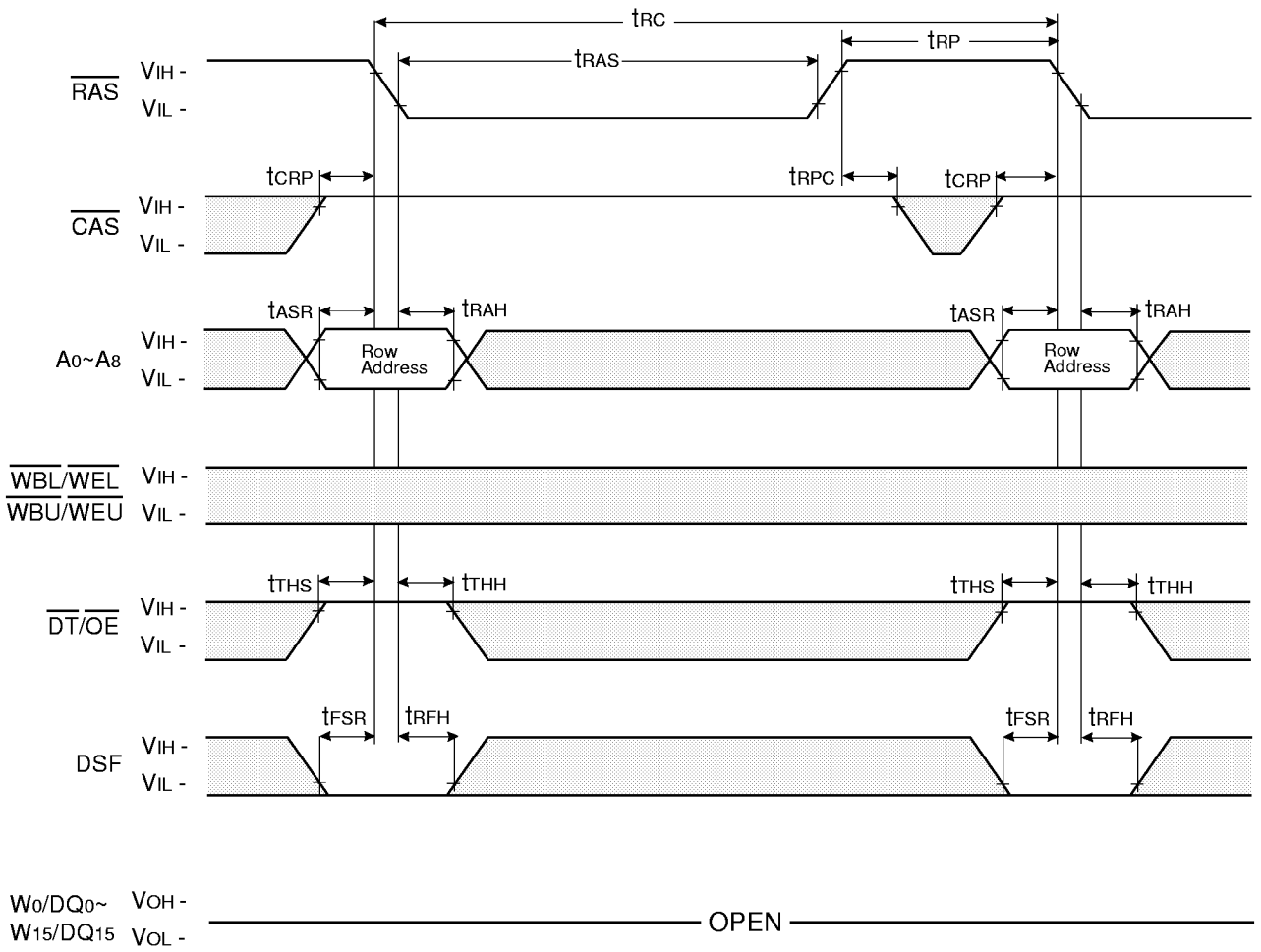
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



Note : In Block Write cycle, only Column Address A_3 ~ A_8 are used.

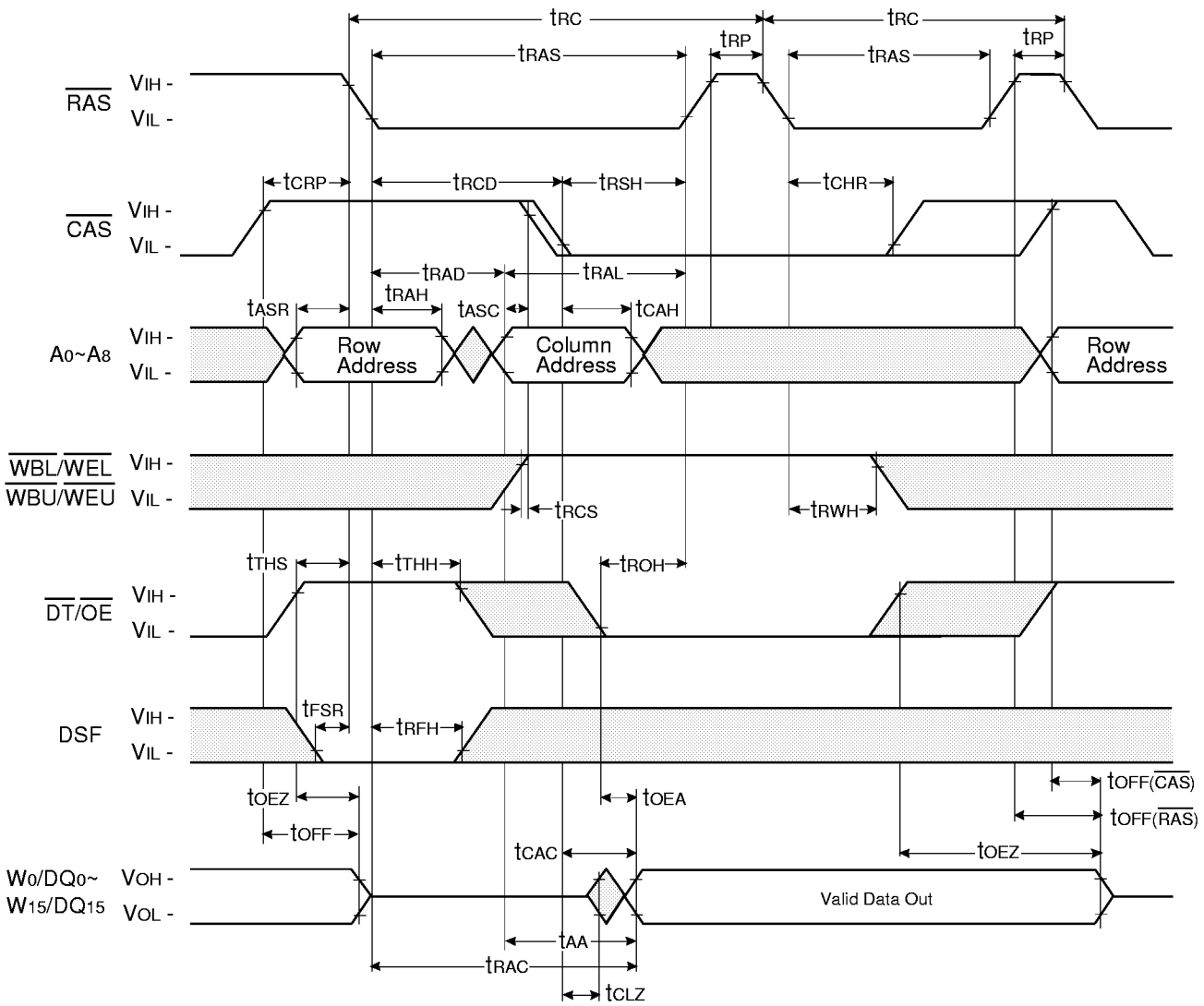
Don't care

$\overline{RAS}$-ONLY REFRESH CYCLE



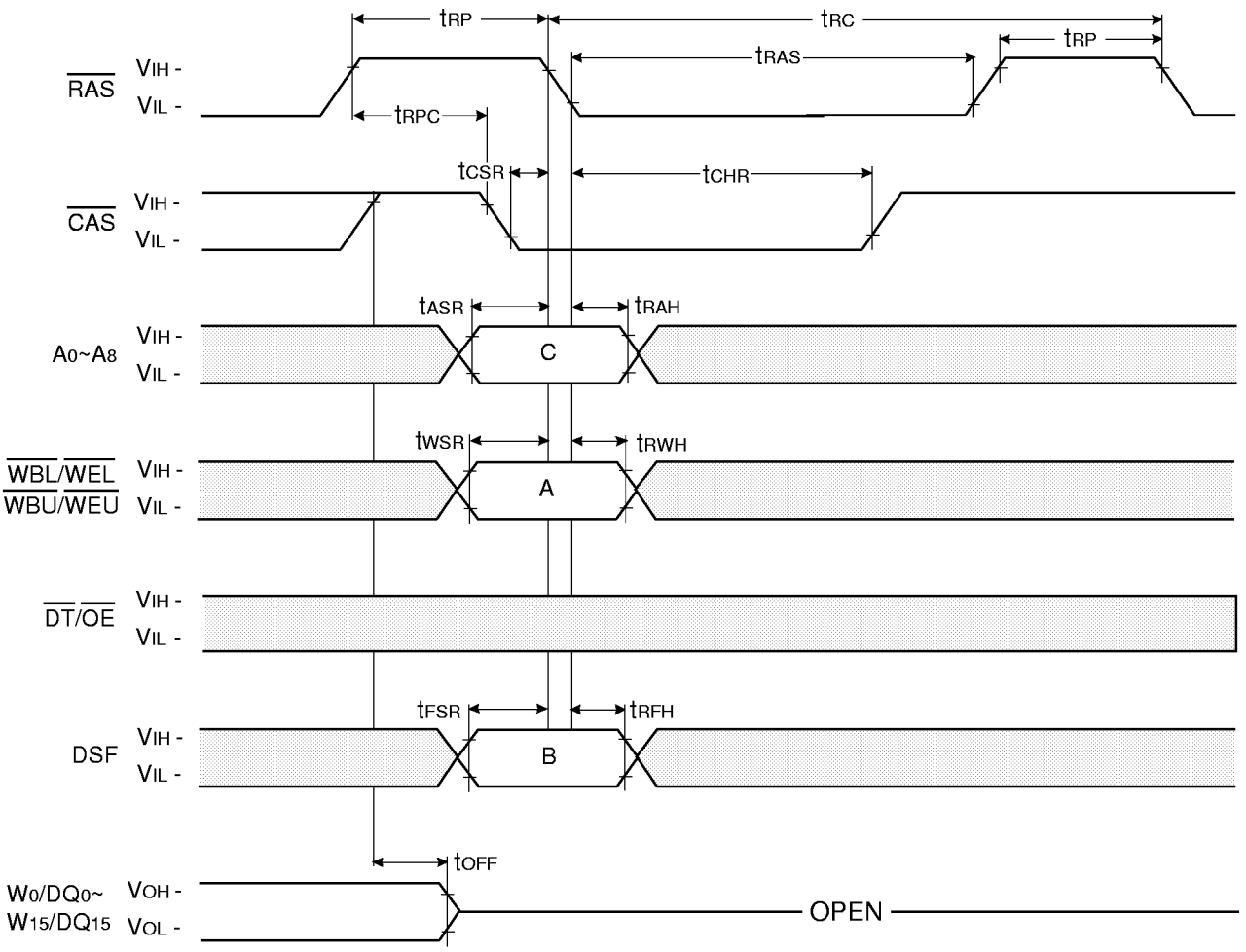
Don't care

HIDDEN REFRESH CYCLE



Don't care

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

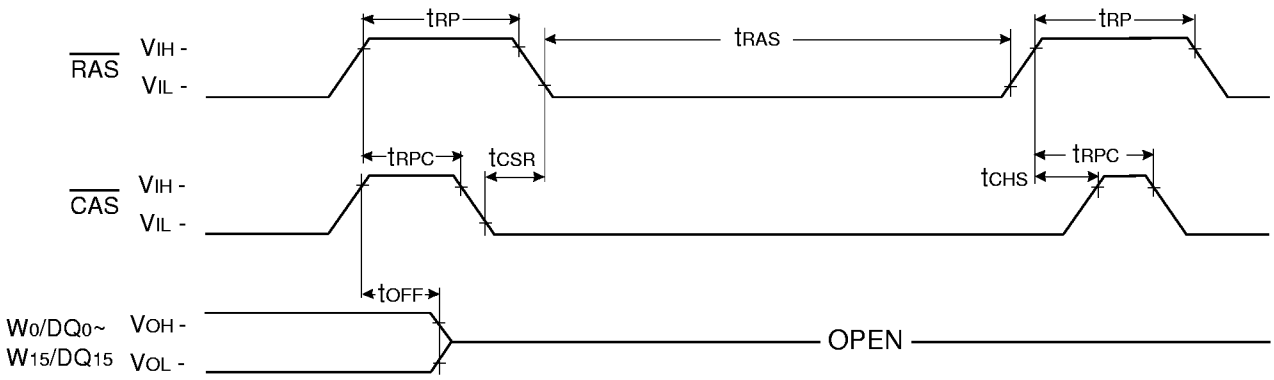


$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle Function Table

FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle (Reset All Options)	CBRR	X	0	X
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle (Stop Register Set)	CBRS	0	1	Stop Address
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle (No Reset)	CBRN	1	1	X

Don't care

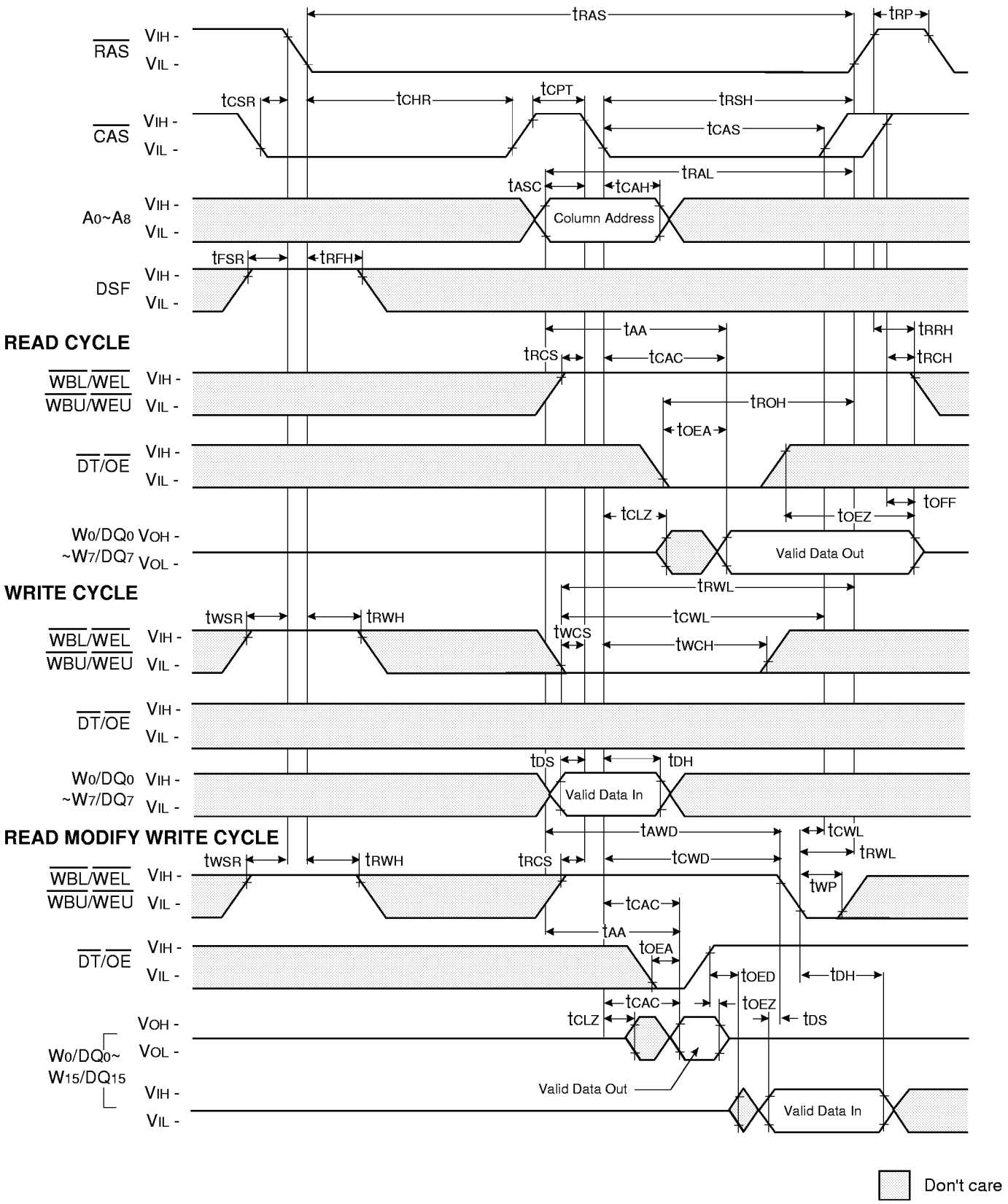
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ SELF REFRESH CYCLE



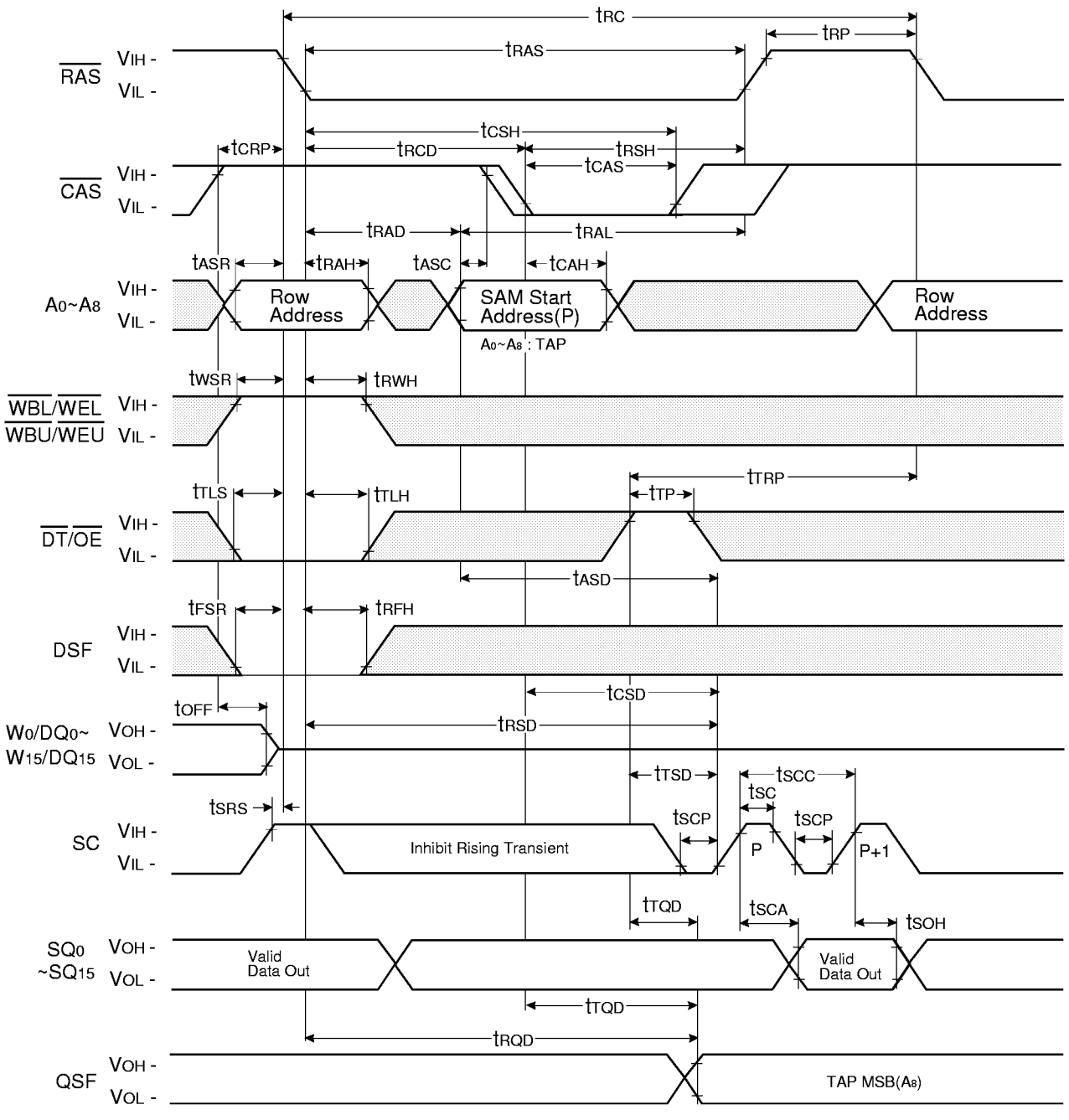
* CBR Self Refresh Cycle is Applicable With CBRR, CBRS, or CBRN Cycle

Don't care

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



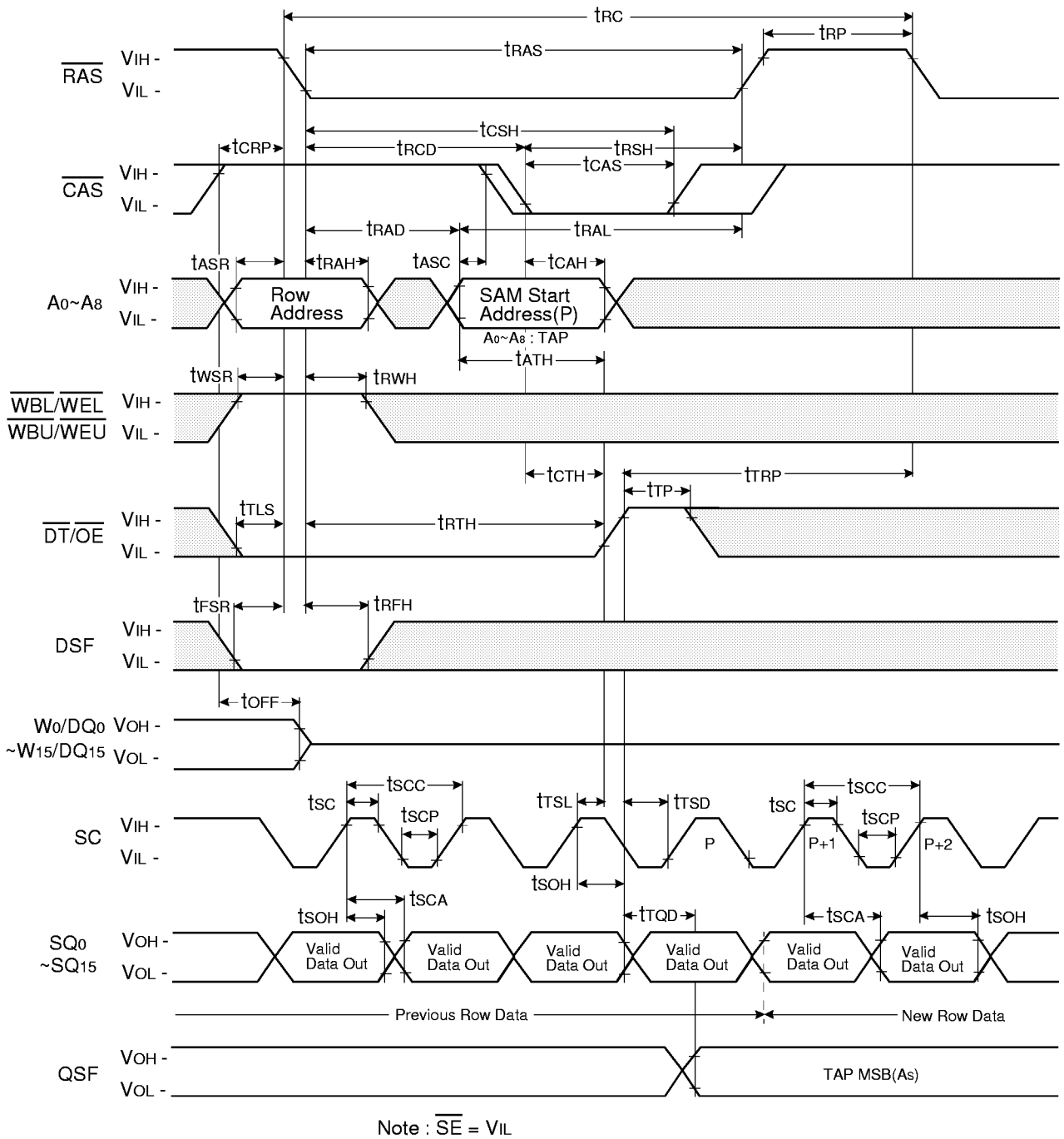
READ TRANSFER CYCLE



Note : $\overline{SE}$ = VIL

Don't care

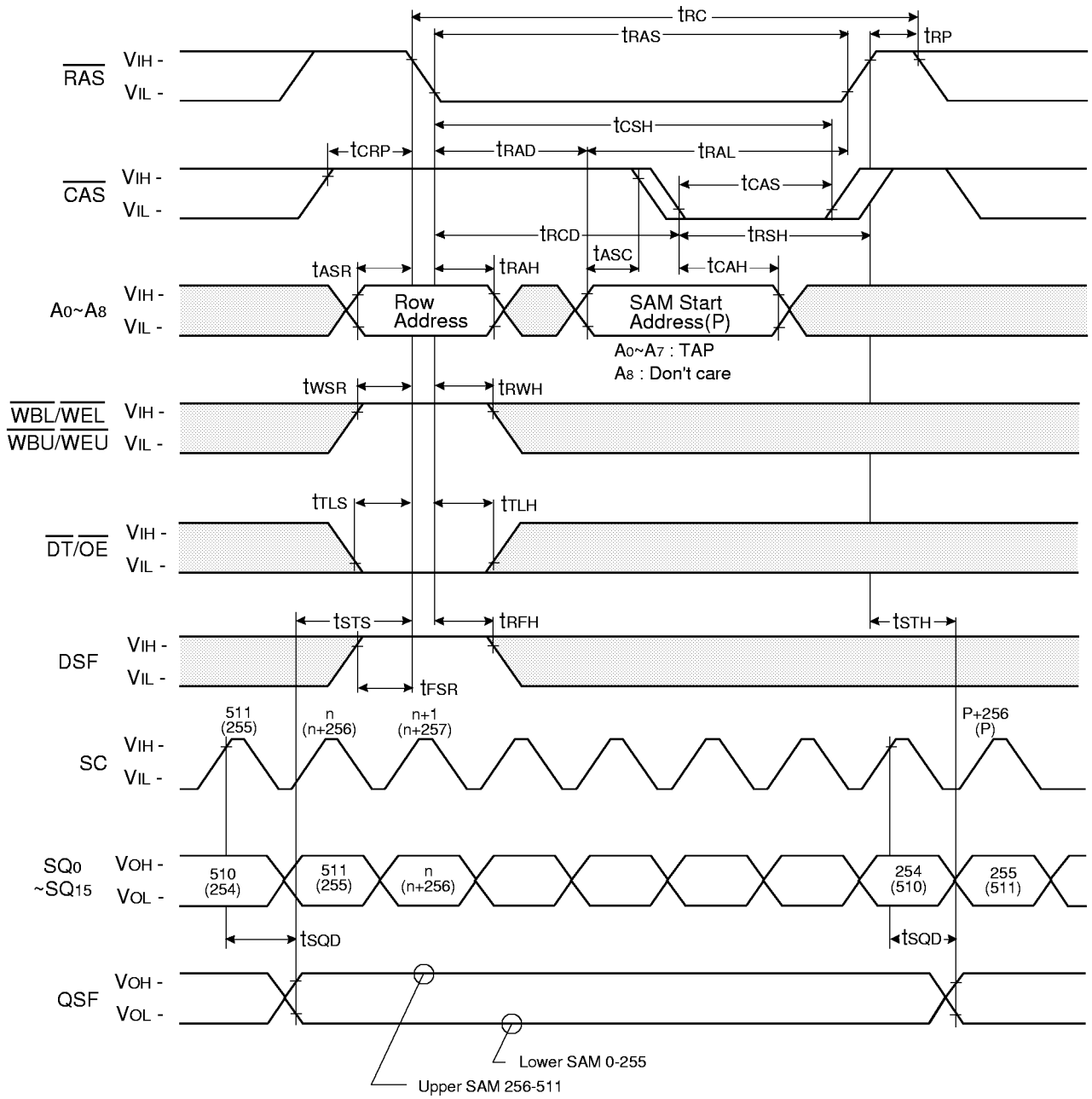
REAL TIME READ TRANSFER CYCLE



Note : $\overline{SE}$ = VIL

Don't care

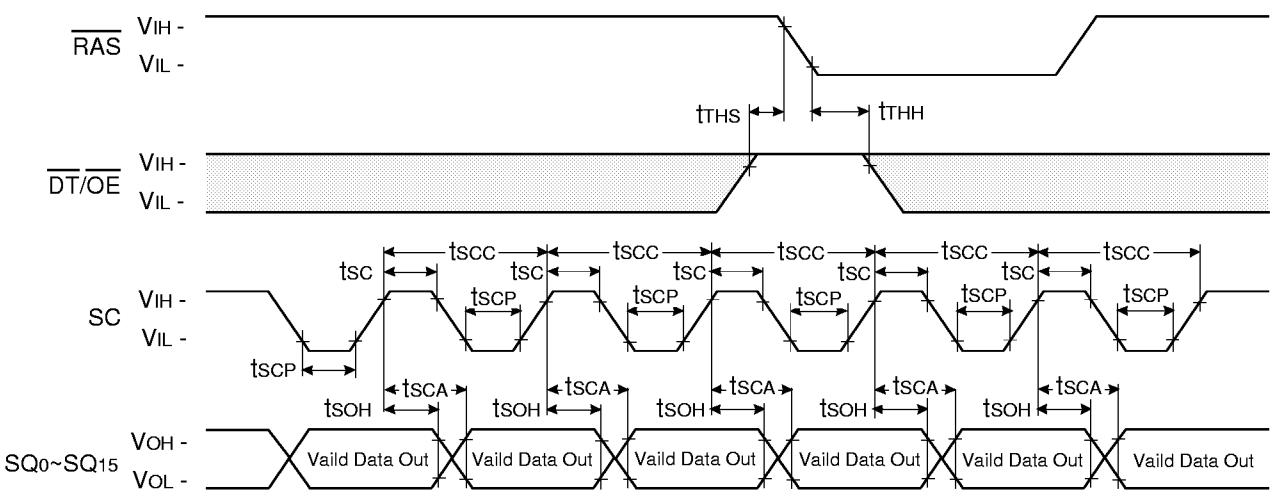
SPLIT READ TRANSFER CYCLE



Note : $\overline{SE}$ = VIL

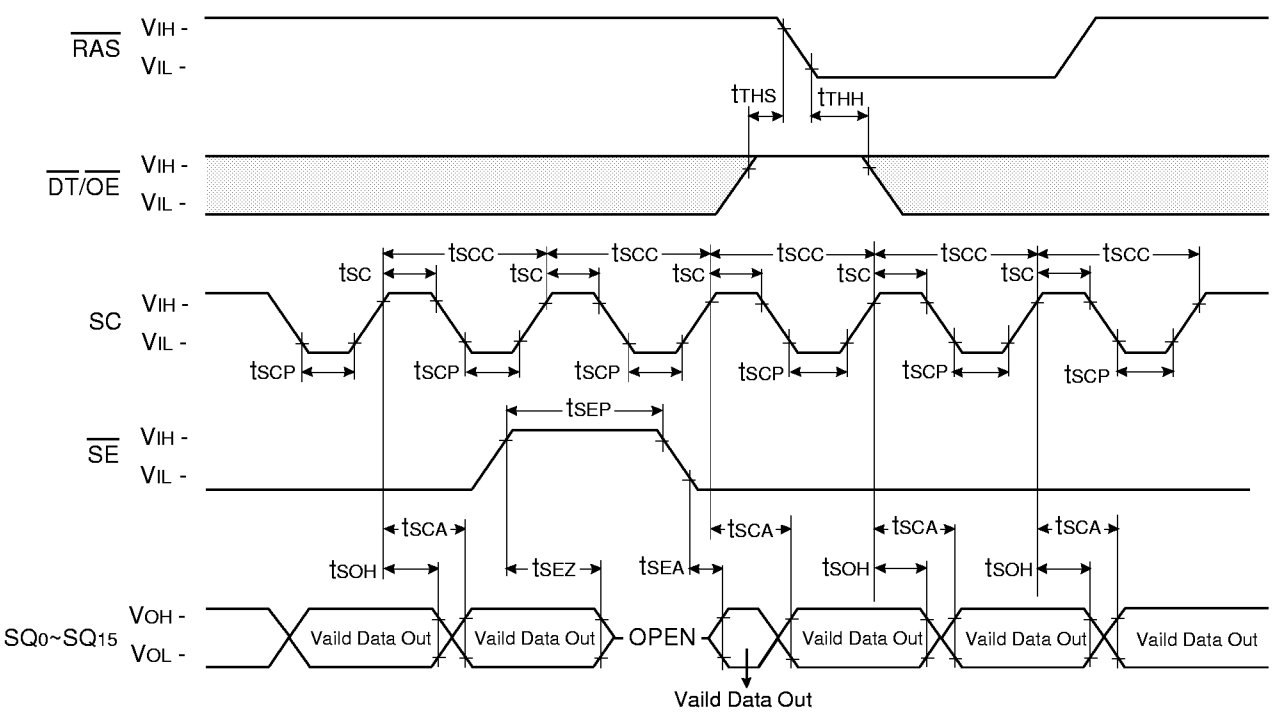
Don't care

SERIAL READ CYCLE ($\overline{SE}$=VIL)



Note : $\overline{SE}$ = VIL

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



Don't care

PACKAGE DIMENSIONS

64 Pin Plastic Small Out Line Package (Units : Millimeters)