

2 Channel Low Capacitance ESD Protection Diode Array

HYESD1025QG is a 2-channel ultra low capacitance rail clamp ESD protection diode array which includes surge rated to protect high speed data lines. Each channel consists of a pair of ESD diodes that steer positive or negative rail. Typical application, the negative rail pin is connected with the ground of the circuit protected. The Positive ESD current is steered to the ground through internal zener diode to protect the power supply of the circuit protected.

FEATURES

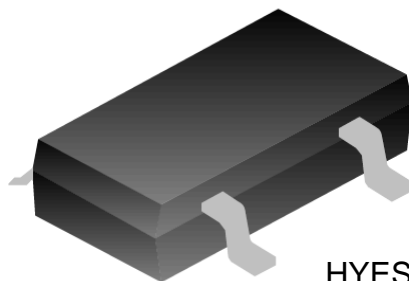
- 2 Channel ESD protection for high speed data line
- Provides ESD protection to IEC61000-4-2 level 4
 - $\pm 15\text{KV}$ Air Discharge
 - $\pm 10\text{KV}$ Contact Discharge
- Ultra low capacitance
 - I/O to GND : 1.4pF (Max)
 - I/O to I/O : 0.7pF (Max)
- Low clamping voltage & 5V operation voltage

APPLICATION

- HDMI / DVI ports
- Display port
- USB 2.0 interface protection
- Flat panel Monitors / TVs
- Set-top box
- PCI Express / Serial ATA

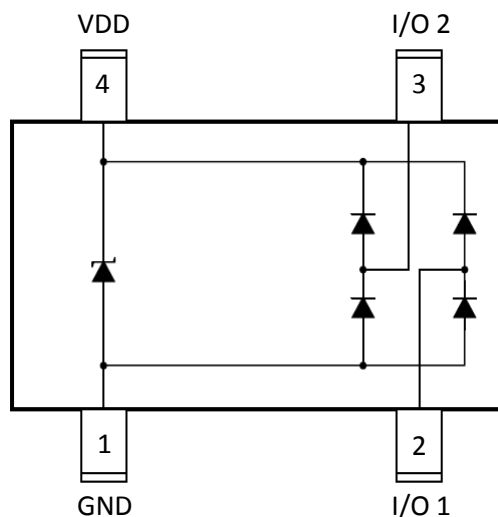
MECHANICAL INFORMATION

- Case : SOT-143 4L Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant



HYESD1025QG
SOT-143 4L

PIN CONFIGURATION



Maximum Rating and Thermal Characteristics ($T_C=25^\circ\text{C}$)

| Parameter | Symbol | Value | Unit |
|---|-----------|-------------------|------------------|
| Peak Pulse Power(8/20 μs) | P_{PP} | 150 | W |
| Peak Pulse Current(8/20 μs) | I_{PP} | 5 | A |
| ESD per IEC 61000-4-2(Air) | V_{ESD} | $\pm 15\text{KV}$ | V |
| ESD per IEC 61000-4-2(Contact) | V_{ESD} | $\pm 10\text{KV}$ | V |
| Operating Temperature Range | T_{op} | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Electrical Characteristics ($T_C=25^\circ\text{C}$, unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------|---|-----|-----|-----|---------------|
| Reverse Working Voltage | V_{RWM} | Any I/O pin to GND | - | - | 5 | V |
| Reverse Breakdown Voltage | V_{BR} | $I_{BR}=1\text{mA}$; I/O pin to GND | 6 | - | | V |
| Reverse Leakage Current | I_R | $V_{RWM}=5\text{V}$, $T=25^\circ\text{C}$; I/O pin to GND | - | - | 1 | μA |
| Positive Clamping Voltage | V_C | $I_{PP}=1\text{A}$, $t_p=8/20\mu\text{s}$; Positive pulse; Any I/O pin to GND | - | 8.5 | 12 | V |
| Negative Clamping Voltage | V_C | $I_{PP}=1\text{A}$, $t_p=8/20\mu\text{s}$; Negative pulse; Any I/O pin to GND | - | 1.8 | - | V |
| Junction Capacitance Between Channel | C_J | $V_R=0\text{V}$, $f=1\text{MHz}$; Between I/O pins | - | 0.6 | 0.7 | pF |
| Junction Capacitance Between I/O And GND | C_J | $V_R=0\text{V}$, $f=1\text{MHz}$; Any I/O pin to GND | - | 1.2 | 1.4 | pF |