

54F/74F378

Parallel D Register With Enable

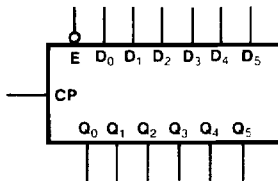
Description

The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

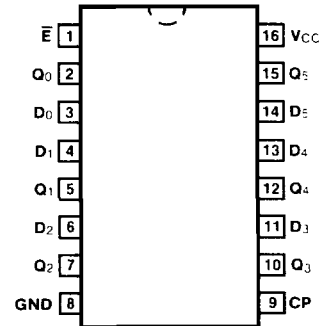
- 6-Bit High-Speed Parallel Register
- Positive Edge-Triggered D-Type Inputs
- Fully Buffered Common Clock and Enable Inputs
- Input Clamp Diodes Limit High-Speed Termination Effects
- Full TTL and CMOS Compatible

Ordering Code: See Section 5

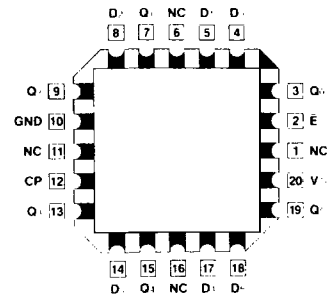
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

| Pin Names | Description | 54F/74F(U.L.) HIGH/LOW |
|--------------------------------|--|------------------------|
| \bar{E} | Enable Input (Active LOW) | 0.5/0.375 |
| D ₀ -D ₅ | Data Inputs | 0.5/0.375 |
| CP | Clock Pulse Input (Active Rising Edge) | 0.5/0.375 |
| Q ₀ -Q ₅ | Outputs | 25/12.5 |

Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops.

When the \bar{E} input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the \bar{E} input is HIGH the register will retain the present data independent of the CP input.

Truth Table

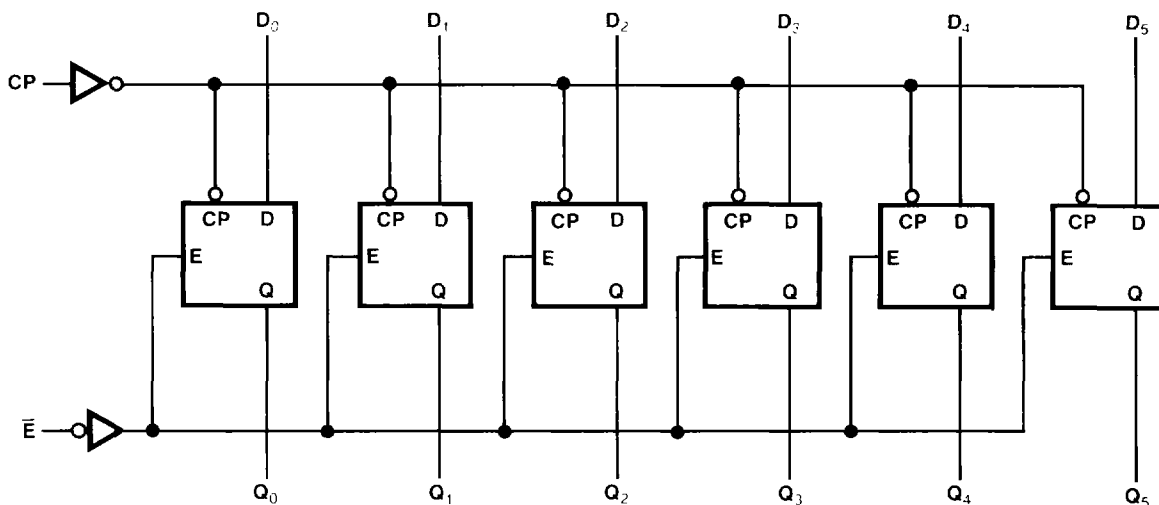
| Inputs | | | Output |
|-----------|----|-------|-----------|
| \bar{E} | CP | D_n | Q_n |
| H | ⌋ | X | No Change |
| L | ⌋ | H | H |
| L | ⌋ | L | L |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

| Symbol | Parameter | 54F/74F | | | Units | Conditions |
|----------|----------------------|---------|-----|-----|-------|-----------------------------------|
| | | Min | Typ | Max | | |
| I_{CC} | Power Supply Current | | 30 | 45 | mA | $V_{CC} = \text{Max}, V_{CP} = 0$ |

AC Characteristics: See Section 3 for waveforms and load configurations

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|------------------|----------------------------------|---|-----|-----|--|------|--|-----|-------|----------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$ | | | $T_A, V_{CC} =$ Mil $C_L = 50\text{ pF}$ | | $T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$ | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| f_{max} | Maximum Input Frequency | 80 | 100 | | 70 | | 80 | MHz | 3-1 | |
| t_{PLH} | Propagation Delay CP to Q_n | 3.0 | 5.5 | 7.5 | 3.0 | 10.0 | 3.0 | 8.5 | ns | 3-1 |
| t_{PHL} | | 3.5 | 6.0 | 8.5 | 3.5 | 10.5 | 3.5 | 9.5 | | 3-7 |

AC Operating Requirements: See Section 3 for waveforms

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|--|--|---|-----|-----|------------------------|-----|------------------------|-----|-------|----------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ | | | $T_A, V_{CC} =$ Mil | | $T_A, V_{CC} =$ Com | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{\text{s(H)}}$ $t_{\text{s(L)}}$ | Setup Time, HIGH or LOW D_n to CP | 4.0 | | | 5.0 | | 4.0 | | ns | 3-5 |
| | | 4.0 | | | 5.0 | | 4.0 | | | |
| $t_{\text{h(H)}}$ $t_{\text{h(L)}}$ | Hold Time, HIGH or LOW D_n to CP | 0 | | | 2.0 | | 0 | | ns | 3-5 |
| | | 0 | | | 2.0 | | 0 | | | |
| $t_{\text{s(H)}}$ $t_{\text{s(L)}}$ | Setup Time, HIGH or LOW \bar{E} to CP | 4.0 | | | 4.5 | | 4.0 | | ns | 3-5 |
| | | 10.0 | | | 13.0 | | 10.0 | | | |
| $t_{\text{h(H)}}$ $t_{\text{h(L)}}$ | Hold Time, HIGH or LOW \bar{E} to CP | 0 | | | 0 | | 0 | | ns | 3-5 |
| | | 0 | | | 0 | | 0 | | | |
| $t_{\text{w(H)}}$ $t_{\text{w(L)}}$ | CP Pulse Width HIGH or LOW | 4.0 | | | 5.0 | | 4.0 | | ns | 3-7 |
| | | 6.0 | | | 7.5 | | 6.0 | | | |