N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package
			TO-92
200V	10Ω	2.0V	VN2010L

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)
- Telecom switching

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

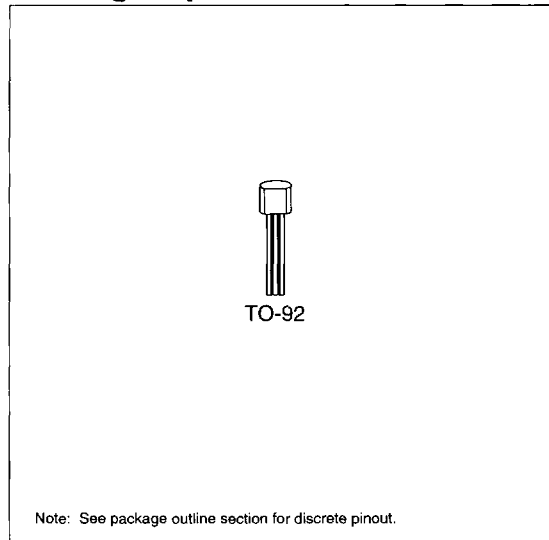
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	250mA	1.0A	1W	170	125	250mA	1.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200			V	$V_{GS} = 0V$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			10	nA	$V_{GS} = \pm 25V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			1.0	µA	$V_{GS} = 0V$, $V_{DS} = 160V$
				100	µA	$V_{GS} = 0V$, $V_{DS} = 160V$ $T_A = 125°C$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10	Ω	$V_{GS} = 4.5V$, $I_D = 50mA$
$I_{D(ON)}$	ON-State Drain Current	100			mA	$V_{GS} = 10V$, $V_{DS} = 10V$
G_{FS}	Forward Transconductance	125			m℧	$V_{DS} = 15V$, $I_D = 0.1A$
C_{ISS}	Input Capacitance			60	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance			15	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
$t_{(ON)}$	Turn-ON Time			20	ns	$V_{DD} = 25V$, $I_D = 0.1A$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			30	ns	$V_{DD} = 25V$, $I_D = 0.1A$ $R_{GEN} = 25\Omega$
V_{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS} = 0V$, $I_{SD} = 250mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit